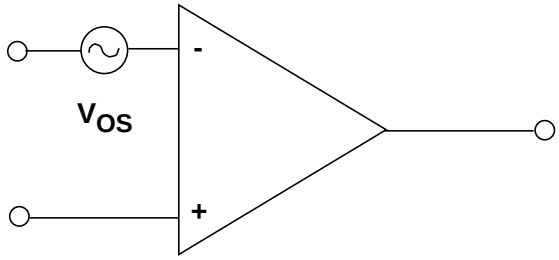
Op Amp Input Offset Voltage

DEFINITION OF INPUT OFFSET VOLTAGE

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the *input offset voltage*, V_{OS}. Input offset voltage is modeled as a voltage source, V_{OS}, in series with the inverting input terminal of the op amp as shown in Figure 1.



- **Offset Voltage: The differential voltage which must be applied to the input of an op amp to produce zero output.**
- **Ranges:**
  - **Chopper Stabilized Op Amps: <1µV**
  - **General Purpose Precision Op Amps: 50-500µV**
  - **Best Bipolar Op Amps: 10-25µV**
  - **Best JFET Input Op Amps: 100-1,000µV**
  - **High Speed Op Amps: 100-2,000µV**
  - **Untrimmed CMOS Op Amps: 5,000-50,000µV**
  - **DigiTrim™ CMOS Op Amps: <100µV-1,000µV**

Figure 1: Typical Op Amp Input Offset Voltage

Chopper stabilized (also called *auto-zero*) op amps have a V_{OS} which is less than 1 µV (e.g. AD8538, AD8551, AD8571, AD8628, AD8630), and the best precision bipolar op amps (super-beta or bias stabilized) can have maximum offsets as low as 25 µV (OP177F). The very best trimmed JFET input types have about 100 µV of offset (AD8610B, AD8620B), and untrimmed CMOS op amps can range from 5 to 50 mV.

However, the ADI DigiTrim™ CMOS op amps have offset voltages less than 100 µV (e.g., AD8603, AD8607, AD8609, AD8605, AD8606, AD8608). Generally speaking, "precision" op amps will have V_{OS} < 0.5 mV, although some high speed amplifiers may be a little worse than this. The DigiTrim process is explained later in this tutorial.

INPUT OFFSET VOLTAGE DRIFT AND AGING EFFECTS

Input offset voltage varies with temperature, and its temperature coefficient is known as TCV_{OS}, or more commonly, *drift*. Offset drift is affected by offset adjustments to the op amp, but when the offset voltage of a bipolar input op amp has been minimized, the drift may be as low as 0.1 µV/°C (typical value for OP177F). More typical drift values for a range of general purpose precision op amps lie in the range 1-10 µV/°C. Most op amps have a specified value of TCV_{OS}, but some, instead, have a second value of maximum V_{OS} that is guaranteed over the operating temperature range. Such a specification is less useful, because there is no guarantee that TCV_{OS} is constant or monotonic.

The offset voltage also changes as time passes, or *ages*. Aging is generally specified in µV/month or µV/1000 hours, but this can be misleading. Since aging is a "drunkard's walk" phenomenon, it is proportional to the *square root* of the elapsed time. An aging rate of 1 µV/1000 hour therefore becomes about 3 µV/year (not 9 µV/year).

Long-term stability of the OP177F is approximately 0.3 µV/month. This refers to a time period *after* the first 30 days of operation. Excluding the initial hour of operation, changes in the offset voltage of these devices during the first 30 days of operation are typically less than 2 µV.

Long-term stability of chopper-stabilized op amps is not specified because the auto-zero circuit removes any offset due to aging.

MEASURING INPUT OFFSET VOLTAGE

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 2 shows a standard circuit for measuring offset voltage. The circuit amplifies the input offset voltage by the noise gain of 1001. The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen by the inputs results in negligible bias current contribution to the measured offset voltage. For example, 2 nA bias current flowing through the 10 Ω resistor produces a 0.02 µV error referred to the input.

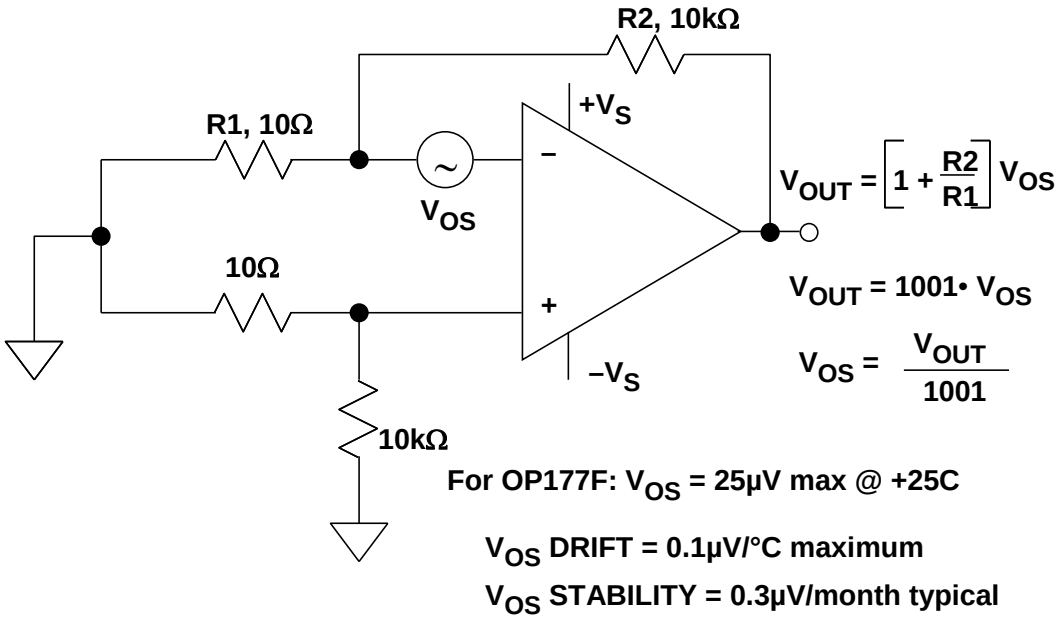


Figure 2: Measuring Input Offset Voltage

As simple as this circuit looks, it can give inaccurate results when testing precision op amps, unless care is taken in implementation. The largest potential error source comes from parasitic thermocouple junctions, formed where two different metals are joined. This thermocouple voltage can range from 2 µV/ºC to more than 40 µV/ºC. Note that in this circuit additional "dummy" resistors have been added to the non-inverting input, in order to exactly match/balance the thermocouple junctions in the inverting input path.

The accuracy of the measurement also depends on the mechanical layout of the components and exactly how they are placed on the PC board. Keep in mind that the two connections of a component such as a resistor create two equal, but opposite polarity thermoelectric voltages (assuming they are connected to the same metal, such as the copper trace on a PC board). These will cancel each other, *assuming both are at exactly the same temperature*. Clean connections and short lead lengths help to minimize temperature gradients and increase the accuracy of the measurement.

In the test circuit, airflow should be minimal so that all the thermocouple junctions stabilize at the same temperature. In some cases, the circuit should be placed in a small closed container to eliminate the effects of external air currents. The circuit should be placed flat on a surface so that convection currents flow up and off the top of the board, not across the components, as would be the case if the board were mounted vertically.

Measuring the offset voltage shift over temperature is an even more demanding challenge. Placing the printed circuit board containing the amplifier being tested in a small box or plastic bag with foam insulation prevents the temperature chamber air current from causing thermal gradients across the parasitic thermocouples. If cold testing is required, a dry nitrogen purge is

recommended. Localized temperature cycling of the amplifier itself using a Thermostream-type heater/cooler may be an alternative, however these units tend to generate quite a bit of airflow that can be troublesome. Generally, the test circuit of Figure 2 can be made to work for many amplifiers. Low absolute values for the small resistors (such as 10 Ω) will minimize bias current induced errors.

An alternate V_{OS} measurement method is shown in Figure 3, and is suitable for cases of high and/or unequal bias currents (as in the case of current feedback op amps). In this measurement method, an in-amp is connected to the op amp input terminals through isolation resistors, and provides the gain for the measurement. The offset voltage of the in-amp (measured with S closed) must then be subtracted from the final V_{OS} measurement.

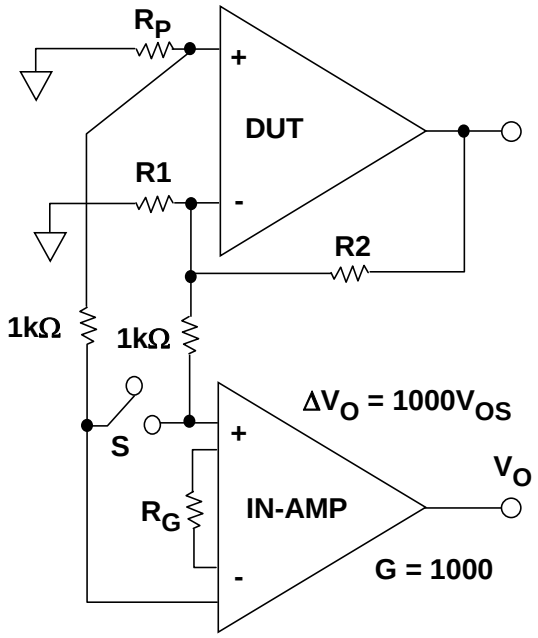
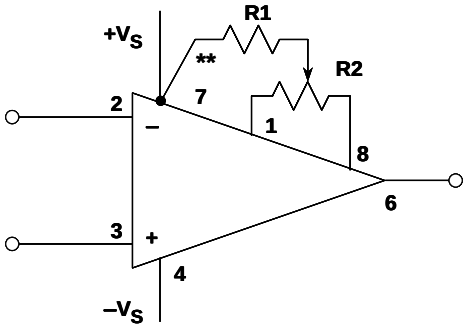


Figure 3: Alternate Input Offset Voltage Measurement Using an In-Amp

OFFSET VOLTAGE ADJUSTMENT USING "NULL" PINS

Many single op amps have pins available for optional offset null. To make use of this feature, two pins are joined by a potentiometer, and the wiper goes to one of the supplies through a resistor, as shown generally in Figure 4. Note that if the wiper is accidentally connected to the wrong supply, the op amp will probably be destroyed—this is a common problem, when one op amp type is replaced by another. The range of offset adjustment in a well-designed op amp is no more than two or three times the maximum V_{OS} of the lowest grade device, in order to minimize sensitivity. Nevertheless, the voltage gain of an op amp at its offset adjustment pins may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins noise-free. Note that it is *never* advisable to use long leads from an op amp to a remote nulling potentiometer.



- ** Wiper connection may be to either $+V_S$ or $-V_S$ depending on op amp
- R values depend on op amp. Consult data sheet
- Use to null out input offset voltage, not system offsets!
- There may be high gain from offset pins to output — Keep them quiet!
- Nulling offset causes increase in offset temperature coefficient, approximately 4µV/°C for 1mV offset null for FET inputs

Figure 4: Offset Adjustment Pins

As was mentioned above, the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. The internal adjustment terminals should therefore be used only to adjust the op amp's own offset, *not to correct any system offset errors*, since doing so would be at the expense of increased temperature drift. The drift penalty for a FET input op amp is in the order of 4 µV/°C for each millivolt of nulled offset voltage. It is generally better to control offset voltage by proper device/grade selection.

OFFSET ADJUSTMENT (EXTERNAL METHODS)

If an op amp doesn't have offset adjustment pins (popular duals and all quads do not), and it is still necessary to adjust the amplifier and system offsets, an external method can be used. This method is also most useful if the offset adjustment is to be done with a system programmable voltage, such as a DAC.

With an inverting op amp configuration, injecting current into the inverting input is the simplest method, as shown in Figure 5A. The disadvantage of this method is that there is some increase in noise gain possible, due to the parallel path of R3 and the potentiometer resistance. The resulting increase in noise gain may be reduced by making $\pm V_R$ large enough so that the R3 value is much greater than R1||R2. Note that if the power supplies are stable and noise-free, they can be used as $\pm V_R$.

Figure 5B shows how to implement offset trim by injecting a small offset voltage into the non-inverting input. This circuit is preferred over Figure 5A, as it results in no noise gain increase (but it requires adding R_P). If the op amp has matched input bias currents, then R_P should equal R1|| R2 (to minimize the added offset voltage). Otherwise, R_P should be less than 50 Ω. For higher values, it may be advisable to bypass R_P at high frequencies.

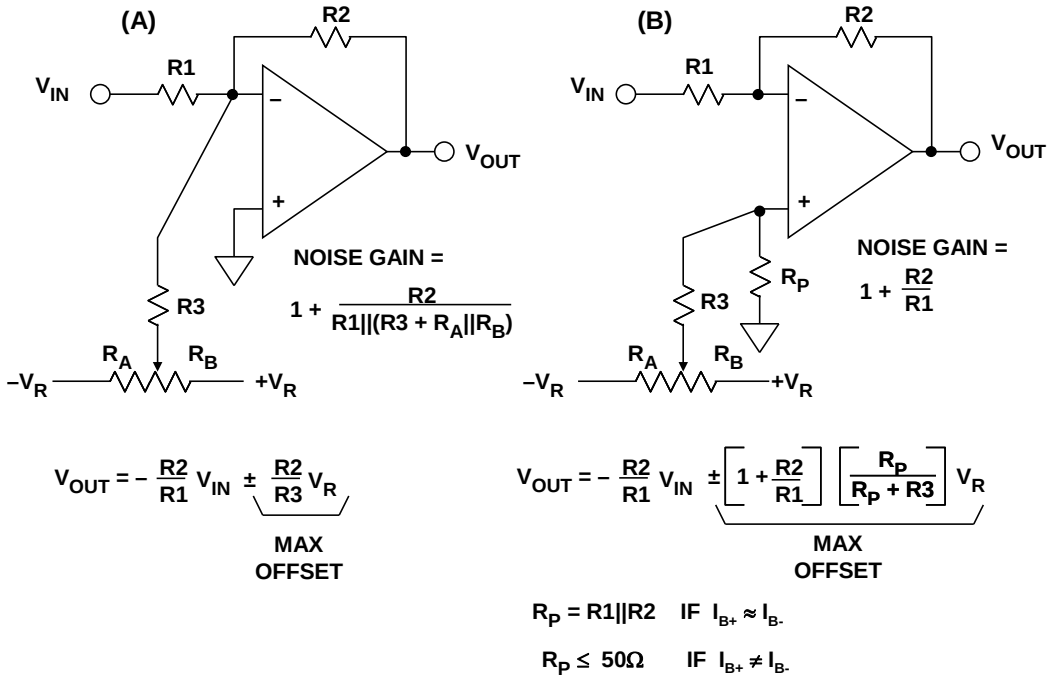


Figure 5: Inverting Op Amp External Offset Trim Methods

The circuit shown in Figure 6 can be used to inject a small offset voltage when using an op amp in the non-inverting mode. This circuit works well for small offsets, where R3 can be made much greater than R1. Note that otherwise, the signal gain might be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage sources, $\pm V_R$.

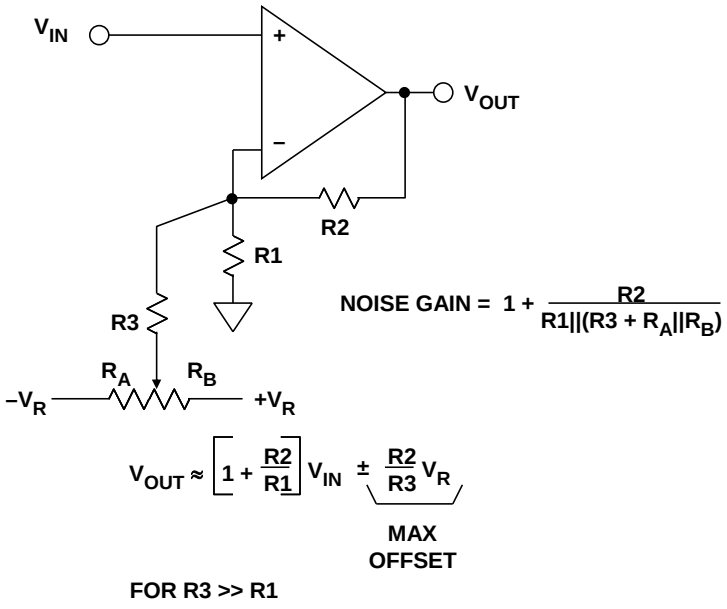


Figure 6: Non-Inverting Op Amp External Offset Trim Methods

OFFSET VOLTAGE TRIM PROCESSES

The DigiTrim™ CMOS op amp family exploits the advantages of digital technology, so as to minimize the offset voltage normally associated with CMOS amplifiers. Offset voltage trimming is done after the devices are packaged. A digital code is entered into the device to adjust the offset voltage to less than 1 mV, depending upon the grade. Wafer testing is not required, and the patented Analog Devices' technique called DigiTrim™ requires no extra pins to accomplish the function. These devices have rail-to-rail inputs and outputs, and the NMOS and PMOS parallel input stages are trimmed separately using DigiTrim to minimize the offset voltage in both pairs. A functional diagram of a typical DigiTrim CMOS op amp is shown in Figure 7.

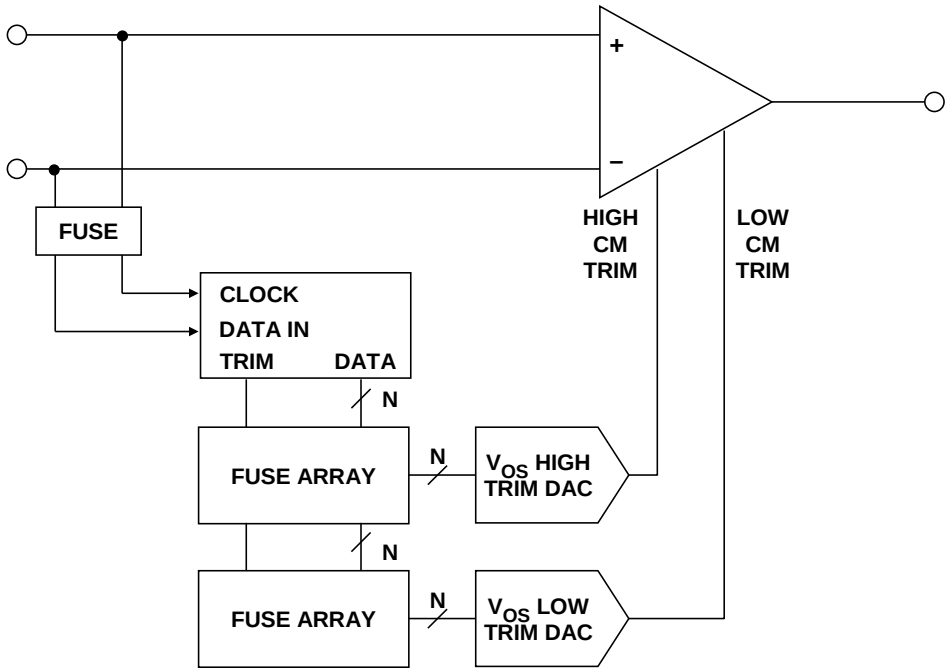


Figure 7: Analog Devices' DigiTrim™ Process for Trimming CMOS Op Amps

DigiTrim adjusts the offset voltage by programming digitally weighted current sources. The trim information is entered through existing pins using a special digital sequence. The adjustment values can be temporarily programmed, evaluated, and readjusted for optimum accuracy before permanent adjustment is performed. After the trim is completed, the trim circuit is locked out to prevent the possibility of any accidental re-trimming by the end user.

The physical trimming, achieved by blowing polysilicon fuses, is very reliable. No extra pads or pins are required, and no special test equipment is needed to perform the trimming. The trims can be done after packaging so that assembly-related shifts can be eliminated. No testing is required at the wafer level because of high die yields.

The first devices to use this new technique are the Analog Devices' AD8601, AD8602, AD8604 (single, dual, quad) rail-to-rail CMOS amplifiers. The offset is trimmed for both high and low

common-mode conditions so that the offset voltage is under 500 µV over the full common-mode input voltage range. The bandwidth of the op amps is 8 MHz, slew rate is 5 V/µs, and supply current is only 640 µA per amplifier.

The AD8603, AD8605, AD8607 (single, dual, quad) family have maximum offset voltages of 50 µV maximum over the full common-mode range. Gain-bandwidth is 400 kHz, and the supply current is only 50 µA per amplifier.

At this point it is useful to review the other popular trim methods. Analog Devices pioneered the use of thin film resistors and laser wafer trimming for precision amplifiers, references, data converters, and other linear ICs. Up to 16-bit accuracy can be achieved with trimming, and the thin film resistors themselves are very stable with temperature and can add to the thermal stability and accuracy of a device, even without trimming. Thin film deposition and patterning are processes that must be tightly controlled. The laser trimming systems are also quite expensive. In-package trimming is not possible, so assembly-related shifts cannot be easily compensated. Nevertheless, thin film trimming at the wafer level provides continuous fine trim resolution in precision integrated circuits where high accuracy and stability are required.

Zener zapping uses a voltage to create a metallic short circuit across the base-emitter junction of a transistor to remove a circuit element. The base-emitter junction is commonly referred to as a zener, although the mechanism is actually avalanche breakdown of the junction. During the avalanche breakdown across the base-emitter junction, the very high current densities and localized heating generate rapid metal migration between the base and emitter connections, leading to a metallic short across the junction. With proper biasing (current, voltage, and time), this short will have a very low resistance value. If a series of these base-emitter junctions are arranged in parallel with a string of resistors, zapping selected junctions will short out portions of the resistor string, thereby adjusting the total resistance value.

It is possible to perform zener zap trimming in the packaged IC to compensate for assembly-related shifts in the offset voltage. However, trimming in the package requires extra package pins. Alternately, trimming at the wafer level requires additional probe pads. Probe pads do not scale effectively as the process features shrink. So, the die area required for trimming is relatively constant regardless of the process geometries. Some form of bipolar transistor is required for the trim structures, therefore a purely MOS-based process may not have zener zap capability. The nature of the trims is discrete since each zap removes a predefined resistance value. Increasing trim resolution requires additional transistors and pads or pins, which rapidly increase the total die area and/or package cost. This technique is most cost-effective for fairly large-geometry processes where the trim structures and probe pads make up a relatively small percentage of the overall die area.

It was in the process of creating the industry standard OP07 in 1975 that Precision Monolithics Incorporated pioneered zener zap trimming. The OP07 and other similar parts must be able to operate from over ±15 V supplies. As a result, they utilize relatively large device geometries to support the high voltage requirements, and extra probe pads don't significantly increase die area.

Link trimming is the cutting of metal or poly-silicon links to remove a connection. In link trimming, either a laser or a high current is used to destroy a "shorted" connection across a parallel resistive element. Removing the connection increases the effective resistance of the combined element(s). Laser cutting works similar to laser trimming of thin films. The high local heat from the laser beam causes material changes that lead to a non-conductive area, effectively cutting a metal or conductive polysilicon connector.

The high-current link trim method works as an inverse to zener zapping—the conductive connection is destroyed, rather than created by a zener-zap.

Link trim structures tend to be somewhat more compact than laser trimmed resistor structures. No special processes are required in general, although the process may have to be tailored to the laser characteristics if laser cutting is used. With the high-current trimming method, testing at the wafer level may not be required if die yields are good. The laser cutting scheme doesn't require extra contact pads, but the trim structures don't scale with the process feature sizes. Laser cutting of links cannot be performed in the package, and requires additional probe pads on the die. In addition, it can require extra package pins for in-package high-current trims. Like zener zapping, link trimming is discrete. Resolution improvements require additional structures, increasing area and cost.

EEPROM trimming utilizes special, non-volatile digital memory to store trim data. The stored data bits control adjustment currents through on-chip D/A converters.
Memory cells and D/A converters scale with the process feature size. In-package trimming and even trimming in the customer's system is possible so that assembly-related shifts can be trimmed out. Testing at the wafer level is not required if yields are reasonable. No special hardware is required for the trimming beyond the normal mixed-signal tester system, although test software development may be more complicated.
Since the trims can be overwritten, it is possible to periodically reprogram the system to account for long-term drifts or to modify system characteristics for new requirements. The number of reprogram cycles possible depends on the process, and is finite. Most EEPROM processes provide enough rewrite cycles to handle routine re-calibration.

This trim method does require special processing. Stored trim data can be lost under certain conditions, especially at high operating temperatures. At least one extra digital contact pad/package pin is required to input the trim data to the on-chip memory.
This technique is only available on MOS-based processes due to the very thin oxide requirements. The biggest drawback is that the on-chip D/A converters are large—often larger than the amplifier circuits they are adjusting. For this reason, EEPROM trimming is mostly used for data converter or system-level products where the trim D/A converters represent a much smaller percentage of the overall die area.

Figure 8 summarizes the key features of each ADI trim method. It can be seen from that all trim methods have their respective places in producing high performance linear integrated circuits.

PROCESS	TRIMMED AT:	SPECIAL PROCESSING	RESOLUTION
DigiTrim™	Wafer or Final Test	None	Discrete
Laser Trim	Wafer	Thin Film Resistor	Continuous
Zener Zap Trim	Wafer	None	Discrete
Link Trim	Wafer	Thin Film or Poly Resistor	Discrete
EEPROM Trim	Wafer or Final Test	EEPROM	Discrete

Figure 8: Summary of ADI Trim Processes

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2. Walter G. Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Also available as *Op Amp Applications Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 1.