

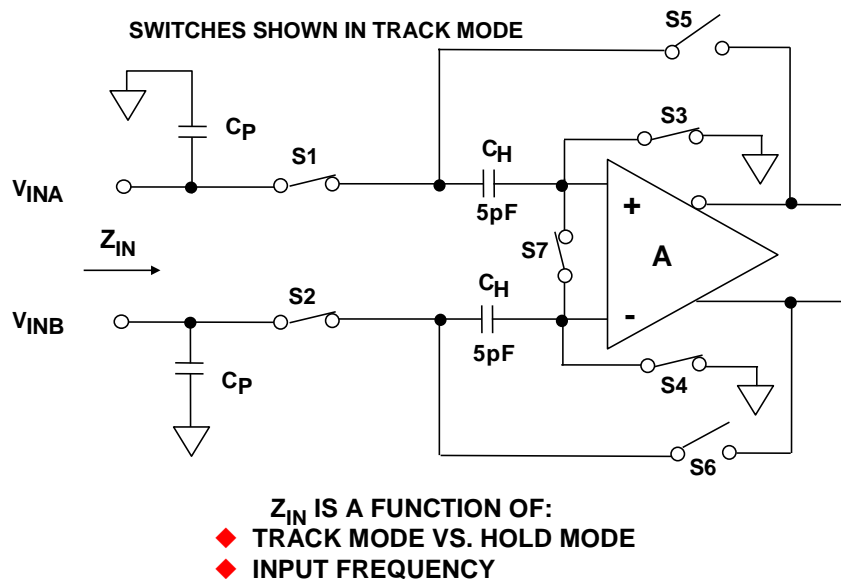
## Differential Drivers for Precision ADCs

### DIFFERENTIAL INPUT ADC CHARACTERISTICS

Many high performance ADCs are now being designed with differential inputs. A fully differential ADC design offers the advantages of good common-mode rejection, reduction in second-order distortion products, and simplified dc trim algorithms. Although they can be driven single-ended, a fully differential driver usually optimizes overall performance.

One of the most common ways to drive a differential input ADC is with a transformer. However, there are many applications where the ADCs cannot be driven with transformers because the frequency response must extend to dc. In these cases, differential drivers are required. This tutorial focuses on driving high resolution 16- to 18-bit ADCs with sampling rates up to 10 MSPS. The bandwidth of the input signals is generally limited to a few MHz. Tutorial [MT-075](#) discusses differential amplifiers suitable for driving higher speed ADCs.

Most high performance CMOS switched capacitor pipelined ADCs have differential inputs similar to that shown in Figure 1.



**Figure 1: Simplified Input Circuit for a Typical Unbuffered Switched Capacitor CMOS Sample-and-Hold**

The differential structure is typically carried through most of the ADC. This makes matching requirements easier as well as reduces second-order products. In addition, the differential structure helps in common-mode noise rejection.

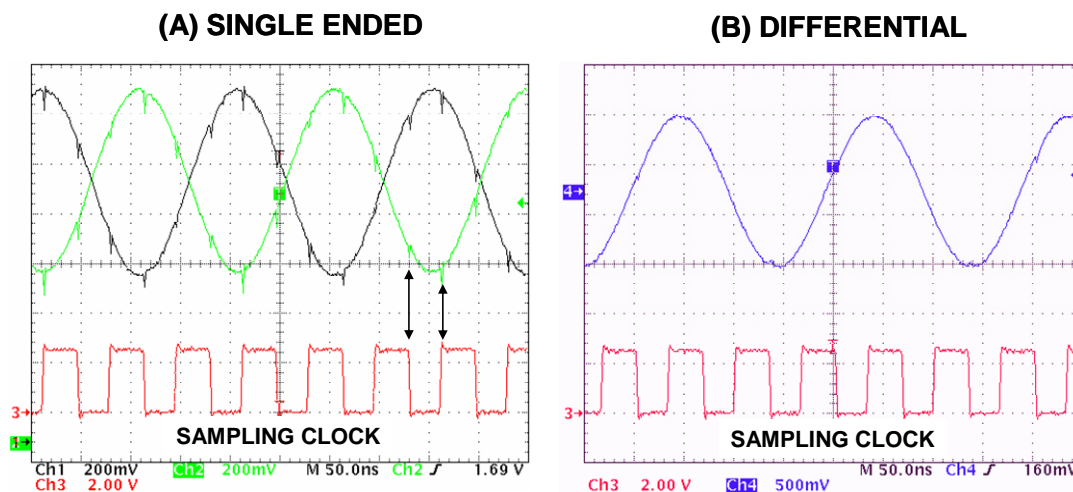
Note that the SHA switches are connected directly to each of the inputs. Switching transients can be significant, because there is no isolation buffer. The drive amplifier settling time to the transients must be fast enough so that the amplifier settles to the required accuracy in less than one-half the sampling period (this settling time must include the effects of any external series resistance).

The differential input impedance of this structure is dynamic and changes when the SHA switches between the sample mode and the hold mode. In addition, the impedance is a function of the analog input frequency.

In the track mode (shown in the figure), the input signal charges and discharges the hold capacitors,  $C_H$ . When the circuit switches to the hold mode the switches reverse their positions, and the voltage across the hold capacitors is transferred to the outputs.

It is highly recommended that this type of input be driven differentially for common-mode rejection of the switching transients. While it is possible to drive them single-ended (with one input connected to the appropriate common-mode voltage), degradation in SFDR will occur because the even-order distortion products are no longer rejected.

Figure 2 (A) shows each of the differential inputs of a typical unbuffered CMOS ADC as well as the sampling clock. The inputs were driven with a 50  $\Omega$  source resistance. Note that a transient occurs on each edge of the sampling clock because of the switching action previously described. Figure 2(B) shows the differential input signal to the ADC under the same conditions as (A). Note that most of the transient current glitches are cancelled because they are common-mode signals. Note that for cancellation to be optimum the two inputs must be driven from a balanced source impedance (the real and reactive components of the impedance must be matched).



- ◆ Differential charge transient is symmetrical around mid-scale and dominated by linear component
- ◆ Common-mode transients cancel with equal source impedance

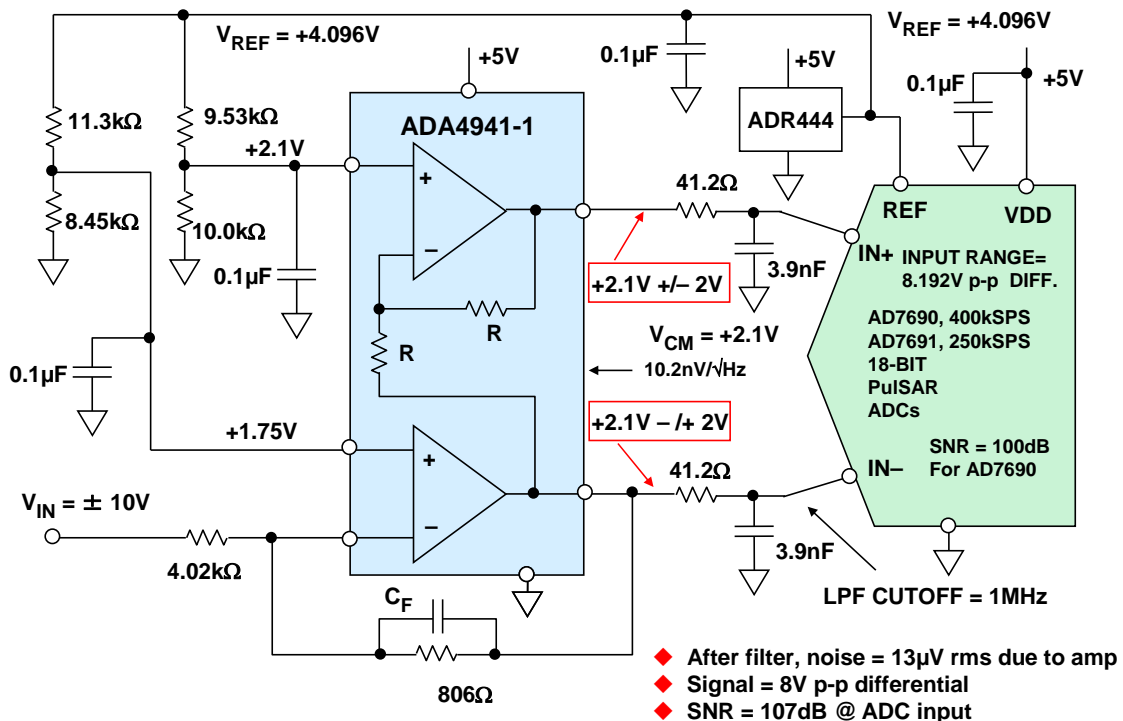
Note: Data Taken with 50 $\Omega$  Source Resistances

**Figure 2: Typical Single-Ended (A) and Differential (B) Input Transients of CMOS Switched Capacitor ADC**

**DRIVING PRECISION 16- AND 18-BIT DIFFERENTIAL INPUT ADCs**

Figure 3 shows the [ADA4941-1](#) driving the 18-bit [PulSAR](#) family of ADCs which have switched capacitor inputs. This is a common application where the signal is single-ended and bipolar and the ADC input is differential. Because of the high resolution, the drive amplifier must have low distortion, low noise, and high dc accuracy, as well as the capability of performing the single-ended to differential conversion. The ADA4941-1 is a low power (2.2 mA @ 3.3 V), low noise (10.2 nV/√Hz @ 1 kHz), low distortion (110 dBc @ 100 kHz) differential driver for ADCs up to 18 bits. Small signal bandwidth is 31 MHz. The amplifier has rail-to-rail output, high input impedance, and a user-adjustable gain.

The ADA4941-1 consists of two op amps. The lower one in the figure is configured as a non-committed non-inverting buffer (with external feedback resistor) and drives an inverting amplifier. The feedforward and feedback resistors for the inverting amplifier are included in the IC. Although there is extra phase shift and delay through the inverting amplifier, this does not introduce significant error at the frequencies of interest (up to 1 MHz or 2 MHz).

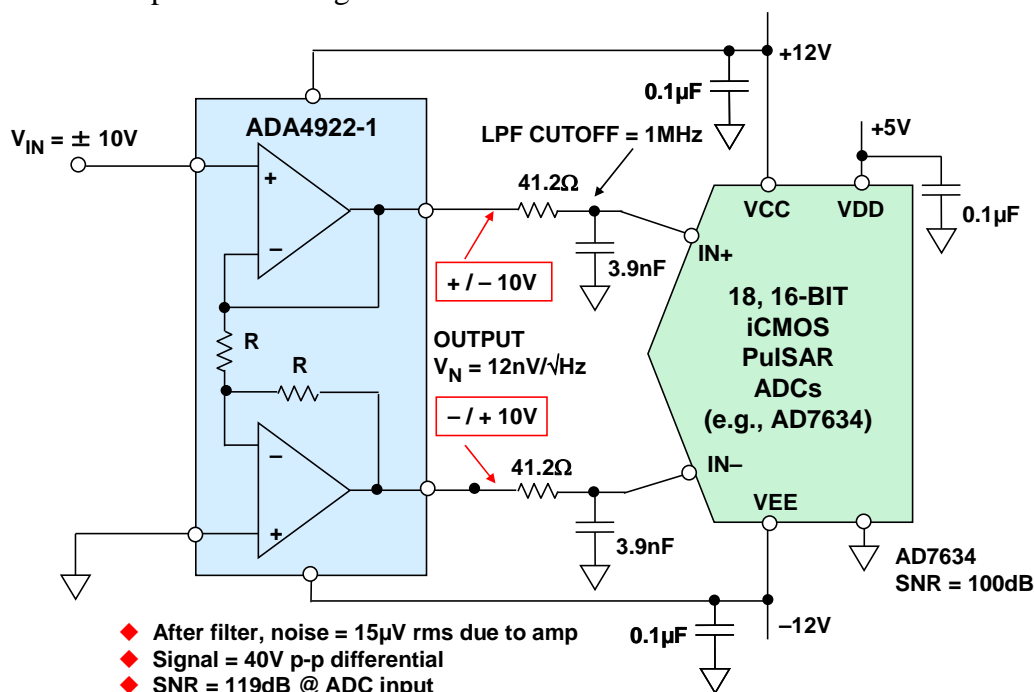


**Figure 3: [ADA4941-1](#) Driving [AD7690](#) 18-Bit PulSAR® ADC in +5V Application**

In this application, the two resistor dividers set the output common-mode voltage of the ADA4941-1 to +2.1 V so that the output only has to go to within 100 mV of ground. This allows sufficient headroom for the rail-to-rail output stages of the amplifier and allows the entire circuit to operate on a single +5 V supply.

The input range of the AD7690 and AD7691 is  $2 \cdot V_{REF}$  p-p differential. The reference used is the [ADR444](#) which is a 4.096 V reference. The  $41.2 \Omega$  resistors and the 3.9 nF capacitors for a lowpass filter with a cutoff frequency of 1 MHz, suitable for use with the AD7690 which has an input bandwidth of 9 MHz. The ADA4941-1 has an output noise spectral density of  $10.2 \text{ nV}/\sqrt{\text{Hz}}$  for the configuration selected. Integrated over the filter bandwidth, this is  $13 \mu\text{V rms}$ . This corresponds to an SNR due to the op amp of 107 dB, which is 7 dB better than the 100 dB SNR of the ADC.

Figure 4 shows another example of driving a high performance [iCMOS™](#) Pulsar™ ADC (e.g., [AD7634](#)). There are many industrial applications where signals as great as  $\pm 10 \text{ V}$  are standard. The iCMOS family of ADCs was developed to handle these applications. Most iCMOS Pulsar ADCs have differential inputs. Here, the [ADA4922-1](#) is driving a 16-bit or 18-bit iCMOS PulsAR ADC. It performs a single-ended to differential conversion.



**Figure 4: [ADA4922-1](#) Driving [AD7634](#) 18-Bit iCMOS PulsAR ADC in  $\pm 12\text{V}$  Industrial Application**

The ADA4922-1 is a differential driver for 16-bit to 18-bit ADCs that have differential input ranges up to 40 V p-p. Small signal bandwidth is 38 MHz. The ADA4922-1 is manufactured on ADI's proprietary second-generation XFCB process that enables the amplifier to achieve excellent noise and distortion performance on high supply voltages.

Noise calculations using the 1 MHz lowpass filter yield  $15 \mu\text{V rms}$  for the op amp. The signal range of the ADC is 40 V p-p, which is 14.14 V rms. This yields an SNR of 119 dB due to the op amp alone.

Using the AD7634 SNR of 100 dB, the rms ADC input noise contribution is calculated to be 141  $\mu\text{V}$  rms. The combined input ADC noise is therefore 142  $\mu\text{V}$  rms, and the contribution due to the op amp is almost negligible.

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