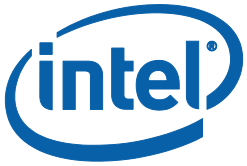

6th Generation Intel® Processor Family

Specification Update

Supporting 6th Generation Intel® Core™ Processor Families based on the H-Processor, S-Processor and Intel® Pentium® Processor

Supporting Intel® Xeon® Processor E3-1500 v5 Product Families based on the H-Platform

Supporting 6th Generation Intel® Core™ Processor Families based on Y-Processor Line, U-Processor Line, Intel® Pentium® Processor, and Intel® Celeron™ Processor

May 2016

Version 1.0

Document Number: 332689-007EN

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Contents

Revision History

Revision	Version	Description	Date
001	N/A	Initial release	July 2015
002	1.0	Updated Errata Chapter	August 2015
003	1.0	Title and Sub Title Changes Updated Processor lines Y/U/S/H S-SPECs Updated Table 7, H-Processor Line Errata Added: SKL054, SKL055, SKL056, SKL057, SKL058, SKL059, SKL060, SKL061, SKL062, SKL063, SKL064, SKL065, SKL066, SKL067, SKL068, SKL069, SKL070, SKL071, SKL072, SKL073, SKL074, SKL075, SKL076, SKL077, SKL078, SKL079, SKL080, SKL081, SKL082, SKL083, SKL084, SKL085, SKL086, SKL087, SKL088, SKL089, SKL090, SKL091, SKL093, SKL094, SKL095, SKL096, SKL097	January 2016
004	1.0	Updated Table 1, Errata Summary Table. Updated Table 5, U-Processor Updated Table 7, H-Processor Errata Added SKL099, SKL100, SKL103, SKL104, SKL105	March 2016
005	1.0	Updated Table 1, Errata Summary Table. Modified Table column headings. Added Table Notes 4 and 5 Updated Tables 4, 5, 6, 7 Updated Table 6 to add 6th Generation Intel® processor I7-6660U SKU	March 2016
006	1.0	Minor updates for clarity Errata Added: SKL106–SKL111	May 2016
007	1.0	Updated Table 7, H-Processor Line	May 2016

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number/Location
6th Generation Intel® Processor Datasheet for S-Platforms, Volume 1 of 2	332687
6th Generation Intel® Processor Datasheet for S-Platforms, Volume 2 of 2	332688
6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2	332986
6th Generation Intel® Processor Datasheet for H-Platforms, Volume 2 of 2	332987
6th Generation Intel® Processor Datasheet for U/Y Platforms, Volume 1 of 2	332990
6th Generation Intel® Processor Datasheet for U/Y Platforms, Volume 2 of 2	332991

Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm

Document Title	Document Number/Location
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architec-tures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

Nomenclature

Errata are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change, or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

Table 1. Errata Summary Table

Number	Stepping / Segment				Status	Title
	D-1	K-1	N-0	R-0, S-0		
SKL001	X			X	No Fix	Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures
SKL002	X			X	No Fix	Instruction Fetch May Cause Machine Check if Page Size and Memory Type Was Changed Without Invalidation
SKL003	X			X	No Fix	Execution of VAESIMC or VAESKEYGENASSIST With An Illegal Value for VEX.vvvv May Produce a #NM Exception
SKL004	X			X	No Fix	The Corrected Error Count Overflow Bit in IA32_MC0_STATUS is Not Updated When The UC Bit is Set
SKL005	X			X	No Fix	VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1
SKL006	X			X	No Fix	SMRAM State-Save Area Above the 4GB Boundary May Cause Unpredictable System Behavior
SKL007	X			X	No Fix	x87 FPU Exception (#MF) May be Signaled Earlier Than Expected
SKL008	X			X	No Fix	Incorrect FROM_IP Value For an RTM Abort in BTM or BTS May be Observed
SKL009	X			X	No Fix	DR6 Register May Contain an Incorrect Value When a MOV to SS or POP SS Instruction is Followed by an XBEGIN Instruction
SKL010	X			X	No Fix	Opcode Bytes F3 0F BC May Execute As TZCNT Even When TZCNT Not Enumerated by CPUID
SKL011	X			X	No Fix	PCIe* Root-port Initiated Compliance State Transmitter Equalization Settings May be Incorrect
SKL012	X			X	No Fix	The SMSW Instruction May Execute Within an Enclave
SKL013	X			X	No Fix	PEBS Record After a WRMSR to IA32_BIOS_UPDT_TRIG May be Incorrect
SKL014	X			X	No Fix	Intel® PT TIP.PGD May Not Have Target IP Payload
SKL015	X			X	No Fix	Operand-Size Override Prefix Causes 64-bit Operand Form of MOVBE Instruction to Cause a #UD
SKL016	X			X	No Fix	Execution of FXSAVE or FXRSTOR With the VEX Prefix May Produce a #NM Exception
SKL017	X			X	No Fix	WRMSR May Not Clear The Sticky Count Overflow Bit in The IA32_MCi_STATUS MSRs' Corrected Error Count Field
SKL018	X			X	No Fix	PEBS Eventing IP Field May be Incorrect After Not-Taken Branch
SKL019	X			X	No Fix	Debug Exceptions May Be Lost or Misreported Following WRMSR to IA32_BIOS_UPDT_TRIG
SKL020	X			X	No Fix	Attempts to Retrain a PCIe* Link May be Ignored
SKL021	X			X	No Fix	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
SKL022	X			X	No Fix	An APIC Timer Interrupt During Core C6 Entry May be Lost
SKL023	X			X	No Fix	Placing an Intel® PT ToPA in Non-WB Memory or Writing It Within a Transactional Region May Lead to System Instability

Number	Stepping / Segment				Status	Title
	D-1	K-1	N-0	R-0, S-0		
SKL024	X			X	No Fix	VM Entry That Clears TraceEn May Generate a FUP
SKL025		X			No Fix	EDRAM Corrected Error Events May Not be Properly Logged After a Warm Reset
SKL026	X			X	No Fix	Performance Monitor Event For Outstanding Offcore Requests And Snoop Requests May be Incorrect
SKL027	X			X	No Fix	Machine Check or Shutdown May Occur When Using The PECI RdIAMSR Command
SKL028	X			X	No Fix	ENCLU[EGETKEY] Ignores KEYREQUEST.MISCMASK
SKL029	X			X	No Fix	POPCNT Instruction May Take Longer to Execute Than Expected
SKL030	X			X	No Fix	ENCLU[EREPORT] May Cause a #GP When TARGETINFO.MISCSELECT is Non-Zero
SKL031	X			X	No Fix	A VMX Transition Attempting to Load a Non-Existent MSR May Result in a Shutdown
SKL032	X			X	No Fix	Transitions Out of 64-bit Mode May Lead to an Incorrect FDP And FIP
SKL033	X			X	No Fix	Intel® PT FUP May be Dropped After OVF
SKL034	X			X	No Fix	ENCLS[ECREATE] Causes #GP if Enclave Base Address is Not Canonical
SKL035	X			X	No Fix	Title: Data Breakpoint May Not be Detected on a REP MOVS
SKL036	X			X	No Fix	Processor Graphics IOMMU Unit May Report Spurious Faults
SKL037	X			X	No Fix	PCIe* and DMI Links With Lane Polarity Inversion May Result in Link Failure
SKL038	X			X	No Fix	PCIe* Expansion ROM Base Address Register May be Incorrect
SKL039	X			X	No Fix	PCIe* Perform Equalization May Lead to Link Failure
SKL040	X			X	No Fix	Two DIMMs Per Channel 2133 MHz DDR4 SODIMM Daisy-Chain Systems With Different Vendors May Hang
SKL041	X			X	No Fix	ENCLS[EINIT] Instruction May Unexpectedly #GP
SKL042	X			X	No Fix	Intel® PT OVF Packet May be Lost if Immediately Preceding a TraceStop
SKL043	X			X	No Fix	Detecting an Intel® PT Stopped or Error Condition Within an Intel® TSX Region May Result in a System Hang
SKL044	X			X	No Fix	WRMSR to IA32_BIOS_UPDT_TRIG May be Counted as Multiple Instructions
SKL045	X			X	No Fix	The x87 FIP May be Incorrect
SKL046	X			X	No Fix	Branch Instructions May Initialize MPX Bound Registers Incorrectly
SKL047	X			X	No Fix	Writing a Non-Canonical Value to an LBR MSR Does Not Signal a #GP When Intel® PT is Enabled
SKL048	X			X	No Fix	Processor May Run Intel® AVX Code Much Slower Than Expected
SKL049	X			X	No Fix	Intel® PT Buffer Overflow May Result in Incorrect Packets
SKL050	X			X	No Fix	Intel® PT PSB+ Packets May be Omitted on a C6 Transition

Number	Stepping / Segment				Status	Title
	D-1	K-1	N-0	R-0, S-0		
SKL051	X			X	No Fix	IA32_PERF_GLOBAL_STATUS.TRACE_TOPA_PMI Bit Cannot be Set by Software
SKL052 [1]	X			X	No Fix	CPUID Incorrectly Reports Bit Manipulation Instructions Support
SKL053 [2]	X			X	No Fix	Intel® Turbo Boost Technology May be Incorrectly Reported as Supported on Intel® Core™ i3 U/H/S, Select Intel® Mobile Pentium®, Intel® Mobile Celeron®, Select Intel® Pentium® G4xxx and Intel® Celeron® G3xxx Processors
SKL054	X			X	No Fix	TSX Abort May Result in Unpredictable System Behavior
SKL055	X			X	No Fix	Use of Prefetch Instructions May Lead to a Violation of Memory Ordering
SKL056	X			X	No Fix	CS Limit Violation May Not be Detected
SKL057	X			X	No Fix	Last Level Cache Performance Monitoring Events May Be Inaccurate
SKL058	X			X	No Fix	#GP Occurs Rather Than #DB on Code Page Split Inside an Intel® SGX Enclave
SKL059	X			X	No Fix	Execution of VAESENCLAST Instruction May Produce a #NM Exception Instead of a #UD Exception
SKL060	X			X	No Fix	Intel® SGX Enclave Accesses to the APIC-Access Page May Cause APIC-Access VM Exits
SKL061	X			X	No Fix	CR3 Filtering Does Not Compare Bits [11:5] of CR3 and IA32_RTIT_CR3_MATCH in PAE Paging Mode
SKL062	X			X	No Fix	Intel® PT PacketEn Change on C-state Wake May Not Generate a TIP Packet
SKL063	X			X	No Fix	Graphics Configuration May Not be Correctly Restored After a Package C8 Exit
SKL064	X			X	No Fix	x87 FDP Value May be Saved Incorrectly
SKL065	X			X	No Fix	PECI Frequency Limited to 1 MHz
SKL066	X			X	No Fix	Processor Graphics IOMMU Unit May Not Mask DMA Remapping Faults
SKL067 [3]				X	No Fix	Processor With Intel® SGX Support May Hang During S3 Wake or Power-On Reset
SKL068	X			X	No Fix	Audio Glitches May Occur After Reset or S3/S4 Exit
SKL069	X			X	No Fix	Intel® PT CYCThresh Value of 13 is Not Supported
SKL070	X			X	No Fix	Exx. Intel® PT May Drop Some Timing Packets After Entering Thread
SKL071	X			X	No Fix	Underflow and Denormal Conditions During a VDPPS Instruction With YMM Operands May Not Produce The Expected Results
SKL072	X			X	No Fix	IA Core Ratio Change Coincident With Outstanding Read to the DE May Cause a System Hang
SKL073	X			X	No Fix	Enabling VMX-Preemption Timer Blocks HDC Operation
SKL074	X			X	No Fix	Certain Processors May be Configured With an Incorrect TDP
SKL075	X			X	No Fix	Display Flicker May Occur When Both VT-d And FBC Are Enabled

Number	Stepping / Segment				Status	Title
	D-1	K-1	N-0	R-0, S-0		
SKL076	X			X	No Fix	System May Hang When Using Intel® TXT And Memory That Supports Address Mirroring
SKL077	X			X	No Fix	System May Hang or Reset During Processor Package C9 Exit
SKL078	X			X	No Fix	Integrated Audio Codec May Not be Detected
SKL079	X			X	No Fix	MOVNTDQA From WC Memory May Pass Earlier MFENCE Instructions
SKL080	X			X	No Fix	APIC Timer Interrupt May be Delivered Early
SKL081		X			No Fix	Processors That Support EDRAM May Not Initialize Properly
SKL082	X			X	No Fix	Processor May Hang And Log a Machine Check Error
SKL083	X	X			No Fix	The Processor May Fail to Properly Exit Package C6 or Deeper
SKL084	X			X	No Fix	Certain Processors May Report Incorrect DID2
SKL085	X			X	No Fix	System May Hang When Entering S3/S4/S5 State
SKL086	X			X	No Fix	Display Flickering May be Observed with Specific eDP Panels
SKL087	X			X	No Fix	x87 FPU Data Pointer Updated Only for Instructions That Incur Unmasked Exceptions
SKL088	X			X	No Fix	Incorrect Branch Predicted Bit in BTS/BTM Branch Records
SKL089	X			X	No Fix	MACHINE_CLEARS.MEMORY ORDERING Performance Monitoring Event May Undercount
SKL090	X			X	No Fix	Some Counters May Not Freeze On Performance Monitoring Interrupts
SKL091	X			X	No Fix	Instructions And Branches Retired Performance Monitoring Events May Overcount
SKL092						Deleted – Please refer to SKL057
SKL093	X	X		X	No Fix	REP MOVS May Not Operate Correctly With EPT Enabled
SKL094				X	No Fix	Ring Frequency Changes May Cause a Machine Check And System Hang
SKL095	X	X		X	No Fix	Some OFFCORE_RESPONSE Performance Monitoring Events May Overcount
SKL096	X	X		X	No Fix	Using BIOS to Disable Cores May Lead to a System Hang
SKL097	X	X		X	No Fix	#GP After RSM May Push Incorrect RFLAGS Value When Intel® PT is Enabled
SKL098						N/A
SKL099	X	X	X	X	No Fix	Access to SGX EPC Page in BLOCKED State is Not Reported as an SGX-Induced Page Fault
SKL100	X	X	X	X	No Fix	MTF VM Exit on XBEGIN Instruction May Save State Incorrectly
SKL101						N/A
SKL102						N/A
SKL103		X	X		No Fix	Enabling S3 on Processors With EDRAM May Cause Unpredictable System Behavior

Number	Stepping / Segment				Status	Title
	D-1	K-1	N-0	R-0, S-0		
SKL104	X	X	X	X	No Fix	PEBS Record May Be Generated After Being Disabled
SKL105	X	X	X	X	No Fix	Software Using Intel® TSX May Result in Unpredictable System Behavior
SKL106	X	X	X	X		Package-C6 Exit Latency May be Higher Than Expected Leading to Display Flicker
SKL107		X	X			EDRAM May Cause Unpredictable System Behavior
SKL108						PCIe* Port Does Not Support DLL Link Activity Reporting
SKL109	X	X	X	X		Enabling Package C8 State or Deeper May Lead to Display Flicker or a System Hang
SKL110		X	X			System May Hang When EDRAM is Enabled And DDR is Operating at 1600 MHz
SKL111	X	X	X	X		DR6.B0-B3 May Not Report All Breakpoints Matched When a MOV/POP SS is Followed by a Store or an MMX Instruction

Notes:

1. Affects 6th Generation Intel® Pentium® processor family and Intel® Celeron™ processor family.
2. Affects 6th Generation Intel® Core™ i3 U/H/S, Intel® Pentium®, Intel® Celeron™, Intel® Pentium® G4xxx and Intel® Celeron™ G3xxx Processors.
3. Affects 6th Generation Intel® Core™ i7 & i5 Desktop and Intel® Xeon® E3-1200 v5 Family Processors.
4. Processor line and Stepping information
   - Y-Processor Line stepping: D-1 (Mobile)
   - U-Processor Line stepping: D-1 (Mobile) / K-1 (Mobile)
   - H-Processor Line stepping: N-0 (Mobile/Desktop) / R-0 (Mobile/Desktop)
   - S-Processor Line stepping: R-0 (Desktop) / S-0 (Desktop)

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Identification Information

Component Identification via Programming Interface

The processor stepping can be identified by the following register contents:

Table 2. Y/U-Processor Lines Component Identification

Reserved	Extended Family	Extended Model	Reserved	Processor Type	Family Code	Model Number	Stepping ID
31:28	27:20	19:16	15:14	13:12	11:8	7:4	3:0
	0000000b	0100b		00b	0110b	1110b	xxxxb

Table 3. H/S-Processor Lines Component Identification

Reserved	Extended Family	Extended Model	Reserved	Processor Type	Family Code	Model Number	Stepping ID
31:28	27:20	19:16	15:14	13:12	11:8	7:4	3:0
	0000000b	0101b		00b	0110b	1110b	xxxxb

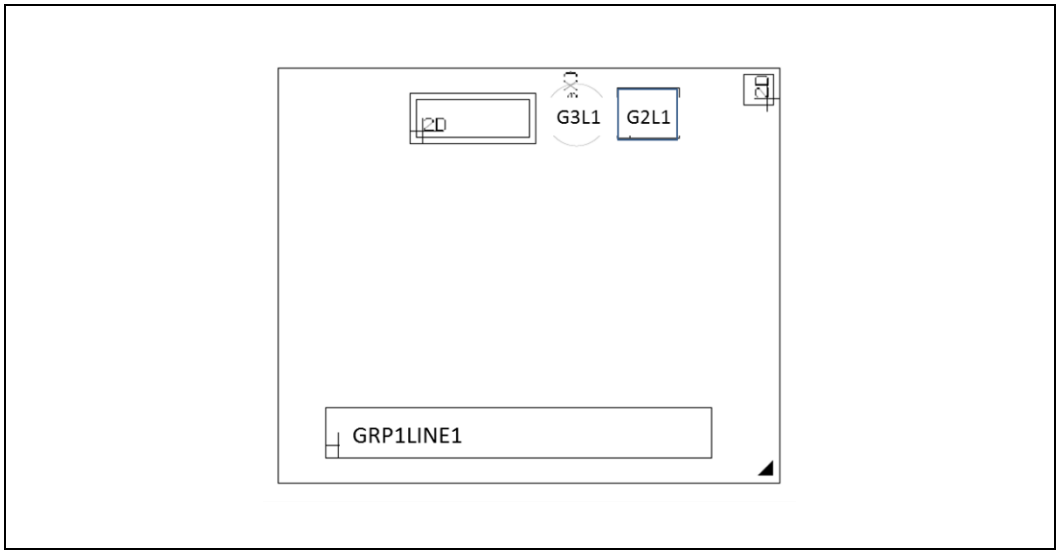
Notes:

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium 4, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. See Table 1 for the processor stepping ID number in the CPUID information.
6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX, and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

Component Marking Information

Figure 1. Y-Processor Line BGA Top-Side Markings



Pin Count: 1515 Package Size: 20 mm x 16.5 mm

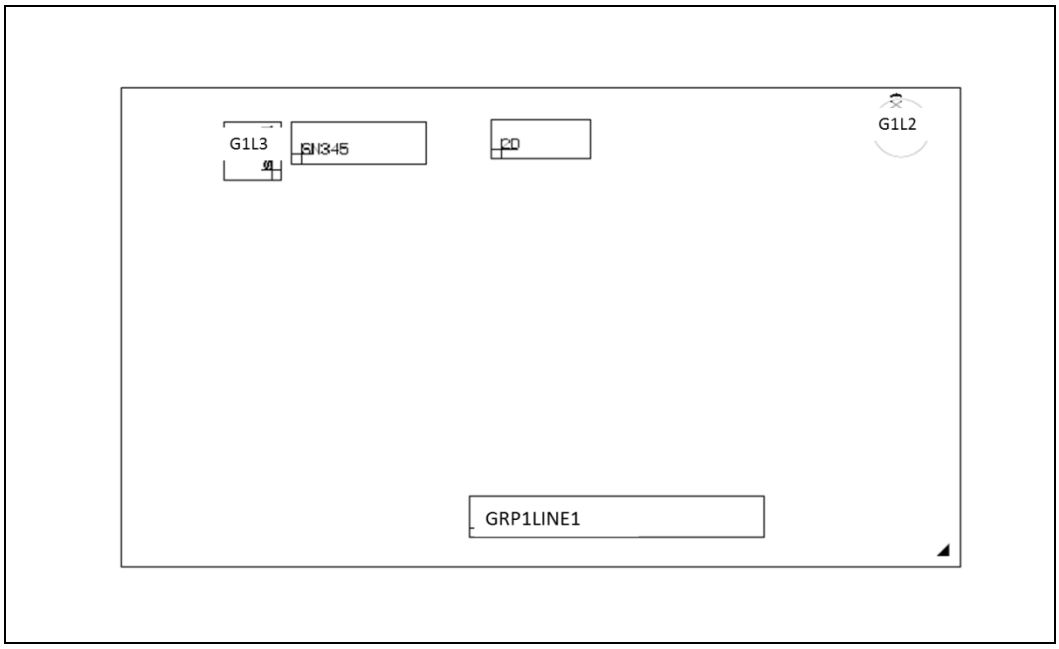
Production (SSPEC):

GRP1LINE1: FPOxxxxxSSPEC
GRP2LINE1 (G2L1): Intel logo
GRP3LINE1 (G3L1): {eX}

Table 4. Y-Processor Line

S-Spec #	Processor Number	Step-ping	Cache Size (MB)	Func-tional Core	Processor Graphics Cores	Processor Graphics Freq. (MHz)	Processor Graphics Turbo Freq. (MHz)	DDR3L Mem. (MHz)	LPDDR3 Mem. (MHz)	Core Freq. (MHz)	Turbo 1 Core Freq. Rate (MHz)	Thermal Design Power (W)	Slot / Socket Type
SR2ER	Pentium 4405Y	D-1	2	2	2	300	800	1600	1866	1500	1500	6	BGA1515
SR2EN	m3-6Y30	D-1	4	2	2	300	850	1600	1866	900	2200	4.5	BGA1515
SR2EM	m5-6Y54	D-1	4	2	2	300	900	1600	1866	1100	2700	4.5	BGA1515
SR2EH	m7-6Y75	D-1	4	2	2	300	1000	1600	1866	1200	3100	4.5	BGA1515
SR2EG	m5-6Y57	D-1	4	2	2	300	900	1600	1866	1100	2800	4.5	BGA1515

Figure 2. U-Processor Line BGA Top-Side Markings



Pin Count: 1356 Package Size: 42 mm x 24 mm

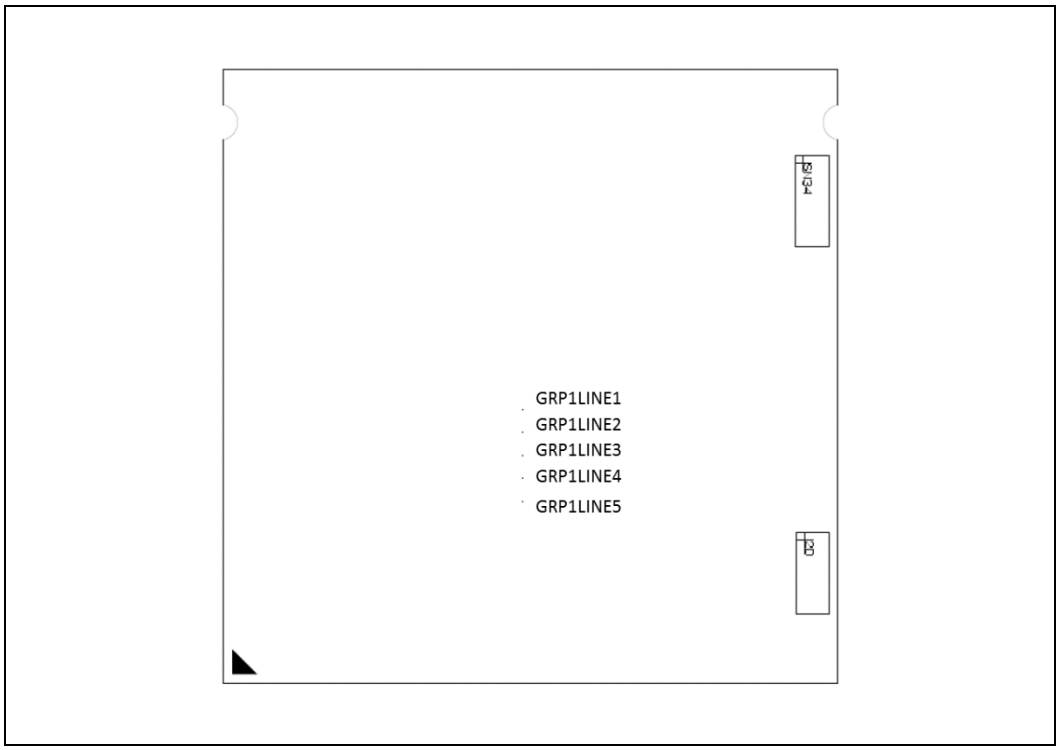
Sample (SSPEC):

GRP1LINE1: FPOxxxxxQxxx
GRP2LINE1 (G2L1): {eX}
GRP3LINE1 (G3L1): Intel logo

Table 5. U-Processor Line

S-Spec #	Processor Number	Step-ping	Cache Size (MB)	Func tional Core	Processor Graphics Cores	Processor Graphics Freq. (MHz)	Processor Graphics Turbo Freq. (MHz)	DDR3L Mem. (MHz)	DDR4 Mem. (MHz)	LPDDR3 Mem. (MHz)	Core Freq. (MHz)	Turbo 1 Core Freq. Rate (MHz)	Thermal Design Power (W)	Slot / Socket Type
SR2F0	i5-6300U	D-1	3	2	2	300	1000	1600	2133	1866	2400	3000	15	BGA1356
SR2F1	i7-6600U	D-1	4	2	2	300	1050	1600	2133	1866	2600	3400	15	BGA1356
SR2EY	i5-6200U	D-1	3	2	2	300	1000	1600	2133	1866	2300	2800	15	BGA1356
SR2EZ	i7-6500U	D-1	4	2	2	300	1050	1600	2133	1866	2500	3100	15	BGA1356
SR2EX	Pentium 4405U	D-1	2	2	1	300	950	1600	2133	1866	2100	2100	15	BGA1356
SR2EV	Celeron 3855U	D-1	2	2	1	300	900	1600	2133	1866	1600	1600	15	BGA1356
SR2EW	Celeron 3955U	D-1	2	2	1	300	900	1600	2133	1866	2000	2000	15	BGA1356
SR2EU	i3-6100U	D-1	3	2	2	300	1000	1600	2133	1866	2300	2300	15	BGA1356
SR2JB	I7-6560U	K-1	4	2	3	300	1050	1600	2133	1866	2200	3200	15	BGA1356
SR2JC	I5-6260U	K-1	4	2	3	300	950	1600	2133	1866	1800	2900	15	BGA1356
SR2JF	I3-6167U	K-1	3	2	3	300	1000	1600	2133	1866	2700	2700	28	BGA1356
SR2JH	I7-6567U	K-1	4	2	3	300	1100	1600	2133	1866	3300	3600	28	BGA1356
SR2JJ	I5-6287U	K-1	4	2	3	300	1100	1600	2133	1866	3100	3500	28	BGA1356
SR2JK	I5-6267U	K-1	4	2	3	300	1050	1600	2133	1866	2900	3300	28	BGA1356
SR2JM	I5-6360U	K-1	4	2	3	300	1000	1600	2133	1866	2000	3100	15	BGA1356
SR2KA	I7-6650U	K-1	4	2	3	300	1050	1600	2133	1866	2200	3400	15	BGA1356
SR2JL	I7-6660U	K-1	4	2	3	300	1050	1600	2133	1866	2400	3400	15	BGA1356

Figure 3. S-Processor Line LGA Top-Side Markings



Pin Count: 1151 Package Size: 37.5 mm x 37.5 mm

Sample (SSPEC):

GRP1LINE1:	Intel logo
GRP1LINE2:	BRAND
GRP1LINE3:	PROC#
GRP1LINE4:	SSPEC SPEED
GRP1LINE5:	{FPO} {eX}

Table 6. S-Processor Line

S-Spec #	Processor Number	Step-ping	Cache Size (MB)	Func-tional Core	Processor Graphics Cores	Processor Graphics Freq. (MHz)	Processor Graphics Turbo Freq. (MHz)	DDR4 Mem. (MHz)	DDR3L Mem. (MHz)	Core Freq. (MHz)	Turbo 1 Core Freq. Rate (MHz)	Thermal Design Power (W)	Slot / Socket Type
SR2BR[1]	i7-6700K	R-0	8	4	2	350	1150	2133	1600	4000	4200	91	LGA1151
SR2BS[1]	i5-6400T	R-0	6	4	2	350	950	2133	1600	2200	2800	35	LGA1151
SR2BT[1]	i7-6700	R-0	8	4	2	350	1150	2133	1600	3400	4000	65	LGA1151
SR2BU[1]	i7-6700T	R-0	8	4	2	350	1100	2133	1600	2800	3600	35	LGA1151
SR2BV[1]	i5-6600K	R-0	6	4	2	350	1150	2133	1600	3500	3900	91	LGA1151
SR2BW[1]	i5-6600	R-0	6	4	2	350	1150	2133	1600	3300	3900	65	LGA1151
SR2BX[1]	i5-6500	R-0	6	4	2	350	1050	2133	1600	3200	3600	65	LGA1151
SR2BY[1]	i5-6400	R-0	6	4	2	350	950	2133	1600	2700	3300	65	LGA1151
SR2BZ[1]	i5-6500T	R-0	6	4	2	350	1100	2133	1600	2500	3100	35	LGA1151
SR2C0[1]	i5-6600T	R-0	6	4	2	350	1100	2133	1600	2700	3500	35	LGA1151
SR2L0	I7-6700K	R-0	8	4	2	350	1150	2133	1600	4000	4100	95	LGA1151
SR2L1	I5-6400T	R-0	6	4	2	350	950	2133	1600	2200	2800	35	LGA1151
SR2L2	I7-6700	R-0	8	4	2	350	1150	2133	1600	3400	4000	65	LGA1151
SR2L3	I7-6700T	R-0	8	4	2	350	1100	2133	1600	2800	3600	35	LGA1151
SR2L4	I5-6600K	R-0	6	4	2	350	1150	2133	1600	3500	3900	95	LGA1151
SR2L5	I5-6600	R-0	6	4	2	350	1150	2133	1600	3300	3900	65	LGA1151
SR2L6	I5-6500	R-0	6	4	2	350	1050	2133	1600	3200	3600	65	LGA1151
SR2L7	I5-6400	R-0	6	4	2	350	950	2133	1600	2700	3300	65	LGA1151
SR2L8	I5-6500T	R-0	6	4	2	350	1100	2133	1600	2500	3100	35	LGA1151
SR2L9	I5-6600T	R-0	6	4	2	350	1100	2133	1600	2700	3500	35	LGA1151
SR2H9	i3-6320	S-0	4	2	2	350	1150	2133	1600	3900	N/A	51	LGA1151
SR2HA	i3-6300	S-0	4	2	2	350	1150	2133	1600	3800	N/A	51	LGA1151
SR2HG	i3-6100	S-0	3	2	2	350	1050	2133	1600	3700	N/A	51	LGA1151
SR2HM	G4520	S-0	3	2	2	350	1050	2133	1600	3600	N/A	51	LGA1151
SR2HJ	G4500	S-0	3	2	2	350	1050	2133	1600	3500	N/A	51	LGA1151
SR2DC	Pentium G4400	R-0	3	4	2	350	1000	2133	1600	3300	N/A	65	LGA1151
SR2HD	i3-6300T	S-0	4	2	2	350	950	2133	1600	3300	N/A	35	LGA1151
SR2HE	i3-6100T	S-0	3	2	2	350	950	2133	1600	3200	N/A	35	LGA1151
SR2HS	G4500T	S-0	3	2	2	350	950	2133	1600	3000	N/A	35	LGA1151

S-Spec #	Processor Number	Step-ping	Cache Size (MB)	Func-tional Core	Processor Graphics Cores	Processor Graphics Freq. (MHz)	Processor Graphics Turbo Freq. (MHz)	DDR4 Mem. (MHz)	DDR3L Mem. (MHz)	Core Freq. (MHz)	Turbo 1 Core Freq. Rate (MHz)	Thermal Design Power (W)	Slot / Socket Type
SR2HC	I3-6320T	S-0	4	2	2	350	950	2133	1600	3400	N/A	35	LGA1151
SR2HQ	G4400T	S-0	3	2	1	350	950	2133	1600	2900	N/A	35	LGA1151
SR2HK	Pentium G4400	S-0	3	2	1	350	1000	2133	1600	3300	N/A	65	LGA1151
SR2HT	Celeron G3900T	S-0	2	2	1	350	950	2133	1600	2600	N/A	35	LGA1151
SR2HV	Celeron G3900	S-0	2	2	1	350	950	2133	1600	2800	N/A	65	LGA1151
SR2HX	Celeron G3920	S-0	2	2	1	350	950	2133	1600	2900	N/A	65	LGA1151

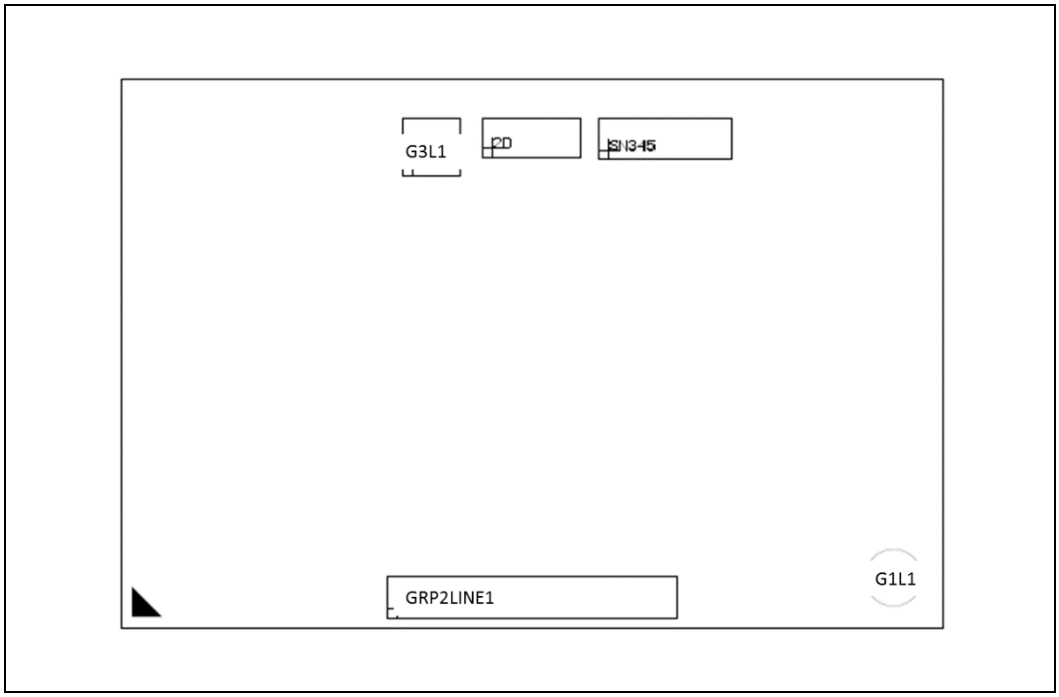
Notes:

1. The following S-Spec is affected by erratum SKL067 which is being addressed by Product Change Notification (PCN) #114074.
2. Intel is initiating new S-Spec and MM numbers for 6th Generation Intel® Core™ i7 & i5 desktop and the Intel® Xeon® E3-1200 v5 family processors for a minor manufacturing configuration change to allow customers to enable Intel® Software Guard Extensions (Intel® SGX) when using these processors.

    - The stepping will not change for these processors; it remains R-0.
    - The CPUID Processor Signature will not change for these processors; it remains 0x506E3.
    - Die size and package will not change for these processors.
    - Link to SKL-S 4+2 PCN #114074 (Product Change Notification) for new S-Specs:

    http://qdms.intel.com/dm/i.aspx/5A160770-FC47-47A0-BF8A-062540456F0A/PCN114074-00.pdf

Figure 4. H-Processor Line BGA Top-Side Markings



Pin Count: 1440 Package Size: 42 mm x 28 mm

Production (SSPEC):

GRP1LINE1 (G1L1): {eX}
GRP2LINE1: FPOxxxxxSSPEC
GRP3LINE1 (G3L1): Intel logo

Table 7. H-Processor Line

S-Spec #	Processor Number	Step-ping	Cache Size (MB)	Func tional Core	Processor Graphics Cores	Processor Graphics Freq. (MHz)	Processor Graphics Turbo Freq. (MHz)	DDR3L Mem. (MHz)	DDR4 Mem. (MHz)	LPDDR3 Mem. (MHz)	Core Freq. (MHz)	Turbo 1 Core Freq. Rate (MHz)	Thermal Design Power (W)	Slot / Socket Type
SR2FM	E3-1535MV5	R-0	8	4	2	350	1050	1600	2133	1866	2900	3800	45	BGA1440
SR2FT	i7-6920HQ	R-0	8	4	2	350	1050	1600	2133	1866	2900	3800	45	BGA1440
SR2FN	E3-1505MV5	R-0	8	4	2	350	1050	1600	2133	1866	2800	3700	45	BGA1440
SR2FU	i7-6820HQ	R-0	8	4	2	350	1050	1600	2133	1866	2700	3600	45	BGA1440
SR2FL	i7-6820HK	R-0	8	4	2	350	1050	1600	2133	1866	2700	3600	45	BGA1440
SR2FQ	i7-6700HQ	R-0	6	4	2	350	1050	1600	2133	1866	2600	3500	45	BGA1440
SR2FS	i5-6440HQ	R-0	6	4	2	350	950	1600	2133	1866	2600	3500	45	BGA1440
SR2FP	i5-6300HQ	R-0	6	4	2	350	950	1600	2133	1866	2300	3200	45	BGA1440
SR2FR	i3-6100H	R-0	3	2	2	350	900	1600	2133	1866	2700	2700	35	BGA1440
SR2QT	E3-1515MV5	N-0	8	4	4	350	1000	1600	2133	1866	2800	3700	45	BGA1440
SR2QU	E3-1545MV5	N-0	8	4	4	350	1050	1600	2133	1866	2900	3800	45	BGA1440
SR2QV	E3-1575MV5	N-0	8	4	4	350	1100	1600	2133	1866	3000	3900	45	BGA1440
SR2R8	E3-1565LV5	N-0	8	4	4	350	1050	1600	2133	1866	2500	3500	35	BGA1440
SR2R9	E3-1585LV5	N-0	8	4	4	350	1150	1600	2133	1866	3000	3700	45	BGA1440
SR2RB	E3-1585V5	N-0	8	4	4	350	1150	1600	2133	1866	3500	3900	65	BGA1440
SR2TT	E3-1578V5	N-0	8	4	4	700	1000	1600	2133	1866	2000	3400	45	BGA1440
SR2TU	E3-1558LV5	N-0	8	4	3	650	1000	1600	2133	1866	1900	3300	45	BGA1440
SR2QW	i7-6970HQ	N-0	8	4	4	350	1050	1600	2133	1866	2800	3700	45	BGA1440
SR2QX	i7-6870HQ	N-0	8	4	4	350	1000	1600	2133	1866	2700	3600	45	BGA1440
SR2QY	i7-6770HQ	N-0	6	4	4	350	950	1600	2133	1866	2600	3500	45	BGA1440
SR2QZ	I5-6350HQ	N-0	6	4	4	350	900	1600	2133	1866	2300	3200	45	BGA1440

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Errata

SKL001	**Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures**
Problem	Bits 53:50 of the IA32_VMX_BASIC MSR report the memory type that the processor uses to access the VMCS and data structures referenced by pointers in the VMCS. Due to this erratum, a VMX access to the VMCS or referenced data structures will instead use the memory type that the MTRRs (memory-type range registers) specify for the physical address of the access.
Implication	Bits 53:50 of the IA32_VMX_BASIC MSR report that the WB (write-back) memory type will be used but the processor may use a different memory type.
Workaround	Software should ensure that the VMCS and referenced data structures are located at physical addresses that are mapped to WB memory type by the MTRRs.
Status	For the steppings affected, see the Summary Table of Changes.

SKL002	**Instruction Fetch May Cause Machine Check if Page Size and Memory Type Was Changed Without Invalidation**
Problem	This erratum may cause a machine-check error (IA32_MCi_STATUS.MCACOD=0150H) on the fetch of an instruction that crosses a 4-KByte address boundary. It applies only if (1) the 4-KByte linear region on which the instruction begins is originally translated using a 4-KByte page with the WB memory type; (2) the paging structures are later modified so that linear region is translated using a large page (2-MByte, 4-MByte, or 1-GByte) with the UC memory type; and (3) the instruction fetch occurs after the paging-structure modification but before software invalidates any TLB entries for the linear region.
Implication	Due to this erratum an unexpected machine check with error code 0150H may occur, possibly resulting in a shutdown. Intel has not observed this erratum with any commercially available software.
Workaround	Software should not write to a paging-structure entry in a way that would change, for any linear address, both the page size and the memory type. It can instead use the following algorithm: first clear the P flag in the relevant paging-structure entry (e.g., PDE); then invalidate any translations for the affected linear addresses; and then modify the relevant paging-structure entry to set the P flag and establish the new page size and memory type.
Status	For the steppings affected, see the Summary Table of Changes.

SKL003	**Execution of VAESIMC or VAESKEYGENASSIST With An Illegal Value for VEX.vvvv May Produce a #NM Exception**
Problem	The VAESIMC and VAESKEYGENASSIST instructions should produce a #UD (Invalid-Opcode) exception if the value of the vvvv field in the VEX prefix is not 1111b. Due to this erratum, if CR0.TS is "1", the processor may instead produce a #NM (Device-Not-Available) exception.
Implication	Due to this erratum, some undefined instruction encodings may produce a #NM instead of a #UD exception.

Workaround	Software should always set the vvvv field of the VEX prefix to 1111b for instances of the VAESIMC and VAESKEYGENASSIST instructions.
Status	For the steppings affected, see the Summary Table of Changes.

SKL004	**The Corrected Error Count Overflow Bit in IA32_ MC0_STATUS is Not Updated When The UC Bit is Set**
Problem	After a UC (uncorrected) error is logged in the IA32_MC0_STATUS MSR (401H), corrected errors will continue to be counted in the lower 14 bits (bits 51:38) of the Corrected Error Count. Due to this erratum, the sticky count overflow bit (bit 52) of the Corrected Error Count will not get updated when the UC bit (bit 61) is set to 1.
Implication	The Corrected Error Count Overflow indication will be lost if the overflow occurs after an uncorrectable error has been logged.
Workaround	None identified
Status	For the steppings affected, see the Summary Table of Changes.

SKL005	**VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1**
Problem	When "XD Bit Disable" in the IA32_MISC_ENABLE MSR (1A0H) bit 34 is set to 1, it should not be possible to enable the "execute disable" feature by setting IA32_EFER.NXE. Due to this erratum, a VM exit that occurs with the 1-setting of the "load IA32_EFER" VM-exit control may set IA32_EFER.NXE even if IA32_MISC_ENABLE bit 34 is set to 1. This erratum can occur only if IA32_MISC_ENABLE bit 34 was set by guest software in VMX non-root operation.
Implication	Software in VMX root operation may execute with the "execute disable" feature enabled despite the fact that the feature should be disabled by the IA32_MISC_ENABLE MSR. Intel has not observed this erratum with any commercially available software.
Workaround	A virtual-machine monitor should not allow guest software to write to the IA32_MISC_ENABLE MSR
Status	For the steppings affected, see the Summary Table of Changes.

SKL006	**SMRAM State-Save Area Above the 4GB Boundary May Cause Unpredictable System Behavior**
Problem	If BIOS uses the RSM instruction to load the SMBASE register with a value that would cause any part of the SMRAM state-save area to have an address above 4-GBytes, subsequent transitions into and out of SMM (system-management mode) might save and restore processor state from incorrect addresses.
Implication	This erratum may cause unpredictable system behavior. Intel has not observed this erratum with any commercially available system.
Workaround	Ensure that the SMRAM state-save area is located entirely below the 4GB address boundary.
Status	For the steppings affected, see the Summary Table of Changes.

SKL007	x87 FPU Exception (#MF) May be Signaled Earlier Than Expected
Problem	x87 instructions that trigger #MF normally service interrupts before the #MF. Due to this erratum, if an instruction that triggers #MF is executing when an Enhanced Intel SpeedStep® Technology transitions, an Intel® Turbo Boost Technology transitions, or a Thermal Monitor events occurs, the #MF may be taken before pending interrupts are serviced.
Implication	Software may observe #MF being signaled before pending interrupts are serviced.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL008	Incorrect FROM_IP Value For an RTM Abort in BTM or BTS May be Observed
Problem	During RTM (Restricted Transactional Memory) operation when branch tracing is enabled using BTM (Branch Trace Message) or BTS (Branch Trace Store), the incorrect EIP value (From_IP pointer) may be observed for an RTM abort.
Implication	Due to this erratum, the From_IP pointer may be the same as that of the immediately preceding taken branch.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL009	DR6 Register May Contain an Incorrect Value When a MOV to SS or POP SS Instruction is Followed by an XBEGIN Instruction
Problem	If XBEGIN is executed immediately after an execution of MOV to SS or POP SS, a transactional abort occurs and the logical processor restarts execution from the fallback instruction address. If execution of the instruction at that address causes a debug exception, bits [3:0] of the DR6 register may contain an incorrect value.
Implication	When the instruction at the fallback instruction address causes a debug exception, DR6 may report a breakpoint that was not triggered by that instruction, or it may fail to report a breakpoint that was triggered by the instruction.
Workaround	Avoid following a MOV SS or POP SS instruction immediately with an XBEGIN instruction.
Status	For the steppings affected, see the Summary Table of Changes.

SKL010	Opcode Bytes F3 0F BC May Execute As TZCNT Even When TZCNT Not Enumerated by CPUID
Problem	If CPUID.(EAX=07H, ECX=0):EBX.BMI1 (bit 3) is 1 then opcode bytes F3 0F BC should be interpreted as TZCNT otherwise they will be interpreted as REP BSF. Due to this erratum, opcode bytes F3 0F BC may execute as TZCNT even if CPUID.(EAX=07H, ECX=0):EBX.BMI1 (bit 3) is 0.
Implication	Software that expects REP prefix before a BSF instruction to be ignored may not operate correctly since there are cases in which BSF and TZCNT differ with regard to the flags that are set and how the destination operand is established.
Workaround	Software should use the opcode bytes F3 0F BC only if CPUID.(EAX=07H, ECX=0):EBX.BMI1 (bit 3) is 1 and only if the functionality of TZCNT (and not BSF) is desired.

Status	For the steppings affected, see the Summary Table of Changes.

SKL011	**PCIe* Root-port Initiated Compliance State Transmitter Equalization Settings May be Incorrect**
Problem	If the processor is directed to enter PCIe Polling.Compliance at 5.0 GT/s or 8.0 GT/s transfer rates, it should use the Link Control 2 Compliance Preset/De-emphasis field (bits [15:12]) to determine the correct de-emphasis level. Due to this erratum, when the processor is directed to enter Polling.Compliance from 2.5 GT/s transfer rate, it retains 2.5 GT/s de-emphasis values.
Implication	The processor may operate in Polling.Compliance mode with an incorrect transmitter de-emphasis level.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL012	**The SMSW Instruction May Execute Within an Enclave**
Problem	The SMSW instruction is illegal within an SGX (Software Guard Extensions) enclave, and an attempt to execute it within an enclave should result in a #UD (invalid-opcode exception). Due to this erratum, the instruction executes normally within an enclave and does not cause a #UD.
Implication	The SMSW instruction provides access to CR0 bits 15:0 and will provide that information inside an enclave. These bits include NE, ET, TS, EM, MP and PE.
Workaround	None identified. If SMSW execution inside an enclave is unacceptable, system software should not enable SGX.
Status	For the steppings affected, see the Summary Table of Changes.

SKL013	**PEBS Record After a WRMSR to IA32_BIOS_UPDT_TRIG May be Incorrect**
Problem	A PEBS record generated by a WRMSR to IA32_BIOS_UPDT_TRIG MSR (79H) may have an incorrect value in the Eventing EIP field if an instruction prefix was used on the WRMSR.
Implication	The Eventing EIP field of the generated PEBS record may be incorrect. Intel has not observed this erratum with any commercially available software.
Workaround	Instruction prefixes have no architecturally-defined function for the WRMSR instruction; instruction prefixes should not be used with the WRMSR instruction.
Status	For the steppings affected, see the Summary Table of Changes.

SKL014	**Intel® PT TIP.PGD May Not Have Target IP Payload**
Problem	When Intel PT (Intel Processor Trace) is enabled and a direct unconditional branch clears IA32_RTIT_STATUS.FilterEn (MSR 571H, bit 0), due to this erratum, the resulting TIP.PGD (Target IP Packet, Packet Generation Disable) may not have an IP payload with the target IP.
Implication	It may not be possible to tell which instruction in the flow caused the TIP.PGD using only the information in trace packets when this erratum occurs.
Workaround	The Intel PT trace decoder can compare direct unconditional branch targets in the

	source with the FilterEn address range(s) to determine which branch cleared FilterEn.
Status	For the steppings affected, see the Summary Table of Changes.

SKL015	**Operand-Size Override Prefix Causes 64-bit Operand Form of MOVBE Instruction to Cause a #UD**
Problem	Execution of a 64 bit operand MOVBE instruction with an operand-size override instruction prefix (66H) may incorrectly cause an invalid-opcode exception (#UD).
Implication	A MOVBE instruction with both REX.W=1 and a 66H prefix will unexpectedly cause an #UD (invalid-opcode exception). Intel has not observed this erratum with any commercially available software.
Workaround	Do not use a 66H instruction prefix with a 64-bit operand MOVBE instruction.
Status	For the steppings affected, see the Summary Table of Changes.

SKL016	**Execution of FXSAVE or FXRSTOR With the VEX Prefix May Produce a #NM Exception**
Problem	Attempt to use FXSAVE or FXRSTOR with a VEX prefix should produce a #UD (Invalid-Opcode) exception. If either the TS or EM flag bits in CR0 are set, a #NM (device-not-available) exception will be raised instead of #UD exception.
Implication	Due to this erratum a #NM exception may be signaled instead of a #UD exception on an FXSAVE or an FXRSTOR with a VEX prefix.
Workaround	Software should not use FXSAVE or FXRSTOR with the VEX prefix.
Status	For the steppings affected, see the Summary Table of Changes.

SKL017	**WRMSR May Not Clear The Sticky Count Overflow Bit in The IA32_MCi_STATUS MSRs' Corrected Error Count Field**
Problem	The sticky count overflow bit is the most significant bit (bit 52) of the Corrected Error Count Field (bits[52:38]) in IA32_MCi_STATUS MSRs. Once set, the sticky count overflow bit may not be cleared by a WRMSR instruction. When this occurs, that bit can only be cleared by power-on reset.
Implication	Software that uses the Corrected Error Count field and expects to be able to clear the sticky count overflow bit may misinterpret the number of corrected errors when the sticky count overflow bit is set. This erratum does not affect threshold-based CMCI (Corrected Machine Check Error Interrupt) signaling.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL018	**PEBS Eventing IP Field May be Incorrect After Not-Taken Branch**
Problem	When a PEBS (Precise-Event-Based-Sampling) record is logged immediately after a not-taken conditional branch (Jcc instruction), the Eventing IP field should contain the address of the first byte of the Jcc instruction. Due to this erratum, it may instead contain the address of the instruction preceding the Jcc instruction.
Implication	Performance monitoring software using PEBS may incorrectly attribute PEBS events that occur on a Jcc to the preceding instruction.

Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL019	**Debug Exceptions May Be Lost or Misreported Following WRMSR to IA32_BIOS_UPDT_TRIG**
Problem	If the WRMSR instruction writes to the IA32_BIOS_UPDT_TRIG MSR (79H) immediately after an execution of MOV SS or POP SS that generated a debug exception, the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information.
Workaround	Software should avoid using WRMSR instruction immediately after executing MOV SS or POP SS
Status	For the steppings affected, see the Summary Table of Changes.

SKL020	**Attempts to Retrain a PCIe* Link May be Ignored**
Problem	A PCIe link should retrain when Retrain Link (bit 5) in the Link Control register (Bus 0; Device 1; Functions 0,1,2; Offset 0xB0) is set. Due to this erratum, if the link is in the L1 state, it may ignore the retrain request.
Implication	The PCIe link may not behave as expected.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL021	**Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets**
Problem	Some Intel Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.
Implication	Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.
Workaround	Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.
Status	For the steppings affected, see the Summary Table of Changes.

SKL022	**An APIC Timer Interrupt During Core C6 Entry May be Lost**
Problem	Due to this erratum, an APIC timer interrupt coincident with the core entering C6 state may be lost rather than held for servicing later.
Implication	A lost APIC timer interrupt may lead to missed deadlines or a system hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL023	Placing an Intel® PT ToPA in Non-WB Memory or Writing It Within a Transactional Region May Lead to System Instability
Problem	If an Intel PT (Intel® Processor Trace) ToPA (Table of Physical Addresses) is not placed in WB (writeback) memory or is written by software executing within an Intel® TSX (Intel® Transactional Synchronization Extension) transactional region, the system may become unstable.
Implication	Unusual treatment of the ToPA may lead to system instability.
Workaround	None identified. Intel PT ToPA should reside in WB memory and should not be written within a Transactional Region.
Status	For the steppings affected, see the Summary Table of Changes.

SKL024	VM Entry That Clears TraceEn May Generate a FUP
Problem	If VM entry clears Intel® PT (Intel Processor Trace) IA32_RTIT_CTL.TraceEn (MSR 570H, bit 0) while PacketEn is 1 then a FUP (Flow Update Packet) will precede the TIP.PGD (Target IP Packet, Packet Generation Disable). VM entry can clear TraceEn if the VM-entry MSR-load area includes an entry for the IA32_RTIT_CTL MSR.
Implication	When this erratum occurs, an unexpected FUP may be generated that creates the appearance of an asynchronous event taking place immediately before or during the VM entry.
Workaround	The Intel PT trace decoder may opt to ignore any FUP whose IP matches that of a VM entry instruction.
Status	For the steppings affected, see the Summary Table of Changes.

SKL026	Performance Monitor Event For Outstanding Offcore Requests And Snoop Requests May be Incorrect
Problem	The performance monitor event OFFCORE_REQUESTS_OUTSTANDING (Event 60H, any Umask Value) should count the number of offcore outstanding transactions each cycle. Due to this erratum, the counts may be higher or lower than expected.
Implication	The performance monitor event OFFCORE_REQUESTS_OUTSTANDING may reflect an incorrect count.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL027	Machine Check or Shutdown May Occur When Using The PECI RdIAMSR Command
Problem	Under certain circumstances, reading a core Machine Check register using the PECI (Platform Environmental Control Interface) RdIAMSR command may result in a Machine Check or Shutdown.
Implication	Machine Check or Shutdown may be observed.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL028	ENCLU[EGETKEY] Ignores KEYREQUEST.MISCMASK
Problem	The Intel® SGX (Software Guard Extensions) ENCLU[EGETKEY] instruction ignores the MISCMASK field in KEYREQUEST structure when computing a provisioning key, a provisioning seal key, or a seal key.
Implication	ENCLU[EGETKEY] will return the same key in response to two requests that differ only in the value of KEYREQUEST.MISCMASK. Intel has not observed this erratum with any commercially available software.
Workaround	When executing the ENCLU[EGETKEY] instruction, software should ensure the bits set in KEYREQUEST.MISCMASK are a subset of the bits set in the current SECS's MISCSELECT field.
Status	For the steppings affected, see the Summary Table of Changes.

SKL029	POPCNT Instruction May Take Longer to Execute Than Expected
Problem	POPCNT instruction execution with a 32 or 64 bit operand may be delayed until previous non-dependent instructions have executed.
Implication	Software using the POPCNT instruction may experience lower performance than expected.
Workaround	None identified
Status	For the steppings affected, see the Summary Table of Changes.

SKL030	ENCLU[EREPORT] May Cause a #GP When TARGETINFO.MISCSELECT is Non-Zero
Problem	The Intel® SGX (Software Guard extensions) ENCLU[EREPORT] instruction may cause a #GP (general protection fault) if any bit is set in TARGETINFO structure's MISCSELECT field.
Implication	This erratum may cause unexpected general-protection exceptions inside enclaves.
Workaround	When executing the ENCLU[EREPORT] instruction, software should ensure the bits set in TARGETINFO.MISCSELECT are a subset of the bits set in the current SECS's MISCSELECT field.
Status	For the steppings affected, see the Summary Table of Changes.

SKL031	A VMX Transition Attempting to Load a Non-Existent MSR May Result in a Shutdown
Problem	A VMX transition may result in a shutdown (without generating a machine-check event) if a non-existent MSR is included in the associated MSR-load area. When such a shutdown occurs, a machine check error will be logged with IA32_MCi_STATUS.MCACOD (bits [15:0]) of 406H, but the processor does not issue the special shutdown cycle. A hardware reset must be used to restart the processor.
Implication	Due to this erratum, the hypervisor may experience an unexpected shutdown.
Workaround	Software should not configure VMX transitions to load non-existent MSRs.
Status	For the steppings affected, see the Summary Table of Changes.

SKL032	Transitions Out of 64-bit Mode May Lead to an Incorrect FDP And FIP
Problem	A transition from 64-bit mode to compatibility or legacy modes may result in cause a subsequent x87 FPU state save to zeroing bits [63:32] of the FDP (x87 FPU Data Pointer Offset) and the FIP (x87 FPU Instruction Pointer Offset).
Implication	Leaving 64-bit mode may result in incorrect FDP and FIP values when x87 FPU state is saved.
Workaround	None identified. 64-bit software should save x87 FPU state before leaving 64-bit mode if it needs to access the FDP and/or FIP values.
Status	For the steppings affected, see the Summary Table of Changes.

SKL033	Intel® PT FUP May be Dropped After OVF
Problem	Some Intel PT (Intel Processor Trace) OVF (Overflow) packets may not be followed by a FUP (Flow Update Packet) or TIP.PGE (Target IP Packet, Packet Generation Enable).
Implication	When this erratum occurs, an unexpected packet sequence is generated.
Workaround	When it encounters an OVF without a following FUP or TIP.PGE, the Intel PT trace decoder should scan for the next TIP, TIP.PGE, or PSB+ to resume operation.
Status	For the steppings affected, see the Summary Table of Changes.

SKL034	ENCLS[ECREATE] Causes #GP if Enclave Base Address is Not Canonical
Problem	The ENCLS[ECREATE] instruction uses an SECS (SGX enclave control structure) referenced by the SRCPAGE pointer in the PAGEINFO structure, which is referenced by the RBX register. Due to this erratum, the instruction causes a #GP (general-protection fault) if the SECS attributes indicate that the enclave should operate in 64-bit mode and the enclave base linear address in the SECS is not canonical.
Implication	System software will incur a general-protection fault if it mistakenly programs the SECS with a non-canonical address. Intel has not observed this erratum with any commercially available software.
Workaround	System software should always specify a canonical address as the base address of the 64-bit mode enclave.
Status	For the steppings affected, see the Summary Table of Changes.

SKL035	Title: Data Breakpoint May Not be Detected on a REP MOVS
Problem	A REP MOVS instruction that causes an exception or a VM exit may not detect a data breakpoint that occurred on an earlier memory access of that REP MOVS instruction.
Implication	A debugger may miss a data read/write access if it is done by a REP MOVS instruction.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL036	Processor Graphics IOMMU Unit May Report Spurious Faults
Problem	The IOMMU unit for Processor Graphics pre-fetches context (or extended-context) entries to improve performance. Due to the erratum, the IOMMU unit may report

	spurious DMA remapping faults if prefetching encounters a context (or extended-context) entry which is not marked present.
Implication	Software may observe spurious DMA remapping faults when the present bit for the context (or extended-context) entry corresponding to the Processor Graphics device (Bus: 0; Device: 2; Function: 0) is cleared. These faults may be reported when the Processor Graphics device is quiescent.
Workaround	None identified. Instead of marking a context not present, software should mark the context (or extended-context) entry present while using the page table to indicate all the memory pages referenced by the context entry is not present.
Status	For the steppings affected, see the Summary Table of Changes.

SKL037	**PCIe* and DMI Links With Lane Polarity Inversion May Result in Link Failure**
Problem	The processor's PCIe and DMI links may fail after exiting Package C7 or deeper if the platform requires the link to utilize lane polarity inversion.
Implication	Due to this erratum, the processor cannot support lane polarity inversion on the PCIe or DMI links when Package C7 or deeper is enabled.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL038	**PCIe* Expansion ROM Base Address Register May be Incorrect**
Problem	After PCIe 8.0 GT/s Link Equalization on a root port (Bus 0; Device 1; Function 0, 1, 2) has completed, the Expansion ROM Base Address Register (Offset 38H) may be incorrect.
Implication	Software that uses this BAR may behave unexpectedly. Intel has not observed this erratum with any commercially available software.
Workaround	It is possible for the BIOS to contain a partial workaround for this erratum. Software should wait at least 5ms following link equalization before accessing these Expansion ROM Base Address Register.
Status	For the steppings affected, see the Summary Table of Changes.

SKL039	**PCIe* Perform Equalization May Lead to Link Failure**
Problem	Due to this erratum, when a processor PCIe port operating at 8.0 GT/s is directed to redo equalization, either via software or from the link partner, incorrect coefficients may be conveyed during Equalization Phase 3.
Implication	If the link partner accepts the incorrect coefficients, the link may become unstable. Note this affects 8.0 GT/s only.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL040	**Two DIMMs Per Channel 2133 MHz DDR4 SODIMM Daisy-Chain Systems With Different Vendors May Hang**
Problem	When, on a single memory channel with 2133 MHz DDR4 SODIMMs, mixing different vendors or mixing single rank and dual rank DIMMs, may lead to a higher rate of

	correctable errors or system hangs.
Implication	Due to this erratum, reported correctable error counts may increase or system may hang.
Workaround	Use a single vendor for and do not mix single rank and dual rank 2133 MHz DDR4 SODIMM.
Status	For the steppings affected, see the Summary Table of Changes.

SKL041	**ENCLS[EINIT] Instruction May Unexpectedly #GP**
Problem	When using Intel® SGX (Software Guard Extensions), the ENCLS[EINIT] instruction will incorrectly cause a #GP (general protection fault) if the MISCSELECT field of the SIGSTRUCT structure is not zero.
Implication	This erratum may cause an unexpected #GP, but only if software has set bits in the MISCSELECT field in SIGSTRUCT structure that do not correspond to extended features that can be written to the MISC region of the SSA (State Save Area). Intel has not observed this erratum with any commercially available software.
Workaround	When executing the ENCLS[EINIT] instruction, software should only set bits in the MISCSELECT field in the SIGSTRUCT structure that are enumerated as 1 by CPUID.(EAX=12H,ECX=0):EBX (the bit vector of extended features that can be written to the MISC region of the SSA).
Status	For the steppings affected, see the Summary Table of Changes.

SKL042	**Intel® PT OVF Packet May be Lost if Immediately Preceding a TraceStop**
Problem	If an Intel PT (Intel® Processor Trace) internal buffer overflow occurs immediately before software executes a taken branch or event that enters an Intel PT TraceStop region, the OVF (Overflow) packet may be lost.
Implication	The trace decoder will not see the OVF packet, nor any subsequent packets (e.g., TraceStop) that were lost due to overflow.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL043	**Detecting an Intel® PT Stopped or Error Condition Within an Intel® TSX Region May Result in a System Hang**
Problem	While executing within an Intel TSX (Intel® Transactional Synchronization Extensions) transactional region with Intel PT (Intel® Processor Trace) enabled and an event occurs that causes either the Error bit (bit 4) or Stopped bit (bit 5) in the IA32_RTIT_STATUS MSR (0571H) to be set then, due to this erratum, the system may hang.
Implication	A system hang may occur when Intel PT and Intel TSX are used together.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL044	**WRMSR to IA32_BIOS_UPDT_TRIG May be Counted as Multiple Instructions**
Problem	When software loads a microcode update by writing to MSR IA32_BIOS_UPDT_TRIG

	(79H) on multiple logical processors in parallel, a logical processor may, due to this erratum, count the WRMSR instruction as multiple instruction-retired events.
Implication	Performance monitoring with the instruction-retired event may over count by up to four extra events per instance of WRMSR which targets the IA32_BIOS_UPDT_TRIG register.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL045	**The x87 FIP May be Incorrect**
Problem	The x87 FPU should update the x87 FIP (FPU instruction pointer) for every non-control x87 instruction executed. Due to this erratum, the FIP is valid only if the last non-control FP instruction had an unmasked exception.
Implication	When this erratum occurs, an instruction that saves FIP (e.g., FSTENV) may save an incorrect value. Software that depends on the FIP value for x87 non-control instructions without unmasked exceptions may not operate as expected.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL046	**Branch Instructions May Initialize MPX Bound Registers Incorrectly**
Problem	Depending on the current Intel® MPX (Memory Protection Extensions) configuration, execution of certain branch instructions (near CALL, near RET, near JMP, and Jcc instructions) without a BND prefix (F2H) initialize the MPX bound registers. Due to this erratum, such a branch instruction that is executed both with CPL = 3 and with CPL < 3 may not use the correct MPX configuration register (BNDCFGU or BNDCFGS, respectively) for determining whether to initialize the bound registers; it may thus initialize the bound registers when it should not, or fail to initialize them when it should.
Implication	A branch instruction that has executed both in user mode and in supervisor mode (from the same linear address) may cause a #BR (bound range fault) when it should not have or may not cause a #BR when it should have.
Workaround	An operating system can avoid this erratum by setting CR4.SMEP[bit 20] to enable supervisor-mode execution prevention (SMEP). When SMEP is enabled, no code can be executed both with CPL = 3 and with CPL < 3.
Status	For the steppings affected, see the Summary Table of Changes.

SKL047	**Writing a Non-Canonical Value to an LBR MSR Does Not Signal a #GP When Intel® PT is Enabled**
Problem	If Intel PT (Intel Processor Trace) is enabled, WRMSR will not cause a general-protection exception (#GP) on an attempt to write a non-canonical value to any of the following MSRs: • MSR_LASTBRANCH_{0 - 31}_FROM_IP (680H – 69FH) • MSR_LASTBRANCH__{0 - 31}_TO_IP (6C0H – 6DFH) • MSR_LASTBRANCH_FROM_IP (1DBH) • MSR_LASTBRANCH_TO_IP (1DCH) • MSR_LASTINT_FROM_IP (1DDH) • MSR_LASTINT_TO_IP (1DEH)Instead the same behavior will occur as if a canonical

	value had been written. Specifically, the WRMSR will be dropped and the MSR value will not be changed.
Implication	Due to this erratum, an expected #GP may not be signaled.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL048	**Processor May Run Intel® AVX Code Much Slower Than Expected**
Problem	After a C6 state exit, the execution rate of AVX instructions may be reduced.
Implication	Applications using AVX instructions may run slower than expected.
Workaround	It is possible for the BIOS to contain a workaround
Status	For the steppings affected, see the Summary Table of Changes.

SKL049	**Intel® PT Buffer Overflow May Result in Incorrect Packets**
Problem	Under complex micro-architectural conditions, an Intel PT (Processor Trace) OVF (Overflow) packet may be issued after the first byte of a multi-byte CYC (Cycle Count) packet, instead of any remaining bytes of the CYC.
Implication	When this erratum occurs, the splicing of the CYC and OVF packets may prevent the Intel PT decoder from recognizing the overflow. The Intel PT decoder may then encounter subsequent packets that are not consistent with expected behavior.
Workaround	None Identified. The decoder may be able to recognize that this erratum has occurred when a two-byte CYC packet is followed by a single byte CYC, where the latter 2 bytes are 0xf302, and where the CYC packets are followed by a FUP (Flow Update Packet) and a PSB+ (Packet Stream Boundary+). It should then treat the two CYC packets as indicating an overflow.
Status	For the steppings affected, see the Summary Table of Changes.

SKL050	**Intel® PT PSB+ Packets May be Omitted on a C6 Transition**
Problem	An Intel PT (Processor Trace) PSB+ (Packet Stream Boundary+) set of packets may not be generated as expected when IA32_RTIT_STATUS.PacketByteCnt[48:32] (MSR 0x571) reaches the PSB threshold and a logical processor C6 entry occurs within the following one KByte of trace output.
Implication	After a logical processor enters C6, Intel PT output may be missing PSB+ sets of packets.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL051	**IA32_PERF_GLOBAL_STATUS.TRACE_TOPA_PMI Bit Cannot be Set by Software**
Problem	A WRMSR that attempts to set Trace_ToPA_PMI (bit 55) in the IA32_PERF_GLOBAL_STATUS MSR (38EH) by writing a '1' to bit 55 in the IA32_PERF_GLOBAL_STATUS_SET (MSR (391H) will cause a #GP fault.
Implication	Software cannot set the Trace_ToPA_PMI bit.

Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL052	**CPUID Incorrectly Reports Bit Manipulation Instructions Support**
Problem	Executing CPUID with EAX = 7 and ECX = 0 may return EBX with bits [3] and [8] set, incorrectly indicating the presence of BMI1 and BMI2 instruction set extensions.
Implication	Attempting to use instructions from the BMI1 or BMI2 instruction set extensions will result in a #UD exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL053	**Intel® Turbo Boost Technology May be Incorrectly Reported as Supported on Intel® Core™ i3 U/H/S, Select Intel® Mobile Pentium®, Intel® Mobile Celeron®, Select Intel® Pentium® G4xxx and Intel® Celeron® G3xxx Processors**
Problem	These processors may incorrectly report support for Intel® Turbo Boost Technology via CPUID.06H.EAX bit 1.
Implication	The CPUID instruction may report Turbo Boost Technology as supported even though the processor does not permit operation above the Base Frequency.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL054	**TSX Abort May Result in Unpredictable System Behavior**
Problem	Certain micro-architectural conditions during an Intel® TSX (Intel® Transactional Synchronization Extensions) abort may result in unpredictable system behavior.
Implication	Software using Intel TSX may be unreliable.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL055	**Use of Prefetch Instructions May Lead to a Violation of Memory Ordering**
Problem	Under certain micro architectural conditions, execution of a PREFETCHh instruction or a PREFETCHW instruction may cause a load from the prefetched cache line to appear to execute before an earlier load from another cache line.
Implication	Software that relies on loads executing in program order may not operate correctly.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL056	**CS Limit Violation May Not be Detected**
Problem	A CS (code segment) limit reduction may not be properly applied.
Implication	Instructions may be executed beyond the CS limit. Intel has not observed this

	erratum to impact the operation of any commercially available software.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL057	**Last Level Cache Performance Monitoring Events May be Inaccurate**
Problem	The performance monitoring events LONGEST_LAT_CACHE.REFERENCE (Event 2EH; Umask 4FH) and LONGEST_LAT_CACHE.MISS (Event 2EH; Umask 41H) count requests that reference or miss in the last level cache. However, due to this erratum, the count may be incorrect.
Implication	LONGEST_LAT_CACHE events may be incorrect.
Workaround	None identified. Software may use the following OFFCORE_REQUESTS model-specific sub events that provide related performance monitoring data: DEMAND_DATA_RD, DEMAND_CODE_RD, DEMAND_RFO, ALL_DATA_RD, L3_MISS_DEMAND_DATA_RD, ALL_REQUESTS.
Status	For the steppings affected, see the Summary Table of Changes.

SKL058	**#GP Occurs Rather Than #DB on Code Page Split Inside an Intel® SGX Enclave**
Problem	When executing within an Intel® SGX (Software Guard Extensions) enclave, a #GP (general-protection exception) may be delivered instead of a #DB (debug exception) when an instruction breakpoint is detected. This occurs when the instruction to be executed spans two pages, the second of which has an entry in the EPCM (enclave page cache map) that is not valid.
Implication	Debugging software may not be invoked when an instruction breakpoint is detected.
Workaround	Software should ensure that all pages containing enclave instructions have valid EPCM entries.
Status	For the steppings affected, see the Summary Table of Changes.

SKL059	**Execution of VAESENCLAST Instruction May Produce a #NM Exception Instead of a #UD Exception**
Problem	Execution of VAESENCLAST with VEX.L= 1 should signal a #UD (Invalid Opcode) exception, however, due to the erratum, a #NM (Device Not Available) exception may be signaled.
Implication	As a result of this erratum, an operating system may restore AVX and other state unnecessarily.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL060	**Intel® SGX Enclave Accesses to the APIC-Access Page May Cause APIC-Access VM Exits**
Problem	In VMX non-root operation, Intel SGX (Software Guard Extensions) enclave accesses to the APIC-access page may cause APIC-access VM exits instead of page faults.
Implication	A VMM (virtual-machine monitor) may receive a VM exit due to an access that should

	have caused a page fault, which would be handled by the guest OS (operating system).
Workaround	A VMM avoids this erratum if it does not map any part of the EPC (Enclave Page Cache) to the guest's APIC-access address; an operating system avoids this erratum if it does not attempt indirect enclave accesses to the APIC.
Status	For the steppings affected, see the Summary Table of Changes.

SKL061	**CR3 Filtering Does Not Compare Bits [11:5] of CR3 and IA32_RTIT_CR3_MATCH in PAE Paging Mode**
Problem	In PAE paging mode, the CR3[11:5] are used to locate the page-directory-pointer table. Due to this erratum, those bits of CR3 are not compared to IA32_RTIT_CR3_MATCH (MSR 572H) when IA32_RTIT_CTL.CR3Filter (MSR 570H, bit 7) is set.
Implication	If multiple page-directory-pointer tables are co-located within a 4KB region, CR3 filtering will not be able to distinguish between them so additional processes may be traced.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL062	**Intel® PT PacketEn Change on C-state Wake May Not Generate a TIP Packet**
Problem	A TIP.PGE (Target IP, Packet Generation Enabled) or TIP.PGD (Target IP, Packet Generation Disabled) packet may not be generated if Intel PT (Processor Trace) PacketEn changes after IA32_RTIT_STATUS.FilterEn (MSR 571H, bit 0) is re-evaluated on wakeup from C6 or deeper sleep state.
Implication	When code enters or exits an IP filter region without a taken branch, tracing may begin or cease without proper indication in the trace output. This may affect trace decoder behavior.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL063	**Graphics Configuration May Not be Correctly Restored After a Package C8 Exit**
Problem	The processor should ensure internal graphics configuration is restored during a Package C8 or deeper exit event. Due to this erratum, some internal graphics configurations may not be correctly restored.
Implication	When this erratum occurs, a graphics driver restart may lead to system instability. Such a restart may occur when upgrading the graphics driver.
Workaround	It is possible for the BIOS to contain a workaround for this erratum
Status	For the steppings affected, see the Summary Table of Changes.

SKL064	**x87 FDP Value May be Saved Incorrectly**
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an

	unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, see the Summary Table of Changes.

SKL065	**PECI Frequency Limited to 1 MHz**
Problem	The PECI (Platform Environmental Control Interface) 3.1 specification's operating frequency range is 0.2 MHz to 2 MHz. Due to this erratum, PECI may be unreliable when operated above 1 MHz.
Implication	Platforms attempting to run PECI above 1 MHz may not behave as expected.
Workaround	None identified. Platforms should limit PECI operating frequency to 1 MHz.
Status	For the steppings affected, see the Summary Table of Changes.

SKL066	**Processor Graphics IOMMU Unit May Not Mask DMA Remapping Faults**
Problem	Intel® Virtualization Technology for Directed I/O specification specifies setting the FPD (Fault Processing Disable) field in the context (or extended-context) entry of IOMMU to mask recording of qualified DMA remapping faults for DMA requests processed through that context entry. Due to this erratum, the IOMMU unit for Processor Graphics device may record DMA remapping faults from Processor Graphics device (Bus: 0; Device: 2; Function: 0) even when the FPD field is set to 1.
Implication	Software may continue to observe DMA remapping faults recorded in the IOMMU Fault Recording Register even after setting the FPD field.
Workaround	None identified. Software may mask the fault reporting event by setting the IM (Interrupt Mask) field in the IOMMU Fault Event Control register (Offset 038H in GFXVTBAR).
Status	For the steppings affected, see the Summary Table of Changes.

SKL067	**Processor With Intel® SGX Support May Hang During S3 Wake or Power-On Reset**
Problem	Processors that support Intel SGX (Intel Software Guard Extensions) may experience hangs when waking from S3 (Standby) system sleep state or during a power-on reset. This erratum may occur even if the Intel SGX feature is not enabled.
Implication	Due to this erratum, the system may not wake after entering standby sleep state or may not start up after a power-on reset
Workaround	It is possible for the BIOS to contain a workaround for this erratum. For systems that do not power gate Vcc Sustain, if the workaround detects this erratum, support for Intel SGX will be removed until platform power is disconnected and reapplied.
Status	For the steppings affected, see the Summary Table of Changes.

SKL068	Audio Glitches May Occur After Reset or S3/S4 Exit
Problem	After a reset or S3/S4 exit the processor may operate at a lower than expected frequency.
Implication	When this erratum occurs, the processor may be unable to adequately support audio playback resulting in several seconds of audio glitches.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL069	Intel® PT CYCThresh Value of 13 is Not Supported
Problem	Intel PT (Intel® Processor Trace) CYC (Cycle Count) threshold is configured through CYCThresh field in bits [22:19] of IA32_RTIT_CTL MSR (570H). A value of 13 is advertised as supported by CPUID (leaf 14H, sub-lead 1H). Due to this erratum, if CYCThresh is set to 13 then the CYC threshold will be 0 cycles instead of 4096 (213-1) cycles.
Implication	CYC packets may be issued in higher rate than expected if threshold value of 13 is used.
Workaround	None identified. Software should not use value of 13 for CYC threshold.
Status	For the steppings affected, see the Summary Table of Changes.

SKL070	Exx. Intel® PT May Drop Some Timing Packets After Entering Thread
Problem	Intel PT (Intel® Processor Trace) may temporarily stop sending MTC (Mini Time Counter) and CYC (Cycle) packets after entering thread C3 state. MTC and CYC packets may be missing in up to 1KB of trace output after entering thread C3.
Implication	Some Intel PT timing packets may temporarily not be sent after thread C3 is entered.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL071	Underflow and Denormal Conditions During a VDPPS Instruction With YMM Operands May Not Produce The Expected Results
Problem	A VDPPS (Vector Dot Product of Packed Single Precision Floating-Point Values) instruction operating on YMM registers with denormal operand(s) or experiencing an underflow may not produce the expected result if the exception is masked in the MXCSR. This may also happen when intermediate multiply results have underflow conditions.
Implication	VDPPS with YMM registers may not produce the expected result.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL072	IA Core Ratio Change Coincident With Outstanding Read to the DE May Cause a System Hang
Problem	An outstanding read from an IA core to the DE (Display Engine) that is coincident with an IA core ratio change may result in a system hang.

Implication	Due to this erratum, the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL073	**Enabling VMX-Preemption Timer Blocks HDC Operation**
Problem	HDC (Hardware Duty Cycling) will not put the physical package into the forced idle state while any logical processor is in VMX non-root operation and the "activate VMX-preemption timer" VM-execution control is 1.
Implication	HDC will not provide the desired power reduction when the VMX-preemption timer is active in VMX non-root operation.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL074	**Certain Processors May be Configured With an Incorrect TDP**
Problem	Certain processors should be configured with a TDP (Thermal Design Power) limit of 54 or 51 watts. Due to this erratum, these processors may be incorrectly configured at 65 W TDP. The following processors are affected by this erratum: Intel® Core™ i3 Processor Series, Celeron® and Pentium® (Dual-Core With GT1/GT2). A processor that reports a value of 0x208 in TDP_POWER_OF_SKU field in MSR PACKAGE_POWER_SKU (MSR 614H [14:0]) are affected by this erratum.
Implication	Processors affected by this erratum may spend more time in turbo and thus may experience unexpected thermal throttling events.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL075	**Display Flicker May Occur When Both VT-d And FBC Are Enabled**
Problem	Display flickering may occur when both FBC (Frame Buffer Compression) and VT-d (Intel® Virtualization Technology for Directed I/O) are enabled and in use by the display controller.
Implication	Due to this erratum, display flickering may be observed.
Workaround	It is possible for the graphics driver to contain a workaround for this erratum. This workaround will disable FBC.
Status	For the steppings affected, see the Summary Table of Changes.

SKL076	**System May Hang When Using Intel® TXT And Memory That Supports Address Mirroring**
Problem	Within platforms that utilize memory that supports address mirroring, processors that utilize Intel TXT (Intel Trusted Execution Technology) measured launch environment may fail to boot and hang.
Implication	Due to this erratum, system may hang.
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status	For the steppings affected, see the Summary Table of Changes.

SKL077	**System May Hang or Reset During Processor Package C9 Exit**
Problem	Under a complex set of conditions, during a processor Package C9 exit, display artifacts may be seen, the processor may hang, or the processor may incur a machine check exception with an Internal Unclassified error reported in IA32_MCi_STATUS with MCACOD (bits[15:0]) equal to 0x402 and MSCOD (31:16)] equal to 0x94yy (where y can be any value).
Implication	Display artifacts may be seen or the system may log a machine check error and reset or hang when resuming from C9.
Workaround	It is possible for the BIOS and Intel® Graphics Driver 15.40.11.4308 or later to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL078	**Integrated Audio Codec May Not be Detected**
Problem	Integrated Audio Codec may lose power when LPSP (Low-Power Single Pipe) mode is enabled for an eDP* (embedded DisplayPort) or HDMI ports. Platforms with Intel® SST (Intel® Smart Sound Technology) enabled are not affected.
Implication	The Audio Bus driver may attempt to do enumeration of Codecs when eDP or HDMI port enters LPSP mode, due to this erratum, the Integrated Audio Codec will not be detected and audio maybe be lost.
Workaround	Intel® Graphics Driver 15.40.11.4312 or later will prevent the Integrated Audio Codec from losing power when LPSP mode is enabled.
Status	For the steppings affected, see the Summary Table of Changes.

SKL079	**MOVNTDQA From WC Memory May Pass Earlier MFENCE Instructions**
Problem	An execution of MOVNTDQA or VMOVNTDQA that loads from WC (write combining) memory may appear to pass an earlier execution of the MFENCE instruction.
Implication	When this erratum occurs, an execution of MOVNTDQA or VMOVNTDQA may appear to execute before memory operations that precede the earlier MFENCE instruction. Software that uses MFENCE to order subsequent executions of the MOVNTDQA instructions may not operate properly.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL080	**APIC Timer Interrupt May be Delivered Early**
Problem	When the APIC timer is configured to TSC Deadline Mode, a timer interrupt may occur before the expected deadline if any of IA32_TSC_DEADLINE MSR (6E0H) bits [63:56] are set.
Implication	A timer interrupt may be delivered earlier than specified by the IA32_TSC_DEADLINE MSR.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.

Status	For the steppings affected, see the Summary Table of Changes.

SKL081	**Processors That Support EDRAM May Not Initialize Properly**
Problem	During platform initialization, the processor's eDRAM interface may fail to complete its training and configuration sequence.
Implication	When this erratum occurs, a processor that supports eDRAM may not initialize properly.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL082	**Processor May Hang or Cause Unpredictable System Behavior**
Problem	Under complex microarchitecture conditions, processor may hang with an internal timeout error (MCACOD 0400H) logged into IA32_MCi_STATUS or cause unpredictable system behavior
Implication	When this issue occurs, the system may cause unpredictable system behavior
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL083	**The Processor May Fail to Properly Exit Package C6 or Deeper**
Problem	When the processor exits Package C6 or deeper, it may hang, generate a machine check exception with an Internal Unclassified error reported in IA32_MCi_STATUS with MCACOD (bits[15:0]) equal to 0x402 and MSCOD (31:16)] equal to 0x94yy (where y can be any value), or exhibit unpredictable system behavior.
Implication	Due to this erratum, unpredictable system behavior may occur.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL084	**Certain Processors May Report Incorrect DID2**
Problem	The U-processor with GT3 and TDP of 28W may report an incorrect value of 1926H in DID2 (Processor Graphics Device ID) (Bus 0, Device 2, Function 0; offset 2h; bits [15:0]) register. This value should be 1927H.
Implication	Software that decodes DID2 values may not function as expected.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL085	**System May Hang When Entering S3/S4/S5 State**
Problem	When entering S3/S4/S5 state, it may hang and generate a machine check with an Internal Unclassified error reported in IA32_MCi_STATUS with MCACOD (bits[15:0]) equal to 0x402 and MSCOD (31:16)] equal to 0x77yy (where y can be any value).
Implication	Due to this erratum a system hang may occur.

Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL086	**Display Flickering May be Observed with Specific eDP* Panels**
Problem	The processor may incorrectly configure transmitter buffer characteristics if the associated eDP panel requests VESA equalization preset 3, 5, 6, or 8.
Implication	Display flickering or display loss maybe observed.
Workaround	Intel® Graphics Driver version 15.40.12.4326 or later contains a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL087	**x87 FPU Data Pointer Updated Only for Instructions That Incur Unmasked Exceptions**
Problem	The x87 FPU data pointer is the pointer to data (operand) for the last x87 non-control instruction executed. Due to this erratum, it contains the pointer to data (operand) for the last x87 non-control instruction that incurred an unmasked x87 exception. This behavior should hold only if CPUID.(EAX=07H,EXC=0H):EBX. FDP_EXCPTN_ONLY [bit 6] is enumerated as 1, which is not the case.
Implication	If the most recent x87 non-control instruction did not incur an unmasked x87 exception, software that then examines the x87 FPU data pointer will see an incorrect value.
Workaround	It is possible for the BIOS to contain a workaround for this erratum. This workaround will cause CPUID.(EAX=07H,EXC=0H):EBX. FDP_EXCPTN_ONLY [bit 6] to be enumerated as 1. Software should examine the x87 FPU data pointer only when the most recent x87 non-control instruction incurred an unmasked x87 exception.
Status	For the steppings affected, see the Summary Table of Changes.

SKL088	**Incorrect Branch Predicted Bit in BTS/BTM Branch Records**
Problem	BTS (Branch Trace Store) and BTM (Branch Trace Message) send branch records to the Debug Store management area and system bus respectively. The Branch Predicted bit (bit 4 of eighth byte in BTS/BTM records) should report whether the most recent branch was predicted correctly. Due to this erratum, the Branch Predicted bit may be incorrect.
Implication	BTS and BTM cannot be used to determine the accuracy of branch prediction.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL089	**MACHINE_CLEARS.MEMORY_ORDERING Performance Monitoring Event May Undercount**
Problem	The performance monitoring event MACHINE_CLEARS.MEMORY_ORDERING (Event C3H; Umask 02H) counts the number of machine clears caused by memory ordering conflicts. However due to this erratum, this event may undercount for VGATHER*/VPGATHER* instructions of four or more elements.
Implication	MACHINE_CLEARS.MEMORY_ORDERING performance monitoring event may

	undercount.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL090	**Some Counters May Not Freeze On Performance Monitoring Interrupts**
Problem	The FREEZE_PERFMON_ON_PMI flag in IA32_DEBUGCTL (bit 12, MSR 1D9H) freezes performance counters when a PMI is triggered. However, due to this erratum, IA32_PMC4-7 (MSR C5-C8H) may not stop counting. IA32_PMC4-7 are only available when a processor core is not shared by two logical processors.
Implication	General performance monitoring counters 4-7 may not freeze when FREEZE_PERFMON_ON_PMI flag is used.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL091	**Instructions And Branches Retired Performance Monitoring Events May Overcount**
Problem	The performance monitoring events INST_RETIRED (Event C0H; any Umask value) and BR_INST_RETIRED (Event C4H; any Umask value) count instructions retired and branches retired, respectively. However, due to this erratum, these events may overcount in certain conditions when: - Executing VMASKMOV* instructions with at least one masked vector element - Executing REP MOVS or REP STOS with Fast Strings enabled (IA32_MISC_ENABLES MSR (1A0H), bit 0 set) - An MPX #BR exception occurred on BNDLDX/BNDSTX instructions and the BR_INST_RETIRED (Event C4H; Umask is 00H or 04H) is used.
Implication	INST_RETIRED and BR_INST_RETIRED performance monitoring events may overcount.
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL092	**Deleted – Please refer to SKL057**
Problem	
Implication	
Workaround	
Status	For the steppings affected, see the Summary Table of Changes.

SKL093	**REP MOVS May Not Operate Correctly With EPT Enabled**
Problem	Execution of REP MOVS may incorrectly change [R/E]CX, [R/E]SI, and/or [R/E]DI register values during instruction execution. This erratum occurs only if the execution would set an accessed or dirty flag in a paging structure to which EPT does not allow writes.
Implication	Incorrect changes to RCX, RSI, and/or RDI may lead to a block-copy operation with

	an unexpected length, an unexpected source location, and/or an unexpected destination location.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL094	**Ring Frequency Changes May Cause a Machine Check And System Hang**
Problem	Ring frequency changes may lead to a system hang with the processor logging a machine check in IA32_MCi_STATUS where the MCACOD (bits[15:0]) value is 0x0402 and the MSCOD (bits[31:16]) value is 0x77yy (yy is any 8-bit value).
Implication	When this erratum occurs, the system will log a machine check and hang. Power management activity, including system power state changes, can result in ring frequency changes that may trigger this erratum.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL095	**Some OFFCORE_RESPONSE Performance Monitoring Events May Overcount**
Problem	The performance monitoring events OFFCORE_RESPONSE (Events B7H and BBH) should count off-core responses matching the request-response configuration specified in MSR_OFFCORE_RSP_0 and MSR_OFFCORE_RSP_1 (1A6H and 1A7H, respectively) for core-originated requests. However, due to this erratum, DMND_RFO (bit 1), DMND_IFETCH (bit 2) and OTHER (bit 15) request types may overcount.
Implication	Some OFFCORE_RESPONSE events may overcount.
Workaround	None identified. Software may use the following model-specific events that provide related performance monitoring data: OFFCORE_REQUESTS (all sub-events), L2_TRANS.L2_WB and L2_RQSTS.PF_MISS.
Status	For the steppings affected, see the Summary Table of Changes.

SKL096	**Using BIOS to Disable Cores May Lead to a System Hang**
Problem	Using the BIOS hardware core disable facility may cause the processor to hang when it attempts to enter or exit Package C6.
Implication	When this erratum occurs, attempting to enter or exit Package C6 state will hang the system.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL097	**Instructions Fetch #GP After RSM During Inter® PT May Push Incorrect RFLAGS Value on Stack**
Problem	If Intel PT (Processor Trace) is enabled, a #GP (General Protection Fault) caused by the instruction fetch immediately following execution of an RSM instruction may push an incorrect value for RFLAGS onto the stack.
Implication	Software that relies on RFLAGS value pushed on the stack under the conditions described may not work properly.

Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

SKL099	**Access to SGX EPC Page in BLOCKED State is Not Reported as an SGX-Induced Page Fault**
Problem	If a page fault results from attempting to access a page in the SGX (Intel® Software Guard Extensions) EPC (Enclave Page Cache) that is in the BLOCKED state, the processor does not set bit 15 of the error code and thus fails to indicate that the page fault was SGX-induced.
Implication	Due to this erratum, software may not recognize these page faults as being SGX-induced.
Workaround	Before using the EBLOCK instruction to marking a page as BLOCKED, software should use paging to mark the page not present.
Status	For the steppings affected, see the Summary Table of Changes.

SKL100	**MTF VM Exit on XBEGIN Instruction May Save State Incorrectly**
Problem	Execution of an XBEGIN instruction while the monitor trap flag VM-execution control is 1 will be immediately followed by an MTF VM exit. If advanced debugging of RTM transactional regions has been enabled, the VM exit will erroneously save as instruction pointer the address of the XBEGIN instruction instead of the fallback instruction address specified by the XBEGIN instruction. In addition, it will erroneously set bit 16 of the pending-debug-exceptions field in the VMCS indicating that a debug exception or a breakpoint exception occurred.
Implication	Software using the monitor trap flag to debug or trace transactional regions may not operate properly. Intel has not observed this erratum with any commercially available software.
Workaround	None identified
Status	For the steppings affected, see the Summary Table of Changes.

SKL103	**Enabling S3 on Processors With EDRAM May Cause Unpredictable System Behavior**
Problem	Entering S3 when EDRAM is enabled may lead to unpredictable system behavior.
Implication	When this erratum occurs, the system may exhibit unpredictable system behavior.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL104	**PEBS Record May Be Generated After Being Disabled**
Problem	A performance monitoring counter may generate a PEBS (Precise Event Based Sampling) record after disabling PEBS or the performance monitoring counter by clearing the corresponding enable bit in IA32_PEBS_ENABLE MSR (3F1H) or IA32_PERF_GLOBAL_CTRL MSR (38FH).
Implication	A PEBS record generated after a VMX transition will store into memory according to the post-transition DS (Debug Store) configuration. These stores may be unexpected

	if PEBS is not enabled following the transition.
Workaround	It is possible for the BIOS to contain a workaround for this erratum. A software workaround is possible through disallowing PEBS during VMX non-root operation and disabling PEBS prior to VM entry.
Status	For the steppings affected, see the Summary Table of Changes.

SKL105	**Software Using Intel® TSX May Result in Unpredictable System Behavior**
Problem	Under a complex set of internal timing conditions and system events, software using the Intel TSX (Transactional Synchronization Extensions) instructions may result in unpredictable system behavior.
Implication	This erratum may result in unpredictable system behavior.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, see the Summary Table of Changes.

SKL106	**Package-C6 Exit Latency May be Higher Than Expected Leading to Display Flicker**
Problem	Package-C6 exit latency may be higher than expected.
Implication	Due to this erratum, the display may flicker or other Isochronous devices may be affected.
Workaround	It is possible for the BIOS to contain a workaround for this erratum
Status	For the steppings affected, see the Summary Table of Changes.

SKL107	**EDRAM May Cause Unpredictable System Behavior**
Problem	EDRAM, under certain low power conditions, may lead to unpredictable behavior.
Implication	When this erratum occurs, the system will behave unpredictably
Workaround	It is possible for the BIOS to contain a workaround for this erratum
Status	For the steppings affected, see the Summary Table of Changes.

SKL108	**PCIe* Port Does Not Support DLL Link Activity Reporting**
Problem	The PCIe Base specification requires DLL (Data Link Layer) Link Activity Reporting when 8 GT/s link speed is supported. Due to this erratum, link activity reporting is not supported
Implication	Due to this erratum, PCIe port does not support DLL Link Activity Reporting when 8 GT/s is supported.
Workaround	None identified
Status	For the steppings affected, see the Summary Table of Changes.

SKL109	**Enabling Package C8 State or Deeper May Lead to Display Flicker or a System Hang**
Problem	Under certain conditions, when Package C8 state or deeper is enabled, display

	flickering may be observed and/or the system may hang.
Implication	When this erratum occurs, the display may flicker and/or the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum
Status	For the steppings affected, see the Summary Table of Changes.

SKL110	**System May Hang When EDRAM is Enabled And DDR is Operating at 1600 MHz**
Problem	When EDRAM is enabled and the DDR operating frequency is 1600 MHz, a system hang may occur
Implication	When this erratum occurs, the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum
Status	For the steppings affected, see the Summary Table of Changes.

SKL111	**DR6.B0-B3 May Not Report All Breakpoints Matched When a MOV/POP SS is Followed by a Store or an MMX Instruction**
Problem	Normally, data breakpoints matches that occur on a MOV SS, r/m or POP SS will not cause a debug exception immediately after MOV/POP SS but will be delayed until the instruction boundary following the next instruction is reached. After the debug exception occurs, DR6.B0-B3 bits will contain information about data breakpoints matched during the MOV/POP SS as well as breakpoints detected by the following instruction. Due to this erratum, DR6.B0-B3 bits may not contain information about data breakpoints matched during the MOV/POP SS when the following instruction is either an MMX instruction that uses a memory addressing mode with an index or a store instruction.
Implication	When this erratum occurs, DR6 may not contain information about all breakpoints matched. This erratum will not be observed under the recommended usage of the MOV SS,r/m or POP SS instructions (i.e., following them only with an instruction that writes (E/R)SP).
Workaround	None identified.
Status	For the steppings affected, see the Summary Table of Changes.

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Specification Changes

There are no Specification Changes in this Specification Update revision.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no documentation changes in this Specification Update revision.

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