



Off-chip ESD Protection Anticipates IC Scaling

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As next-generation transceivers and digital communications ICs scale to smaller geometries, the challenge for IC manufacturers to maintain reasonable levels of on-chip ESD protection becomes greater. Proposed decreases in on-chip ESD protection mean that system designers must be more aware of building ESD protection into their designs by choosing the right devices and following key design principles.

In the race to provide more and faster functionality, on-chip ESD protection is often sacrificed in favor of chip performance. According to the ESD Association, the ICs of tomorrow will not sustain the current levels (2kV) of on-chip ESD protection. In fact, there is a proposal to lower on-chip ESD stress target levels by more than half. At the system level, as on-chip protection is reduced, ICs will be more sensitive to transients such as cable discharge events and ESD from the human body. With increased ESD sensitivity of current and future ICs, the need to protect systems with more robust off-chip transient voltage suppression is greater than ever.

Several models exist for simulating ESD events. There is often confusion when talking about chip- vs. system-level models or standards. At the chip level, a device is tested to a minimum 2kV discharge through a 1.5k Ω resistor per MIL-STD 883, Method 3015 (ANSI/ESD STM5.1). With the resistor, the model approximates a current source of about 1.33A. There is a proposal to lower the discharge voltage to 1kV with expectations that it will be sub-500V in the future. Given today's ESD control procedures and the manufacturing requirements of submicron ICs, these levels are reasonable.

At the system level, however, electronic equipment is subject to more severe ESD events. The most internationally recognized system-level ESD standard is currently IEC 61000-4-2. This standard is used by manufacturers to model ESD events from human contact. Not only is it important for ensuring product reliability, but compliance is required for products aimed at world markets. IEC 61000-4-2 is divided into four threat levels with discharges of 2-, 4-, 6- or 8kV through a 330 Ω resistor. Most of today's systems require compliance with L3 or L4, where a maximum current of 30A is developed (see Table). This is more than 20 times the current at chip level. With the proposed on-chip protection levels, next generation ICs will be at risk of great damage after even a single discharge.

Threat level	First peak current (A)	Peak current at 30ns (A)	Peak Current at 60ns (A)	Test voltage (Contact discharge) (kV)	Test voltage (Air discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

Table: Most of today's systems require compliance with L3 or L4 of IEC 61000-4-2.

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Relative to other overvoltage events, ESD is a very quick transient pulse. The rise time is modeled by IEC 61000-4-2 at 700ps to 1ns, while the pulse duration is 60ns (refer to Figure 1). This explains why the common ESD event presents challenges when designing for ESD immunity at the board level.

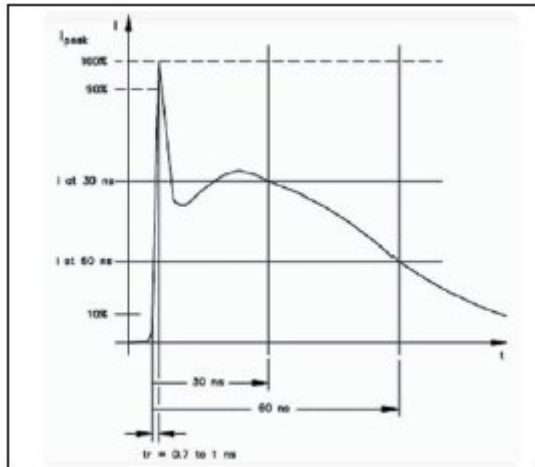


Figure 1: The rise time is modeled by IEC 61000-4-2 at 700ps to 1ns, while the pulse duration is 60ns.

TVS diodes

Protecting electronic devices from damage is not always a straightforward task. With their low clamping voltages and fast response times, transient voltage suppression (TVS) diodes have long been used to protect systems against ESD transients. Other types of suppression devices exist on the market, but an ill-chosen device can provide a false sense of security. A device rated for IEC 61000-4-2 gives no guarantee that the system will pass ESD testing. The best way to evaluate how a TVS device will perform in the system is to examine the clamping voltage, which is the voltage across the protection device during the ESD event. Consequently, this is the stress voltage seen by the protected IC. High clamping voltage will produce more stress on the protected device and increase the probability of failure. Due to their low clamping characteristics, TVS diodes have emerged as a dominant technology for protecting sensitive electronics. If properly used, they will limit the voltage across the protected device to a level just above the normal operating voltage and well below the destructive threshold.

Clamping performance of a device is usually presented as a graph showing the clamp voltage vs. ESD voltage. Complicating matters further, two TVS devices from different manufacturers can have very different clamping responses. Designers should insist that a data sheet provide more information other than claiming compliance to IEC 61000-4-2. An ESD protection device's data sheet must include clamping performance graphs or it should not be considered for use.

From the perspective of the TVS device, one thing is clear: the lower the clamping voltage, the better. In fact, the lower the clamping voltage, the more likely the system will pass ESD immunity testing the first time at the compliance lab. Nothing is guaranteed, but with a good layout and a TVS with a low clamping voltage, the chances of ESD system immunity are maximized.

The device's operating voltage must also be considered. The goal is to have the protection device turn on just above the normal operating voltage of the circuit. Conventional p-n junction devices are available with operating voltages as low as 5V. However, as systems have moved to sub-5V operating voltages, lower-voltage protection devices are required. Semtech has developed a low-voltage process that yields protection devices that operate at 2.8V and 3.3V levels with low leakage current and high surge capacity.

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Board layout

To implement a solution for ESD protection, here are some additional considerations with respect to board layout and device selection:

- Place your TVS devices as close as possible to the interface connector. Given the fast rise time of ESD, it is clearly undesirable to couple a pulse into nearby traces. Placing TVS devices as close as possible to interface ports will suppress the energy at the entry point of your PCB and will reduce the secondary effects of radiated emissions emanating from the ESD event.
- Reduce the effect of parasitic inductance ($V = L \cdot di/dt$) by minimizing trace length from the TVS device to the protected I/O line. Considering that the rise time of a simulated ESD event is 1ns, a 30A pulse (L4 IEC 61000-4-2) on a 1nH series inductance trace can raise the clamping voltage of the device by 30V.
- When possible, make ground connections from the TVS device directly to the ground plane. If vias are required, multiple vias to the ground plane are suitable.
- On high-speed digital signals, the capacitance of the TVS device becomes an important consideration. To preserve signal integrity, select devices that will present minimal capacitive loading without sacrificing clamping performance. For example, the RClamp0524P presents a capacitance of 0.5pF, making it electrically transparent on high-speed interfaces.
- When available, use flow-through packages on high speed traces. These packages allow engineers to place the protection device directly over the PCB differential pair. This eliminates stubs and bends in the traces, which helps preserve signal integrity. Figure 2 (below) shows an example of how flow-through packages can be implemented.

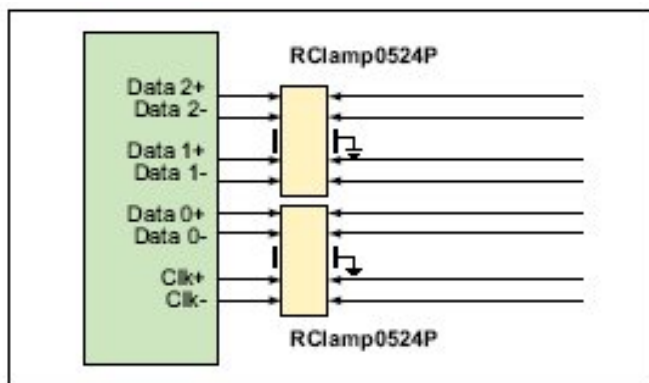


Figure 2: Flow-through packages allow engineers to place the protection device directly over the PCB differential pair, eliminating stubs and bends in the traces.

- Reduce trace lengths as much as possible. Long signal traces can mimic antennas and couple noise from an ESD event. With the trend to smaller IC geometries and less on-chip ESD protection, designers have an increased mandate to design in system reliability. While IC sensitivity is increasing, the physical phenomenon of ESD is not decreasing. Tomorrow's electronic products need more robust off-chip ESD protection to provide the current level of system protection. By selecting a protection TVS with good clamping performance and applying some basic layout techniques, designers can maximize the chance of passing ESD testing the first time at the compliance lab and ensure greater product reliability in the field.