

Product Overview

The Qorvo® QPF4588 is an integrated front end module (FEM) designed for Wi-Fi 802.11ax systems. The compact form factor and integrated matching minimizes layout area in the application.

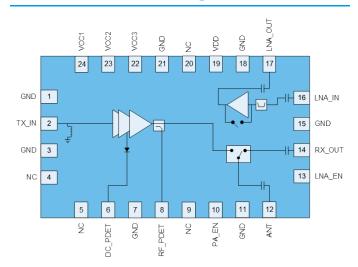
Performance is focused on optimizing the PA for a 5V supply voltage that conserves power consumption while maintaining the highest linear output power and leading edge throughput. Receive path matches the optimal technologies to maximize Rx sensitivity through noise figure performance that is consistent over a wider variety of conditions.

The receive path is pinned out so external filtering can be added in the optimal position. Integrated die level filtering for 2nd and 3rd harmonics as well as 2.4 GHz rejection for DBDC operation are included.

There are two options for power detect, a DC power detector which has voltage output and an RF power detector with an RF output from a directional coupler.

The QPF4588 integrates a 5 GHz power amplifier (PA), regulator, single pole two throw switch (SP2T), bypassable low noise amplifier (LNA) and coupler into a single device

Functional Block Diagram



Top View

QOCVO QPF4588

24 Pin 5x3 mm QFN Package

Key Features

- 5150 5925 MHz
- P_{OUT} = +16dBm MCS11 HE80 -47dB Dynamic EVM
- P_{OUT} = +18dBm MCS11 HE80 -43dB Dynamic EVM
- P_{OUT} = +23dBm MCS9 VHT80 -35dB Dynamic EVM
- P_{OUT} = +24dBm MCS7 HT20/40 -30dB Dynamic EVM
- P_{OUT} = +26dBm MCS0 HT20 Spectral Mask Compliance
- Optimized for +5 V Operation
- 33 dB Tx Gain
- 2 dB Noise Figure
- 16 dB Rx Gain & 7 dB Bypass Loss
- 30 dB 2.4 GHz Rejection on Rx Path
- Integrated RF Power Detector Coupler as well as DC Power Detector

Applications

- · Access Points
- Wireless Routers
- Residential Gateways
- Customer Premise Equipment
- Internet of Things

Ordering Information

Part Number	Description
QPF4588SB	Sample bag with 5 pieces
QPF4588SQ	Sample bag with 25 pieces
QPF4588SR	7" reel with 100 pieces
QPF4588TR13-5K	13" reel with 5,000 pieces
QPF4588PCK-01	Assembled Evaluation Board + 5 pieces



Absolute Maximum Ratings

Parameter	Conditions	Rating
DC Supply Voltage		-0.5 to +6 V
Control Voltage	PA_EN & LNA_EN	-0.5 to +6 V
Storage Temperature		-40 to 150 °C
Junction Temperature	MTTF > 1.5x10 ⁶ hours	160 °C
	MTTF > 1.0x10 ⁶ hours	170 °C
RF Input Power at TX_IN	Into 50 Ω Load for 802.11a/n/ac/ax (No Damage), Transmit Mode	+10 dBm
RF Input Power at ANT	(No Damage), Receive LNA On Mode	+10 dBm
RF Input Power at ANT	(No Damage), Receive Bypass Mode	+25 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. This is an InGaP device designed for high duty cycle applications with Tj>30 °C over ambient.

Recommended Operating Conditions

Parameter	Min.	Тур.	Max.	Units
Operating Frequency	5150		5850	MHz
Extended Operating Frequency	5150		5925	MHz
Device Voltage (V _{CC} & V _{DD})	+4.5	+5	+5.25	V
Control Voltage – High	+1.6	+1.8	Vcc	V
Control Voltage - Low	0		+0.4	V
Toperating *	-40		+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. * Toperating is temperature at package ground.

Electrical Specifications

Parameter	Conditions	Min.	Тур.	Max.	Units
Transmit (TX_IN-ANT) Mode	Unless otherwise noted: V _{CC} =5V, T=+25°C, PA_EN=High, LNA_EN=Low, Only through path between RX_OUT and LNA_IN			ow,	
11ax HE80 Output Power	MCS11 1024QAM		16		dBm
Dynamic EVM	IVICSTT 1024QAIVI			-47	dB
11ax HE80 Output Power	NOC44 40040 ANA		18		dBm
Dynamic EVM	MCS11 1024QAM			-43	dB
11ac VHT80 Output Power	M000 0500 AM	22	23		dBm
Dynamic EVM	MCS9 256QAM			-35	dB
11n HT20/40 Output Power	N007.040AM	23	24		dBm
Dynamic EVM	MCS7 64QAM			-30	dB
Margin to VHT20 Spectral Mask	P _{OUT} = +26 dBm, 11n MCS0		7	0	dBc
Gain		31	33		dB
Gain Flatness	Across any 80 MHz Channel	-0.5		+0.5	dB
Out of David Cain	f = 3300-3800MHz			-10	dB
Out of Band Gain	f > 7000MHz			4	dB



Parameter	Conditions	Min.	Тур.	Max.	Units
TX_IN Port Return Loss		4	12		dB
ANT Port Return Loss		9	14		dB
Quiescent Current	RF Off		150		mA
	P _{OUT} = +16 dBm		195		mA
Operating Current	P _{OUT} = +18 dBm		215		mA
Operating Current	P _{OUT} = +23 dBm		290	320	mA
	P _{OUT} = +26 dBm		375	435	mA
2 nd Harmonics	P _{OUT} = +27 dBm 802.11a 6 MBps		-45	-40	dBm/MHz
3 rd Harmonics	P _{OUT} = +27 dBm 802.11a 6 MBps		-55	-45	dBm/MHz
ANT-LNA_OUT Isolation			40		dB
RF Power Detect Coupling			17		dB
	RF Off		0.26		V
DC Dawar Datast Valtage	P _{OUT} = +16 dBm		0.43		V
DC Power Detect Voltage	P _{OUT} = +23 dBm		0.70		V
	P _{OUT} = +27 dBm		1.00		V
RECEIVE (ANT-LNA_OUT) LNA ON	Unless otherwise noted: V _{CC} =5V,	T=+25°C, PA_	EN=Low,	LNA_EN=I	ligh,
MODE	Only through path be	tween RX_OU	T and LNA	A_IN	
Gain		15	16		dB
Gain Flatness Across any 80 MHz Channel		-0.1		+0.1	dB
Out of Band Gain	f = 2400-2500 MHz		-30		dB
Noise Figure			2	2.4	dB
LNA_OUT Port Return Loss		8	10		dB
ANT Port Return Loss		10	11		dB
Input P _{1dB}		-6	-4		dBm
Input IP3		+8	+12		dBm
Rx Operating Current			20		mA
RECEIVE (ANT-LNA_OUT) BYPASS MODE	Unless otherwise noted: V _{CC} =5V _s Only through path be	_		_	Low,
Bypass Loss			7	7.5	dB
Loss Flatness Across any 80 MHz Channel		-0.1		+0.1	dB
Out of Band Gain	f = 2400-2500 MHz		-30		dB
LNA_OUT Port Return Loss		10	12		dB
ANT Port Return Loss		8	10		dB
Input P _{1dB}		+24	+27		dBm
Input IP3		+30	+39		dBm
GENERAL SPECIFICATIONS	Unless otherwise noted: V _{CC} =5V, T=+2 Only through path be				acy +/-1dB
Control Current - High	Only through path be		10		μΑ
Control Current - Low			1.0	1	μΑ
Condition Low	Transmit to LNA On or Bypass Mode			400	nS
	LNA On to Bypass Mode			200	nS
Switching Time	Bypass to LNA On Mode			200	nS
	LNA On or Bypass to Transmit Mode			400	nS
	LIVITOR Dypass to Transmit Wode			700	110



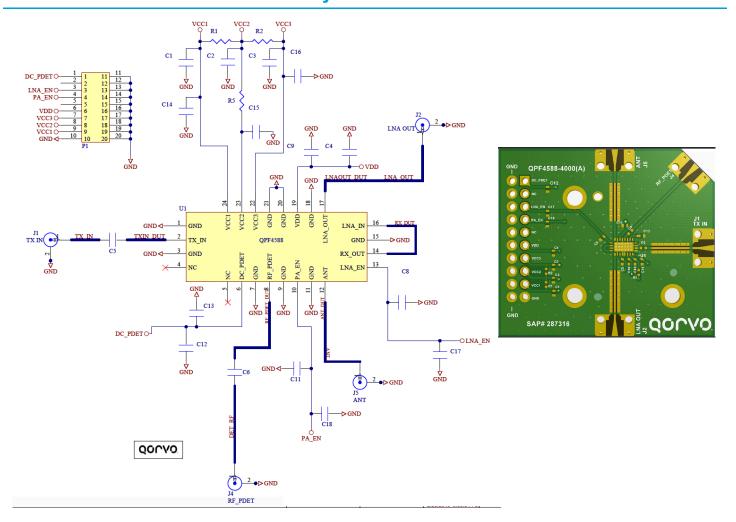
Parameter	Conditions	Min.	Тур.	Max.	Units
PA Stability - Output VSWR	CW No Spurious above -41.25dBm/MHz		10:1		
Output Power Range		0		27	dBm
Thermal Resistance, θ _{ic}	Junction to case		31		°C/W

Logic Truth Table

Mode	PA_EN	LNA_EN
Bypass	Low	Low
Transmit	High	Low
LNA On	Low	High
Not Used	High	High



Evaluation Board Schematic and Layout

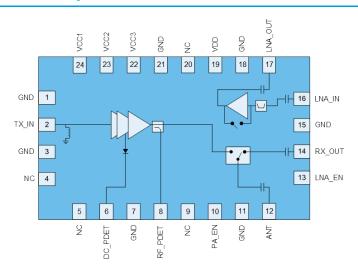


Bill of Material

Ref. Des.	Value	Description	Manuf.	Part number
_	-	Printed Circuit Board		
U1	-	5GHz Wi-Fi Front End Module	Qorvo	QPF4588
C5, C13	10 pF	Capacitor, Chip, 5%, 50V, C0G, 0402	Murata	GRM1555C1H100JA01D
C8, C9, C11	1000 pF	Capacitor, Chip, 10%, 50V, X7R, 0402	Murata	GRM155R71H102KA01D
C14, C15, C16	2.2 µF	Capacitor, Chip, 10%, 6.3V, X5R, 0402	Taiyo Yuden	RM JMK105BJ225KV-F
R1, R2, R5, C6	0 Ω	Resistor, Chip, 5%, 1/10W, 0402	Kamaya	RMC1/16SJPTH
C1, C2, C3, C4, C12, C17, C18	-	Do Not Install		



Pin Configuration and Description



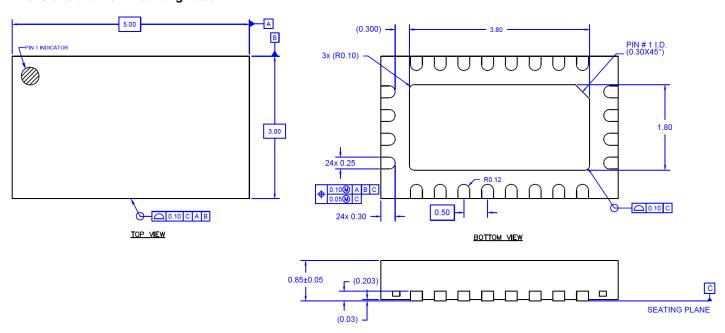
Top View

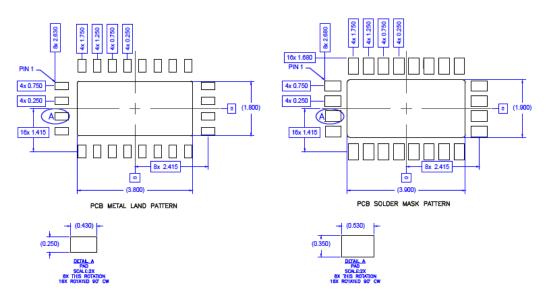
Pin Number	Label	Description
1	GND	Ground connection.
2	TX_IN	RF input. Internally matched to 50 Ω and DC Shorted.
3	GND	Ground connection.
4	NC	No electrical connection.
5	NC	No electrical connection.
6	DC_PDET	DC power detector. Provides an output voltage proportional to the RF output power level
7	GND	Ground connection.
8	RF_PDET	RF power detector. Provides an RF output proportional to the RF output power level
9	NC	No electrical connection.
10	PA_EN	Control pin.
11	GND	Ground connection.
12	ANT	RF bi-directional antenna port. Internally matched to 50 Ω and DC blocked.
13	LNA_EN	Control pin.
14	RX_OUT	RF output from the RX branch of the T/R switch. Internally matched to 50 Ω and DC blocked.
15	GND	Ground connection.
16	LNA_IN	RF input to the low noise amplifier. Internally matched to 50 Ω and DC blocked.
17	LNA_OUT	RF output from the low noise amplifier. Internally matched to 50 Ω and DC blocked.
18	GND	Ground connection.
19	VDD	LNA supply voltage.
20	NC	No electrical connection.
21	GND	Ground connection.
22	VCC3	3 rd stage supply voltage
23	VCC2	2 nd stage supply voltage
24	VCC1	1st stage supply voltage
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.



Mechanical Information

Dimensions and PCB Mounting Pattern





Thermal vias for center slug should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the evaluation board layout.

Notes:

- 1. All dimensions are in millimeters. Angles are in degrees.
- 2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
- 3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B (750V)	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C2a (750V)	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020



Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: NiPdAu-Ag

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- · Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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