UG0726
User Guide
PolarFire FPGA Board Design

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Following is a summary of changes made in revision 2.0 of this document:

- Values in the Power-Supply Decoupling Capacitors—MPF300-FCG484 table are updated. For more information, see Table 2, page 6.
- Values and parameters are updated in the SPI Master Mode Programming Pins table. For more information, see Table 8, page 14.
- Updated Figure 2. For more information, see Figure 3, page 8.
- Added the unused power-supply pins table. For more information, see Table 4, page 9.
- Updated Figure 9. For more information, see Figure 9, page 15.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 PolarFire FPGA Board Design

Good board design practices are required to achieve expected performance from both PCBs and PolarFire™ devices. High-quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines must be treated as a supplement to the standard board-level design practices.

This chapter is intended for readers who have a good understanding of the PolarFire device, are experienced in digital and analog board design, and are knowledgeable in the electrical characteristics of systems. It discusses power supplies, high-speed interfaces, various control interfaces, and the associated peripheral components of PolarFire FPGAs. Background information on the key theories and concepts of board-level design is available in *High Speed Digital Design: A Handbook of Black Magic*[1], and other industry literature.

2.1 Designing the Board

The PolarFire FPGA is a fifth-generation flash-based FPGA that supports various high-speed memory interfaces such as DDR3/DDR4; lowest power 12.7 Gbps transceiver (XCVR); built-in low-power dual PCIe Gen2 and fabric I/Os such as high-speed I/O (HSIO); and general-purpose I/O (GPIO).

The PolarFire FPGA HSIO is a multi-standard I/O optimized for low-power DDR3, DDR4, LPDDR2, and LPDDR3 performance. Transceiver I/Os are dedicated to high-speed serial communication protocols such as PCIe, 10 GbE, Interlaken, JESD204B, CPRI, and Serial Digital Video, as well as user-defined high-speed serial protocol implementation in fabric.

Routing high-speed serial data over a PCB is a challenge because losses, dispersion, and crosstalk effects increase with speed. Channel losses and crosstalk decrease the signal-to-noise ratio and limit the data rate on the channel.

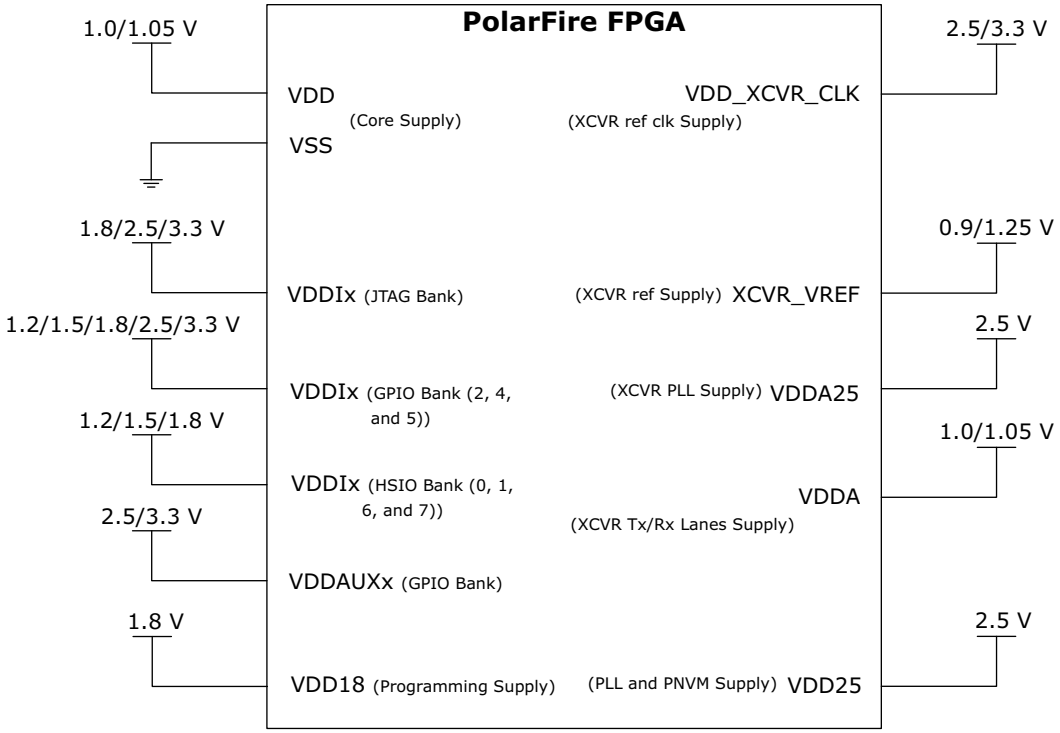
Subsequent sections discuss the following:

1. Johnson, Howard, and Martin Graham, High Speed Digital Design: A Handbook of Black Magic. Prentice Hall PTR, 1993. ISBN-10 0133957241 or ISBN-13: 978-0133957242

2.2 Power Supplies

The following illustration shows the typical power supply requirements for PolarFire devices, and the recommended connections of power rails when every part of the device is used in a system. For information on decoupling capacitors associated with individual power supplies, see Table 3, page 7.

Figure 1 • **Power Supplies**



Note: The XCVR_VREF supply is required when the VDD_XCVR_CLK supply is used. V_{DD} and V_{DDA} can use the same power supply from 1.0 V to 1.05 V; separate regulator supplies are not required. External RC filters are not required for PLL power supplies.

For the device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All overshoots and undershoots must be within the absolute maximum ratings provided in the *DS0141: PolarFire FPGA Datasheet*.

2.2.1 Core Power Supply Operations

The PolarFire device core supply operates either at 1.0 V or 1.05 V. Logic in the fabric operates faster with the 1.05 V device core supply. VDD and VDDA (XCVR Tx/Rx lane supply) can operate at the same voltage either at 1.0 V or 1.05 V.

The various power supplies required for PolarFire FPGAs are as follows:

- VDD—is the main power supply for PolarFire devices. VDD supplies must be connected to the appropriate power rail.
  - VDD18—is a programming power supply for PolarFire devices and must use the correct power supply to connect a rail. For more information about power supplies, see Figure 1, page 5.
  - VDD25—is a PLL and PNVM supply for PolarFire devices and must use the correct power supply to connect a rail. For more information about power supplies, see Figure 1, page 5.
- VDDIx—supplies power to I/O banks in the PolarFire devices. For more information about unused pins, see Unused Power Supply, page 9.
- VREFx—is the reference voltage for LPDDR2, DDR3, and DDR4 signals, which is powered through the corresponding bank supply such as VDDIx.

- VDDAUXx—is the auxiliary power supply for PolarFire devices. VDDAUXx supplies must be connected to the appropriate power rail. It supports LVDS and must keep the rail noise free.

Note: It is recommended to power up the core supplies in the following sequence: VDD, VDD18, and VDD25. All the other supplies can be powered up in any sequence. VDD, VDDA, VDD25, and VDDA25 operating voltage tolerance is 3%, and VDDI operating voltage tolerance is 5%.

For detailed pin descriptions, see *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide*.

2.2.2 Power-Supply Decoupling

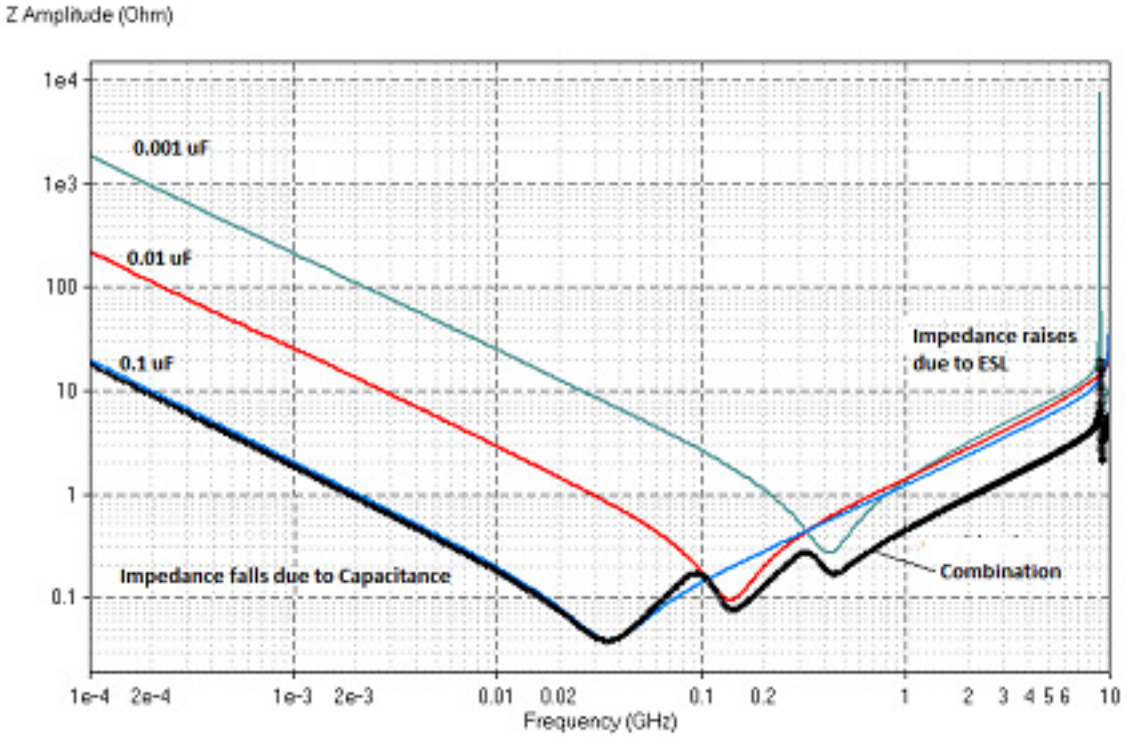
To reduce any potential fluctuation on the power-supply lines, decoupling capacitors, bypass capacitors, and other power supplies, filtering techniques must be used. Solid power and ground planes are needed in PCB in conjunction with the decoupling recommendations to ensure a proper device operation.

Ceramic capacitors are preferred for high-frequency noise elimination and tantalum capacitors for low-frequency noise elimination.

- For values ranging from 1 nF to 100 µF, use X7R or X5R (dielectric material) type capacitors.
- For values ranging from 100 µF to 1000 µF, use tantalum capacitors.

The following figure shows an impedance versus frequency graph for effective combinations of three values of capacitors. From the graph, it is evident that impedance is less for wider frequency bands when different capacitors are in parallel.

Figure 2 • **Impedance of Three Capacitors in Parallel**



The following table lists the recommended number of on-board decoupling capacitors for the MPF300-FCG1152 device.

Table 1 • **Power-Supply Decoupling Capacitors—MPF300-FCG1152**

		Ceramic				Tantalum		
Pin Name	**No. of Pins**	**0.01 µF**	**0.1 µF**	**10 µF**	**4.7 µF**	**47 µF**	**100 µF**	**1 µF**
VDD[1]	28		28	1		2		
VDD_XCVR_CLK[2]	3		2	1				
VDD18[3]	12		5			1		
VDD25[4]	6		6	1				
VDDA[1]	35		6	1	3	1		
VDDA25[4]	4		4			1		
VDDAUX2[5]	5		5			1		
VDDAUX4[5]	5		5			1		
VDDAUX5[5]	4		4			1		
VDDI0[6]	10		5			1		
VDDI1[6]	6		5			1		
VDDI2[7]	13		5			1		
VDDI3[8]	2		2	1				
VDDI4[7]	12		5			1		
VDDI5[7]	9		5			1		
VDDI6[9]	12		5			1		
VDDI7[9]	12		5			1		
XCVR_VREF[10]	2		2					

1. Must connect VDD and VDDA to 1.0 V or 1.05 V
2. Must connect VDD_XCVR_CLK to 2.5 V or 3.3 V
3. Must connect VDD18 to 1.8 V
4. Must connect VDD25 and VDDA25 to 2.5 V
5. Must connect VDDAUX2, VDDAUX4, and VDDAUX5 to 2.5 V or 3.3 V
6. Must connect VDDI0 and VDDI1 to 1.2 V, 1.5 V, or 1.8 V
7. Must connect VDDI2, VDDI4, and VDDI5 to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V
8. Must connect VDDI3 to 1.8 V, 2.5 V, or 3.3 V
9. Must connect VDDI6 and VDDI7 to 1.2 V, 1.5 V, or 1.8 V
10. Must connect XCVR_VREF to 0.9 V or 1.25 V

Note: The listed power supplies must be connected and the voltage range is optional based on board design requirements.

The following table lists the recommended number of on-board decoupling capacitors for the MPF300-FCG484 device.

Table 2 • **Power-Supply Decoupling Capacitors—MPF300-FCG484**

		Ceramic				Tantalum		
Pin Name	**No. of Pins**	**0.01 µF**	**0.1 µF**	**10 µF**	**4.7 µF**	**47 µF**	**100 µF**	**1 µF**
VDD	14		14	1		2		
VDD_XCVR_CLK	2		2	1				
VDD18	4		4			1		
VDD25	5		5	1				
VDDA	16		6	1	3	1		
VDDA25	4		4	1				
VDDAUX2	4		4			1		
VDDAUX4	3		3			1		
VDDI0	6		5			1		
VDDI1	6		5			1		
VDDI2	12		5			1		
VDDI3	2		2	1				
VDDI4	8		5			1		
XCVR_VREF	2		2					

- These decoupling capacitor values are subject to change based on characterization results.
- Decoupling capacitors other than those listed in Table 1, page 5 can be used if the physical sizes of capacitors meet or exceed the performance of the network given in this example. Substitution would require analysing the resulting power distribution system's impedance versus frequency to ensure that no resonant impedance spikes result. See Figure 1, page 3 for power supply schematics design.

For VDD, VDDA, VDD25, and VDDA25 supplies, the higher power-supply tolerance rate is 3%. When designing the board, the following constraints are recommended for PolarFire devices.

- A large electrolytic or a tantalum capacitor such as 10 µF or 100 µF must be placed no more than two inches away from the chip. The capacitor functions as a reservoir to supply instantaneous charge to the circuits—the charge is not necessarily passed through the inductance of the power trace.
- A smaller cap such as 0.01 µF or 0.1 µF must be placed as close as possible to the power pins of the chip. Placing the smaller cap capacitors closer helps reducing the high-frequency noise in the chip.
- All decoupling capacitors must connect to a large-area, low-impedance ground plane through a via or short trace to minimize the inductance.
- Optionally, a small ferrite bead in series with the supply pin localizes noise in the system, keeps external high-frequency noise from the IC, and keeps internally generated noise from propagating to the rest of the system.
- Feedback resistors' tolerance must be ±1% for values.

The following table lists internal package capacitance details for power supplies associated with the FCG1152 package.

Table 3 • **Internal Package Capacitance for FCG1152**

Supply Name	EIA[1] Size	Code	Description	Part Number	Manufacturer
VDD	0508	IDC	CAP 0508 2.2 µF±20% X7S 4 V LESL8T	W2L14Z225MAT1S	AVX
VDDI0	0306	LICC	CAP 0306 1 µF 20% 4 V X7S CESR 100 mΩ	LLR185C70G105ME01L	MURATA
VDDI1	0306	LICC	CAP 0306 1 µF 20% 4V X7S CESR 100 mΩ	LLR185C70G105ME01L	MURATA
VDDI2	0306	LICC	CAP 0306 1 µF ±20% X7S 6.3 V	LLL185C70J105ME14K	MURATA
VDDI4	0306	LICC	CAP 0306 1 µF ±20% X7S 6.3 V	LLL185C70J105ME14K	MURATA
VDDI5	0306	LICC	CAP 0306 1 µF ±20% X7S 6.3 V	LLL185C70J105ME14K	MURATA
VDDI6	0306	LICC	CAP 0306 1 µF 20% 4 V X7S CESR 100 mΩ	LLR185C70G105ME01L	MURATA
VDDI7	0306	LICC	CAP 0306 1 µF 20% 4 V X7S CESR 100 mΩ	LLR185C70G105ME01L	MURATA
VDDA	0201	MLCC	CAP 0201 4.7 nF 10% 6.3 V X7R 100 mΩ	GRM033R70J472KA01	MURATA
	0201	MLCC	CAP 0201 2.2 nF 10% 6.3 V X7R 200 mΩ	GRM033R70J222KA01	MURATA
	0201	MLCC	CAP 0201 1.5 nF 10% 6.3 V X7R 200 mΩ	GRM033R70J152KA01	MURATA
	0201	MLCC	CAP 0201 1.0 nF 10% 16 V X7R 300 mΩ	CGA1A2X7R1C102K030BA	TDK
VDD18	0306	LICC	CAP 0306 1 µF 20% 4 V X7S CESR 100 mΩ	LLR185C70G105ME01L	MURATA
VDD25	0306	LICC	CAP 0306 1 µF ±20% X7S 6.3 V	LLL185C70J105ME14K	MURATA

1. EIA stands for Electronic Industries Alliance.

2.2.3 Power Supply Sequencing and Power-on Reset

Each PolarFire device includes sophisticated power-up management circuitry. These circuits ensure easy transition from the power-off to power-up state of the device. The embedded system controller is responsible for systematic power-on reset whenever the device is powered on or reset. All the user I/Os are held in a high-impedance state by the system controller until all power supplies are at their required levels and the system controller has completed the reset sequence. The specified ramp rates must be >200 us/V and <100 ms/V. The auto update or IAP recovery uses the ramp rate of >1 ms/V <100 ms/V to power down supplies. The ramp rate applies to both power-up and power-down supplies.

The power-on reset circuitry requires the VDD, VDD25, and VDD18 supplies to ramp monotonically from 0 V to the minimum recommended operating voltage within a predefined time. There is a mandatory sequencing requirement for VDD, VDD18, and VDD25. Power-on reset delay options are available in Libero® SoC PolarFire during design generation.

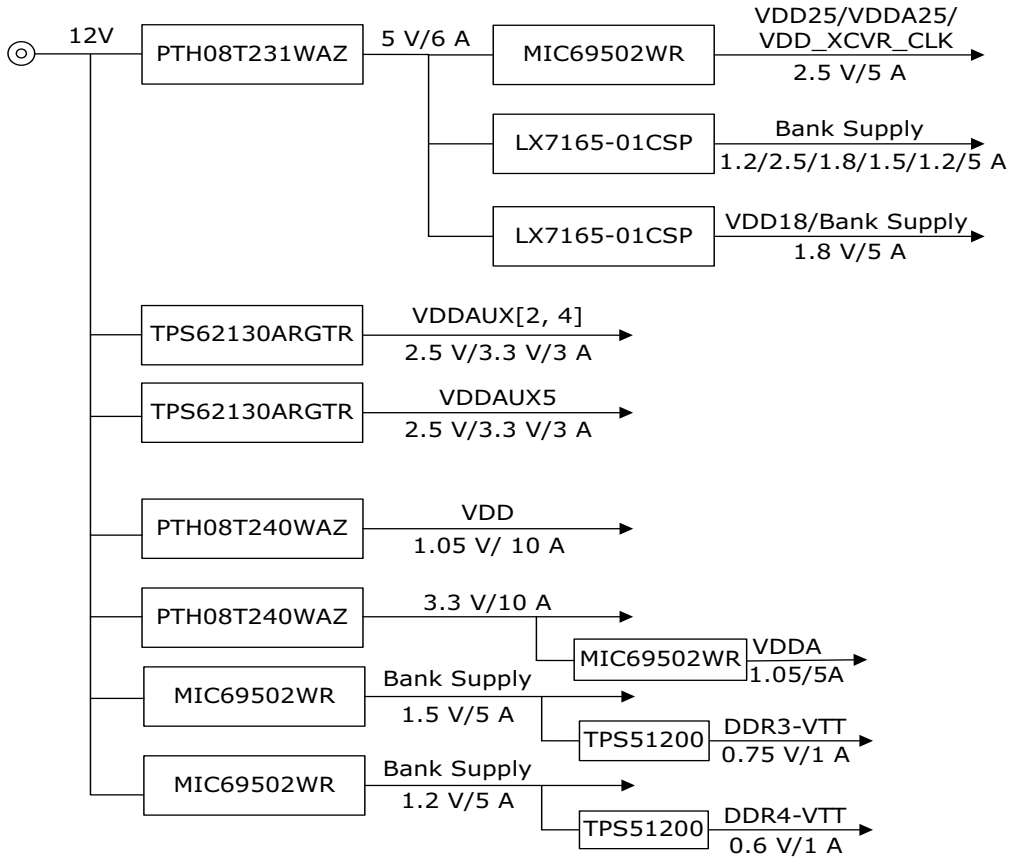
All user I/O bank supplies do not need to be powered up to exit the power-up state. The I/O bank supply must not be floating for unused banks—must be connected to ground to power down.

The VDDA supply is required for the transceiver I/Os to operate, and the VDD_XCVR_CLK supply is required for transceiver reference clocks. For more information, see *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*.

2.2.4 Power-Supply Topology

PolarFire FPGAs require multiple power supplies. The following illustration shows one topology for generating the required power supplies from a single 12 V source. This example power supply topology is based on the PolarFire MPF300-FCG1152 device with DDR3 and DDR4 interfaces.

Figure 3 • **Example of Power-Supply Topology**



2.2.5 I/O Behavior During Power-Up

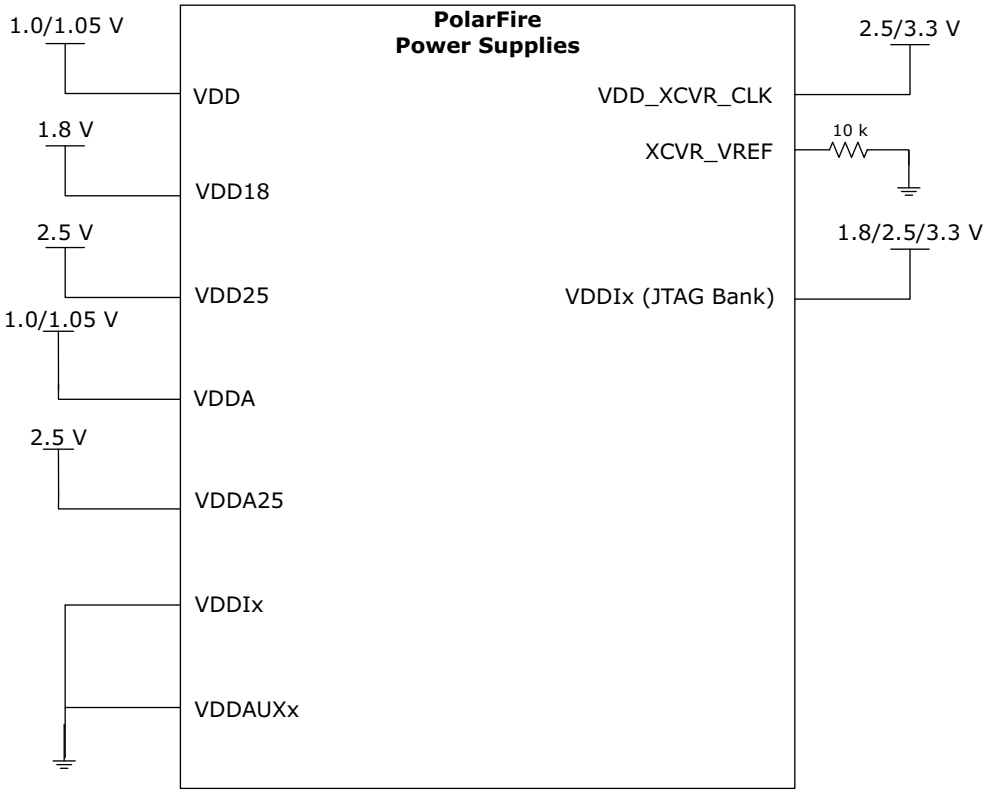
During power-up, dedicated I/O banks are enabled first, for example, bank 3 is the dedicated I/O bank in the MPF300-FCG1152, so user I/Os are enabled before transceiver I/O banks. For more information about power-up, see *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*.

2.2.6 Unused Power Supply

Multiple power supplies are used by PolarFire FPGA I/O banks to provide power to HSIO while VDDI (0, 7, 1, and 6) = 1.2 V, 1.5 V, or 1.8 V and GPIO while VDDI (2, 4, and 5) = 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V lanes. If none of the I/Os are used in a particular bank, then that bank supply can be powered off or connected to ground.

The following illustration shows the recommended connections of power rails when power supplies of unused I/O banks are grounded.

Figure 4 • **Power Supply for I/O Banks**



Note: Tie-offs to VSS can be grouped into a single 10 kΩ resistor. To simplify the board-level routing, 10 kΩ resistors can be used as required.

The following table lists the power-supply pins that can be used in two ways depending on the requirements.

Table 4 • **Unused Power-Supply Pins**

Pin Name	Option 1	Option 2	Description
VDD	1.0/1.05 V		Core voltage
VDD18	1.8 V		Programming voltage
VDD25	2.5 V		PLL and NVM voltage
VDDA	1.0/1.05 V		SerDes Core Voltage
VDDA25	2.5 V		Transceiver PLL power supply
VDDIx (HSIO Banks)	1.2/1.5/1.8 V	Connect to VSS through a 10 kΩ resistor	I/O voltage

Table 4 • **Unused Power-Supply Pins** ***(continued)***

Pin Name	Option 1	Option 2	Description
VDDIx (GPIO Banks)	1.2/1.5/1.8/2.5/3.3 V	Connect to VSS through a 10 kΩ resistor	I/O voltage
VDDI3	1.8/2.5/3.3 V		Dedicated bank voltage
VDDAUXx	2.5/3.3 V	Connect to VSS through a 10 kΩ resistor	Auxiliary voltage
VDD_XCVR_CLK	2.5/3.3 V	Connect to VSS through a 10 kΩ resistor	Supply for reference clock
XCVR_VREF		Connect to VSS through a 10 kΩ resistor	Supply for reference voltage

Note: XCVR_TX and RX signals are not required to be defined on the board rather define them in Libero SoC and the changes are updated on the board automatically.. XCVR_REFCLK pins must be connected to DNC or use it as a global clock.

2.3 User I/Os

PolarFire FPGAs have two types of I/O buffers: HSIO and GPIO. HSIO buffers are optimized for single-ended buffers with supplies from 1.2 V to 1.8 V. GPIO buffers support single-ended and true differential interfaces with supplies from 1.2 V to 3.3 V. Both HSIO and GPIO are PVT compensated I/O buffers.

Note: When the HSIO bank is configured as an LVDS receiver on the board, it requires an external 100 Ω termination.

For more information about key features of I/O buffers and supported standards, see *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide* and *UG0686: PolarFire FPGA User I/O User Guide*.

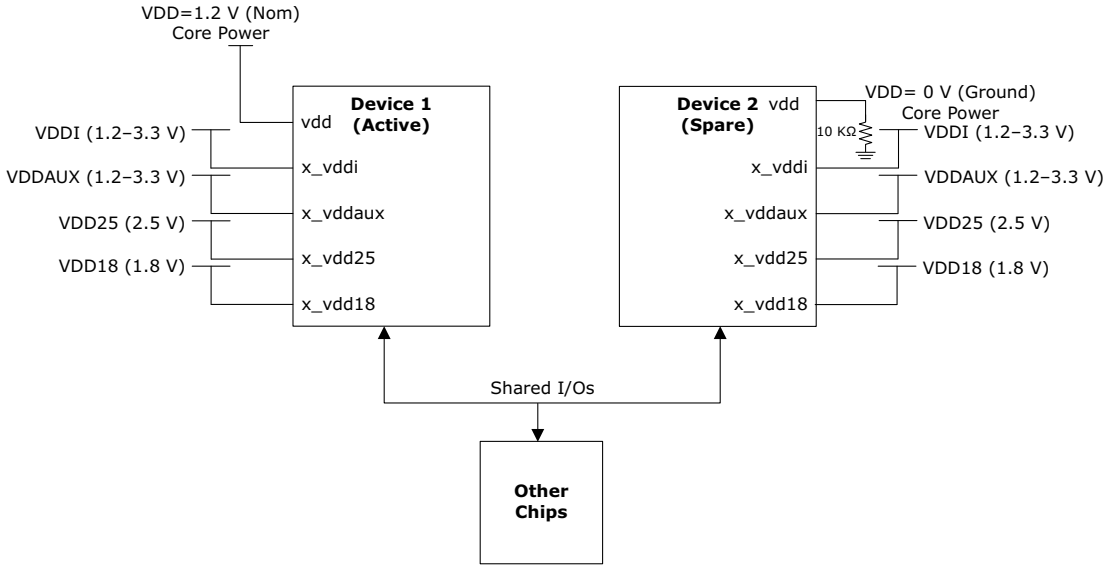
2.3.1 Cold Sparing

PolarFire devices support cold sparing for GPIO and HSIO. Cold sparing is implemented by connecting the devices as shown in the following figure. The system board has two PolarFire devices in parallel and the devices share I/Os. The active PolarFire device has its core powered up and is functional until it is necessary to swap with the spare device. The spare device has its I/O banks powered up to prevent I/O leakage through the ESD diodes and fabric core unpowered, which establishes low power and a protected state for the spare device. At any point, the swap can be made by powering down the core of the active device and powering up the core of the spare device.

The following are advantages of cold sparing:

- I/Os must be tri-stated before and during power-up
- Voltage applied to an I/O must not power up any part of the device
- Device reliability must not be compromised if voltage is applied to I/Os before or during power-up
- Power-up in any sequence
- Spare device is in de-activated mode
- All I/O banks with active I/Os must be powered up
- Spare device I/O buffers are disabled, but powered

Figure 5 • **Cold Sparing**



The de-activated device must tie the core (vdd) to ground, not floating. The VPP (x_vdd25/x_vdd18) supply, all active bank supplies (x_vddi, x_vdd25, x_vdd18, and x_vddaux), and the VPP programming supplies (x_vdd18 and x_vdd25) must be powered on the de-activated device.

Note: Transceiver and JTAG pins do not support the cold sparing feature.

2.3.2 Hot Socketing (GPIO Only)

Hot socketing (also known as hot swapping or hot plug-in) prevents damage to the PolarFire FPGA if, at any time, voltage is detected at I/Os while the device is powered off. It also helps prevent disruptions that may occur in the rest of the system if the I/Os of a device are connected without a valid power supply.

GPIO supports hot socketing. When hot socketing is used, it disables the parasitic n-well diode from the associated pad to V_{DDIx} to reduce pad leakage currents. Hot socketing is not used for applications (such as PCI) that require a parasitic n-well diode to remain enabled.

In hot socketing, GPIOs are in high-impedance (hi-Z) state. This state is used for disabling output drive modes, termination modes, weak pull-up/pull-down modes, the PCI clamp (the clamp between pad and V_{DDIx}), receivers, and all V_{REF} input pads.

The GPIO maintains the following high-impedance state until the power supplies are at a valid state.

- V_{DDAUx} is greater than or equal to 1.6 V
- V_{DDIx} is greater than or equal to 0.8 V
- V_{DD} and V_{DD25} are both high and the PolarFire FPGA controller has asserted the global I/O ring signal (IO_EN)

Note: For I/Os that implement the V_{REF} pin for a terminated I/O standard, the current flowing in and out of the pin must be minimized so that the external V_{REF} signal is not affected.

2.3.2.1 Over-Voltage Tolerance for GPIO

If GPIO is configured with the following settings, GPIO supports over-voltage tolerance, ensuring that the I/O signal at the pad is at a higher potential than the V_{DDIx} power supply.

Table 5 • **Over-Voltage Tolerance**

Standard	OE	Clamp Diode	V_{REF} (Input)	Weak Pull-Up/ Pull-Down	Termination	Hot-plug
PCI	x	On	On	On	On	Disabled

Table 5 • **Over-Voltage Tolerance *(continued)***

Standard	OE	Clamp Diode	V_{REF} (Input)	Weak Pull-Up/ Pull-Down	Termination	Hot-plug
GPIO	1	On	On	On	On	Disabled
	0	Off	Off	Off	Off	Enabled

For recommended operating conditions about over-voltage tolerance, see *DS0141: PolarFire FPGA Datasheet*.

2.4 Clocks

PolarFire devices offer two on-chip RC oscillators (one 2 MHz and one 160 MHz) to generate free-running clocks. The clocks do not have any I/O pads and do not require external components to operate.

The following table lists the number of RC oscillators available in PolarFire devices.

Table 6 • **RC Oscillator Count**

Resource	Supported Range (MHz)	MPF100	MPF200	MPF300	MPF500
On-chip oscillator	2	1	1	1	1
	160	1	1	1	1

For more information about clocking in PolarFire devices, see *UG0684: PolarFire FPGA Clocking Resources User Guide*.

2.5 Reset

PolarFire devices have a dedicated asynchronous Schmitt Trigger reset input pin (DEVRST_N) with a maximum slew rate not faster than 1 µs. The active-low DEVRST_N signal must be asserted only when the device is unresponsive due to unforeseen circumstances. It is not recommended to use this reset as a design reset. Design resets must be implemented using an HSIO or a GPIO pin of the FPGA.

It is not recommended to assert this pin during programming operation, as this may cause severe consequences including corruption of the device configuration. Asserting the DEVRST_N signal tri-states all user I/Os and resets the system. De-asserting the DEVRST_N signal enables the system controller to begin its startup sequence.

If unused, DEVRST_N must be pulled up to VDDI3 through a 10 kΩ resistor. Adding a capacitor to ground on DEVRST_N prevents high-frequency noise and unwanted glitches that may reset the device. For more information about reset, see *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*.

2.6 Device Programming

The PolarFire device can be programmed using one of two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- JTAG programming
- SPI master mode programming
- SPI slave mode programming

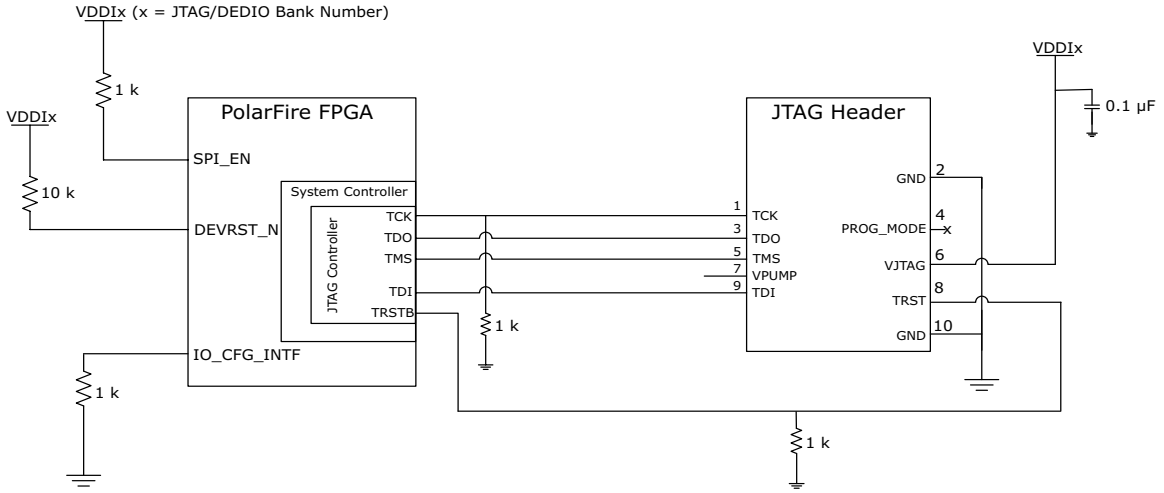
The PolarFire FPGA supports programming modes through the internal system controller using SPI master mode, or an external master using JTAG or SPI interfaces. For detailed information on hardware connections for each programming mode, see *UG0714: PolarFire FPGA Programming User Guide*.

2.6.1 JTAG Programming

The JTAG interface is used for device programming and testing, or for debugging firmware. When the device reset (DEVRST_N) is asserted, JTAG I/Os are still enabled but cannot be used as the TAP controller in reset. JTAG I/Os are powered by VDDI in the I/O bank where they reside.

The following illustration shows the board-level connectivity for JTAG programming mode in PolarFire devices.

Figure 6 • **JTAG Programming**



The following table lists the JTAG pin names and descriptions.

Table 7 • **JTAG Pins**

Pin Names	Direction	Weak Pull-Up /Unused Condition	Description
JTAG_TMS	Input	Yes/DNC	JTAG test mode select.
JTAG_TRSTB	Input	Yes[1]	JTAG test reset. Must be held low during device operation.
JTAG_TDI	Input	Yes/DNC	JTAG test data in.
JTAG_TCK	Input	No[2]	JTAG test clock. Microsemi recommends that TCK be tied to VSS or VDDI through a resistor on the board when unused per IEEE 1532 requirements. This prevents to tempole current on the input buffer.
JTAG_TDO	Output	No/DNC	JTAG test data out.

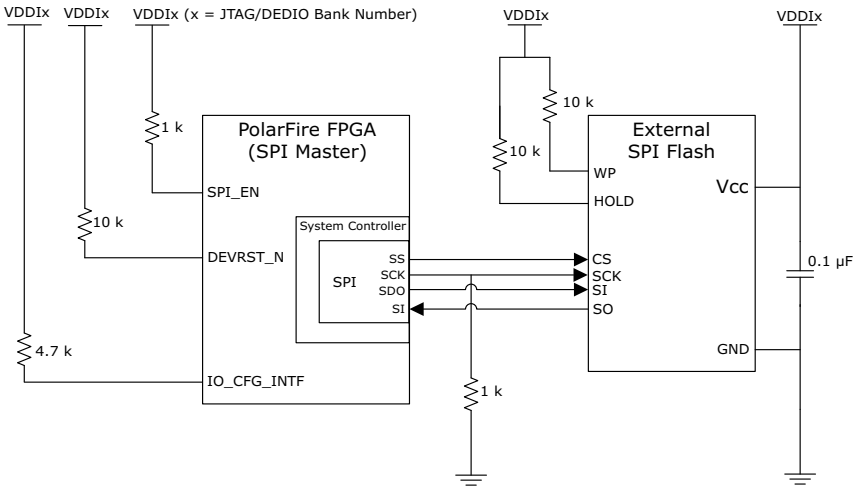
1. Must connect to VDDI3 through 1 kΩ resistor per pin, not to be shared with any other pins.
2. Must connect to VSS through 10 kΩ resistor.

2.6.2 SPI Master Mode Programming

The embedded system controller contains a dedicated SPI block for programming, which can operate in master or slave mode. In master mode, the PolarFire device interfaces are used to download programming data through the external SPI flash. In slave mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

The following illustration shows the board-level connectivity for SPI master mode programming in PolarFire devices.

Figure 7 • **SPI Master Mode Programming**



The following table lists the SPI master mode programming pin names and descriptions.

Table 8 • **SPI Master Mode Programming Pins**

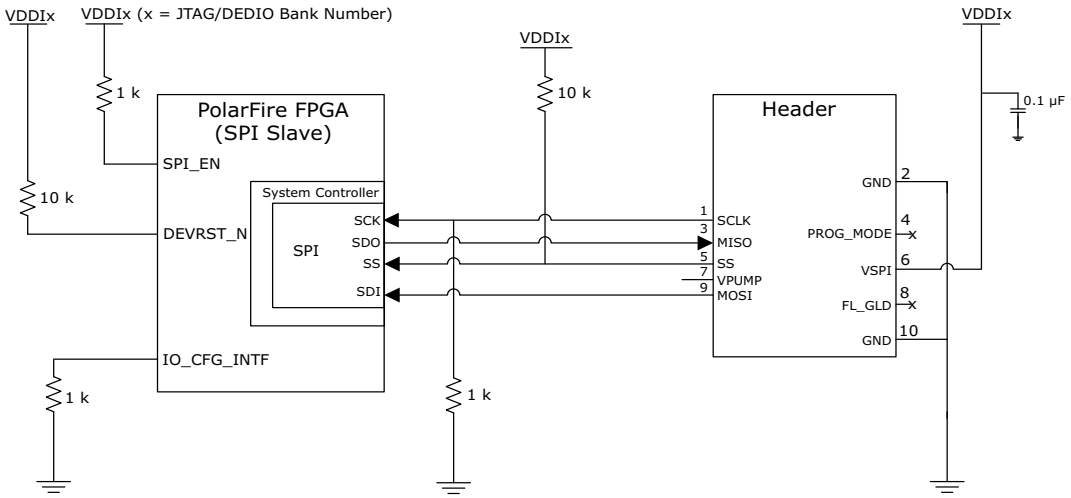
SPI Pin Name	Direction	Weak Pull-Up Resistor	Unused Condition	Description
SCK	Bidirectional		Connect to VSS through a 10 kΩ resistor	SPI clock.[1]
SS	Bidirectional		Connect to VSS through a 10 kΩ resistor	SPI slave select.[1]
SDI	Input	Pull-up	Connect to VDDI3 through a 10 kΩ resistor	SDI input.[1]
SDO	Output		DNC	SDO output.[1]
SPI_EN	Input		Connect to VSS through a 10 kΩ resistor	SPI enable. 0: SPI output tri-stated 1: Enabled Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input		Connect to VSS through a 10 kΩ resistor	SPI I/O configuration. 0: SPI slave interface 1: SPI master interface Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a master or slave.

1. The SCK, SS, SDI, and SDO pins are shared between the system controller and the FPGA fabric. When the system controller's SPI is enabled and configured as a master, the system controller hands over the control of the SPI to the fabric (after device power-up).

2.6.3 SPI Slave Mode Programming

The following illustration shows the board-level connectivity for SPI slave mode programming in PolarFire devices.

Figure 8 • **SPI Slave Mode Programming**

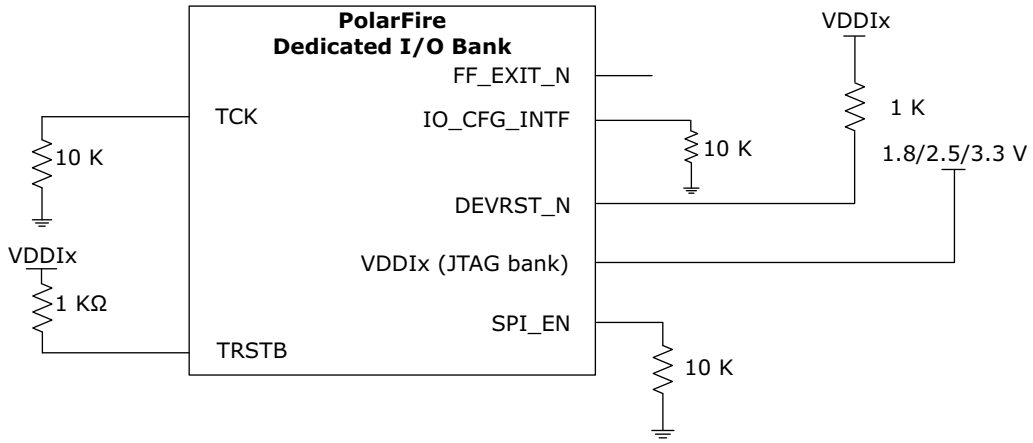


2.6.4 Unused Dedicated Pins

When dedicated pins are unused, they must be connected to power supply through resistors or grounded to reduce leakage currents.

The following illustration shows the recommendation for unused dedicated pins. The TCK, TRSTB, and SPI_EN pins are unused, and grounded through resistors.

Figure 9 • **Recommendation for Unused Dedicated Pins**



Note: TRSTB must be connected to VDDIx through 1 kΩ resistors for each pin. The pin is dedicated to VDDIx.

2.7 Transceiver

The following table lists the transceiver features supported in PolarFire devices, and transceiver blocks are located on the east corner of the device.

Table 9 • **Transceiver Feature Support in PolarFire Devices**

Feature	Supported in PolarFire Devices
Data rate	250 Mbps to 12.7 Gbps
Power supplies	Analog (VDDA25)—2.5 V Digital (VDDA)—1.0 V
Spread spectrum clock generation	Yes
Pre-tap and post-tap de-emphasis	Yes
CTLE	Yes
DFE	Yes
Hot-socketing	Yes

For more information about implementing PCIe interfaces, see *UG0685: PolarFire FPGA PCI Express User Guide*. For more information about implementing other transceiver based interfaces and power supplies, see *UG0677: PolarFire FPGA Transceiver User Guide*.

The following table lists the number of transceivers supported in various PolarFire devices.

Table 10 • **Transceiver Support in PolarFire Devices**

Device	Transceiver Lane	Tx PLL	Reference Clock I/Os
MPF100	8	6	12
MPF200	16	11	22
MPF300	16	11	22
MPF500	24	15	30

For more information about supported I/O standards, see *UG0686: PolarFire FPGA User I/O User Guide*.

2.7.1 Reference Clock

A transceiver reference clock is delivered to each transmit PLL for transmit functions and for receive clock data recovery (CDR).

2.7.1.1 Transceiver Reference Clock Requirements

The selection of the reference clock source or clock oscillator is driven by many parameters such as frequency range, output voltage swing, jitter (deterministic, random, and peak-to-peak), rise and fall times, supply voltage and current, noise specification, duty cycle and duty cycle tolerance, and frequency stability. For transceiver reference clock pins, the internal ODT option should be enabled.

The following are requirements for the transceiver reference clock:

- Must be within the range of 20 MHz to 400 MHz.
- Must be within the tolerance range of I/O standards. The reference input buffer is provided and is expected to support these input standards directly without external components on the board: 1.2 V PCML, 1.5 V PCML, and 2.5 V PCML, Differential LVPECL also supports single-ended PECL such as HCSL, LVDS, HSTL, LVTTL, and LVCMOS, which support the power supply range of 1.5 V, 1.8 V, 2.5 V, and 3.3 V, with external termination resistors.

- The input clock for PCIe is typically a 100 MHz reference clock provided by the host slot for an end point device through the PCIe connector of the motherboard. If two components connected through the PCIe bus use the same 100 MHz clock source, it is called common clock mode. In any other case, the PCIe device is in separated clock mode where one component either does not use a 100 MHz reference clock or uses a 100 MHz reference clock that does not have the same source and phase as the one used by the connected component.

See the *PCI Express Base specification Rev 2.1* for detailed PHY specifications. Also, see the *PCIe Add-in Card Electro-Mechanical (CEM)* specifications.

2.8 AC Coupling

Each transmit channel of a PCIe lane must be AC-coupled to allow link detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops when the data signal contains a long string of consecutive identical bits. For non-PCIe applications, a PolarFire device requires the receive inputs to be AC-coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 µF) for AC-coupling capacitors must be used to maximize link signal quality and must conform to *DS0141: PolarFire FPGA Datasheet* electrical specifications.

2.9 Brownout Detection

The PolarFire FPGA functionality is guaranteed only if V_{DD} is above the recommended level specified in the datasheet. Brownout detection occurs when V_{DD} drops below the minimum recommended operating voltage. When this occurs, the device operation may not be reliable. The design might continue to malfunction even after the supply is brought back to the recommended values because parts of the device might have lost functionality during brownout. The V_{DD} supply is protected by an built-in brownout detection circuit.

When V_{DD} is not stable, brownout detection occurs. The following instructions can be followed to avoid brownout detection:

- The V_{DD} supply regulator must be placed close to the load devices to minimize the interconnection impedance and the conduction voltage drop across the PCB traces to achieve the best voltage regulation, load transient response, and system efficiency.
- The large current copper shape must be short and wide to minimize the PCB inductance, resistance, and voltage drop.
- The solid copper shape represents the continuous current path.
- Provide the sufficient vias to carry the current to chip.
- Remote sense signals must be route to the chip VDD pins.

For more information about brownout detection, see *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*.

3 Layout Design Considerations

This chapter provides guidelines for the hardware board layout that incorporates PolarFire devices. Good board layout practices are essential to achieve the expected performance from PCBs and PolarFire devices. They help achieve high-quality and reliable results such as low-noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This chapter is intended for readers who have a good understanding of the PolarFire FPGA chip, experience in digital and analog board layout, and knowledge of transmission line theory and signal integrity. For recommended guidelines to design PolarFire FPGA-based boards, see PolarFire FPGA Board Design, page 2.

Note: The target impedance calculated in this chapter is with respect to the development board. The simulations show the impedance that meets the target impedance of the development board. The target impedance depends on the logic implemented on PolarFire FPGAs; hence, Microsemi recommends calculating the target impedance of the board.

3.1 Power Supply

In power supply design, it is important to know the target impedance of power planes, which varies depending on the design. Complex FPGA designs have increasing amounts of current transients switching across the power bus. Simultaneously switching outputs (SSO) contribute a major share of instantaneous current issues.

Power supply design helps in planning the requirement of the number of decoupling capacitors based on the target impedance. The number of decoupling capacitors varies based on the design. Decoupling is necessary to prevent the instantaneous currents. It is only effective when inductance is minimized. Low inductance decoupling provides localized high-frequency energy to decouple noise from the switching currents of the device power bus. This is most effective when capacitors are in close proximity to the device. Some of these high frequency capacitors are required to be placed directly by the FPGA.

To calculate the number of decoupling capacitors, it is important to know the target impedance of the power plane. Target impedance is calculated based on EQ1:

$$Z_{Min} = \%\ Ripple \times V_{supply}/I_{trans}$$

Where,

- **V_{supply}**: Supply voltage of the power plane.
- **% Ripple**: Percentage of ripples allowed on the power plane. See *DS0141: PolarFire FPGA Datasheet* for details.
- **I_{trans}**: Transient current drawn on the power plane. Generally, transient current is half of the maximum current, which is taken from the power calculator sheet.
- **Z_{min}**: Target impedance of the plane.

The plane shapes given in this chapter are with reference to the *UG0747: PolarFire FPGA Evaluation Kit User Guide*. This may vary depending on the design.

PolarFire FPGA power supplies are classified as:

- Core Power Supply (VDD), page 19
- DDR, page 21
- I/O Power Supply, page 22
- Transceiver, page 23
- Termination Schemes, page 28
- PCB Capacitor Placement and Mounting Techniques, page 29

3.2 Core Power Supply (VDD)

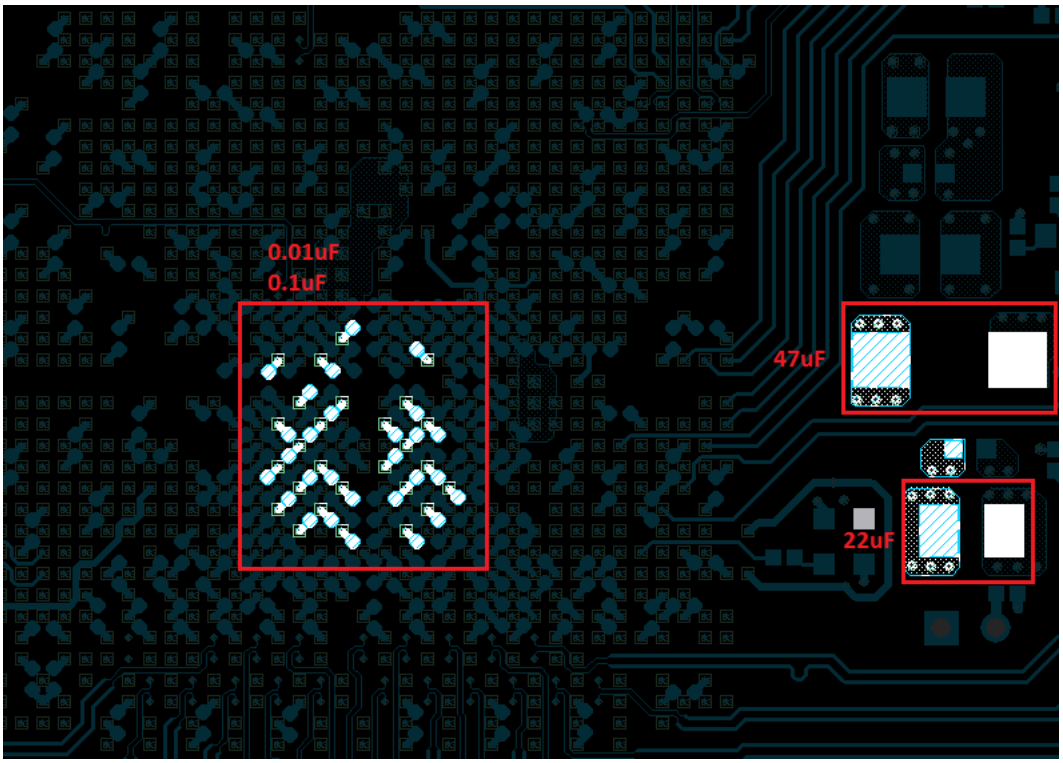
The core power supply must have low-noise and low-ripple voltages, as prescribed in the *DS0141: PolarFire FPGA Datasheet*. Proper care should be taken while designing the power supply (VDD) for core. Optimal placement of decoupling capacitors and plane geometry greatly influences the power supply distribution for PolarFire devices.

3.2.1 Component Placement

- The bulk capacitors (330 µF and 100 µF) should be placed near the PolarFire device.
- The bypass capacitors (47 µF and 22 µF) should be placed near the device or, if possible, on the periphery of the device.

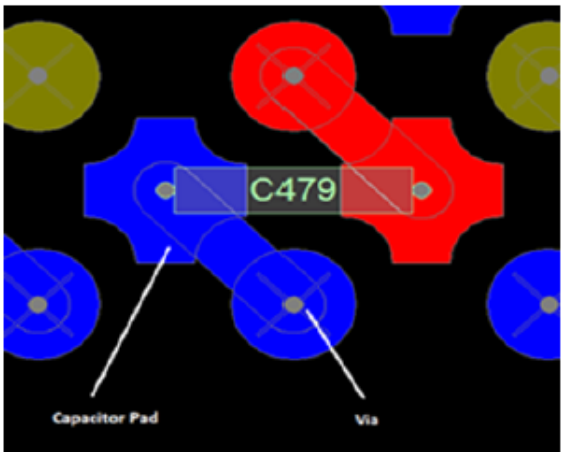
The following figure shows a sample bulk capacitor placement on the *UG0747: PolarFire FPGA Evaluation Kit User Guide*.

Figure 10 • **Placement of Capacitors for VDD Plane**



All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or as small as possible because they are required to be mounted on the back side of the board. They should fit between the adjacent vias of ball grid array (BGA) package pins. Decoupling capacitors are selected to have low impedance over operating frequency and temperature range. Capacitor pad to via-trace should be as small as possible. Figure 11, page 20 shows how these capacitors need to be mounted. Microsemi recommends placing the capacitor pad directly on the corresponding vias. The capacitors must not share ground vias. Each decoupling capacitor should have its own via connection to the PCB ground plane.

Figure 11 • **Capacitor Placement under BGA Vias**

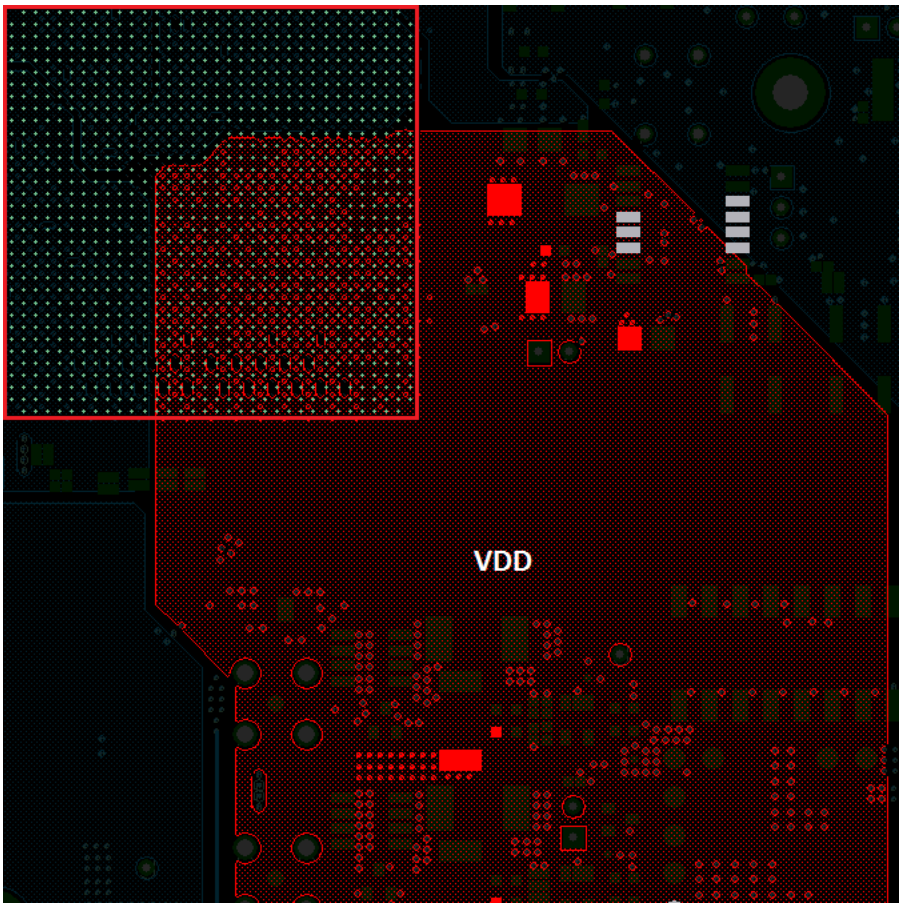


3.2.2 Plane Layout

Microsemi recommends using the VDD plane, as shown in the following figure.

Note: The plane can be routed in multiple methods. The goal is to have a dedicated, low-impedance plane.

Figure 12 • **VDD Plane**



3.3 DDR

Some of the variants support the LPDDR2, DDR3, DDR3L, LPDDR3, and DDR34 in PolarFire devices. For more information about DDR support in PolarFire devices, see *DS0141: PolarFire FPGA Datasheet*. The layout guidelines of the respective VDDIO should be followed.

Also, it requires VREF voltage for an internal reference. Noise on VREF impacts the read performance of PolarFire devices. VREF lines should be placed away from aggressive nets or switching power supplies. For DDR memory layout guidelines, see the *Micron DDR3 Memory Layout Guidelines*[1]. The VDDIO guidelines should be followed for DDR bank VDDIO.

3.3.1 Component Placement

This section provides component placement guidelines for VREF.

3.3.1.1 VREF

- The 10 µF bypass capacitor should be placed near the device, or at the edge of the device if possible.
- All 0.1 µF and 0.01 µF decoupling capacitors should be 0402 or as small as possible because they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. Decoupling capacitors are selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via-trace should be as small as possible. Figure 10, page 19 shows how these capacitors are mounted. Microsemi recommends placing the capacitor pad directly on the corresponding vias.

3.3.2 Plane Layout

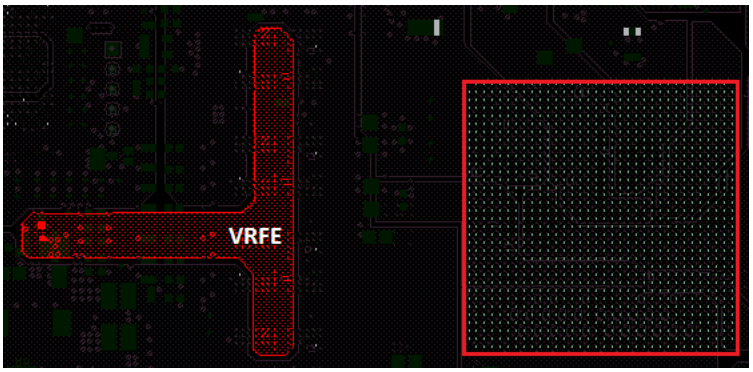
This section provides plane layout guidelines for both VREF and VDDIO.

3.3.2.1 VREF

Noise on VREF impacts the read performance of PolarFire devices. The VREF lines should be routed with no aggressive net or switching power supply nearby. Even though the current is low, VREF should not be routed as trace because it is very susceptible to noise.

The following figure shows the layout of VREF.

Figure 13 • **Layout of VREF**



1.TN-46-14: Hardware Tips for Point-to-Point System Design from Micron

3.3.2.2 VDDIO

- The 47 µF and 22 µF bypass capacitors should be placed near the device, or at the edge of the device if possible.
- All 0.1 µF and 0.01 µF decoupling capacitors should be 0402 or as small as possible because they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. Decoupling capacitors are selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via-trace should be as small as possible. Figure 10, page 19 shows how these capacitors are mounted. These capacitors can also be mounted directly on the pad available on the vias.

3.3.3 Plane Layout

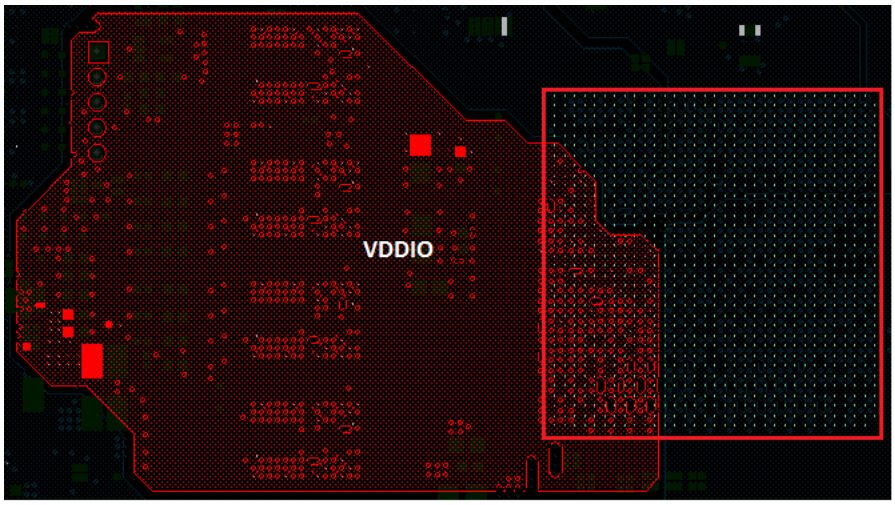
This section provides plane layout guidelines for VDDIO.

3.3.3.1 VDDIO

The shape of the plane does not have a specific requirement. The width of the plane should be sufficient to carry the required current.

The following figure shows the sample layout for VDDIO plane.

Figure 14 • **Layout of VDDIO**



3.4 I/O Power Supply

This section describes the component placement and plane layout of I/O power supply.

3.4.1 Component Placement

- The bypass capacitors (47 µF and 22 µF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted under BGA package. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are selected to have low impedance over operating frequency and temperature range.
- The capacitor pad to via-trace should be as small as possible. Figure 10, page 19 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias. The decoupling capacitors should not be shared via connections.

3.4.2 Plane Layout

The shape of the plane does not have a specific requirement. The width of the plane should be sufficient enough to carry the required current.

3.5 Transceiver

Collateral material of the PolarFire FPGA transceiver enables the system implementation easier for the designer by providing the system solution. Transceivers are high-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 12.7 Gbps. For these transceiver-based interfaces, the system designer must be familiar with the industry specifications, transceivers technology, or RF/microwave PCB design. However, the PCB design can be evaluated by a knowledgeable high-speed digital PCB designer.

3.5.1 Layout Considerations

This section describes differential traces and skew matching, which must be taken care while designing the PCB layout.

3.5.1.1 Differential Traces

A well-designed differential trace must not have the following qualities:

- Mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points must be considered while routing the high-speed differential traces to meet the previous qualities.

- The traces should be routed with tight length matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals in Common mode signals.
- The differential pair should be routed such that the skew within differential pairs is less than 5 mils. The length match should be used by matching techniques.

3.5.1.2 Skew Matching

The length of differential lanes should be matched within the TX and RX group. This applies only to specific protocols such as XAUI.

Differential pairs should be routed symmetrically in-to and out of structures, as shown in Figure 16, page 23.

The following figure shows the skew matching.

Figure 15 • **Skew Matching**

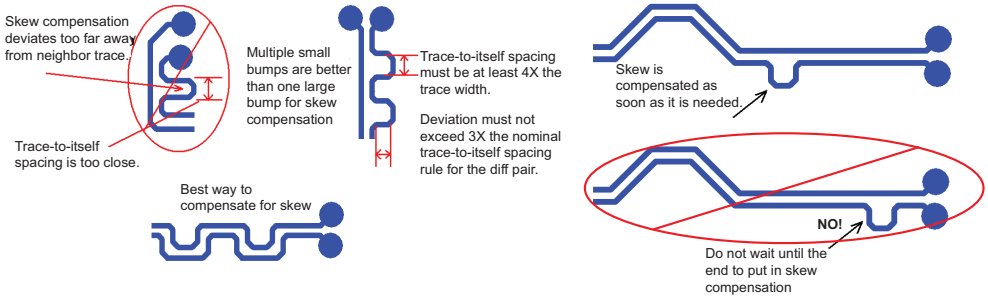


Figure 16 • **Example of Asymmetric and Symmetric Differential Pairs Structure**

Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace must be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To minimize dielectric loss, use low dissipation factor (DF) PCB materials such as Nelco 4000-13. Cost is significantly higher than FR4 PCB material, but FR4 PCB material can provide increased eye-opening performance when longer trace interconnections are required. Ensure that a 100 Ω differential impedance is maintained. This is an important guideline to be followed if the data rate is 5 Gbps or higher.

Far end crosstalk is eliminated by using stripline routing. However, this type of routing in stripline causes more dielectric loss and more variation in impedance. Crosstalk only has an impact only when there is high-density routing. In order to minimize dielectric loss, it is better to route as a microstrip if there is enough space between differential pairs (>4 times the width of the conductor). Simulations are recommended to see the best possible routing.

2116 or 2113 glass-weaving PCB materials should be used to avoid the variations in the impedance. Also, zig-zag routing must be used instead of straight line routing to avoid glass weaving effect on impedance variations, as shown in Figure 17, page 24. Instruct the fabrication vendor to use these PCB materials before manufacturing.

3.5.1.3 Zig-Zag Routing

These traces should be kept away from the aggressive nets or clock traces. For example, on MPF300 devices, the transceiver and DDR traces should not be adjacent to each other.

Separation between coupled differential trace pairs should be 1x. Spacing between channels should be >3x separation. Trace stubs should be avoided. The stub length should not exceed 40 mils for 5 Gbps data rate.

Trace lengths should be kept as small as possible.

It is recommended to use low roughness, that is, smooth copper. As the speed increases insertion loss due to the copper, then roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. The roughness courses this loss proportional to frequency. Microsemi recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

Split reference planes should be avoided. Ground planes must be used for reference for all transceiver lanes.

Figure 17 • **Zig-Zag Routing**

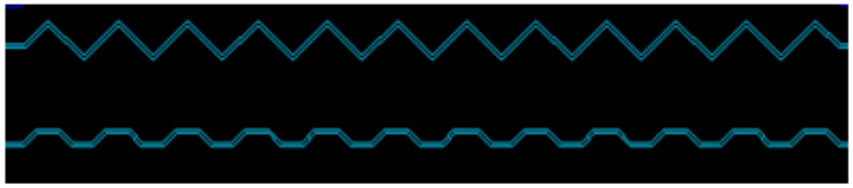
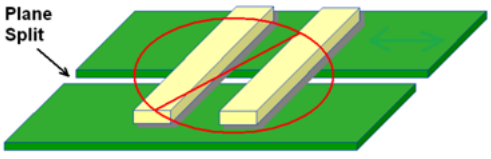


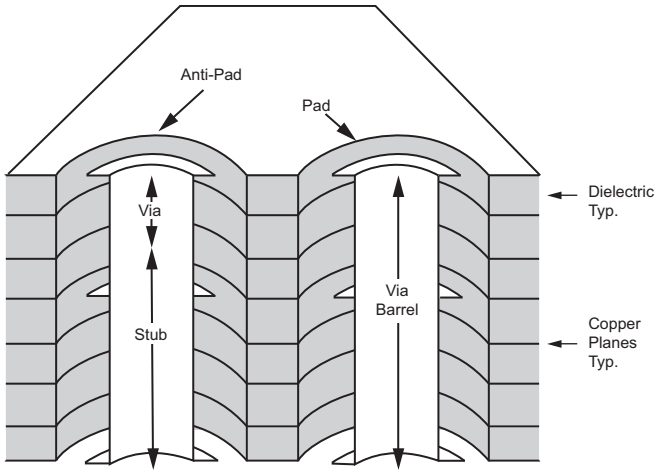
Figure 18 • **Ground Planes for Reference**



3.5.1.4 Via

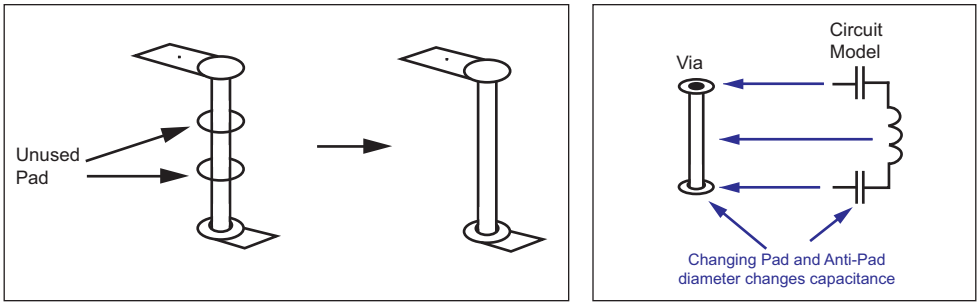
The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver should be used to optimize the via according to the stack-up.

Figure 19 • **Via Illustration**



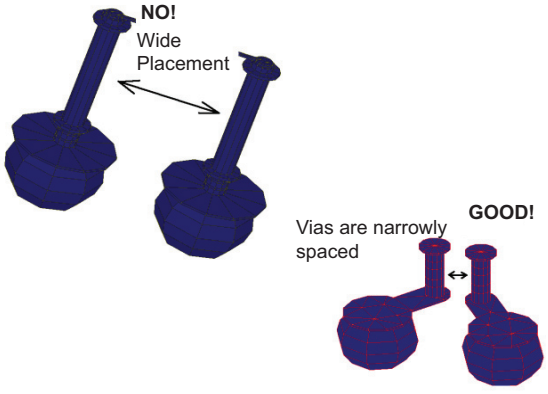
- Many vias on different traces should be avoided, or minimized as much as possible. Transceiver signals should be routed completely on a single layer with the exception of via transitions from the component layer to the routing layer (3-via maximum).
- The length of via stubs should be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried vias. Using blind-vias and back drilling are good methods to eliminate via stubs and reduce reflections.
- The stub length should be kept below 100 mils if the data rate is 2.5 Gbps and 40 mils for 5 Gbps.
- If feasible, non-functional pads should be removed. Non-functional pads on-via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

Figure 20 • **Non-Functional Pads of Via**



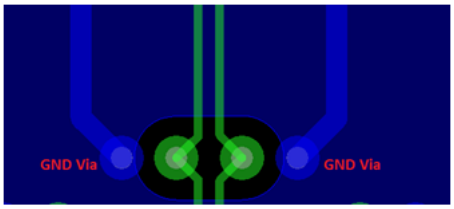
Using tight via-to-via pitches helps reducing the effect of crosstalk, as shown in the following figure.

Figure 21 • **Via-to-Via Pitch**



Symmetrical ground vias (return vias) should be used to reduce discontinuity for Common mode signal components, as shown in the following figure. Common mode of part of the signal requires continuous return path RX to TX and GND. Return vias help maintain the continuity.

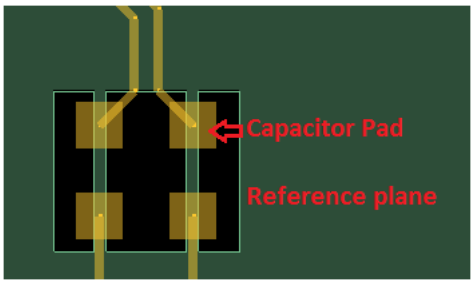
Figure 22 • **GND Via or Return Via**



3.5.2 DC Blocking Capacitors

The plane underneath the pads of DC blocking capacitors should be removed, as shown in the following figure, to match the impedance of the pad to 50 µ. This is required only for the immediate reference plane, not for all planes.

Figure 23 • **Capacitor Pad Reference Plane**



3.5.3 DDR3 and DDR4 Layout Guidelines

3.5.3.1 Placement

It is required to ensure an L-shaped placement of the DDR3 and DDR4 memories, where memories are at the bottom of the L and controllers are at the top of the L. This allows enough space to route DQ signals with fewer layers. This is not mandatory to follow the suggested placement. However, the placement also depends on the board constraints. The trace length of each signal in the placement should not be more than 7 inches.

Figure 24 • **DDR3 Memories**

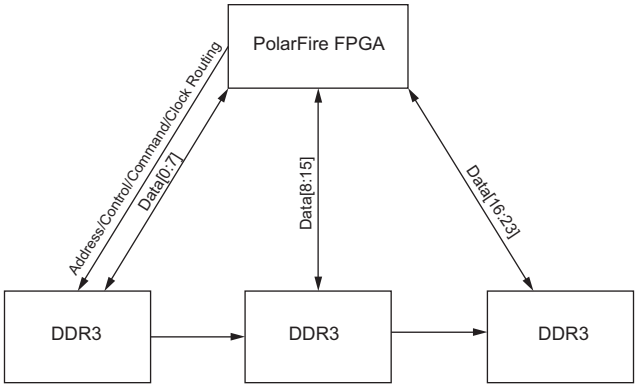
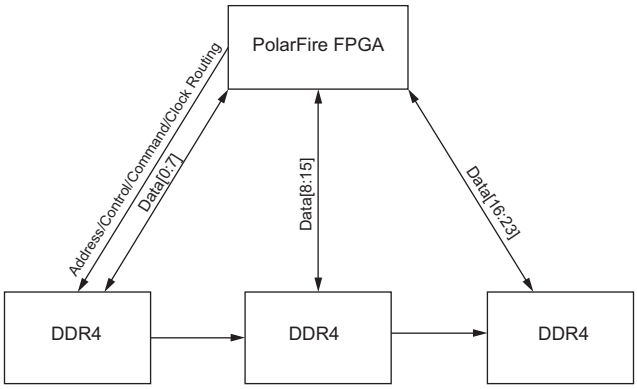


Figure 25 • **DDR4 Memories**



Termination resistors are not required for the DQ and DQS signals because these signals have on-chip ODTs. They are placed at the end of the address, command, control, and clock signals because these signals use fly-by topology. The VTT plane/island is thick enough to handle the current required by termination resistors; typically, a minimum of 150 mil trace is required. The sense pin of the VTT regulator should be connected to the center of the VTT island.

3.5.4 Routing

The reliability of the DDR interface depends on the quality of the layout. There are many layout guidelines available from memory vendors. The following recommendations can also be used for routing DDR3 signals. The following table lists DDR3 signals under each group.

Table 11 • **Grouping of DDR3 Signals**

Group	Signals
Data	DQ[0:7], DQ[8:15], DQ[16:23], DQ[24:31] DQS[0:3], and DM[0:3]
Address/Command	A[0:15], BA[0:2], RAS#, CAS#, and WE#
Control	CS#, CKE, ODT, BG0, BG1, ALERT_N, PARITY, ACT_N, and TEN
Clock	CK and CK#

3.5.4.1 Data Group Signal Routing

The data signals should not be over the split planes.

- The reference plane for data signals should be the GND plane and should be contiguous between memory and PolarFire.
- Traces should not be routed at the edge of the reference plane and over via anti pads.
- When routing the data signals, the longest signals should be routed first—allows length adjustment for the short length signals.
- Serpentine routing should be used to adjust the data group signals to meet this requirement.
- The DQS signal should be routed along with the associated data byte lane on the same critical layer with the same via count. Avoid using more than three vias in the connection between the FPGA controller and memory device.
- The impedance of the data traces depends on the stack-up and trace width. There are options to select the impedance based on the stack-up and trace width.
  - 40 Ω impedance, which requires wide traces (~7 mils to 8 mils). This gives the less crosstalk and less spacing between the traces (~2x). Spacing between non-DDR signals and DDR signals should be ~4x.
  - 50 Ω impedance, which requires smaller trace width (~4 mils to 6 mils). This requires more spacing between the traces (~3x). Spacing between non-DDR signals and DDR signals should be ~4x.

- All data lanes should be matched to within 0.5 inch.
- Within each of the data lanes, each trace should be matched to within ±10 mils of the associated data strobe.
- The DQS and DQS# need to be matched within ± 5 mils.
- The differential impedance should be between 75 Ω to 95 Ω. If the data rate is more than 1600 MT/s, then the impedance should be in the range of 90 Ω to 95 Ω..
- Avoid differential traces adjacent to noisy signals or clock chips.
- Spacing between differential lines should be 5 mils to 8 mils.

3.5.4.2 Address, Control, Command, and Clock Routing

- These signals should be routed using fly-by topology, and terminated by using an appropriate termination resistor at the end of the signals. The resistor termination should not have a stub longer than 600 mil.
- The impedance for the trace depends on the stack-up and trace width. The following are options to select the impedance based on the stack-up and trace width:
  - 40 Ω impedance, which requires wide traces (~7 mils to 8 mils). This gives the less crosstalk and less spacing between the traces (~2x). Spacing between non DDR signals and DDR signals should be ~4x.
  - 50 Ω impedance, which requires smaller trace width (~4 mils to 6 mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4w to avoid crosstalk issues.
  - Address and control signals can be referenced to a power plane if a ground plane is not available. The power plane should be related to the memory interface. However, a ground reference is preferred. Address and control signals should be kept on a different routing layer than DQ, DQS, and DM signals to isolate crosstalk between the signals.

3.5.4.3 Clock

- Clock signals are routed differentially, and the length matches between traces should be ± 5 mils. The clock trace length should be more than strobe length.
- Clock signals should be referenced to a ground plane.
- The space between clock and other signals should be 25 mils.
- One clock signal is routed per rank of the DIMM, that is, one clock for single-ranked DIMM, and two clock signals for the dual ranked DIMM. For non-DIMM systems, the differential terminations used by the CK/CK# pair must be located as close as possible to the memory.
- The max skew between the clock and each DQS should be less than 10 inches.
- If more than one CS is used, the same clock to DQS skew should be applied to all CS.
- Address/control signals and the associated CK and CK# differential FPGA clock should be routed with trace matching of ±100 mil.

3.6 Termination Schemes

Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load receiver. The ringing reduces the dynamic range of the receiver and can cause false triggering. To eliminate reflections, the impedance of the source (ZS) must equal the impedance of the trace (Z0), as well as the impedance of the load (ZL). Stratix devices feature support for on-chip implementation of a termination resistor. The following are the signal-termination schemes used for board design layout:

- Series termination
- Parallel termination
- Thevenin parallel termination
- RC parallel termination

3.7 PCB Capacitor Placement and Mounting Techniques

This section describes the PCB capacitor placement and mounting techniques that must be considered when designing the layout.

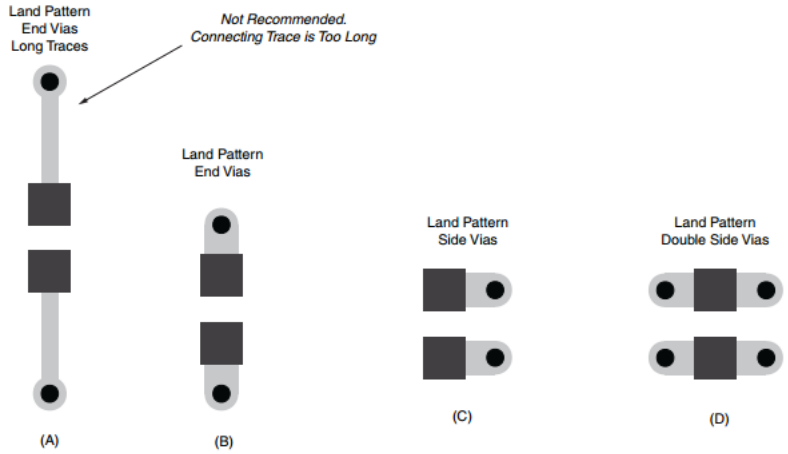
3.7.1 PCB Bulk Capacitors

Bulk capacitors such as D, 1210 are large and sometimes are difficult to place very close to the FPGA. Fortunately, this is not a problem because the low-frequency energy covered by bulk capacitors. Bulk capacitors are not sensitive to capacitor location. They can be placed almost anywhere on the PCB, but the best placement is as close as possible to the FPGA. Capacitor mounting must follow normal PCB layout practices, tending toward short and wide shapes connecting to power planes with multiple vias.

3.7.2 0805 and 0603 Ceramic Capacitors

The 0805 and 0603 capacitors cover the middle frequency range. Placement has some impact on their performance. The capacitors must be placed as close as possible to the FPGA. Any placement within two electrical inches of the device's pinpoint of load is acceptable. The capacitor mounting (solder lands, traces, and vias) must be optimized for low inductance. Vias must be butted directly against the pads. Vias can be located at the ends of the pads, but are more optimally located at the sides of the pads, as shown in the following figure. Via placement at the sides of the pads decreases the mounting's overall parasitic inductance by increasing the mutual inductive coupling of one via to the other. Dual vias can be placed on both sides of the pads for even lower parasitic inductance, but with diminishing returns.

Figure 26 • **Land Pattern—Connecting Traces**



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