MCS3142 Memory Programming Specification

This document includes the programming specifications for the following device:

- MCS3142

1.0 OVERVIEW

The MCS3142 contains 128 bytes of nonvolatile memory. This array is used to store the various encryption parameters and device configuration options. Details of the individual Configuration bits is described in the device data sheet.

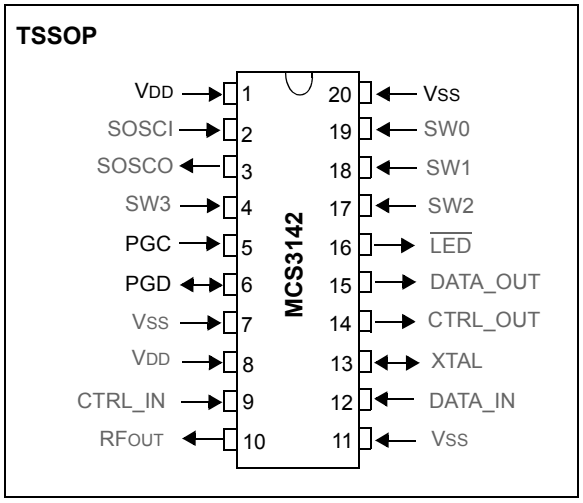
The device is programmed serially using a clock input and bidirectional data signal. A special entry sequence is used to prevent accidental Program mode entry. Further, the device can only be programmed immediately after power-up.

TABLE 1-1: PIN DESCRIPTION DURING PROGRAMMING

Pin Name	During Programming		
	Function	Type	Description
PGC	Programming Clock	I	TTL Input
PGD	Programming Data	I/O	TTL Input/Output
VDD	Power	P	Power
VSS	Ground	P	Ground

2.0 DEVICE PINOUTS

FIGURE 2-1: 20-PIN DIAGRAM FOR MCS3142



3.0 MEMORY MAP

The program memory map for this device begins at 0x00 and extends as shown in Table 3-1. As the device is being programmed, the address counter automatically increments to the next byte location after receiving a data byte.

Data is sent Least Significant Byte (LSB) first.

TABLE 3-1: MEMORY MAP

Address	Size (bytes)	Description
0x00 - 0x07	8	Classic KEELOQ® Encryption Key
0x08 - 0x0F	8	Classic KEELOQ Seed Value
0x10 - 0x13	4	Classic KEELOQ Serial Number
0x14 - 0x15	2	Classic KEELOQ DISC Value
0x16 - 0x17	2	Classic KEELOQ Encoder Configuration
0x18 - 0x19	2	Classic KEELOQ Transmitter Configuration
0x1A	1	Classic KEELOQ Minimum Packet
0x1B - 0x1C	2	Classic KEELOQ Maximum Packet
0x1D	1	Classic KEELOQ TE PR2 Value
0x1E - 0x2D	16	Ultimate KEELOQ Encryption Key
0x2E - 0x3D	16	Ultimate KEELOQ Seed Value
0x3E - 0x41	4	Ultimate KEELOQ Serial Number
0x42 - 0x43	2	Reserved
0x44 - 0x53	16	Ultimate KEELOQ Authorization Key
0x54 - 0x55	2	Ultimate KEELOQ Encoder Configuration
0x56 - 0x57	2	Ultimate KEELOQ Transmitter Configuration
0x58	1	Ultimate KEELOQ Minimum Packet
0x59 - 0x5A	2	Ultimate KEELOQ Maximum Packet
0x5B	1	Ultimate KEELOQ TE PR2 Value
0x5C - 0x5E	3	Encoder Frequency Setting
0x5F - 0x60	2	Encoder Button Configuration
0x61 - 0x62	2	Seed Packet Button Configuration
0x63 - 0x65	3	Ultimate KEELOQ Synchronization Counter, Copy 1
0x66	1	Ultimate KEELOQ Synchronization Counter CRC, Copy 1
0x67 - 0x68	2	Classic KEELOQ Synchronization Counter, Copy 1
0x69	1	Classic KEELOQ Synchronization Counter CRC, Copy 1
0x6A - 0x6B	2	Ultimate KEELOQ Resynchronization Counter, Copy 1
0x6C	1	Ultimate KEELOQ Resynchronization Counter CRC, Copy 1
0x6D - 0x70	4	Ultimate KEELOQ Low-speed Timer, Copy 1
0x71	1	Ultimate KEELOQ Low-speed Timer CRC, Copy 1
0x72 - 0x74	3	Ultimate KEELOQ Synchronization Counter, Copy 2
0x75	1	Reserved
0x76 - 0x77	2	Classic KEELOQ Synchronization Counter, Copy 2
0x78	1	Reserved
0x79 - 0x7A	2	Ultimate KEELOQ Resynchronization Counter, Copy 2
0x7B	1	Reserved
0x7C - 0x7F	4	Ultimate KEELOQ Low-speed Timer, Copy 2

4.0 PROGRAMMING

All configurable options are programmed serially via the PGD and PGC pins of the device. The programming cycle must include all 888 bits of programmable data, which is stored in the device's nonvolatile memory upon completion.

Device programming must begin within a specific window after device power-up. The PGD and PGC pins are configured as inputs upon Reset and, if the programming sequence is started, will remain as inputs until the Verify stage is reached.

The device's memory is only readable during the Verify stage. There is no procedure to read memory except immediately after programming.

4.1 Entering Programming Mode

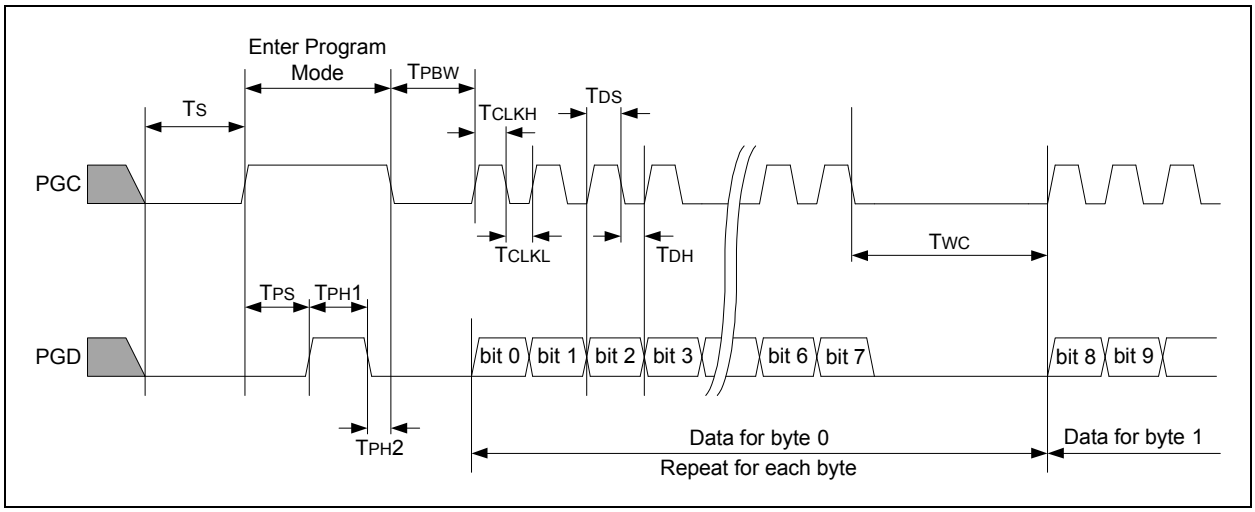
Programming is initiated by forcing the PGD line high after the PGC line has been held high for the appropriate length of time. The programming sequence must happen immediately after device power-up. See Figure 4-1 and Table 5-2 for details. A delay must be provided for the automatic Bulk Erase cycle to complete after entering the Program mode sequence. The device can then be programmed by clocking in 8 bits at a time, using PGC as the clock line and PGD as the data line.

4.2 Serial Program Mode

Write cycles are performed a byte at a time throughout the entire programming sequence. A delay after each 8-bit byte is required for the internal program cycle to complete.

Data bytes are sent Least Significant bit (LSb) first. See Figure 4-1.

FIGURE 4-1: PROGRAMMING WAVEFORM

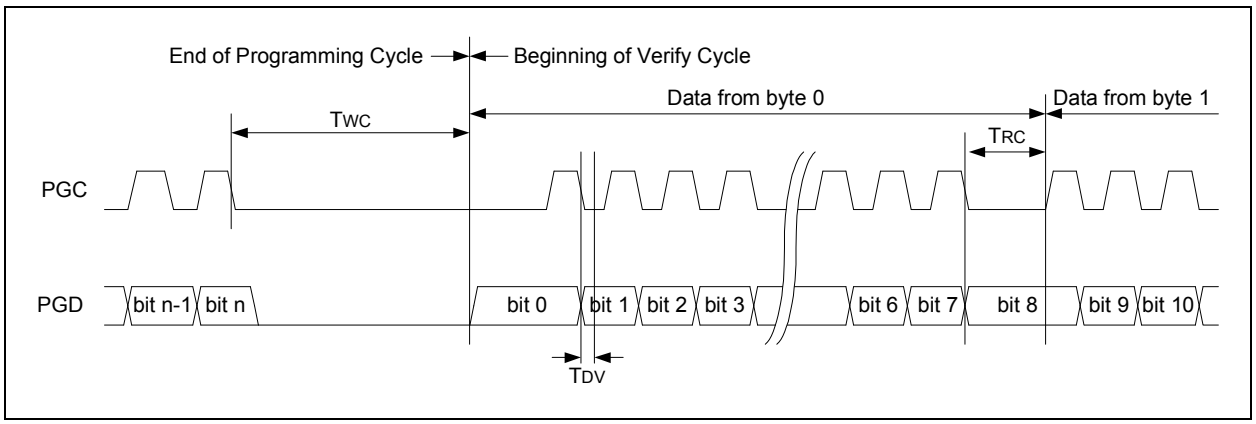


4.3 Serial Verify Mode

A verify operation is available immediately following the programming operation. It must be completed at the end of the programming sequence, before exiting the Programming mode.

The programmer must provide a delay time to allow for write cycle completion. Afterwards, the programmer can provide clock cycles to begin reading data. See Figure 4-2.

FIGURE 4-2: VERIFY WAVEFORMS



5.0 ELECTRICAL SPECIFICATIONS

Refer to the device data sheet for absolute maximum ratings.

TABLE 5-1: DC CHARACTERISTICS

Symbol	Item	Min.	Max.	Units
V_{DD}	—	2.1	3.6	V
V_{IH}	Input High Level	0.25 V_{DD} + 0.8	—	V
V_{IL}	Input Low Level	—	0.15 V_{DD}	V
V_{OH}	Output High Level	V_{DD} - 0.7	—	V
V_{OL}	Output Low Level	—	0.6	V

TABLE 5-2: PROGRAM/VERIFY TIMING REQUIREMENTS

Parameter	Symbol	Min.	Max.	Units
Entry Start-up Delay	T_S	10	—	ms
Program Mode Setup Time	T_{PS}	3.5	11.5	ms
Hold time 1	T_{PH1}	3.5	—	ms
Hold time 2	T_{PH2}	3.5	—	ms
Bulk Write Time	T_{PBW}	11	—	ms
Program Cycle Time	T_{WC}	8	—	ms
Program Read Cycle	T_{RC}	5	—	ms
Clock Low Time	T_{CLKL}	50	—	µs
Clock High Time	T_{CLKH}	50	—	µs
Data Setup Time	T_{DS}	0	—	µs
Data Hold Time	T_{DH}	30	—	µs
Data Out Valid Time	T_{DV}	—	30	µs

APPENDIX A: REVISION HISTORY

Revision A (08/2013)

Initial release.

Revision B (01/2014)

Updated Table 3-1.

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