

High Speed Converter Survival Guide: Digital Data Outputs

by Jonathan Harris, Product Applications Engineer,
Analog Devices, Inc.

IDEA IN BRIEF

With a multitude of analog-to-digital converters (ADCs) available for designers to choose from, an important parameter to consider in the selection process is the type of digital data outputs included. Currently, the three most common types of digital outputs utilized by high speed converters are complementary metal oxide semiconductor (CMOS), low voltage differential signaling (LVDS), and current mode logic (CML). Each of these digital output types used in ADCs has its advantages and disadvantages that designers should consider in their particular application. These factors depend on the sampling rate and resolution of the ADC, the output data rates, the power requirements of the system design, and others. In this article, the electrical specifications of each type of output will be discussed along with what makes each type suited for its particular application. These different types of outputs will be compared in terms of physical implementation, efficiency, and the applications best suited for each type.

CMOS DIGITAL OUTPUT DRIVERS

In ADCs with sample rates of less than 200 MSPS, it is common to find that the digital outputs are CMOS. A typical CMOS driver employed consists of two transistors, one NMOS and one PMOS, connected between the power supply (V_{DD}) and ground, as shown in Figure 1a. This structure results in an inversion in the output, so as an alternative, the back-to-back structure in Figure 1b can be used in order to avoid the inversion in the output. The input of the CMOS output driver is high impedance while the output is low impedance. At the input to the driver, the impedance of the gates of the two CMOS transistors is quite high since the gate is isolated from any conducting material by the gate oxide. The impedances at the input can range from kilo ohms to mega ohms. At the output of the driver, the impedance is governed by the drain current, I_D , which is typically small. In this case, the

impedance is usually less than a few hundred ohms. The voltage levels for CMOS swing from approximately V_{DD} to ground and can, therefore, be quite large depending on the magnitude of V_{DD} .

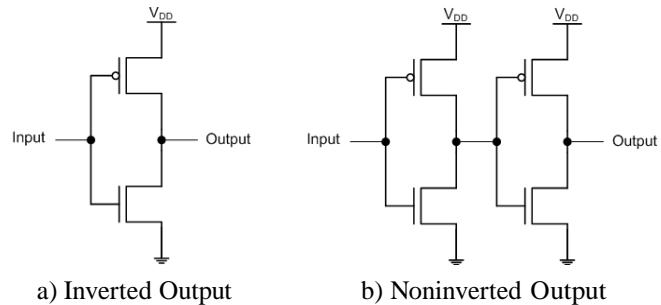


Figure 1. Typical CMOS Digital Output Driver

Since the input impedance is high and the output impedance is relatively low, an advantage that CMOS has is that one output can typically drive multiple CMOS inputs. Another advantage to CMOS is the low static current. The only instance where there is significant current flow is during a switching event on the CMOS driver. When the driver is in either a low state, pulled to ground, or in a high state, pulled to V_{DD} , there is little current flow through the driver. However, when the driver is switching from a low state to a high state or from a high state to a low state, there is a momentary low resistance path from V_{DD} to ground. This transient current is one of the main reasons why other technologies are used for output drivers when converter speeds go beyond 200 MSPS.

Another reason to note is that a CMOS driver is required for each bit of the converter. If a converter has 14 bits, there are 14 CMOS output drivers required to transmit each of those bits. Commonly, more than one converter is placed in a given package, and up to eight converters in a single package are common. When using CMOS technology, this could mean that there would be up to 112 output pins required just for the data outputs. Not only would this be inhibitive from a packaging standpoint, but it would also have high power consumption and increase the complexity of board layout. To combat these issues, an interface using low voltage differential signaling (LVDS) was introduced.

LVDS DIGITAL OUTPUT DRIVERS

LVDS offers some nice advantages over CMOS technology. It operates with a low voltage signal, approximately 350 mV, and is differential rather than single ended. The lower voltage swing has a faster switching time and reduces EMI concerns. By virtue of being differential, there is also the benefit of

common-mode rejection. This means that noise coupled to the signals tends to be common to both signal paths and is mostly cancelled out by the differential receiver. The impedances in LVDS need to be more tightly controlled. In LVDS, the load resistance needs to be approximately $100\ \Omega$ and is usually achieved by a parallel termination resistor at the LVDS receiver. In addition, the LVDS signals need to be routed using controlled impedance transmission lines. The single-ended impedance required is $50\ \Omega$ while the differential impedance is maintained at $100\ \Omega$. Figure 2 shows the typical LVDS output driver.

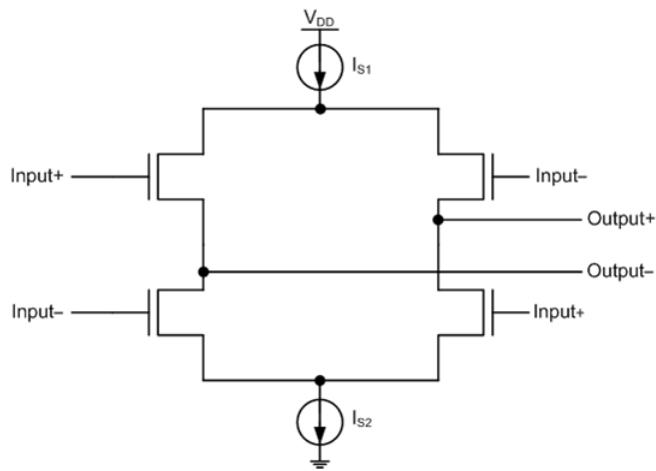


Figure 2. Typical LVDS Output Driver

As can be seen by the topology of the LVDS output driver in Figure 2, the circuit operation results in a fixed dc load current on the output supplies. This avoids current spikes that would be seen in a typical CMOS output driver when the output logic state transitions. The nominal current source/sink in the circuit is set to 3.5 mA which results in a typical output voltage swing of 350 mV with a $100\ \Omega$ termination resistor. The common-mode level of the circuit is typically set to 1.2 V, which is compatible with 3.3 V, 2.5 V, and 1.8 V supply voltages.

There are two standards that have been written to define the LVDS interface. The most commonly used is the ANSI/TIA/EIA-644 specification entitled “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.” The other is the IEEE standard 1596.3 entitled “IEEE Standard for Low Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI).”

LVDS does require that special attention be paid to the physical layout of the routing of the signals but offers many advantages for converters when sampling at speeds of 200 MSPS or greater. The constant current of the LVDS driver allows for many outputs to be driven without the large amount of current draw that CMOS would require. In addition, it is possible to operate LVDS in a double-data rate

(DDR) mode where two data bits can be routed through the same LVDS output driver. This reduces the number of pins required by one half compared to CMOS. In addition, the amount of power consumed for the same number of data outputs is reduced. LVDS does offer numerous benefits over CMOS for the data outputs of converters, but it eventually has its limitations as CMOS does. As converter resolution increases, the number of data outputs required by an LVDS interface becomes more difficult to manage for PCB layouts. In addition, the sample rates of converters eventually push the required data rates of the interface beyond the capabilities of LVDS.

CML OUTPUT DRIVERS

The latest trend in digital output interfaces for converters is to use a serialized interface that uses current mode logic (CML) output drivers. Typically, converters with higher resolutions (≥ 14 bits), higher speeds (≥ 200 MSPS), and the desire for smaller packages with less power utilize these types of drivers. The CML output driver is employed in JESD204 interfaces that are being used on the latest converters.

Utilizing CML drivers with serialized JESD204 interfaces allows data rates on the converter outputs to go up to 12 Gbps (with the current revision of the specification JESD204B). In addition, the number of output pins required is dramatically reduced. Routing a separate clock signal is no longer necessary since the clock becomes embedded in the 8b/10b encoded data stream. The number of data output pins is also reduced with a minimum of two being required. As the resolution, speed, and channel count of the converter increase, the number of data output pins may be scaled to account for the greater amount of throughput required. Since the interface employed with CML drivers is typically serial, however, the increase in the number of pins required is much smaller than that compared with CMOS or LVDS (the data transmitted in CMOS or LVDS is parallel, which requires a much great number of pins).

Since CML drivers are employed in serialized data interfaces, the number of pins required is much smaller. Figure 3 shows a typical CML driver used for converters with JESD204 or similar data outputs. The figure gives a generalization of the typical architecture of a CML driver. It shows the optional source termination resistor and the common-mode voltage. The inputs to the circuit drive the switches to the current sources which drive the appropriate logic value to the two output terminals.

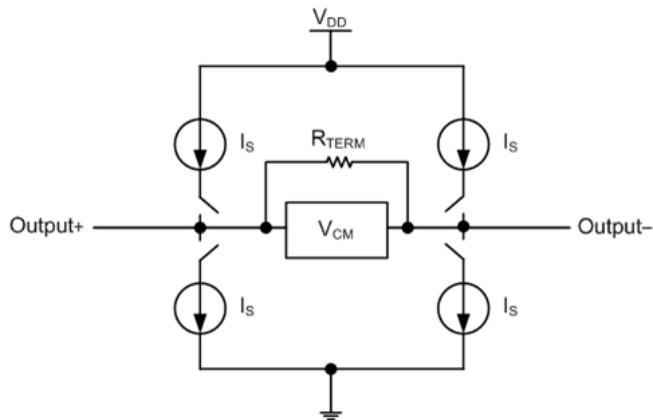


Figure 3. Typical CML Output Driver

A CML driver is similar to the LVDS driver in that it operates in a constant current mode. This also gives the CML driver an advantage in terms of power consumption. Operating in a constant current mode requires fewer output pins, and the total power consumption is reduced. As with LVDS, a load termination is required, as well as controlled impedance transmission lines having a single-ended impedance of $50\ \Omega$ and a differential impedance of $100\ \Omega$. The driver itself may also have terminations, as shown in Figure 3, to help with any signal reflections due to the sensitivity with such high bandwidth signals. In converters employing the JESD204 standard, there are different specifications for the differential and common-mode voltage levels depending upon the speed of operation. Operating at speeds up to 6.375 Gbps, the differential voltage level is nominally 800 mV while the common mode is approximately 1.0 V. When operating above speeds of 6.375 Gbps, but less than 12.5 Gbps, the differential voltage level is specified at 400 mV while the common mode is again approximately 1.0 V. As converter speed and resolution increase, CML outputs look to be the desired driver type to deliver the speeds necessary to keep pace with technology demands placed on converters for their various applications.

DIGITAL TIMING—THINGS TO LOOK OUT FOR

Each of the digital output driver types has timing relationships that need to be monitored closely. Since there are multiple data outputs with CMOS and LVDS, attention must be directed to the routing paths of the signals to minimize skew. If there is too large of a difference, then proper timing at the receiver may not be achieved. In addition, there is a clock signal that needs to be routed and aligned with the data outputs. Careful attention must be given to the routing paths between the clock output, and also the data outputs, to ensure that the skew is not too large.

In the case of CML in the JESD204 interface, attention must also be directed to the routing paths between the digital outputs. There are significantly less data outputs to manage, so this task does become easier but cannot be neglected altogether. In this case, there should be no concern with regards to timing skew between the data outputs and the clock output since the clock is embedded in the data. However, attention must be given to an adequate clock and data recovery (CDR) circuit in the receiver.

In addition to the skew, the setup and hold times must also be given attention with CMOS and LVDS. The data outputs must be driven to their appropriate logic state in sufficient time before the edge transition of the clock and must be maintained in that logic state for a sufficient time after the edge transition of the clock. This can be affected by the skew between the data outputs and the clock outputs, so it is important to maintain good timing relationships. LVDS has the advantage over CMOS due to the lower signal swings and differential signaling. The LVDS output driver does not have to drive such a large signal to many different outputs and does not draw a large amount of current from the power supply when switching logic states, as the CMOS driver would. This makes it less likely for there to be an issue delivering a change in logic state. If there were many CMOS drivers switching simultaneously, the power supply voltage could get pulled down and introduce issues driving the right logic values to the receiver. The LVDS drivers would maintain a constant level of current such that this particular issue would not arise. In addition, the LVDS drivers are inherently more immune to common-mode noise due to its use of differential signaling. The CML drivers have similar benefits to LVDS. These drivers also have a constant level of current, but unlike LVDS, fewer numbers are required due to the serialization of the data. In addition, the CML drivers also offer immunity to common-mode noise since they also use differential signaling.

As converter technology has progressed with increased speeds and resolutions, the digital output drivers have adapted and evolved to meet the requirements necessary to transmit data. CML outputs are becoming more popular as the digital output interfaces in converters transition to serialized data transmission. However, CMOS and LVDS digital outputs are still being utilized today in current designs. There are applications where each type of digital output is best suited and makes the most sense to use. Each type of output comes with challenges and design considerations, and each type of output has its advantages. In converters with sampling speeds less than 200 MSPS, CMOS is still an appropriate technology to employ. When sampling speeds increase above 200 MSPS, LVDS becomes a more viable option in many applications as compared to CMOS. To further increase

efficiency and reduce power and package size, CML drivers can be employed with a serialized data interface such as JESD204.

REFERENCES

Bloomingdale, Cindy and Gary Hendrickson. [AN-586 Application Note. LVDS Data Outputs for High-Speed Analog-to-Digital Converters](#). Analog Devices, Inc., 2002.

JEDEC Standard JESD204 (April 2006). JEDEC Solid State Technology Association. www.jedec.org.

JEDEC Standard JESD204A (April 2008). JEDEC Solid State Technology Association. www.jedec.org.

JEDEC Standard JESD204B (July 2011). JEDEC Solid State Technology Association. www.jedec.org.

ABOUT THE AUTHOR

Jonathan Harris is a product applications engineer in the High Speed Converter Group at Analog Devices (Greensboro, NC). He has over seven years of experience as an applications engineer, supporting products in the RF industry. Jonathan received his MSEE from Auburn University and his BSEE from UNC-Charlotte. He can be reached via email at jonathan.harris@analog.com.

RESOURCES

Share this article on



