LDO FAQ's

Q: How do I calculate if I have exceeded the maximum Tjunction?
A:
Pdiss = IOUT(MAX)*(VIN(MAX) - VOUT) + IGND*(VIN(MAX)) , note the 2nd term is usually negligible

Trise = thetaJA*Pdiss

Tj = Ta + Trise, must be <125°C in general

Q: Why is my LDO not regulating properly?
A: Many reasons possible: current limit has been activated, thermal shutdown has been exceeded, dropout voltage spec not obeyed, ESR of caps rules not obeyed, etc.

Q: What is the efficiency of my LDO?
A: Conversion efficiency is Vout/Vin expressed as a %.

Q: Why on some LDO datasheets does Tjmax state +150°C for some packages, and +125°C for others?
A: These are older datasheets - the +150°C is the max the package/case may see, where +125°C is the maximum Tj.

Q: What is the difference between the "A" and "non-A" versions of LT1963/A, LT1764/A?
A: The "A" version is a newer, pin compatible design that is stable with very low ESR capacitors such as ceramic caps, in addition to tantalum and electrolytic.

Q: What is the difference between thermal limiting and thermal shutdown?
A: With *thermal shutdown*, the part is actually shut off and the die must cool down by the amount of hysteresis built into the thermal shutdown circuitry. Once the part has cooled down, the part is restarted. If the fault or overload exists, the part heats back up to the thermal shutdown temperature and turns back off. Therefore, the part sits and thermally oscillates at some low frequency and duty cycle depending on the thermal shutdown temperature, the amount of hysteresis, the package and the associated thermal time constants. Linear Technology's higher current (i.e. ≥500mA) LDOs generally utilize this type of protection. *Thermal limiting* is a slightly less sophisticated technique than thermal shutdown, in which the maximum die temperature is controlled by the protection circuit limiting the power dissipation on the die. Linear Technology's lower current LDOs generally have this protection.

Q: What is current limit foldback?
A: This is a current limiting technique to limit the peak power dissipation to prevent thermal destabilization or thermal runaway in the power transistor (which usually leads to the part destroying itself), to keep it in its SOA (safe operating area).

Q: What is the typical thermal shutdown/limiting temperature?
A: Typically 150°C-165°C Tjunction, it is not tested in production. Typical variation in thermal shutdown is due to fab lot-to-lot variation and is normally +/-15°C.

Q: How may I obtain the reference voltage out of an adjustable LDO?
A: Hook the ADJ pin directly to Vout; no resistor divider is required.

Q: May I obtain higher current by paralleling regulators?
A: Yes, on most of the family an op amp and some external passive devices are required; on the LT308x family they may be directly paralleled with small PCB trace resistance as ballast.

Q: To what potential should I connect the power tab of a DD Pak or TO-220 or the backside power slug of a DFN or MSOP package, etc. to?
A: For positive LDOs, it is either GND or VOUT. However, for the negative LDOs, it is tied to -VIN. Refer directly to the pin configuration in the datasheet of each part for exact connection.

Q: What is the effect of Vout on output noise?
A: Noise tends to increase with increasing Vout as the error amplifier gains it up.

Q: Do all LDOs have a minimum output load requirement?
A: Not the LT17xx, LT19xx, LT300x, LT302x nor VLDO families.

Q: What will the PSRR of my LDO look like at high frequency (1MHz and up)?
A: This is a function of the output capacitor network. These frequencies are beyond the loop bandwidth of the LDO. The loop is no longer in control of the PSRR. Instead, the LDO forms an impedance divider with the pass element and the output capacitor network and load. Because of this, the major component that controls PSRR at high frequency that can be adjusted is the output capacitor network.

Q: How much input capacitor do I need? Should it be low ESR?
A: If the output capacitor meets LDO requirements and you find that the LDO still oscillates or drops too far during a transient, then increase the size of the input capacitor, and look at the ESR. If it is a higher ESR capacitor, then go to a lower ESR capacitor.

Q: What parameters don't vary with output voltage? What about with input voltage?
A: For a bipolar (“LT” prefix) device, dropout voltage and PSRR are constant with both input and output voltage. Ground current will vary with input voltage on a bipolar device. For a MOS-based (“LTC” prefix) device, ground current is constant with both input and output voltage, other parameters vary with voltage. See the product datasheet under the Electrical Characteristics or Typical Performance Curves sections for further details.

Q: What is the accuracy of my LDO?
A: The accuracy of the LDO is the VREF (ADJ) voltage accuracy. It is typically 1% at certain conditions. If a resistor divider is used for an ADJ device, the total accuracy will be affected by the external resistance tolerance. For example, if the resistors have 1% tolerance each (worst-case), the accuracy of the output is about 3% (2% for external resistors, +1% VREF accuracy). For the single-resistor LT308x LDO family, the total accuracy is 2% (1%+1%) for all output voltages.

Q: Will my LDO ground current vary with load current?
A: For a bipolar (“LT” prefix) product, yes; for a MOS-based (“LTC” prefix) product, typically, no.