Design Guide for Off-line Fixed Frequency DCM Flyback Converter

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I. Introduction

Flyback is the most widely used SMPS topology for low power application from 100W down to under 1W, where the output needs to be isolated from the input. Its best initial attraction is the low system cost, simplicity and ease of implementation. For low current output and power level below 50W, DCM flyback is the popular operating mode. The objective of this paper is to develop a comprehensive, practical and easy to follow approach in designing an off line DCM Flyback power supply. This includes component selection guide, design knowledge and practical tips for a fast and well optimized design.

II. Fixes Frequency Flyback Modes of Operation: DCM vs CCM

Figure 1 shows the basic circuit diagram of a Flyback converter. Its main parts are the transformer, the primary switching MOSFET Q1, secondary rectifier D1, output capacitor C1 and the PWM controller IC. Depending on the manner T1 delivered it stored energy to the secondary, Flyback can operate either in CCM or DCM mode.

In DCM, all the energy stored in the core is delivered to the secondary during the turn off phase (flyback period). While for CCM, the energy stored in the transformer is not completely transferred to the secondary that is, the flyback current (ILPK and ISEC) does not reach zero before the next turn on cycle. Figure 2 shows the difference between DCM and DCM mode in terms of Flyback primary and secondary current waveforms.

Table 1 lists the advantage of Flyback operating in DCM over CCM mode. DCM operation requires a higher peak currents to deliver the required output power compared to CCM operation. This translates to a higher RMS current rating on the primary MOSFET and output capacitor. When these higher peak and RMS current limits the design requirement, (e.g. larger output capacitor required or very high conduction loss on the MOSFET and transformer) a CCM mode operation is the desired choice. This condition usually occur on the design wherein output voltage is low and output current is relatively high (> 6A).

While for DCM the main advantage is the smaller transformer required, fast transient response and zero reverse recovery loss on the rectifier diode since it turns off when the current is zero, it is the best choice for below 50W power or a Flyback with a high output voltage and low output current requirement. While a Flyback converter can be design to operate in both modes, it is important to take note that when the system shifts from DCM to CCM operation, its transfer function is changed (two pole system with low output impedance) thus, additional design rules have to be taken into account including different loop and slope compensation.
Given these advantages of DCM mode, it is the preferred choice for a simple, easy to design, low power Flyback SMPS. The following is a step by step design guide on designing a DCM operation flyback converter.

III. DCM Flyback Design Equations and Sequential Decision Requirements

STEP 1: Define and determine system requirements:

Every SMPS design starts in determining the required system requirement and specification. The following parameters need to be defined and determined:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VACmax</td>
<td>Maximum AC input voltage</td>
</tr>
<tr>
<td>VACmin</td>
<td>Minimum AC input Voltage</td>
</tr>
<tr>
<td>fsaw</td>
<td>Switching Frequency</td>
</tr>
<tr>
<td>Eff</td>
<td>Efficiency</td>
</tr>
<tr>
<td>Pout</td>
<td>Output Power (maximum)</td>
</tr>
<tr>
<td>Vout</td>
<td>Main Output voltage</td>
</tr>
<tr>
<td>fline</td>
<td>AC Line frequency</td>
</tr>
<tr>
<td>∆Vout</td>
<td>Output ripple voltage</td>
</tr>
</tbody>
</table>

Table 2: Input specs and system requirement

Efficiency is required to calculate the maximum input power, if no previous reference is available use 75%-80%. Choosing $f_{sw}$ is usually a tradeoff between the magnetic size and switching loss, commonly used is between 50kHz-100kHz. Finally if there are more than one output voltage involved, $P_{out}$ max should be the sum of each individual output.

STEP 2: Choose the right controller considering the output power requirement:

Choosing a Flyback controller usually depends on specific application and other design consideration such as cost, design form factor and ease of design. Other requirements such as standby power and protection features are easily be met by choosing the right controller. Table 3 shows a selection guide using Infineon’s solution for fixed frequency flyback with regards to its maximum output power. An integrated solution offers low parts count and easier implementation while a separate controller and MOSFET approach has more flexibility specially on thermals.

Table 3: Infineon FF Flyback Controller

Choosing a Flyback controller usually depends on specific application and other design consideration such as cost, design form factor and ease of design. Other requirements such as standby power and protection features are easily be met by choosing the right controller. Table 3 shows a selection guide using Infineon’s solution for fixed frequency flyback with regards to its maximum output power. An integrated solution offers low parts count and easier implementation while a separate controller and MOSFET approach has more flexibility specially on thermals.

STEP 3: Determining Input Capacitor $C_{in}$ and the DC input voltage range:

The capacitor $C_{in}$ is also known as the DC link capacitor, depending on the input voltage and input power the rule of the thumb for choosing $C_{in}$ is shown below.

Table 4: Recommended $C_{in}$ per Watt of Input Power
For wide range operation use a DC link capacitor more than 2uF per watt of input power so as to get a better quality of DC input voltage. With the input capacitor chosen the minimum DC input voltage (DC link capacitor voltage) is obtained by:

\[
V_{DC_{min}} = \sqrt{2 \times V_{ac}^2 - \frac{P_{in_{max}} \times (1 - d_{charge})}{C_{in} \times f_{line}}} \quad (Equation 1)
\]

Where: \(d_{charge}\) is the DC link capacitor duty ratio, typically around 0.2.

Figure 3 shows the DC link capacitor voltage. The minimum DC input voltage occurs at maximum output power and minimum AC input voltage while the maximum DC input voltage occurs at minimum input power (no load) and maximum AC input voltage. The maximum DC input voltage can be found during no load condition when the capacitor peak charge to the peak of the AC input voltage and is given by:

\[
V_{DC_{max}} = V_{AC_{max}} \times \sqrt{2} \quad (Equation 2)
\]

**STEP 4:** Decide on the Flyback reflected voltage (VR) and the maximum VDS MOSFET voltage stress: The reflected voltage VR is the voltage across the primary winding when the switch Q1 is turned off. This also affects the maximum VDS rating of Q1. The maximum drain to source voltage is given by:

\[
V_{DS_{max}} = V_{DC_{max}} + VR + V_{spike} \quad (Equation 3)
\]

Where: \(V_{spike}\) is the voltage spike caused by the leakage inductance of the transformer. For starting point assume \(V_{spike} 30\%\) of \(V_{DS_{max}}\). The table below lists a recommended reflected voltage given a 650V and 800V rated MOSFET. As a starting point limit VR below 100V for a wide range input voltage.

<table>
<thead>
<tr>
<th></th>
<th>VDS max</th>
<th>VR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wide range AC Input: 85Vac-264Vac</td>
<td>650V</td>
<td>60V-100V</td>
</tr>
<tr>
<td>Input from High voltage DC: 400VDC</td>
<td>800V</td>
<td>80V-200V</td>
</tr>
</tbody>
</table>

**Table 5: Recommended VR for 650V and 850V MOSFET**

Choosing the VR is a compromise between the primary MOSFET and the secondary rectifier voltage stress. Setting it too high, by means of higher turns ratio, would mean higher VDSmax but lower voltage stress on the secondary diode. While setting it too low, by lower turn ratio, would lower VDSmax but would increase secondary diode stress.

**STEP 5:** Determine Dmax based on Vreflected and Vinmin: The maximum duty cycle will appear during VDCmin, at this condition we will design the transformer to be at the boundary of DCM and CCM. Duty cycle here is given by:

\[
D_{max} = \frac{VR}{VR + V_{DC_{min}}} \quad (Equation 4)
\]

**STEP 6:** Calculate primary inductance and primary peak current: The primary peak current can be found by using Equation 5 and 6.

\[
P_{in_{max}} = \frac{P_{out_{max}}}{n} \quad (Equation 5)
\]

\[
I_p = \frac{2 \times P_{in_{max}}}{V_{DC_{min}} \times D_{max}} \quad (Equation 6)
\]

The primary inductance should then be designed within the limit of maximum duty cycle:

\[
L_{pri_{max}} = \frac{V_{DC_{min}} \times D_{max}}{I_{pri} \times f_{sw}} \quad (Equation 7)
\]

In order to ensure that the Flyack would not enter into CCM operation at all loading condition make sure to consider the maximum power in calculating Poutmax in Equation 5. Increasing inductance beyond the calculated Lprimax can also push the converter towards CCM mode.
DCM Flyback Transformer Design: Steps 7- Step 12

STEP 7: Choosing the proper core type and size: Choosing the core type and geometry for the first time is quite difficult and usually involve a lot of factors and variables to consider. Among these variables to consider are the core geometry (eg. EE core/RM core/PQ core etc), core size (eg. EE19, RM8 PQ20 etc) and core material (eg.3C96, TP4, 3F3 etc).

If there is no previous reference on choosing the right core size, a good way to start is to refer to the manufacturer’s core selection guide. Below are some commonly used core size for 65kHz DCM Flyback with respect to the output power.

<table>
<thead>
<tr>
<th>Pout Range</th>
<th>Core Area, Ae (mm²)</th>
<th>Core Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-10W</td>
<td>5</td>
<td>EE8.8/4.1/2</td>
</tr>
<tr>
<td></td>
<td>10.1</td>
<td>EE13/6/3</td>
</tr>
<tr>
<td></td>
<td>12.4</td>
<td>EE13/7/4</td>
</tr>
<tr>
<td></td>
<td>20.1</td>
<td>EE16/8/5</td>
</tr>
<tr>
<td>10-15W</td>
<td>22.6</td>
<td>EE19/8/5</td>
</tr>
<tr>
<td>15-30W</td>
<td>32</td>
<td>EE20/10/6</td>
</tr>
<tr>
<td>30-50W</td>
<td>52</td>
<td>EE25/13/7</td>
</tr>
</tbody>
</table>

Table 6: Recommended core size for DCM Flyback (Fsw=65kHz)

After selecting core size, the right bobbin can also be chosen on the corresponding core’s data sheet. Choose the bobbin considering the number of pins, through hole or surface mount and horizontal or vertical orientation. Core materials are chosen considering the frequency of operation and considering core losses. Core material name varies depending on the core manufacturer, a suitable core material to start with are 3F3, 3C96 or TP4A.

STEP 8: Determining minimum primary turns: The minimum number of turns on the primary is a function of the magnetic core area and the allowed operating flux density.

\[ N_p = \frac{L_p \times I_{pRMS}}{B_{max} \times A_e} \]  \hspace{1cm} (Equation 8)

Where Bmax is the operating maximum flux density, Lp is the primary inductance, Ip is the primary peak current and Ae is the cross sectional area of the chosen core type.

It is important that operating Bmax should not exceed the saturating flux density (Bsat) given on the core’s data sheet. Bsat of ferrite core varies depending on the core material and temperature but most of them has a Bsat rating close to 400mT. If there is no further reference data used Bmax = 300mT. Higher Bmax allows for lower number of primary turns for lower conduction loss but with higher core loss. For optimized design the sum of both the core loss and the copper loss should be minimized. This usually happened near the point where core loss is equal to the copper loss.

STEP 9: Determine the number of turns for the secondary main output (Ns) and other auxiliary turns (Naux): To get the secondary turns first determine the turns ratio, n

\[ n = \frac{N_p}{N_s} \]  \hspace{1cm} (Equation 9)

\[ n = \frac{V_R}{V_{out} + V_D} \]  \hspace{1cm} (Equation 10)

Where: Np and Ns are the primary and secondary turns respectively, Vout is the output voltage and VD is the secondary diode voltage drop 0.5V for shottky diode.

For additional number turns such as auxiliary winding for VCC supply the number of turns can be calculated as follows; Where Vaux is the flyback auxiliary winding, VDaux is the diode voltage drop on this winding.

\[ N_{aux} = \frac{V_{aux} + V_{Daux}}{V_{out} + V_D} \]  \hspace{1cm} (Equation 11)

Most flyback controller needs an auxiliary winding to supply the IC. Used the start up VCC supply, as indicated on the data sheet, to decide the auxiliary number of turns. For non integer number of turn round off to the next highest integer.

STEP 10: Determining the wire size for each output windings: In order to determine the required wire size the RMS current for each winding should be determined.

Primary winding RMS current:

\[ I_{pRMS} = I_p \times \sqrt{\frac{B_{max}}{3}} \]  \hspace{1cm} (Equation 11)
Secondary Winding RMS current:

\[ I_{sec RMS} = I_{sec pk} \times \left(1 - \frac{D_{max}}{3}\right) \]  \hspace{1cm} (Equation 13)

\[ I_{sec pk} = I_p \times \frac{N_p}{N_s} \] \hspace{1cm} (Equation 12)

A current density between 150 - 400 circular mil per Ampere can be used as a starting point to calculate the required wire gauge. Below is the quick selection for choosing the appropriate wire gauge. Wire diameter with basic insulation for different magnet wire gauges are also shown:

<table>
<thead>
<tr>
<th>Gauge</th>
<th>Diam (mm) Basic</th>
<th>Diam (mm) Reinforced</th>
<th>RMS Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>34</td>
<td>0.262</td>
<td>0.465</td>
<td>0.2</td>
</tr>
<tr>
<td>32</td>
<td>0.305</td>
<td>0.508</td>
<td>0.3</td>
</tr>
<tr>
<td>30</td>
<td>0.356</td>
<td>0.559</td>
<td>0.5</td>
</tr>
<tr>
<td>29</td>
<td>0.389</td>
<td>0.592</td>
<td>0.65</td>
</tr>
<tr>
<td>26</td>
<td>0.584</td>
<td>0.709</td>
<td>1.3</td>
</tr>
<tr>
<td>24</td>
<td>0.716</td>
<td>0.815</td>
<td>1.9</td>
</tr>
<tr>
<td>22</td>
<td>0.744</td>
<td>0.947</td>
<td>3.1</td>
</tr>
</tbody>
</table>

**STEP 11: Transformer Construction and Winding Design**

Iteration: Once transformer parameters have been decided, determine whether the number of turns and the wire size chosen would fit in the given transformer core size. This step may require several iterations between the chosen core, winding gauge and number of turns.

Figure 4 shows the winding area for an EE ferrite core, using the wire diameter and the number of turns for each winding, we can approximate if the desired winding would fit given its winding area (w and h). If winding would not fit, number of turns, wire gauge or core size need to be adjusted.

The winding scheme has a considerable influence on the performance and reliability of the transformer. To reduce leakage inductance, the use of a sandwich construction, as shown in Figure 5, is recommended. It also needs to meet international safety requirements, a transformer must have adequate insulation between primary and secondary windings. This can be achieved by using a margin-wound construction (Figure 5A) or by using triple insulated wire for the secondary winding (Figure 5B).

Using triple insulated wire (reinforced insulation) on the secondary is easier and more preferable way of meeting this safety requirement. Take note that in fitting triple insulated wire on the chosen core/bobbin, the outside diameter is thicker than the same gauge normal magnet wire.

**STEP 12: Design the primary clamp circuit:** During turn off, a high voltage spike due to the transformer’s leakage inductance appears on MOSFET. This excessive voltage spike on the MOSFET may lead to an avalanche breakdown and eventually failure of the MOSFET. A clamping circuit placed across the primary winding helps to limit the voltage spike caused by this leakage inductance to a safe value.

There are two types of clamping circuit that can be used as shown in Figure 4. The easiest way is to use a Zener clamp circuit which consists of a (TVS) diode. Zener diode effectively clips the voltage spike across the diode. The advantage of using this circuit is that it will only dissipate energy when it’s breakdown voltage. At low line and lighter loads where the spike is relatively low, Zener may not clamp at all therefore there is no power dissipated on the clamp.

Choose the zener/TVS diode rating to be twice the reflected voltage VR. The diode should be ultra fast type with voltage rating greater than the maximum DC link voltage.

The RCD type not only clamps the voltage level but somehow slow down MOSFET dv/dt. We can use the RCD clamp if passing EMI compliance is a major consideration. The resistor element is crucial in limiting the maximum voltage spike.
lower Rclamp will help lower Vspike but increases the power dissipation on the other hand higher Rclamp value lower the power dissipation but allows higher Vspike.

Setting VR= Vspike Rclamp can be determined by;  
\[ R_{clamp} = 4 \times \frac{VR^2}{L_{leak} \times I_p^2 \times f_{sw}} \]

Where Lleak is the leakage inductance of the transformer which can be determined through measurement however if this is not known assume Lleak around 2-4% of the primary inductance.

The capacitor Cclamp needs to be large enough to keep a relatively constant voltage while absorbing the leakage energy. Cclamp value may range 100pF- 4.7nF.

**STEP 13: Output Rectifier Diode Selection:**

\[ V_{R \_ diode} = V_{out} + V_{DC \_ max} \times \frac{N_s}{N_p} \]  \(\text{(Equation 14)}\)

\[ I_{sec \_ RMS} = I_{sec \_ pk} \times \sqrt{\frac{1 - D_{max}}{3}} \]  \(\text{(Equation 15)}\)

Chose the output diode such that its VRRM (maximum reverse voltage) is at least 30% higher than VRVdiode and IF (ave forward current) is at least 50% higher than the IsecRMS. Use shottky diode on the main secondary output for lower conduction losses.

**STEP 14: Output Capacitor Selection:** For Flyback converter the proper choice of output capacitor is extremely important. This is because the flyback mode converters have no inductive impedance between the rectifier and output capacitor. The output capacitor need to be selected to meet these 3 important parameters; capacitance, ESR (equivalent series resistance) and RMS current rating.

Determining the minimum output capacitance is a function peak to peak output ripple voltage:

\[ C_{out\_ min} = \frac{I_{out \_ max} \times N_c}{f_{sw} \times V_{out\_ ripple}} \]  \(\text{(Equation 16)}\)

Where: Ncp is the number of internal clock cycle needed by the control loop in reducing the duty cycle from maximum to minimum value. This is usually take around 10-20 switching period. Iout is the maximum output current (\(I_{out} = P_{out \_ max}/V_{out}\)).

The minimum capacitor RMS current rating of the chosen capacitor is:

\[ I_{cap \_ RMS} = \sqrt{I_{sec \_ RMS}^2 - I_{out}^2} \]  \(\text{(Equation 17)}\)

Given the high switching frequency, the high secondary peak current for a Flyback will produce a corresponding ripple voltage across the output capacitor’s equivalent series resistance (ESR). The capacitor is also chosen not to exceed ESRmax.

\[ ESR_{max} < \frac{\Delta V_{out}}{I_{sec \_ pk}} \]  \(\text{(Equation 18)}\)

Make sure to used the ESR on the data sheet at a frequency greater than 1kHz.

Note: Using a single capacitor with lower ESR value could meet the desired output ripple voltage. A small LC filter is also advisable for higher peak currents specially when operating in DCM mode.

**STEP 15: Other Design Considerations**

A. Input Diode Bridge Voltage and Current Rating:

\[ I_{ac \_ RMS} = \frac{P_{in \_ max}}{PF \times V_{ac \_ min}}; \quad V_{RR} > V_{AC \_ max} \times 1.414 \]  \(\text{(Equation 19)}\)

Where PF is the power factor of the power supply, use 0.5 if there is no better reference data available. Select the bridge rectifier rating such that the forward current twice than that of IACRMS. A 600V part is commonly use for maximum input voltage of ~400V.

B. Current Sense Resistor, Rsense: The sense resistor Rsense is used to defined the maximum output power. Vcsth can be found on the controller’s data sheet while Ipmax is the primary peak current while also considering the short term peaks in output power.

\[ Rsense = \frac{V_{csth}}{I_p(max)} \]  \(\text{(Equation 20)}\)
C. **VCC Capacitor:** A right capacitance value is important for proper startup, a value of 22uF - 47uF is usually enough for most application. To low capacitance may trigger the under voltage lockout of the IC before the VCC voltage develops while a larger value will slow down the startup time. In parallel with the VCC capacitor it is always recommended to use a 100nF ceramic capacitor placed very near to VCC pin and IC ground.

D. **Feedback Loop Compensation:** A feedback loop compensation is needed to prevent oscillation. For DCM flyback loop compensation is relatively less complicated compare to CCM. A simple RC (Rcomp, Ccomp) as shown in Figure 6 is usually sufficient to make a stable loop. Typical Rcomp values can range from 1k - 20k while Ccomp would usually range from 100nF - 470nF. A detailed analysis about feedback loop can be found on reference [2].

IV. **DCM Flyback Design Example**

**STEP 1:** System Specifications and Requirements:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>VAC(\text{max})</td>
<td>265V</td>
</tr>
<tr>
<td>VAC(\text{min})</td>
<td>85V</td>
</tr>
<tr>
<td>fs(\text{w})</td>
<td>65kHz</td>
</tr>
<tr>
<td>Eff</td>
<td>80%</td>
</tr>
<tr>
<td>Pout</td>
<td>25Wmax</td>
</tr>
<tr>
<td>Vout</td>
<td>12V ± 2%</td>
</tr>
<tr>
<td>line</td>
<td>60Hz</td>
</tr>
<tr>
<td>Vout ripple</td>
<td>120mV</td>
</tr>
<tr>
<td>No load Pin</td>
<td>&lt;50mW</td>
</tr>
</tbody>
</table>

**STEP 2:** Choosing the right controller considering the Pout: Referring to Table 3, we chooses an integrated controller and MOSFET solution using ICE3BR1065J. Other features include built in startup cell, less than 50mW no load power and frequency jitter and soft driving for lower EMI. Below is the typical Flyback application using ICE3BR1765J

**STEP 3:** Determining Input Capacitor C\(\text{in}\) and the DC input voltage range:

Maximu input power:

\[ P_{\text{in max}} = \frac{P_{\text{out}}}{0.8} = 31W \]

Using 2uF per watt of input power, the required DC capacitor, C\(\text{in}\), is:

\[ C_{\text{in}} = \frac{2uF}{W} \times 31W = 62uF \sim 68uF \]

> Use the standart capacitance value of 68uF/400V

With the input capacitor chosen the minimum DC input voltage (DC link capacitor voltage) is obtained by:

\[ V_{\text{DC min}} = \sqrt{2 \times 85V^2 - \frac{31W \times (1-0.2)}{68uF \times 60Hz}} = 92V \]

\[ V_{\text{DC max}} = 265V\sqrt{2} = 375V \]

**STEP 4:** Flyback reflected voltage (VR) and the Max VDS MOSFET voltage stress: For a 650V MOSFET on ICE3BR0665 CoolSET, VR is chosen at 75V Assuming 30% leakage spike the expected maximum VDS is equal to:

\[ V_{\text{DS max}} = V_{\text{DC max}} + VR + 30\% V_{\text{spike}} \]
DCM Flyback

VDSmax = 375V + 75V + 30% × 375V = 563V

**STEP 5:** Determining Dmax based on Vreflected and Vinmin:

\[ D_{\text{max}} = \frac{V_R}{V_R + V_{DC\text{min}}} = \frac{75V}{75V + 92V} = 44\% \]

**STEP 6:** Calculating primary inductance and primary peak current:

\[ P_{\text{in max}} = 31W ; \quad I_p = \frac{2 \times 31W}{92V \times 0.44} = 1.53A ; \quad L_{pri_{\text{max}}} = \frac{92V \times 0.44}{1.53A \times 65kHz} = 407uH \]

**STEP 7:** Choosing the proper core type and size: Using the table outline on Step 7, we can use EE20/10/6 ferrite core for this 25W power level

- Core: EE20/10/6 Ferroxcube/TDK
- Cross Sectionl Area, Ae=32mm2
- Core Material: 3C96/Ferroxcube, TP4A/TDK
- Bobbin:E20/10/6 coil former, 8 pins

**STEP 8:** Determining minimum primary turns:

\[ N_p = \frac{407uH \times 1.53A}{300mT \times 32mm^2} = 65\text{Turns} \]

**STEP 9:** Determine the number of turns for the secondary main output (Ns) and other auxiliary turns (Naux):

\[ n = \frac{V_R}{V_{out} + V_D} = \frac{75V}{12V + 0.5V} = 6 \]

\[ N_s = \frac{N_p}{n} = \frac{65}{6} = 10.83\sim{11}\text{TURNS}; \quad N_p = 66\text{TURNS} \]

Note: Round off non integer secondary value to the next integer value, in this case Ns =11. Using this setup (Np/Ns=65/11) VR is decreased a bit, we can use this value or increase the primary turns to get the same VR as assumed. In this case we will adjust Np to 66 turns to maintain the same VR. Even turns is also desirable on the primary for low leakage split primary winding construction.

An auxiliary winding, Naux, on the primary is needed for the VCC supply. For ICE3BR4765 a HV startup is used to supply the initial bias before Vaux kicks in. We set Vaux at 15V to be above 11.2V max turnoff voltage.

\[ N_{aux} = \frac{V_{aux} + V_{Daux}}{V_{out} + V_D} = \frac{15V + 0.5V}{12V + 0.5V} = 14\text{TURNS} \]

**STEP 10:** Determining the wire size for each output windings: The RMS current on each winding is calculated using Equation 11-13:

\[ I_{pri_{\text{RMS}}} = I_p \times \sqrt{\frac{D_{\text{max}}}{3}} = 1.53A \times \sqrt{\frac{0.44}{3}} = 0.58A ; \quad I_{sec_{pk}} = I_p \times \frac{N_s}{N_p} = 1.53A \times \frac{66}{11} = 9A \]

\[ I_{sec_{RMS}} = I_{sec_{pk}} \times \sqrt{\frac{1 - D_{\text{max}}}{3}} = 9 \times \sqrt{\frac{1 - 0.44}{3}} = 3.9A \]

From Table 6 we can use: AWG 29-Primary, AWG22-Secondary, AWG 34-Auxiliary winding

*Note: The load on the auxiliary winding is usually just the IC bias and MOSFET gate drive (~0.1A)

**STEP 11:** Transformer Construction and Winding Design Iteration

Using table AWG 29 diameter is 0.389mm, EE 20/10/6 winding area width and height is 14mm and 4mm respectively. This will give us a TPL (turns per layer) on the primary of 35Turns (14/0.389). For our required 66 turn we will need 2 layer on the primary winding.

For the secondary turns we will use triple insulated wire AWG 22, outside diameter is 0.947. TPL fusing this wire is 14 turns (14/0.947) which means a single layer 11...
turns which should fit in. For the auxiliary basic AWG 34 magnet wire will be used (d=0.262mm).
Checking the winding stacked (0.389mm+0.389mm+0.947mm+0.262 ) is 2mm which is less than the winding height. This should give us enough margin for the actual built. We can then use a split primary transformer construction as shown in Figure 11

**STEP 12:** Design the primary clamp circuit: For the primary clamp we will use a Diode-Zener clamp TVS Diode is P6KE160 and fast recovery diode is BYB27C. An RCD clamp value can also be used as suggested on reference design on [2]

**STEP 13:** Output Rectifier Diode Selection: Voltage and current rating for the schottky rectifier diodes are;

\[
VRV_{diode} = V_{out} + V_{DC_{max}} \times \frac{N_x}{N_p} = 12V + 375V \times \frac{11}{66} = 74.5V
\]

Choose 100V rated diode

\[
I_{sec_{RMS}} = 3.9A
\]

Choose IF>5.9A

**STEP 14:** Output Capacitor Selection

\[
C_{out_{min}} = \frac{I_{out_{max}} \times N_{cp}}{f_{sw} \times V_{out_{ripple}}} = \frac{2.1 \times 20}{65kHz \times 0.12V} = 270\mu F
\]

Capacitance must be at least higher than this value

For Flyback output capacitance most of the time the limiting factor is the ripple current rating and ESR.

\[
I_{cap_{RMS}} = \sqrt{I_{sec_{RMS}}^2 - I_{out}^2} = \sqrt{3.9^2 - 2.08^2} = 3.3A
\]

Combined RMS current of output cap used should be higher than this value

\[
ESR_{max} < \frac{\Delta V_{out}}{I_{sec_{pk}}} = \frac{120mV}{9A} = 13mohm
\]

Chose ESR lower than this value

**STEP 15:** Other Considerations

A. Input Diode Bridge Voltage and Current Rating

\[
I_{ac_{RMS}} = \frac{P_{in_{max}}}{PF \times V_{ac_{min}}} = \frac{31W}{0.5 \times 85V} = 0.73A
\]

Chose forward current rating >1.4A

\[VRV > 375V\]

Commonly used is 600V rated bridge rectifier

B. Current Sense Resistor, Rsense

\[
Rsense = \frac{V_{cest}}{I_{p(max)}} = \frac{1V}{1.53A} = 0.65\Omega
\]

Use 1.3 ohm 0.25W x 2 in parallel

C. VCC Capacitor:

\[
V_{cc\ capacitor} = 22\mu F/35V
\]

D. Feedback Loop Compensation: Below shows the complete Flyack schematic including values and implementation of the feedback circuit.
V. References

[1] Switching Power Supply Design by Abraham Pressman

[2] 25W 12V SMPS Evaluation Board with CoolSET ICE3BR1065J
http://www.infineon.com/dgdl/AN_SMPS_ICE2xXXX_V12.pdf?folderId=db3a304412b407950112b418ce5926b2&fileId=db3a304412b407950112b418ce5926b3


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