



AZD098 How to determine a fixed OTP configuration for your standalone device

1 Introduction

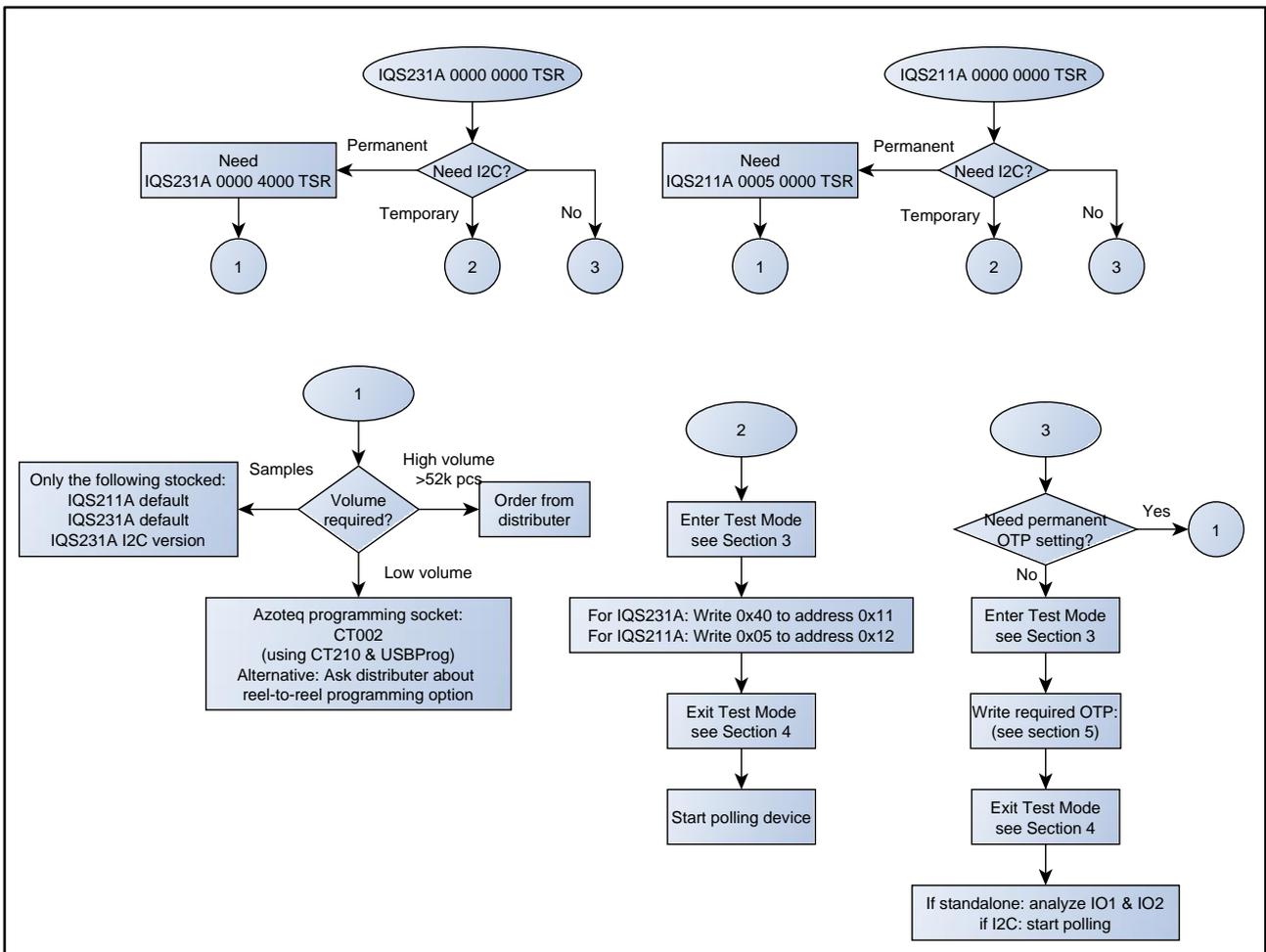
There are a few methods which can be used to determine the settings of your Azoteq device. This guide includes specific details for the following devices:

- IQS231A
- IQS211A

The guide focuses on the following use cases:

- How to get any “standalone” device into I2C mode
- How to test various OTP settings before pre-production (where OTP settings are fixed for standalone operation)

The following chart shows a summary of the contents of this document:



2 Test mode timing

The ICs have a period after power-up where OTP options can be fixed for a power-on cycle (non-permanent)

This time period is known as “Test mode”. During this period, the I2C communication on the IC is enabled and the IC waits for possible polling requests (according to the I2C address stated in the table below).

Once the “Test mode” period has expired, the IC will be configured with the OTP settings which are

- Permanently programmed at production (or programmed in socket or on module)
- Written during “Test mode” (these override permanent settings)

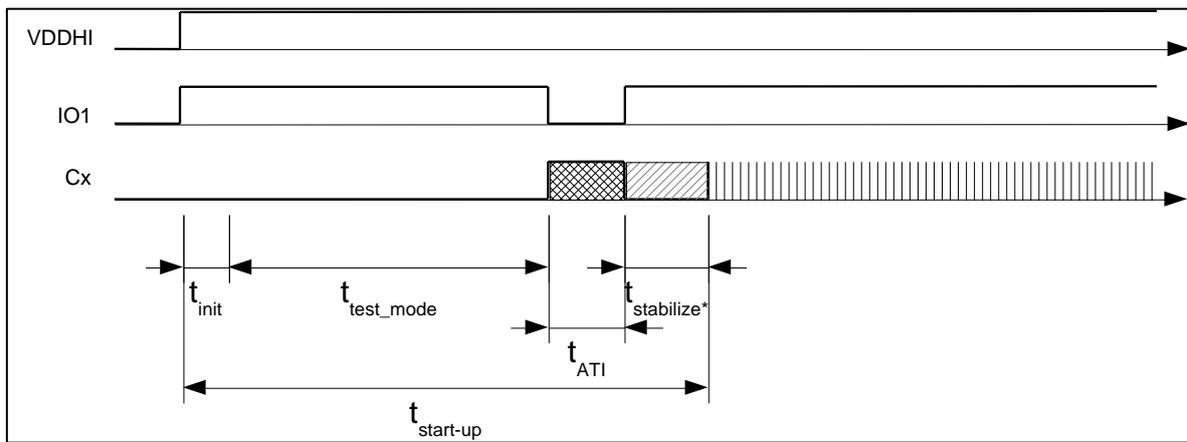


Figure 2.1 Start-up timings for IQS231A and IQS211A

	IQS231A	IQS211A	Unit
t_{init}	2	2	ms
t_{test_mode}	340	15	ms
$t_{start-up}$	n/a (see datasheet)	n/a	ms
$t_{stabilize}$	n/a (see datasheet)	n/a	ms
t_{ATI}	n/a (typical 40ms)	n/a (typical 40ms)	ms
I ² C address	0x45 (test mode only)	0x47 (all modes)	n/a

3 Entering Test mode

By polling the device within t_{test_mode} AND receiving an “ACK” (acknowledge), test mode will be entered.

Confirm this by the following:

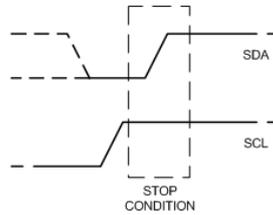
- Write 0x0F (register address to confirm test mode)
- Read data
- If data = 0xA5, then test mode = True

If only a NACK is received, repeat the polling by address until receiving an “ACK”

If no “ACK” is achieved, review the t_{test_mode} time to ensure polling is done within the correct window.

4 Exit Test mode

If Test mode has been entered, an I²C stop sequence will cause test mode to exit



5 Changing OTP settings (temporary)

Please check the latest datasheet versions for accurate and updated OTP configuration options.

Note the OTP structures of the ICs are as follows:

5.1 IQS211A OTP bank summary

OTP Bank	Bit 7	6	5	4	3	2	1	Bit 0
Bank 0	User OTP options (A)							
Bank 1	User OTP options (B)							
Bank 2	User OTP options (C)							
Bank 3	*System use				User OTP options (D)			
Bank 4	*System use				User OTP options (E)			
Bank 5	*System use							

Order code translation for IQS211A:

IQS211A	z	z	zz	zz	zz	TS R
	E	D	C	B	A	

5.2 IQS231A OTP bank summary

OTP Bank	Bit 7	6	5	4	3	2	1	Bit 0
Bank 0	User OTP options (A)							
Bank 1	User OTP options (B)							
Bank 2	User OTP options (C)							



Bank 3	User OTP options (D)
Bank 4	System use
Bank 5	System use

Order code translation for IQS231A:

IQS231A	zz	zz	zz	zz	TS R DN R CS R
	D	C	B	A	

5.3 Changing OTP settings at power-on

After confirming “Test mode” via register 0x0F as shown in section 3 above, be careful not to send an I²C stop that will cause test mode to exit.

If there is always an I²C stop after a write command in the MCU I²C library, be sure to:

1. Enable an MCU I²C “restart” setup OR
2. Do not confirm “test mode” entry, only write the required OTP settings as indicated below

In test mode, write to the following registers to define the temporary OTP settings:

OTP test mode RAM address	Description
0x10	OTP bank 0
0x11	OTP bank 1
0x12	OTP bank 2
0x13	OTP bank 3
0x14	OTP bank 4

These OTP settings will be lost after a power cycle. For permanently changing settings, see section 6.

6 Change OTP settings (permanent)

Azoteq offers permanent OTP options as follows:

- General stock (default, I2C configured parts and some customer specific parts)
- Customer specific order (MOQ 52k pcs)
- Reel-to-reel programming (MOQ 3k, but higher volume samples are possible)
- CT002 programming socket for programming by hand for engineering and pre-production



Appendix A. Contact information

	USA	Asia	South Africa
Physical Address	6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA	Rm1227, Glittery City Shennan Rd Futian District Shenzhen, 518033 China	109 Main Street Paarl 7646 South Africa
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The following patents relate to the device or usage of the device: US 6,249,089; US 6,952,084; US 6,984,900; US 7,084,526; US 7,084,531; US 8,395,395; US 8,531,120; US 8,659,306; US 8,823,273; US 9,209,803; US 9,360,510; US 9,496,793; US 9,709,614; EP 2,351,220; EP 2,559,164; EP 2,748,927; EP 2,846,465; HK 1,157,080; SA 2001/2151; SA 2006/05363; SA 2014/01541; SA 2015/023634; SA 2017/02224;

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