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Design with MOSFET Load Switch

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INTRODUCTION

In portable equipment markets such as notebook computers, cellular phones, and personal organizers, the demand for more features is colliding head long into the important mean time between charge specification. Manufacturers are being challenged to continue offering longer battery life, while adding more current draining applications. Their solution to this problem is simple: turn off applications when they are not being used.

The mechanism used to turn off the application is referred to as a *load switch*, since the current drawn by each application is considered a *load* on the battery. This application note will detail how to design with Fairchild Semiconductor's new line of MOSFET load switches.

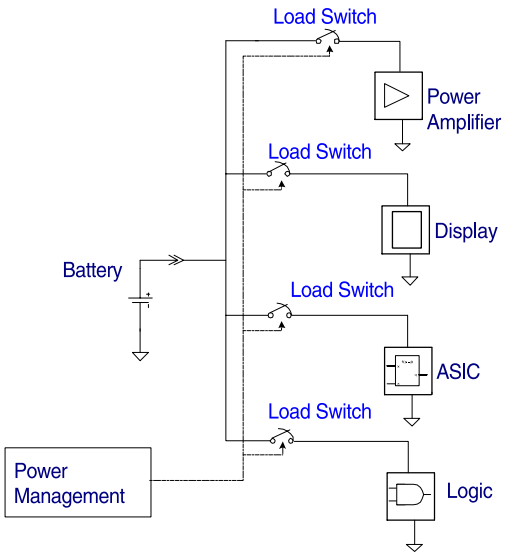

Figure 1. Typical Hand-Held Power Architecture

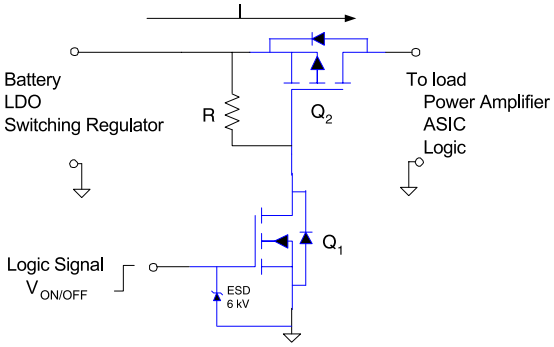

Figure 2. Load Switch Schematic

Theory of Operation

A generic power architecture of a mobile phone is shown in Figure 1. Load switches are placed in series with the Battery and the load, and are switched on or off by the power monitoring logic. A schematic of a Load Switch is shown in Figure 2. A P-Channel MOSFET is the power switch with its gate controlled by a Fairchild N-Channel Digital MOSFET. Logic "High" turns on the PMOS by having its gate pulled to ground by the Digital MOSFET. Logic "Low" turns off the PMOS by turning off the Digital MOSFET, and allowing the PMOS Gate to be passively pulled up to the Source potential through the external resistor.

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Intrinsic Diode

It is important that the output voltage be lower than the input voltage. An output voltage higher than the input will be clamped via the intrinsic diode of the P-Channel MOSFET, which could cause significant current to flow. This is not an issue with single energy sources, but it can become a problem with multiple sources, such as a charger.

Thermal Requirements

Load Switches are sized by their power handling capability, or more precisely - the amount of power they can dissipate in a given environment. Generic current handling graphs are valuable for First Order approximations, but one should evaluate devices to the exact environment in which it will operate.

Design Example

Assume the operating environment will be:

1) T_A = 70°C (Maximum Board Temperature)

The edge of the board will be considered fixed at 70°C. Ambient temperature is a fixed temperature that is closest to where the component is to be placed. In this application, the Ambient is the fixed edge of an FR4 board mounted in a case.

2) $R_{\theta CA}$ = 25°C/Watt (Thermal Resistance Case-to-Ambient)

The thermal resistance from the case of the component to ambient temperature can be measured or calculated. The thermal path is considered a straight conductive path of copper trace on FR4 to Ambient. Thermal resistance is calculated from the equation:

R_θ=(Distance to Ambient)/[(Cross Sectional Area)*(Thermal Conductivity of Material)]

The thermal path can be measured, but it requires a device mounted in the component's position dissipating 1 Watt. The temperature difference is the thermal resistance. It is important that there is no thermal radiation during this test. This type of measurement is usually made once the component is selected, and is done as a check of the previous calculations.

3) I_L = 1.25A (Worse Case Steady-State Current)

At this point, the operating environment has been defined. Some general calculations can now be done, and a component selected.

4) T_{JMAX} = 150°C (Load Switch Absolute Maximum Junction Temperature)

This maximum temperature limit must never be exceeded by the junction temperature of the load switch.

5) $T_{RISE} = T_{JMAX} - T_A$ = 80°C. (Maximum Allowable T_{RISE})

The junction-to-case thermal resistance, $R_{\theta JC}$, for the SSOT-6 and SSOT-8 is as follows:

6) SSOT-6, $R_{\theta JC}$=60°C/Watt

7) SSOT-8, $R_{\theta JC}$=40°C/Watt

The maximum power dissipation of these packages in this specific environment:

8) SSOT-6: $P_D=T_{RISE}/(R_{\theta JC}+R_{\theta CA})$=940mWatt (Maximum Power Dissipation Allowable)

9) SSOT-8: P_D=80/(25+40)=1.23Watt (Maximum Power Dissipation Allowable)

10) The FDC6329L SSOT-6 will be used for evaluation.

The 25°C $R_{DS(ON)}$ value can be calculated from the V_{DROP} ratings in the data sheet.

V_{IN}	Logic ($V_{ON/OFF}$)	V_{DROP}	I_L	$R_{DS(ON)}$(25°C)
5	1.5-8V	0.08V	1A	80mΩ
2.5	1.5-8V	0.11V	1A	110mΩ

The $R_{DS(ON)}$ increases by 50% for a junction temperature of 150°C. The worse case power dissipation is calculated using the worse case $R_{DS(ON)}$ at 150°C.

V_{IN}	Logic ($V_{ON/OFF}$)	I_L	$R_{DS(ON)}$ (150°C)	P_D ($I^2R_{DS(ON)}$)
5	1.5-8V	1.25A	120mΩ	188mWatt
2.5	1.5-8V	1.25A	165mΩ	258mWatt

Recall that the maximum SSOT-6 power dissipation for this application is 940mWatt (step 8), so this device will work. It is important to know the design margin, since there are always assumptions being made in a thermal design.

V_{IN}	Logic ($V_{ON/OFF}$)	I_L	P_D ($I^2R_{DS(ON)}$)	T_J P_D*($R_{\theta JC}$+$R_{\theta CA}$)+T_A
5	1.5-8V	1.25A	188mWatt	86°C
2.5	1.5-8V	1.25A	258mWatt	92°C

Inrush Current

Load switches turning on into capacitors with low ESR can create high inrush currents that can be detrimental to the overall performance of the system. The ESR of the capacitor combined with the $R_{DS(ON)}$ of the MOSFET will determine the peak current of the inrush. A 100µF capacitor with an ESR of 75 mΩ and an 80 mΩ load switch will have a theoretical peak inrush of 32A for a 5 Volt source. These peak currents stress the voltage source, generate high peak powers, and will degrade the overall lifetime of the system. The solution is to slowly turn on the PMOS device, charging the capacitor, and reducing the overall voltage the MOSFET will eventually turn on.

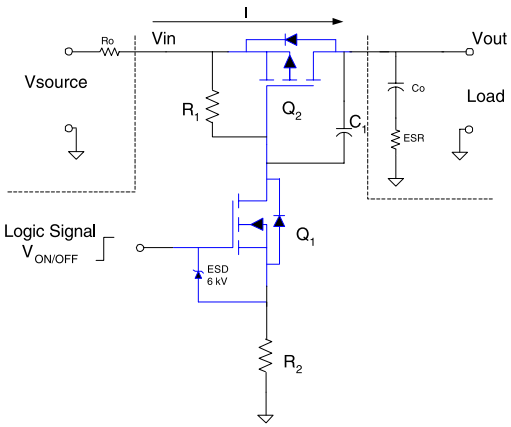

Figure 3. Inrush current

There are two simple ways to slow the turn on of the PMOS. If it is an integrated load switch, add a resistor R_2 at the source of Q_1. If it is a hybrid load switch, add R_2 between the gate of Q_2 and the drain of Q_1. Another way to slow the turn on of the PMOS is to add a capacitor, C_1, across Gate to Drain of Q2.

General Calculation

$$I_{IN} = I_L + I_{LOSS}$$

$$I_L = \frac{V_{OUT}}{R_L}$$

$$I_{LOSS} \approx \frac{V_{IN}}{R_1 + R_2}$$

$$V_{DROP} = V_{OUT} - V_{IN} = I_L \times R_{DS(ON)\,Q2}$$

$R_{DS(ON)\,Q2}$ is a function of $-V_{GS_{Q2}}$ and

$$-V_{GS_{Q2}} \approx V_{IN} \times \frac{R_1}{R_1 + R_2}$$

During turn off, the fall time of V_{OUT} is primarily determined by C_o and R_1 such that $t_{off} \propto R_1 \times C_o$

Definitions:
I_{IN} = Input current
I_L = Load current
I_{LOSS}= Current loss through R1 and R2 during turn on
V_{OUT} = Output voltage
R_L = Load resistor
V_{IN} = Input voltage
V_{DROP}= Voltage drops between input and output voltages
$R_{DS(ON)Q2}$= On resistance of Q2
V_{GSQ2}= Gate-source voltage of Q2
τ_{off} = Time constant for turn off
C_O = Output capacitor

For a typical selection of the external components, please refer to the load switch datasheets.

Conclusion

A MOSFET load switch is a simple way to reduce component count, lower cost and increase the overall the reliability of a system. In order to assist users, load switch SPICE models are available at the Fairchild Semiconductor web site: www.fairchildsemi.com. Further design support is available by the authors at john.bendel@fairchildsemi.com and alan.yi.c.li@fairchildsemi.com.

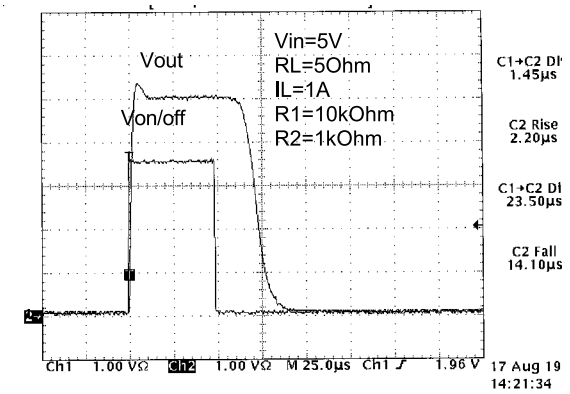

Figure 4. Measured FDC6329L Dynamic Waveforms

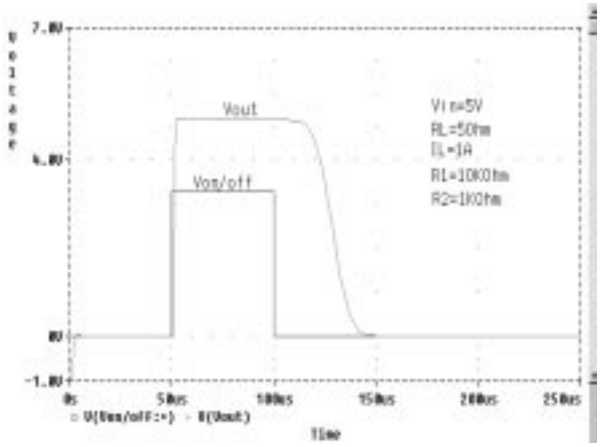

Figure 5. SPICE verification on FDC6329L Dynamic Waveforms

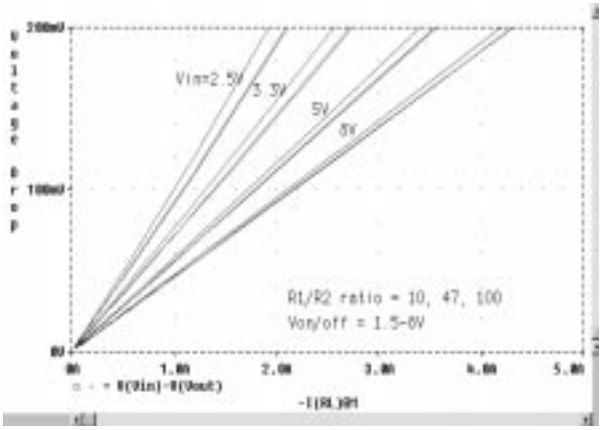

Figure 6. SPICE result of FDC6329L V_{DROP} vs I_L

Appendix A

Heat Flow Theory Applied to Power MOSFETs

When a Power MOSFET operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one dimensional steady-state model of conduction heat transfer is demonstrated in figure 5. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment. There are also secondary heat paths. One is from the package to the ambient air. The other is from the drain lead frame to the detached source and gate leads then to the printed circuit board. These secondary heat paths are assumed to be negligible contributors to the heat flow in this analysis.

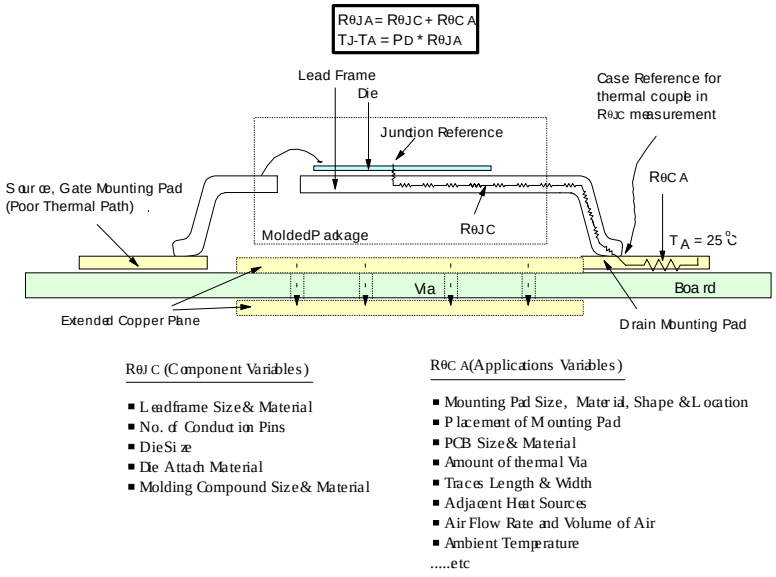

Figure 5: Cross-sectional view of a Power MOSFET mounted on a printed circuit board. Note that the case temperature is measured at the point where the drain lead(s) contact with the mounting pad surface.

The increase of junction temperature above the surrounding environment is directly proportional to dissipated power and the thermal resistance.

The steady-state junction-to-ambient thermal resistance, $R_{\theta JA}$, is defined as
$R_{\theta JA} = (T_J - T_A) / P$

where T_J is the average temperature of the device junction. The term junction refers to the point of thermal reference of the semiconductor device. T_A is the average temperature of the ambient environment. P is the power applied to the device which changes the junction temperature.

$R_{\theta JA}$ is a function of the junction-to-case $R_{\theta JC}$ and case-to-ambient $R_{\theta CA}$ thermal resistance

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where the case of a Power MOSFET is defined at the point of contact between the drain lead(s) and the mounting pad surface. $R_{\theta JC}$ can be controlled and measured by the component manufacturer independent of the application and mounting method and is therefore the best means of comparing various suppliers component specifications for thermal performance. On the other hand, it is difficult to quantify $R_{\theta CA}$ due to heavy dependence on the application. Before using the data sheet thermal data, the user should always be aware of the test conditions and justify the compatibility in the application.

Appendix B

Thermal Measurement

Prior to any thermal measurement, a K factor must be determined. It is a linear factor related to the change of intrinsic diode voltage with respect to the change of junction temperature. From the slope of the curve shown in figure 6, K factor can be determined. It is approximately 2.2mV/°C for most Power MOSFET devices.

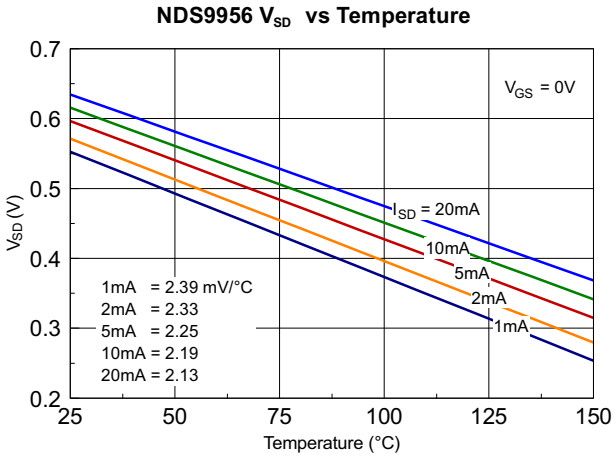

Figure 6. K factors, slopes of a V_{SD} vs temperature curves, of a typical Power MOSFET

After the K factor calibration, the drain-source diode voltage of the device is measured prior to any heating. A pulse is then applied to the device and the drain-source diode voltage is measured 30us following the end of the power pulse. From the change of the drain-source diode voltage, the K factor, input power, and the reference temperature, the time dependent single pulsed junction-to-reference thermal resistance can be calculated. From the single pulse curve on figure 7, duty cycle curves can be determined. Note: a curve set in which $R_{\theta JA}$ is specified indicates that the part was characterized using the ambient as the thermal reference. The board layout specified in the data sheet notes will help determine the applicability of the curve set.

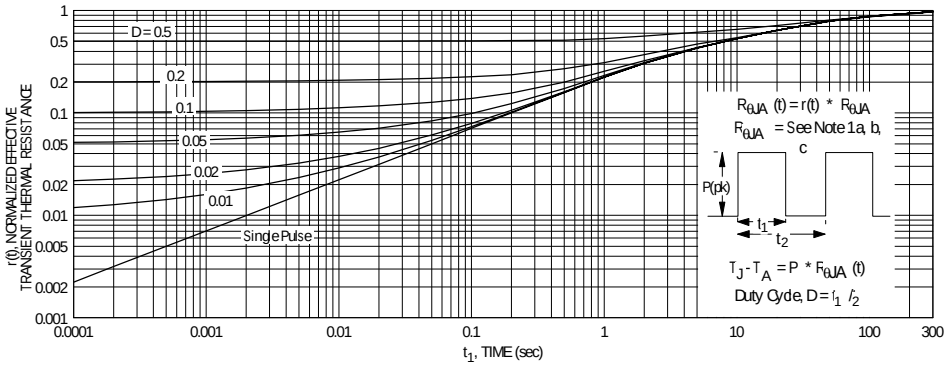

Figure 7. Normalized Transient Thermal Resistance Curves

B.1 Junction-to-Ambient Thermal Resistance Measurement

Equipment and Setup:

- Tesec DV240 Thermal Tester
- 1 cubic foot still air environment
- Thermal Test Board with 16 layouts defined by the size of the copper mounting pad and their relative surface placement. For layouts with copper on the top and bottom planes, there are 0.02 inch copper plated vias (heat pipes) connecting the two planes. See figure 2 and table 1 on the thermal application note for board layout and description. The conductivity of the FR-4 PCB used is 0.29 W/m-C. The length is 5.00 inches ± 0.005; width 4.50 inches ± 0.005; and thickness 0.062 inches ± 0.005. 2Oz copper clad PCB.

The junction-to-ambient thermal measurement was conducted in accordance with the requirements of MIL-STD-883 and MIL-STD-750 with the exception of using 2 Oz copper and measuring diode current at 10mA.

A test device is soldered on the thermal test board with minimum soldering. The copper mounting pad reaches the remote connection points through fine traces. Jumpers are used to bridge to the edge card connector. The fine traces and jumpers do not contribute significant thermal dissipation but serve the purpose of electrical connections. Using the intrinsic diode voltage measurement described above, the junction-to-ambient thermal resistance can be calculated.

B.2 Junction-to-Case Thermal Resistance Measurement

Equipment and Setup:

- Tesec DV240 Thermal Tester
- large aluminum heat sink
- type-K thermocouple with FLUKE 52 K/J Thermometer

The drain lead(s) is soldered on a 0.5 x 1.5 x 0.05 copper plate. The plate is mechanically clamped to a heat sink which is large enough to be considered ideal. Thermal grease is applied in-between the two planes to provide good thermal contact. Theoretically the case temperature should be held constant regardless of the conditions. Thus a thermocouple is used and fixed at the point of contact between the drain lead(s) and the copper plate surface, to account for any heatsink temperature change. Using the intrinsic diode voltage measurement described earlier, the junction-to-case thermal resistance can be obtained. A plot of junction-to-case thermal resistance for

various packages is shown in figure 8. Note $R_{\theta JC}$ can vary with die size and the effect is more prominent as $R_{\theta JC}$ decreases.

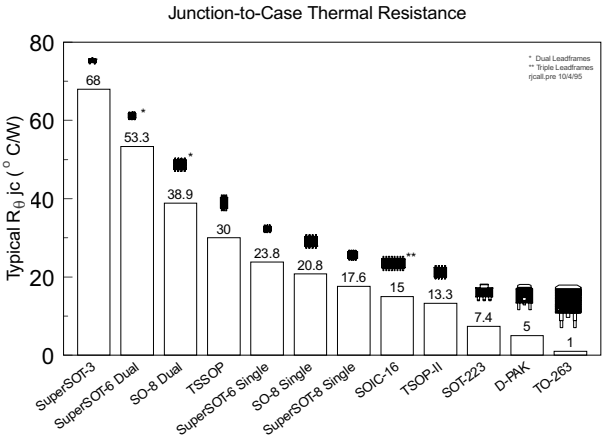

Figure 8. Junction-to-case thermal resistance $R_{\theta JC}$ of various surface mount Power MOSFET packages.

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