ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

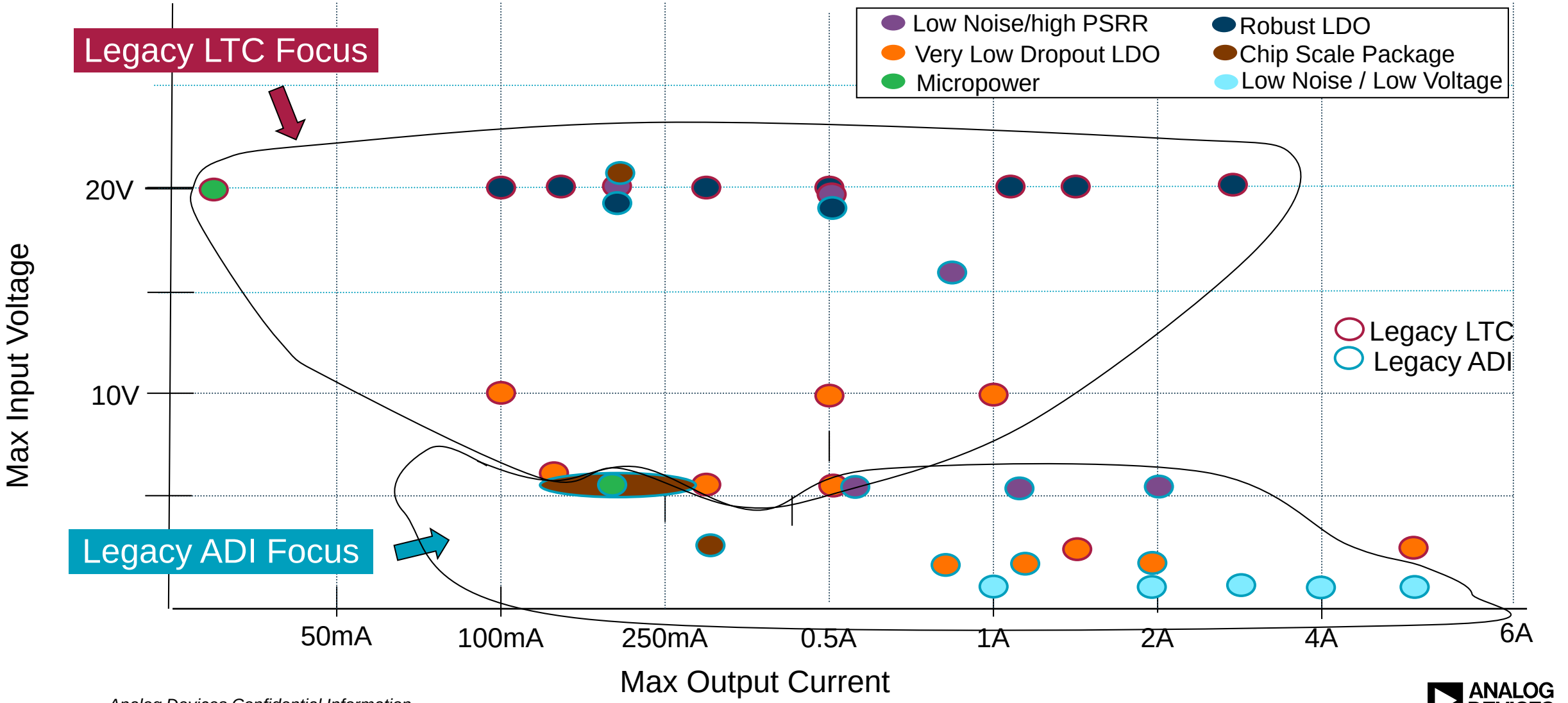
ADI Linear Regulators

ADI LDO Product Portfolio

- Value-Added LDOs from Legacy LTC
- Value-Added and General Purpose LDOs from Legacy ADI

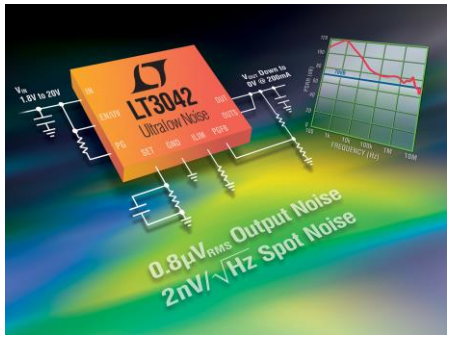
LTC LDOs + ADI LDOs
= Comprehensive LDO Product Portfolio
with Very Little Performance Overlap

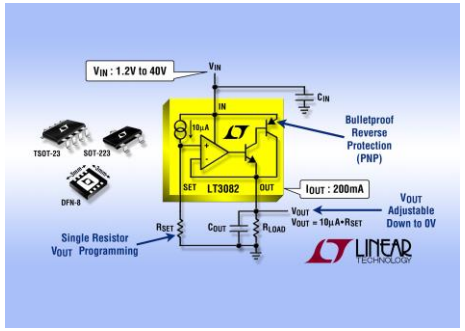
Complementary Positive Linear Regulators with Very Little Functionality Overlap



ADI Value-Added Emphasis

- Lowest Noise / High PSRR LDOs for Wired/Wireless and Audio Systems
- High Performance, Lowest Noise Negative Output LDOs
- Low Voltage, Low Noise LDOs and Very Low Dropout LDOs (VLDOs) Target FPGA/DSP/µC Power
- Current Source LDOs – Low Noise, Easily Paralleled (heat spreading), Single Resistor sets V_{OUT}
- Advanced Small Size Packaging Solutions
- LDO Circuit Performance: Getting all the Performance from your LDO (LT3045-1 spotlight)





Current and Future LDO Development

- **State of the Art Performance**

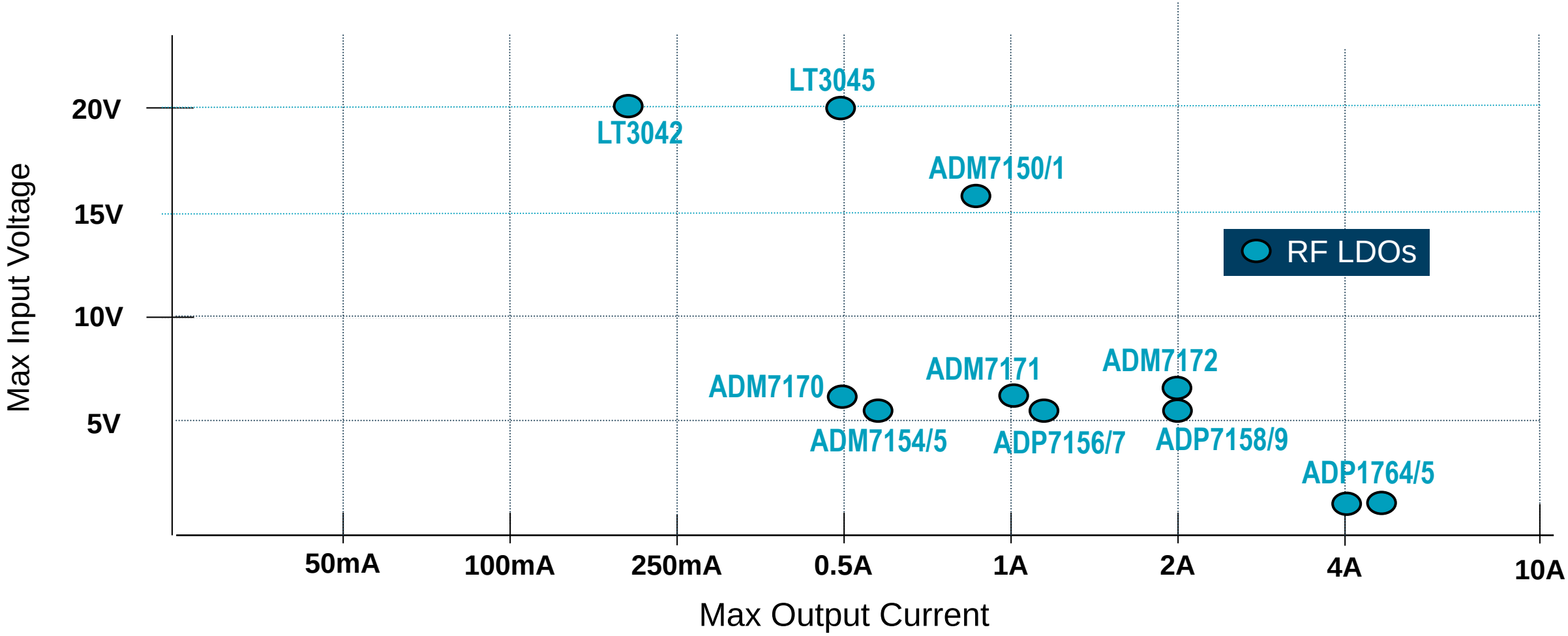
  - Lowest Noise and Highest PSRR performance in the Industry

- **Evolution of the LDO Architecture Improves Performance**

  - Current Source Reference Replaces the Traditional Voltage Reference

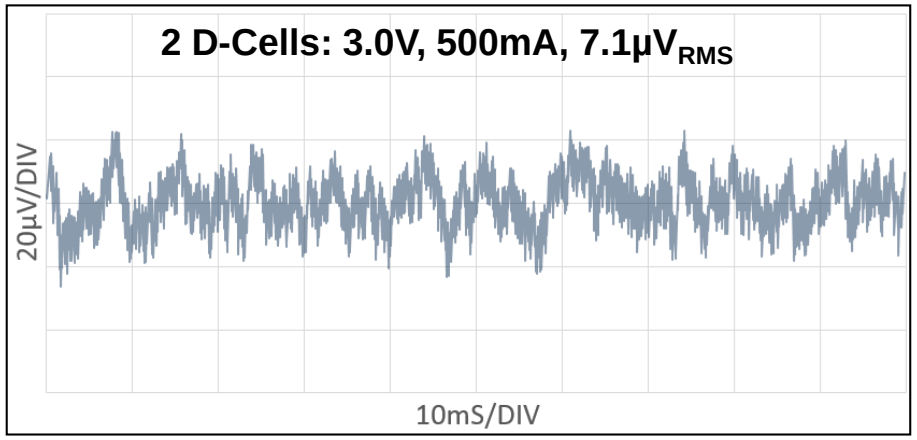
- **Advanced Packaging Technologies**
  - Improve electrical and thermal performance
  - Improve power density
  - Reduce solution size
  - Integrate discrete components on-chip (capacitors, resistors, ferrite beads, etc.)

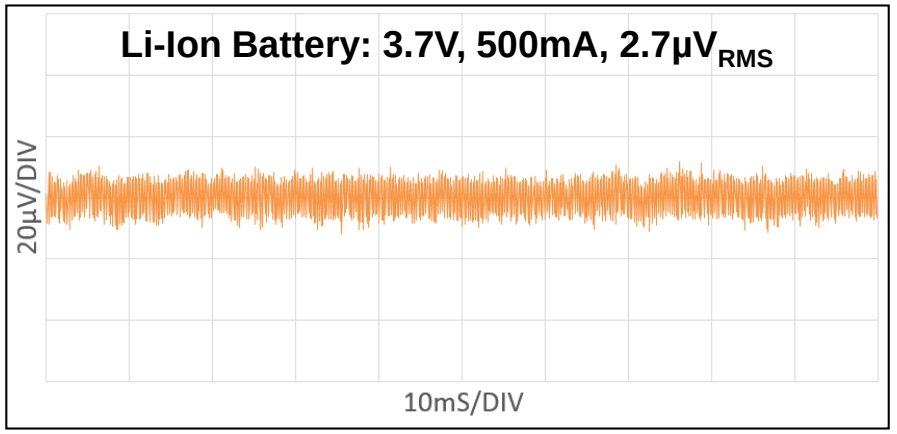
Featured Ultralow Noise Positive Linear Regulators

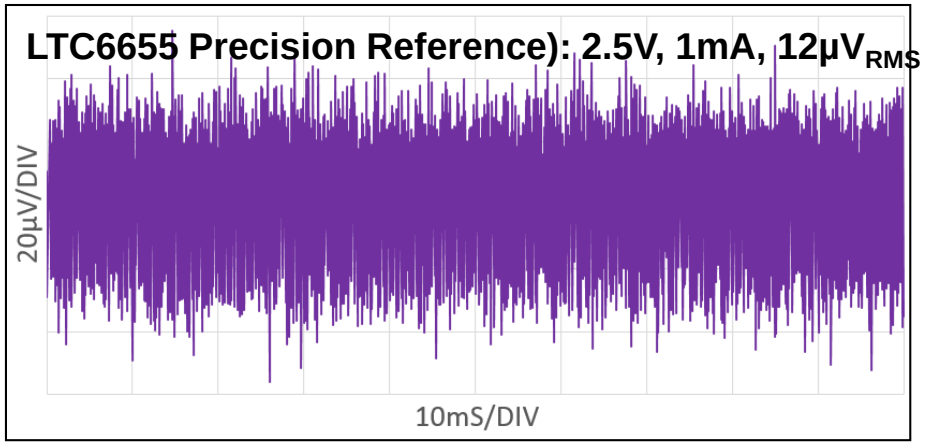


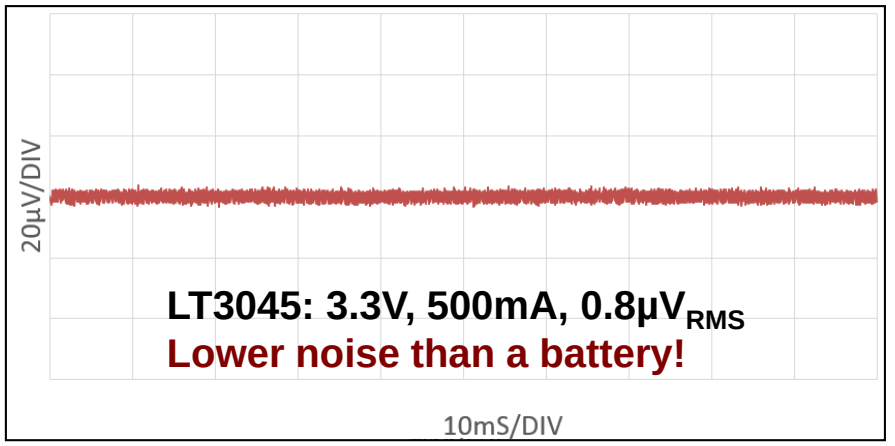
What is Meant By “Low Noise LDO?”

Output Noise (10Hz to 100kHz): D-Cell, Li-Ion, LTC6655 & LT3045





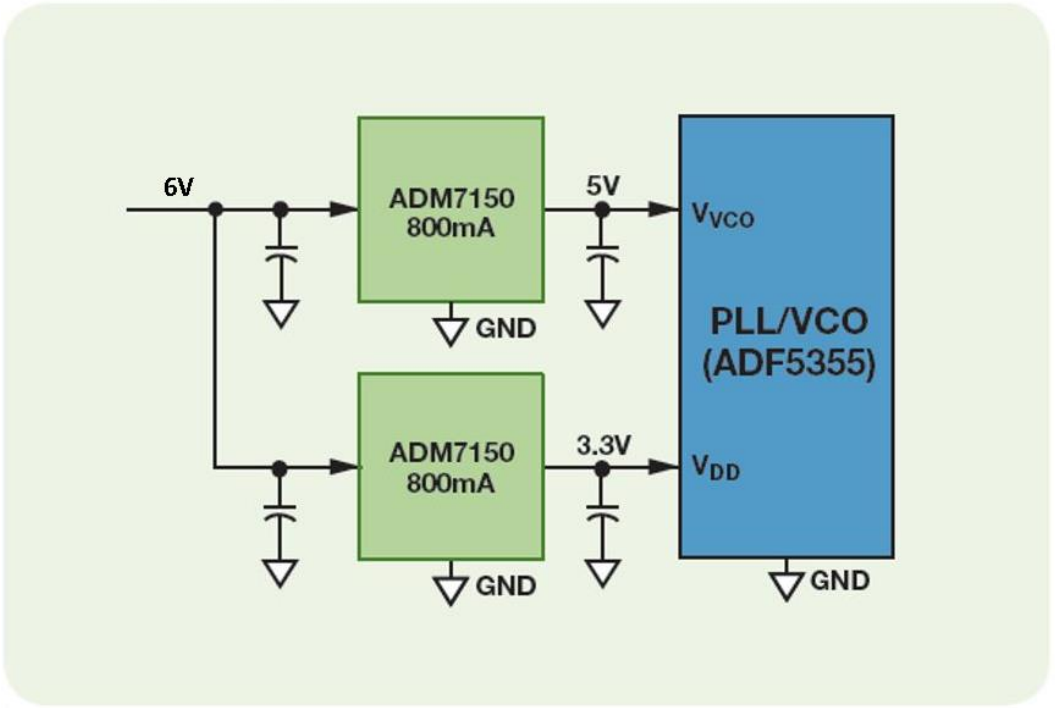


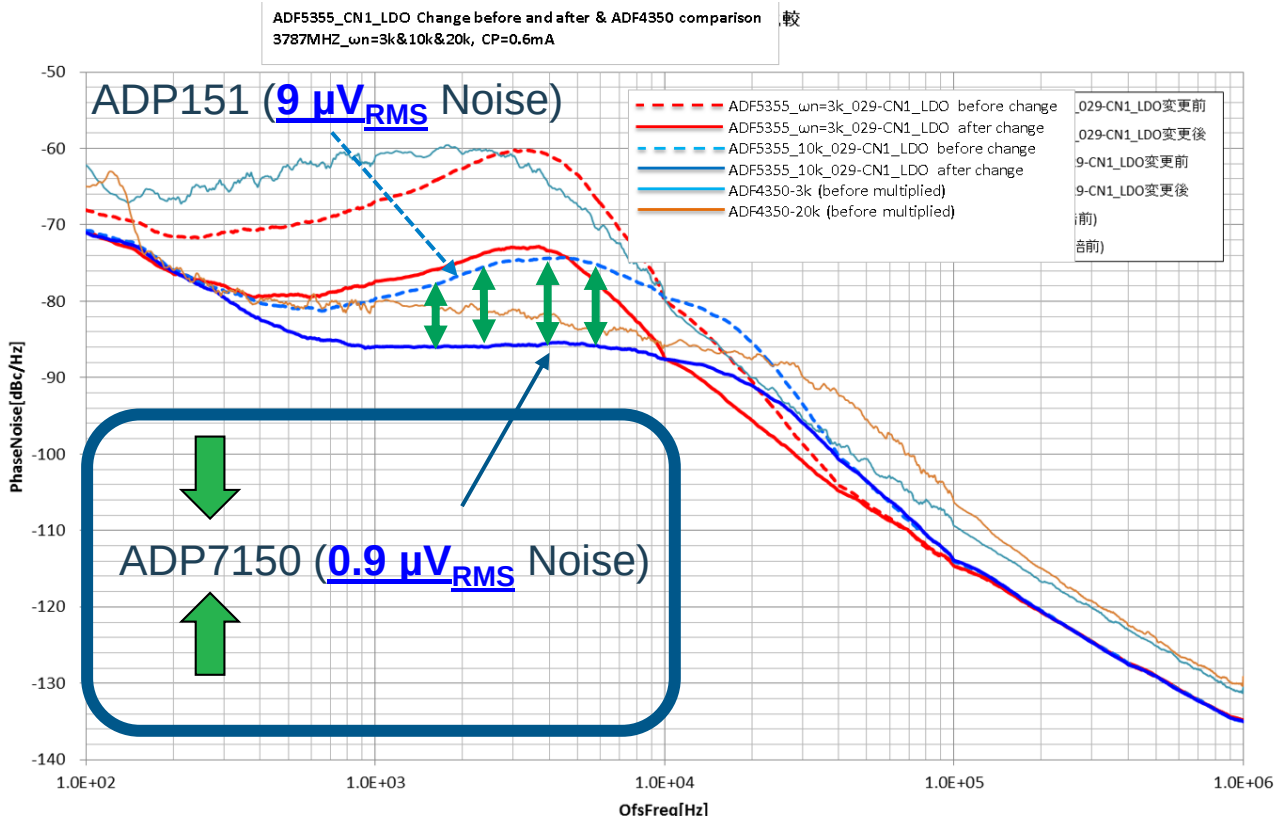


An Ultralow Noise LDO Improves System Performance

- Example ADF5355 PLL Phase Noise vs. Frequency Offset

PLL/VCO Apps Diagram

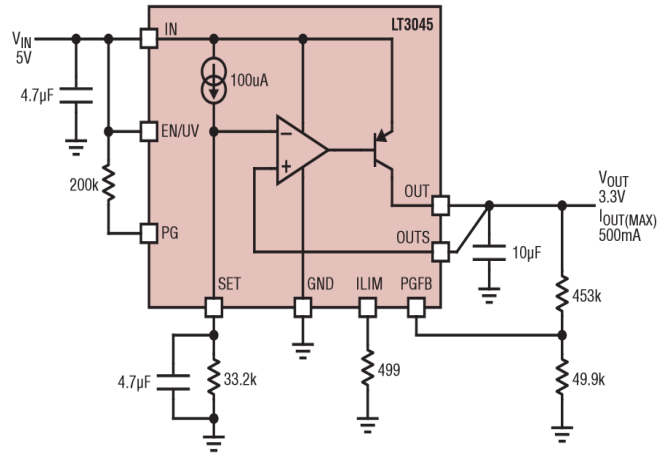




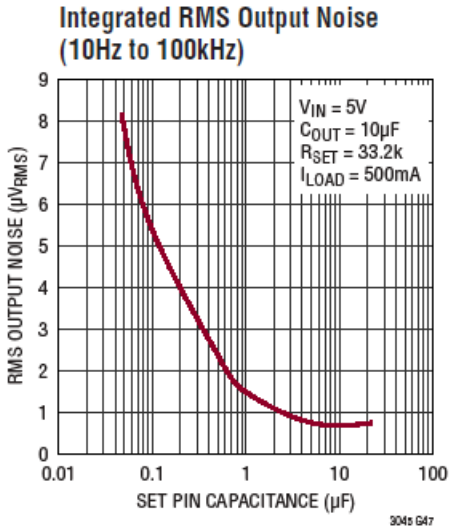
>10dB Phase Noise Improvement at ~4kHz to 5kHz Offset with Ultralow Noise ADP715x LDO family

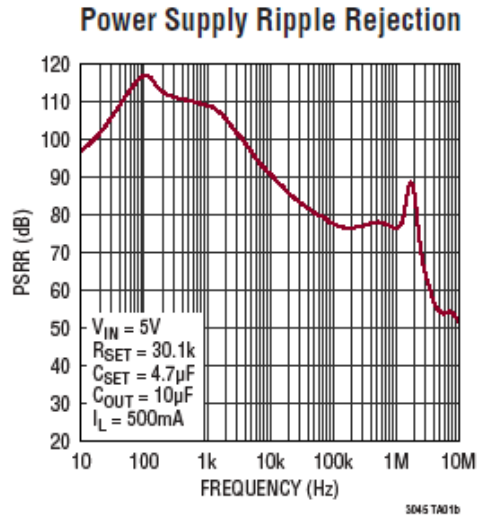
State of the Art Performance: LT3042 and LT3045 Lowest Noise, Highest PSRR LDOs in the Industry

- Key Specifications:
  - Ultralow 0.8μV_{RMS} 10Hz to 100kHz noise
  - Highest PSRR: >70dB @ 2MHz
  - 0.2A (LT3042) and 0.5A (LT3045)



- Ideal for:
  - Low Noise VCOs, PLLs, etc.
  - High Performance, Low Noise Signal Chain Power Supply (ADCs, Amplifiers, etc.)
  - Post-Regulator for Switching Power Supply

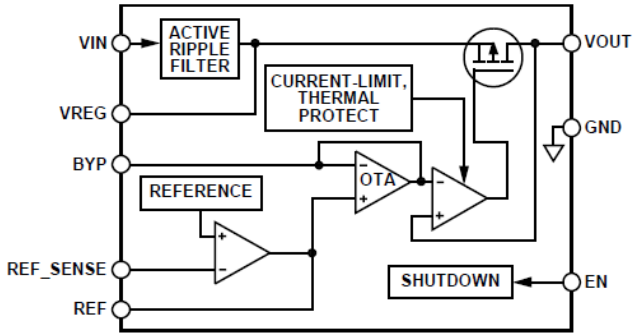


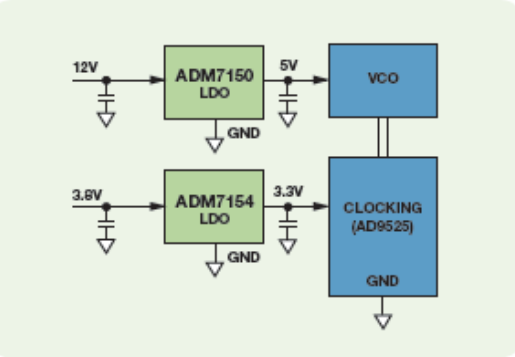


State of the Art Performance: ADM7150 / ADM7154

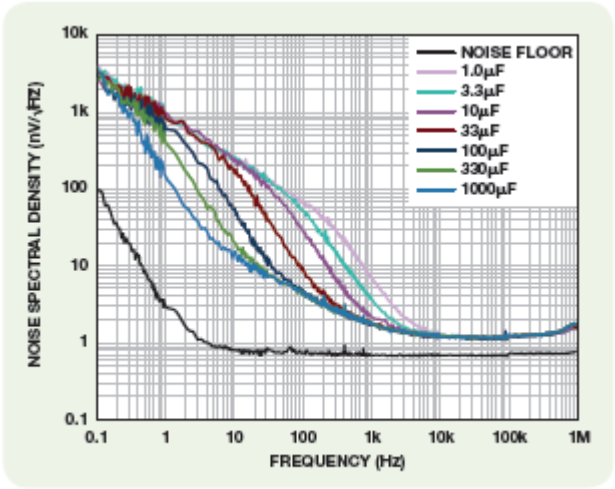
- Key Specifications:
  - Ultralow 1.6μV_{RMS} noise*
  - Lowest noise density: 1.7nV/√Hz
  - 0.6A to 2A output range

ADM7154





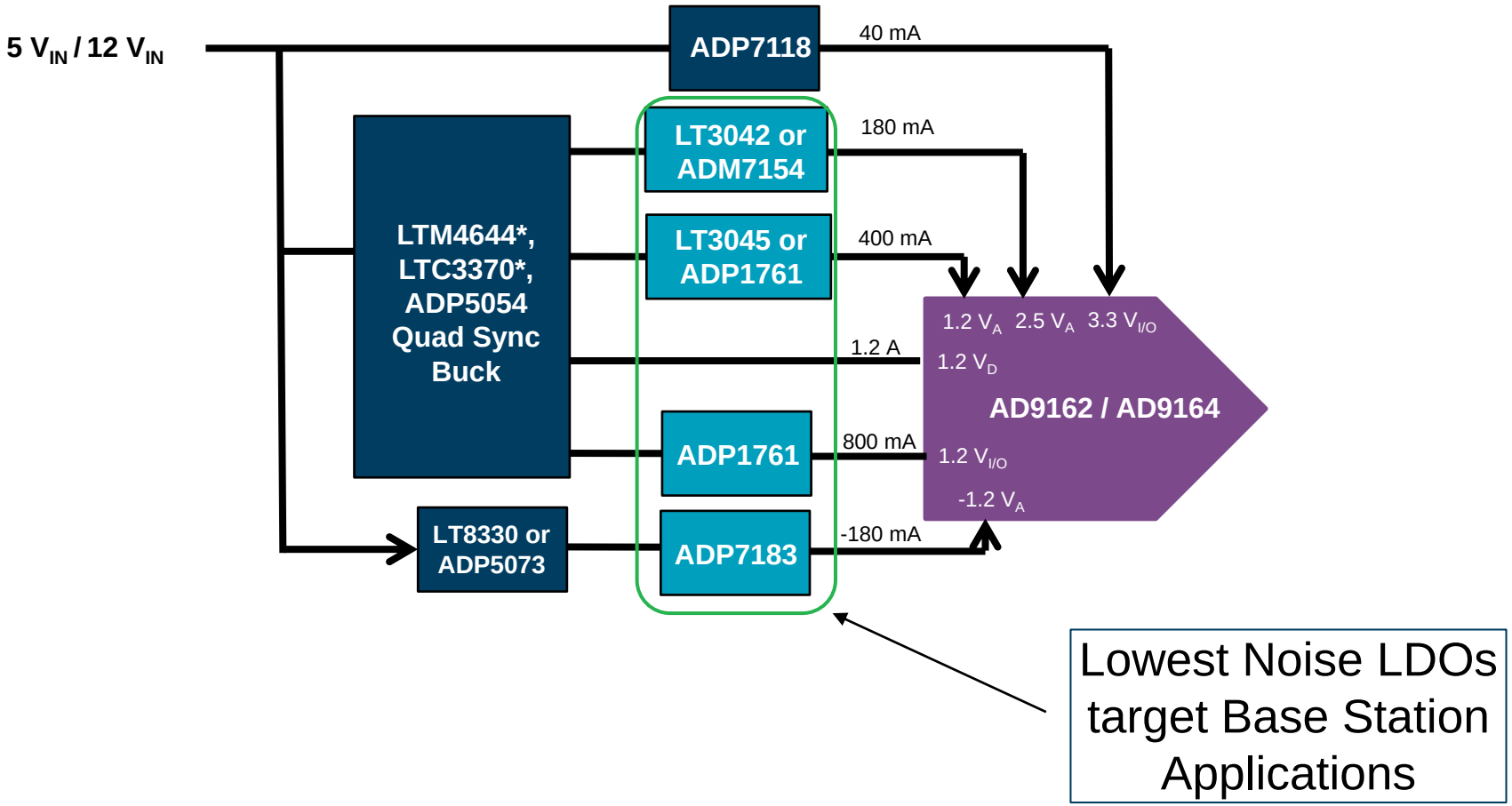
- Ideal for:
  - Low Noise VCOs
  - High Performance, Low Noise Signal Chain Power Supply (ADCs, Amplifiers, etc.)
  - Post-Regulator for Switching Power Supply



ADM7154 noise spectral density.

*10Hz to 100kHz

Low Noise LDO Power Supplies for the AD9162 16-Bit, 12 GSPS RF DAC

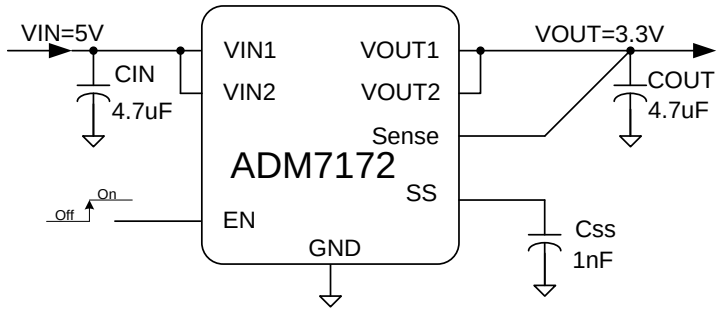


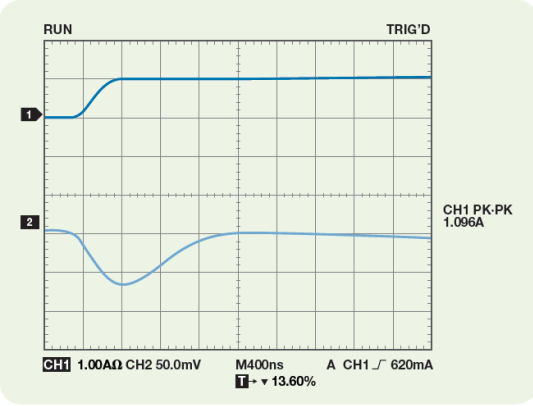
*5V only

Low Noise LDO Highlight: ADM7170, ADM7171, ADM7172

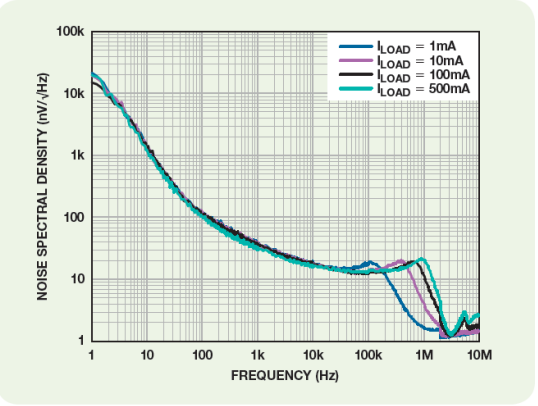
- Key Specifications:
  - Low 6μV_{RMS} noise*
  - Ultrafast transient response < 1.5μs
  - 0.5A to 2A output range
- Ideal for:
  - Low Noise VCOs
  - High Performance, Low Noise Signal Chain Power Supply (ADCs, Amplifiers, etc.)
  - Post-Regulator for Switching Power Supply

*10Hz to 100kHz





ADM7171 full load transient response from 1 mA to 1 A for V_{OUT} = 3.3 V



Output noise spectral density, different output voltages, load current = 100 mA

Ultralow Noise, Fast Transient Response LDO Selection Table

Part Number	V_{IN} Range (V)	V_{OUT} Options or Adj Range (V)	I_{OUT} (mA)	Soft Start	Power Good	PSRR @ 100 kHz (dB)	PSRR @ 1 MHz (dB)	RMS Noise @ 100 Hz to 100 kHz (μV rms)[1]	Noise Spectral Density 100 kHz (nV/√Hz)	Dropout @ Rated I_{OUT} Typ (mV)	Total Accuracy Max (±%)	Package
ADM7170	2.3 to 6.5	Fixed: 1.2 to 5.0 Adjustable: 1.2 to 6.4	500	Yes	No	60	31	5.0	12	42	1.25	3 mm × 3 mm, 8-lead LFCSP
ADM7171	2.3 to 6.5	Fixed: 1.2 to 5.0 Adjustable: 1.2 to 6.4	1000	Yes	No	60	31	5.0	12	84	1.5	3 mm × 3 mm, 8-lead LFCSP
ADM7172	2.3 to 6.5	Fixed: 1.2 to 5.0 Adjustable: 1.2 to 6.3	2000	Yes	No	60	31	5.0	12	172	1.5	3 mm × 3 mm, 8-lead LFCSP

Best-In-Class Low Noise Negative Output LDOs

Part Number	I_{OUT} Range (A)	V_{IN} (V)	RMS Noise (µVrms)*	Package Options (mm)	Key Features
ADP7182	0.2	-2.7 to -28	**18**	2x2 **LFCSP-6**, 3x3 **LFCSP-8**, TSOT-5	Pos/Neg EN, Chip Scale Pkg
LT1964	0.2	-1.9 to -20	30	3x3 DFN-8,SOT-23	**Robust** Protection
ADP7183/ ADP7185	0.3, 0.5	-2.0 to -5.5	**5** (indep of V_{OUT})	2x2 **LFCSP-8**	Low Noise, Pos/Neg EN, Chip Scale Pkg
LT3094 Coming Soon!	0.5	-2 to -20	**0.8**	3x3 DFN-12, MSOP-12E	RF LDO, **Ultralow Noise and High PSRR**
LT1175	0.5	-4.3 to -20	No spec	DDPAK-5,N-8,SO-8,SOT-223,TO-220	Pos/Neg EN, Prog Current Limit, **45µA Iq**
LT3090/ LT3091	0.6, **1.5**	-1.5 to -36	**18**	3x3 DFN-10,MS-12E / 4x3 DFN-14,DDPAK-7,TO-220,TSSOP-16	**I_{SOURCE} V_{REF}**, V_{OUT} to 0V, POS/Neg I_{OUT} monitor
LT1185	3	-4.2 to -35	No spec	DDPAK-5,TO-220	Prog Current Limit, Shutdown, Thermal Shutdown, **High Current**

*10Hz to 100kHz

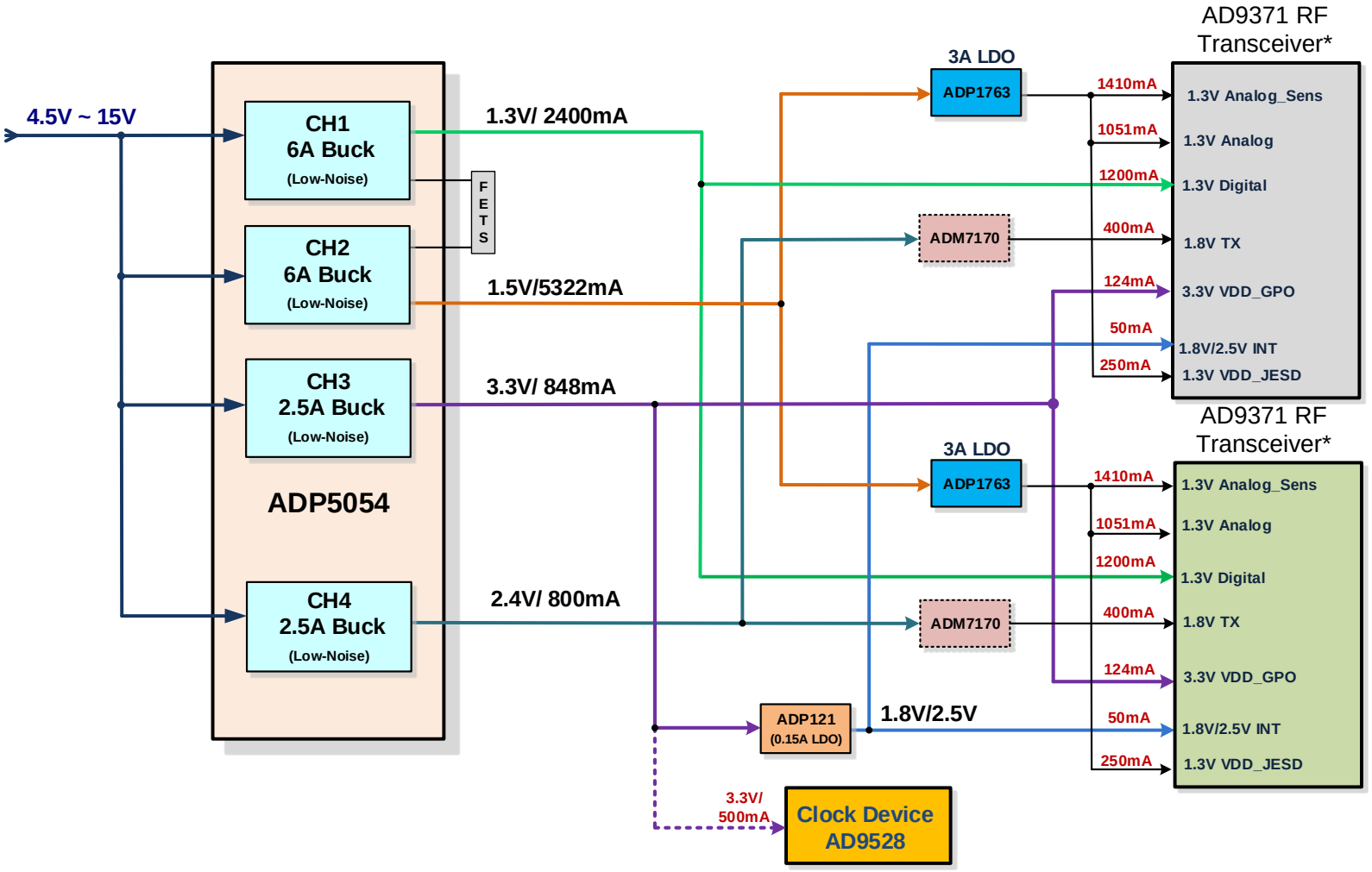
Very Low Dropout LDOs (VLDOs) for FPGAs, DSPs, Digital Chips, etc.

Part Number	I_{OUT} Range (A)	V_{IN} (V)	RMS Noise (μV_{RMS})*	Package (mm)	Key Features
ADP1765	5	1.1 to 1.98	3	3x3 LFCSP	59mV Dropout (typ)
LT3070	5	0.9 to 3.0 V_{BIAS}: 2.2 to 3.6	25	4x5 QFN-28	Prog V_{OUT}: 0.8V to 1.8V, Margining, PGood, 85mV Dropout
LT3071	5	0.9 to 3.0 V_{BIAS}: 2.2 to 3.6	25	4x5 QFN-28	Prog V_{OUT}: 0.8V to 1.8V, Margining, PGood, I_{OUT} Monitor, 85mV Dropout
ADP1764	4	1.1 to 1.98	3	3x3 LFCSP	47mV Dropout (typ)
LT3033	3	0.95 to 10	60	3x4 QFN-20	V_{OUT}: 0.2V to 9.5V, Prog ILIM, I_{OUT} Monitor
ADP1763	3	1.1 to 1.98	12	3x3 LFCSP	95mV Dropout (typ)
ADP1762	2	1.1 to 1.98	12	3x3 LFCSP	62mV Dropout (typ)
ADP1761	1	1.1 to 1.98	12	3x3 LFCSP	30mV Dropout (typ)

Coming Soon!

*10Hz to 100kHz

ADP176x: Low Noise Power for Small Cell Base Station Designs

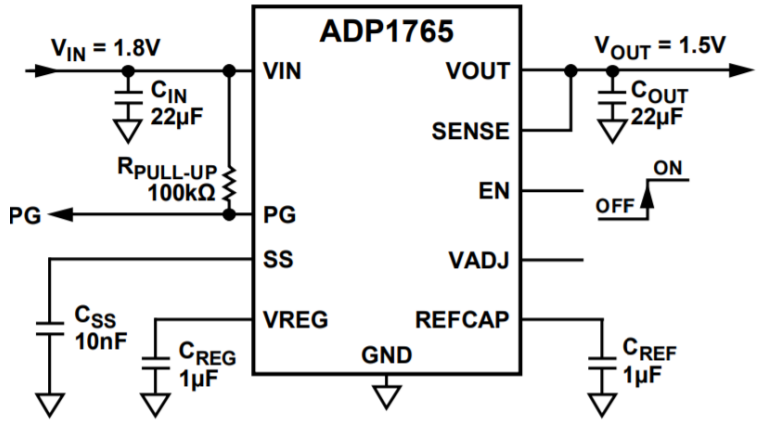


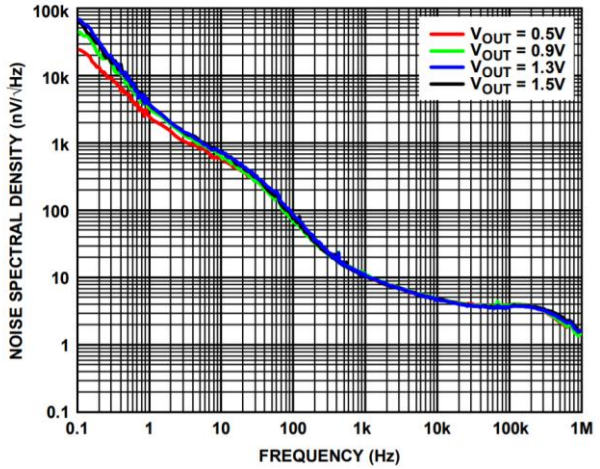
- Power Sequencing & Phase Synchronized using low noise quad ADP5054 synchronous buck converter
- 2x ADP1763 (3A Low Noise LDO)
  - Powers up 1.3V analog, analog sensitive and JESD VTT rails
  - Ferrite bead isolation required for each sensitive pin
- Individual ADM7170s isolate each 1.8V_TX rail
- Shared 3.3V VDD GPO (buck CH 1) and low power 1.8V/2.5V interface supply (ADP121)

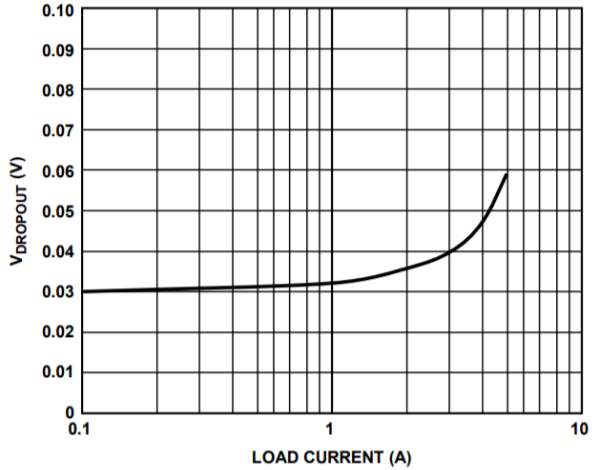
*Additional information available for ADI AD937x Mykonos transceiver reference design

Low Voltage, Low Noise VLDO Highlight: ADP1765/64/63

- Key Specifications:
  - 1.1V to 1.98V input voltage
  - Low 3μV_{RMS} noise* (12μV_{RMS} for the ADP1763)
  - Low dropout: 59mV @ 5A
  - 5A (ADP1765), 4A (ADP1764), 3A (ADP1763)
  - Small 3mm x 3mm LFCSP
- Ideal for:
  - High Performance, Low Noise Signal Chain Power Supply (HS ADCs, DACs, xCVRs, etc.)
  - High Performance FPGA, Mixed-Signal ASIC
  - Post-Regulator for Switching Power Supply

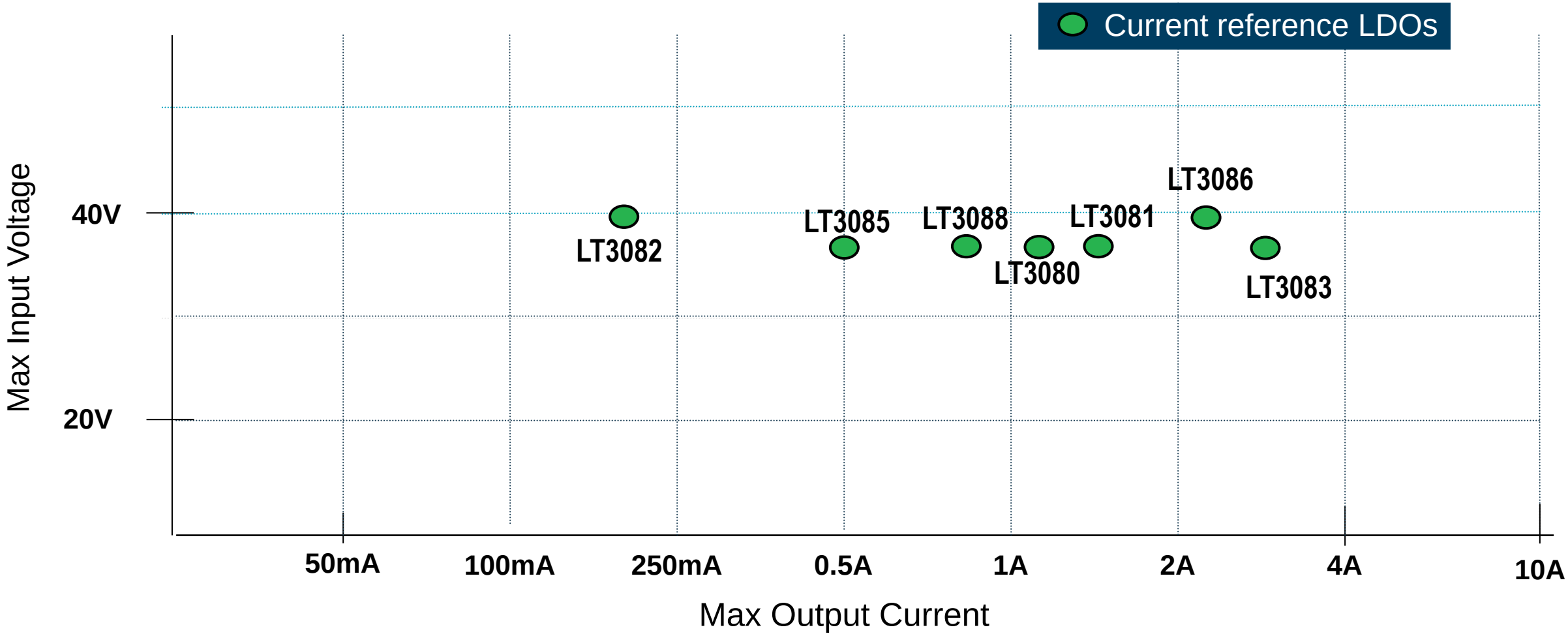




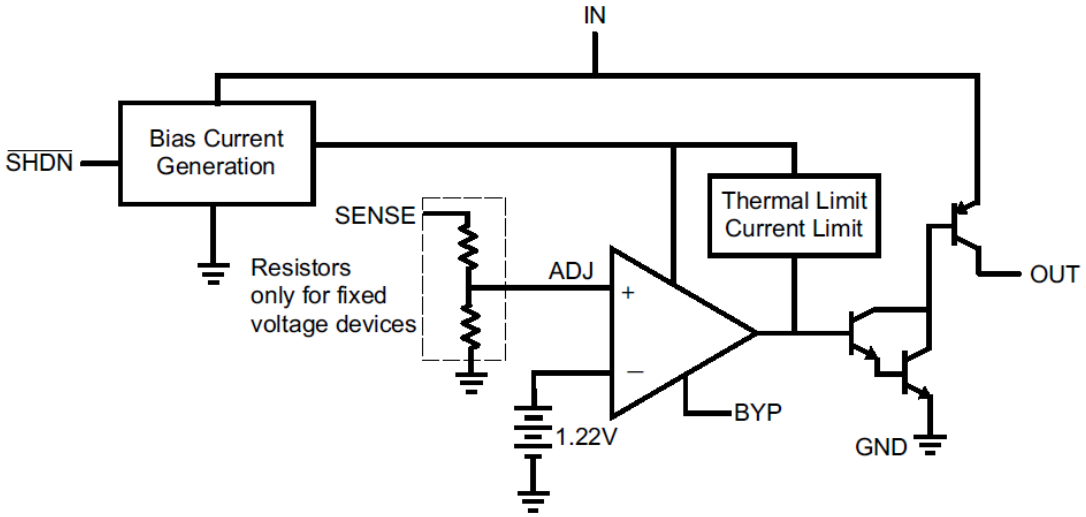


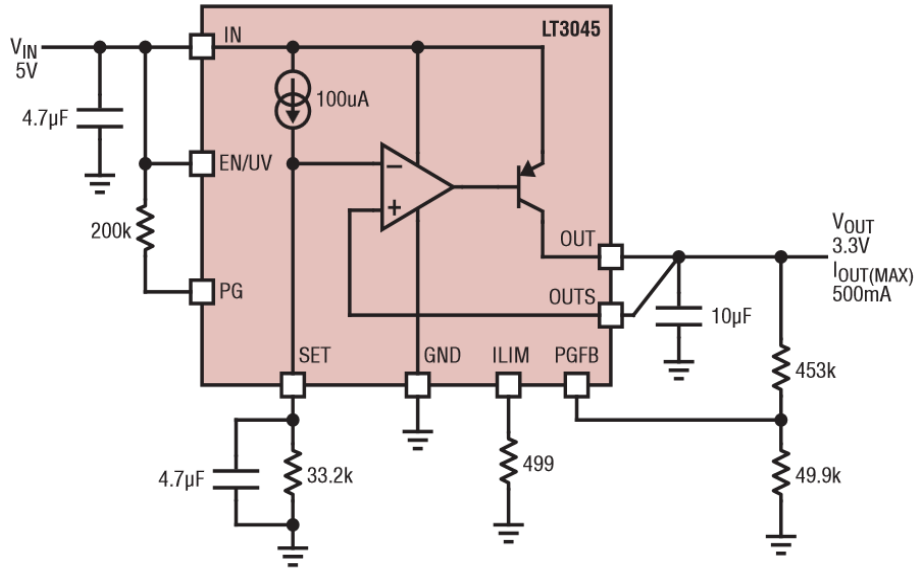
*10Hz to 100kHz

Featured Current Source Reference Linear Regulators



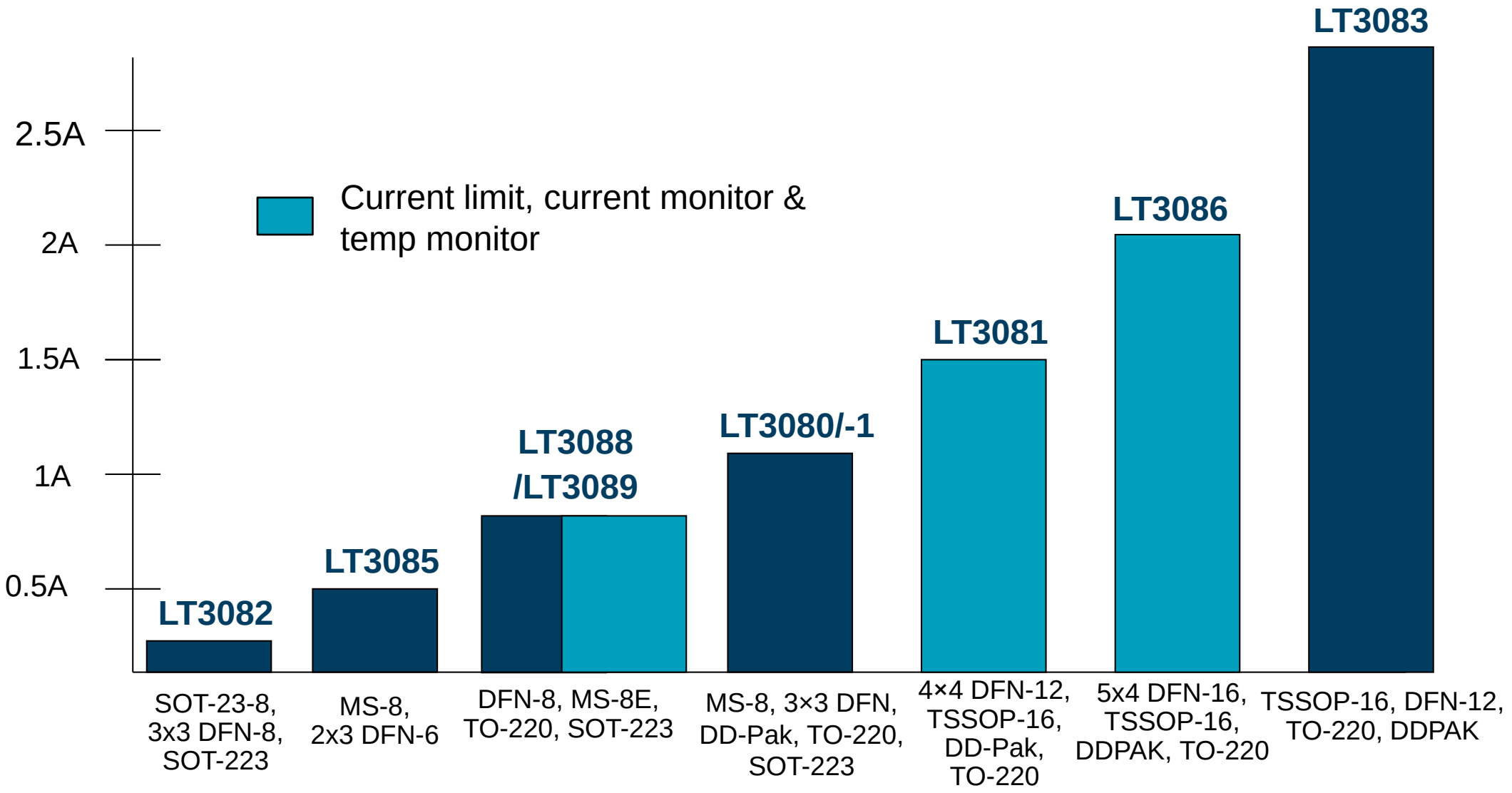
Current Source LDOs: LDO Architecture Innovation





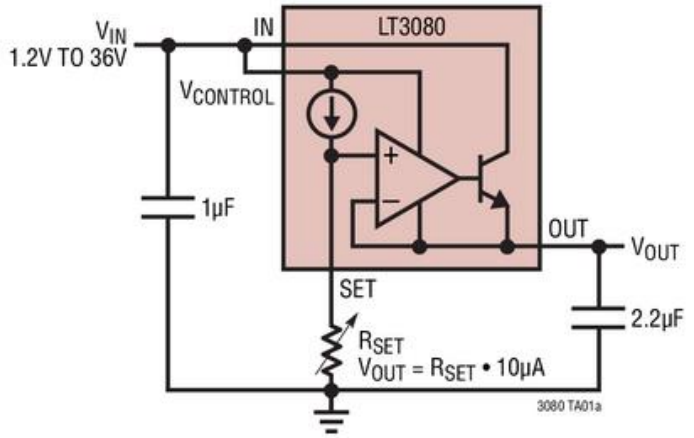
- **Current Source Reference: LDO Benefits over Traditional V_{REF} based LDO**
  - **Linear Regulator always operates in Unity Gain – Maximum Bandwidth**
  - **Bandwidth, Transient Response, Load Reg., Noise and PSRR are independent of V_{OUT}**
  - **Easily Parallel LDOs for higher current and PCB heat spreading**
  - **One Resistor programs V_{OUT} from 0V to (V_{INMAX}-$V_{DROPOUT}$)**

Positive Current Source LDOs



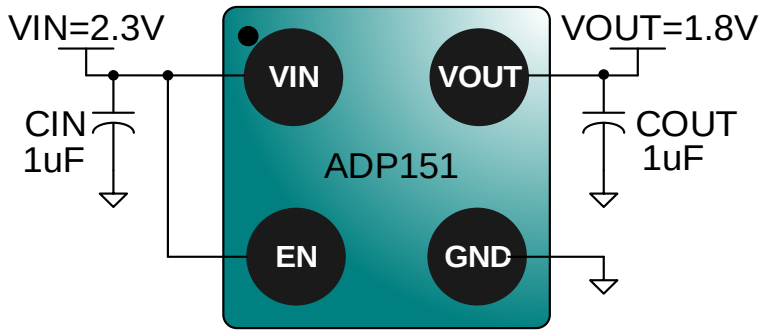
Current Source LDO Performance

- Low Output Noise: ~40μV_{RMS} (10Hz to 100kHz)
- V_{OUT} down to 0V
- Easy to Parallel:
  - Excellent at sharing current
  - LT3080-1 has ballast resistor on-chip
- Wide Input Voltage Range
  - 1.2V up to 36V or 40V (depending on the device)
- Negative Output Voltage Versions Available (**LT3090/LT3091**)
- Require a Minimum Load Current for Stability (500μA over temp)



Ultra-Small LDO Chip-Scale Packages

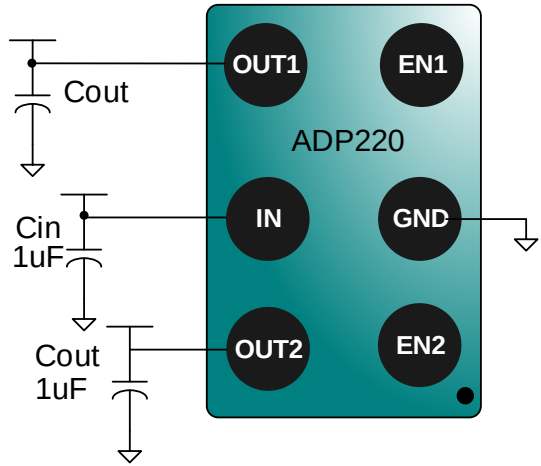
ADP151: 200mA Low Noise ($9\mu V_{RMS}$), Low I_Q (10µA – no load) Performance LDO



4-Ball, 0.4mm pitch WLCSP

Compact: 0.8mm x 0.8mm = 0.64 mm^2

ADP220/1: Dual 200mA LDO



6-Ball, 0.5mm pitch WLCSP

Compact: 1.0mm x 1.5mm = 1.5 mm^2

- Ideal for LDOs with I_{OUT} < 300mA
- Compact: as small as 0.8mm x 0.8mm packages
- High Power Density packages

WLCSP = Wafer Level Chip Scale Packaging

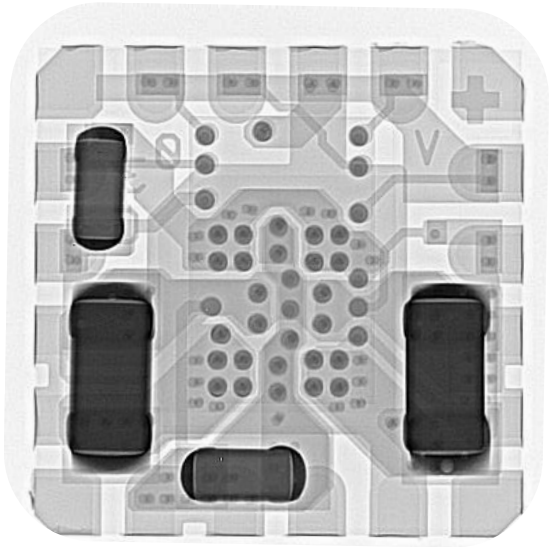
ADI Advanced Packaging Technologies

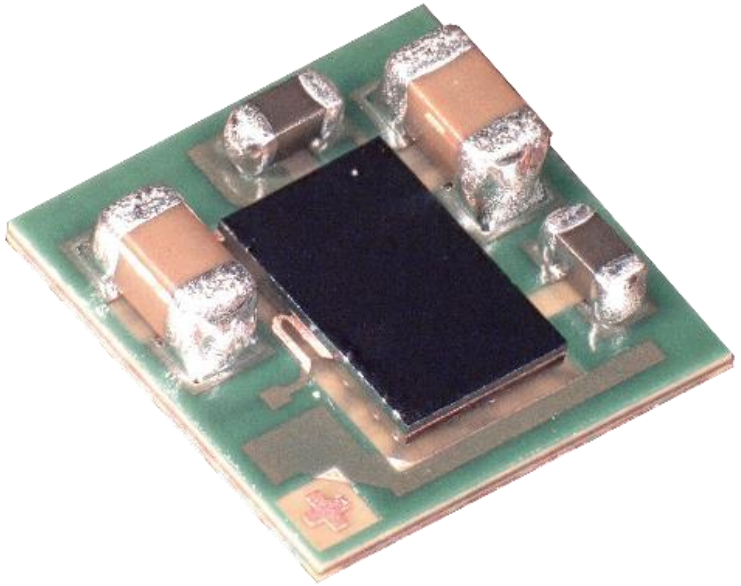
- **Flip-Chip with Copper Pillars**
- Reduces Parasitic Inductance and Resistance due to Bond Wires and Interconnect Metallization
- Enables Lower Dropout Performance
- Improved Power Density
- Comparable Thermal Performance with Exposed Pad Packages

LT3033 Cross-Section

ADI Advanced Packaging Technologies

- **BT-Substrate**
- Configured to look like standard DFN/QFN packages.
- Internal Multi-Layer Interconnect Metallization
- Allows Integration of Discrete Components (Resistors, Capacitors, Ferrite Bead, etc.)

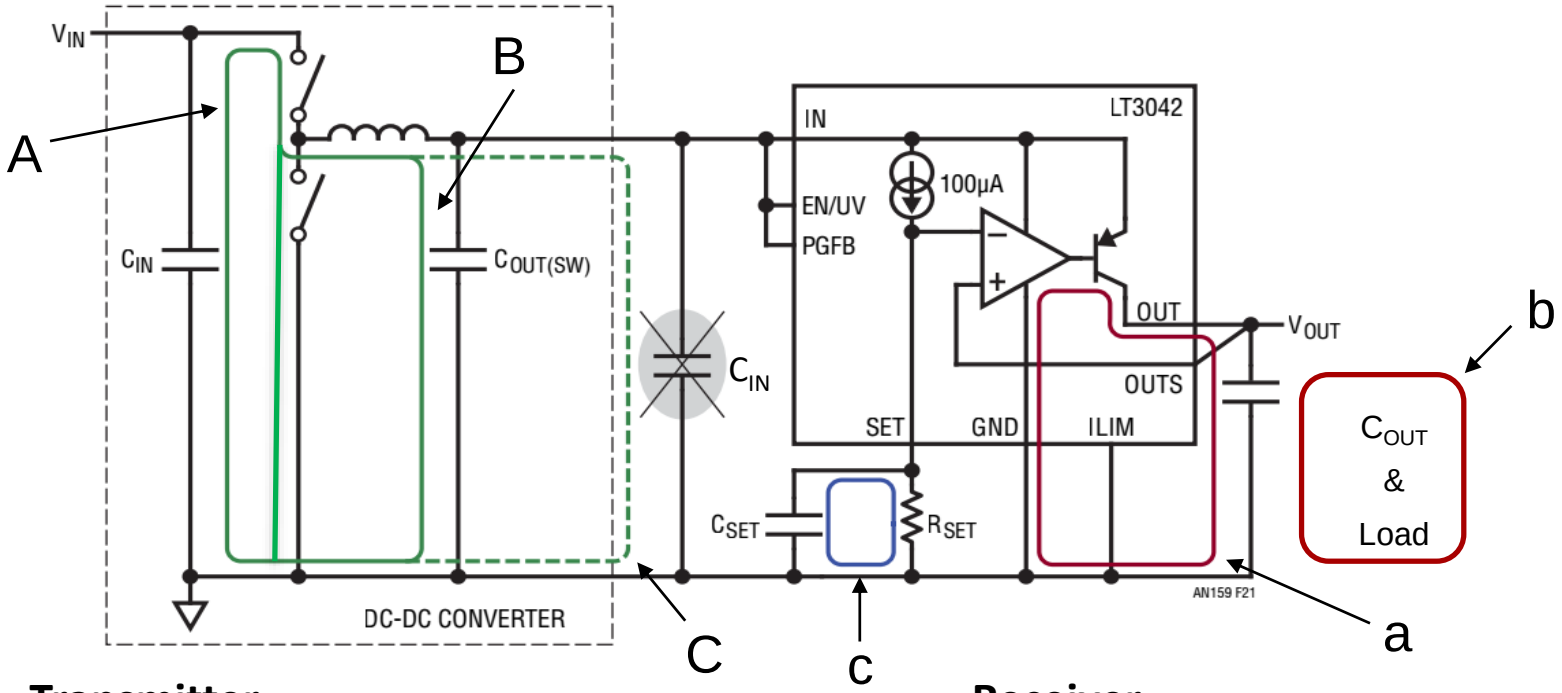




LDOs Post-Regulating Switching Supplies

- Extracting All the PSRR Performance from the LDO
- Principles, FMEA Simulations, Test Results
- PCB Layout IS CRITICAL!
- PHYSICS and Circuit Design: What Can go Wrong Will Go Wrong!

Magnetic Coupling Loops



Transmitter

A. Hot Loop (very high frequency)

B. "Warm" Loop (switching frequency)
   - It is typically (physically) large

C. "Warm" Loop to LDO C_{IN}

Receiver

a) LT3042 output loop

b) C_{OUT}/Load loop

c) LT3042 SET pin loop

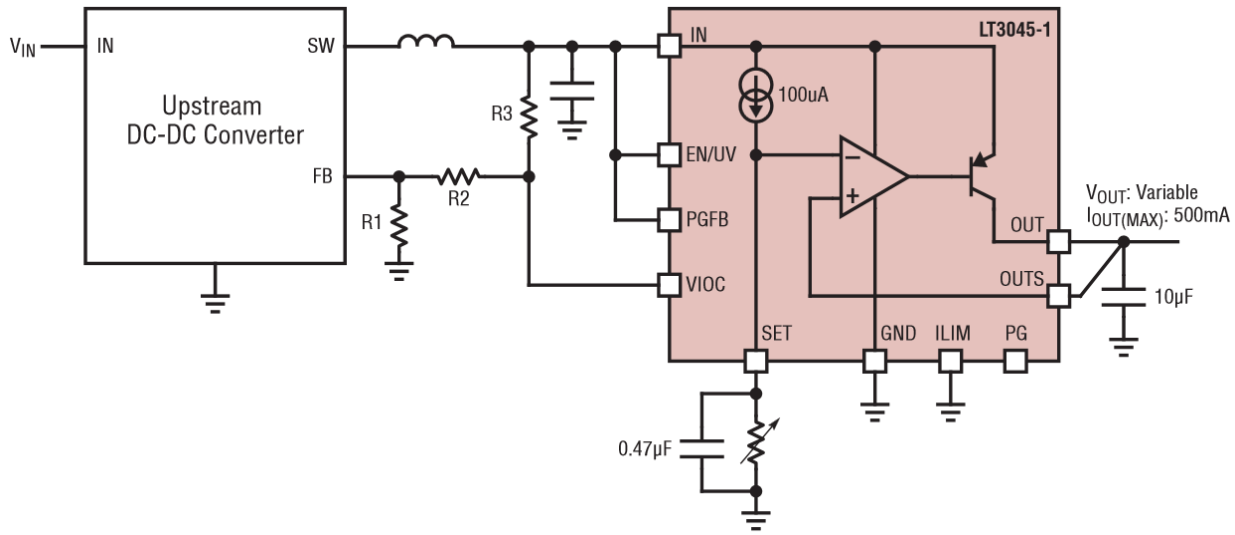
Unique Post-Regulator Functionality: Efficient LDO Operation Using LT3045-1

- VIOC Feature:

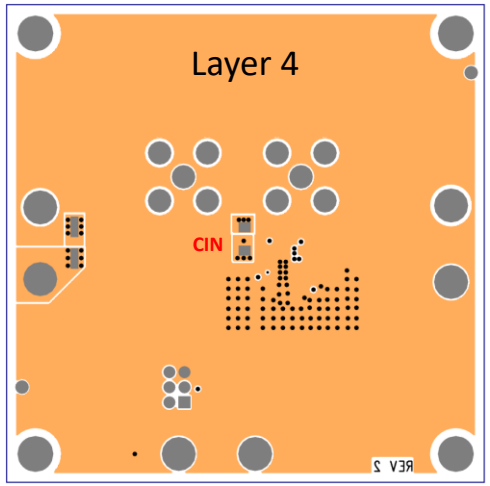
- LDO intelligently controls upstream switching regulator to regulate the LDO's differential voltage ($V_{IN} – V_{OUT}$) to either a constant voltage or an adaptive voltage as a function of I_{LOAD}

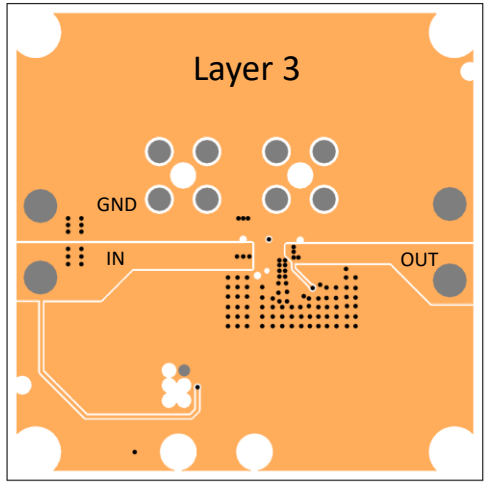
- Optimizes voltage differential for PSRR and transient response performance as well as power dissipation

- Minimizes the switching regulator's output capacitance



LT3045-1 Rev 1 Demo Board: 4.7uF CIN on Backside, Non-Optimized PCB Layout



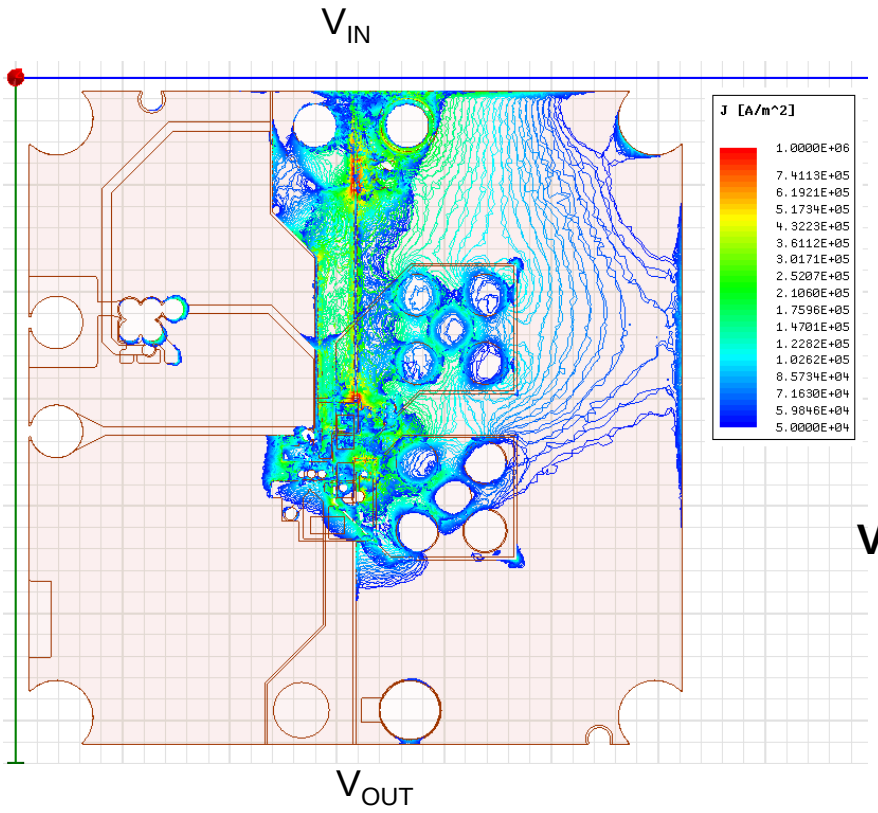


Time Scale: 1us/div

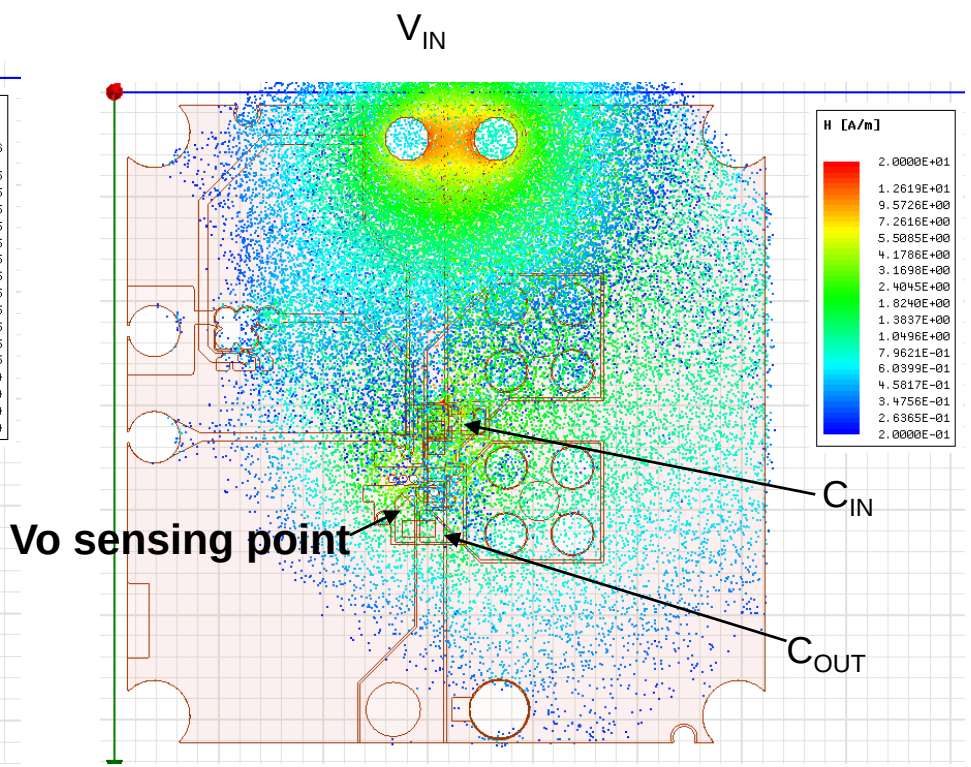
Only 51dB Rejection at 1MHz, way below the LT3045's 76dB capability!

LT3045-1 Rev 1 Demo Board Maxwell FEA Simulation Results*

100mA 1MHz AC current injection as I_{IN}



High current crowding along input and return path of input current

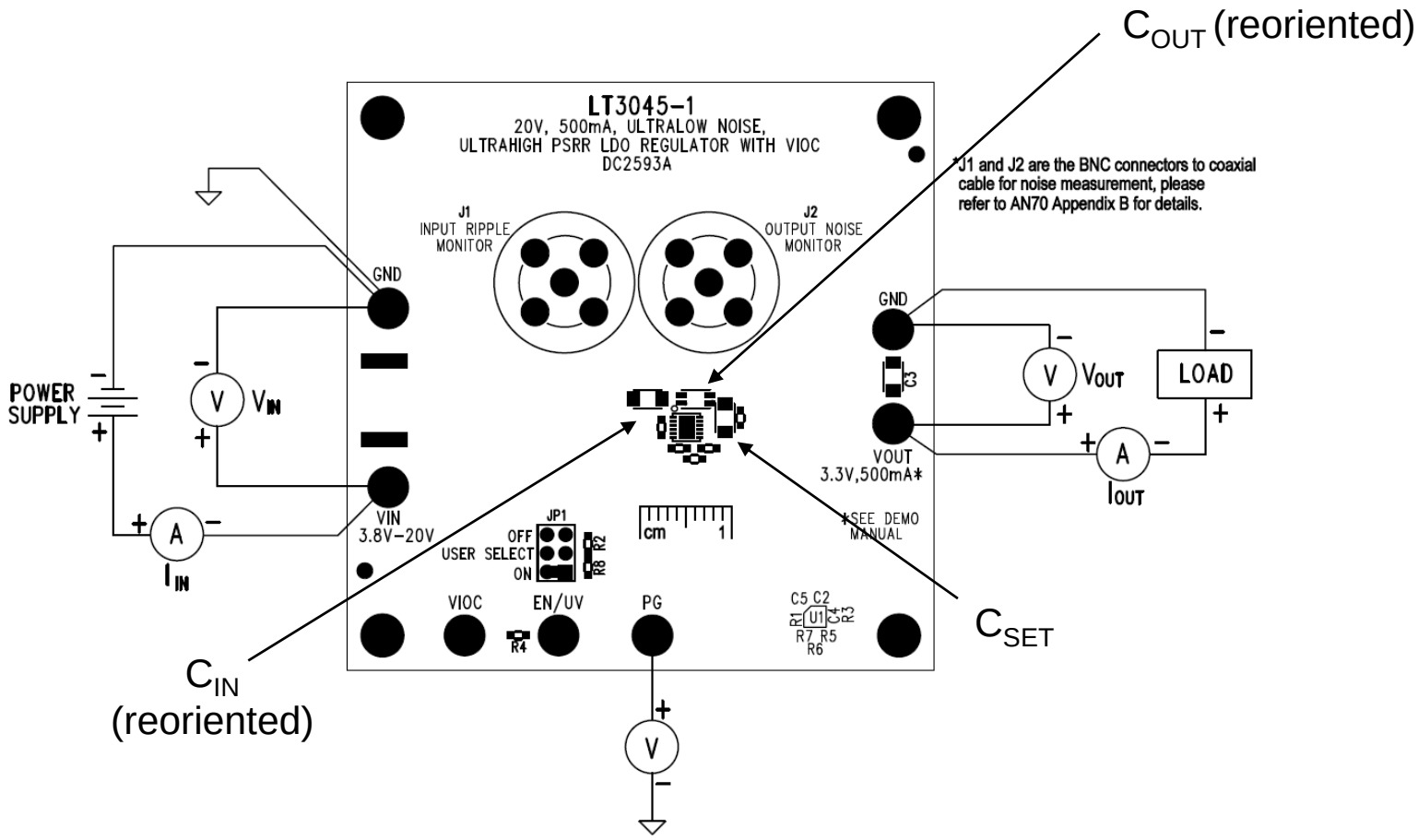


Huge flux around Vo sensing point!

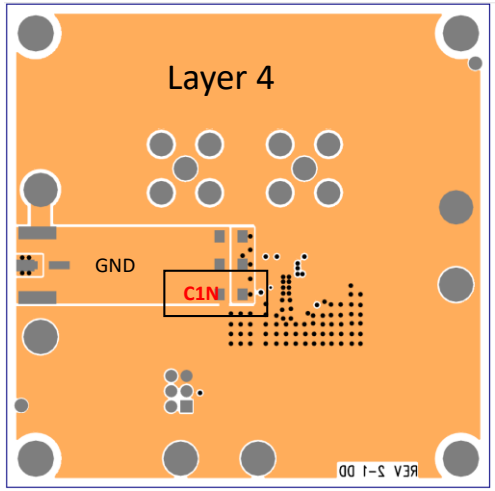
Magnetic coupling from Input to Output significantly degrades PSRR performance

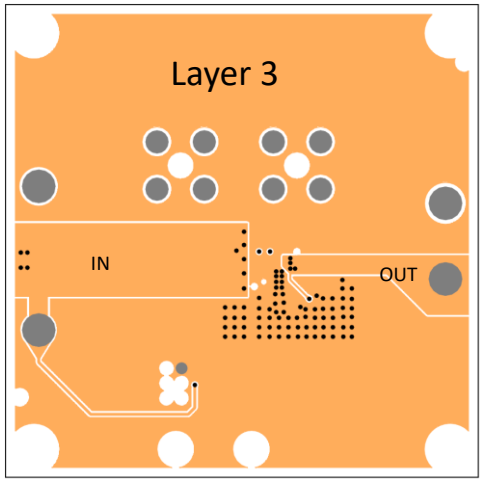
*FEA = Finite Element Analysis

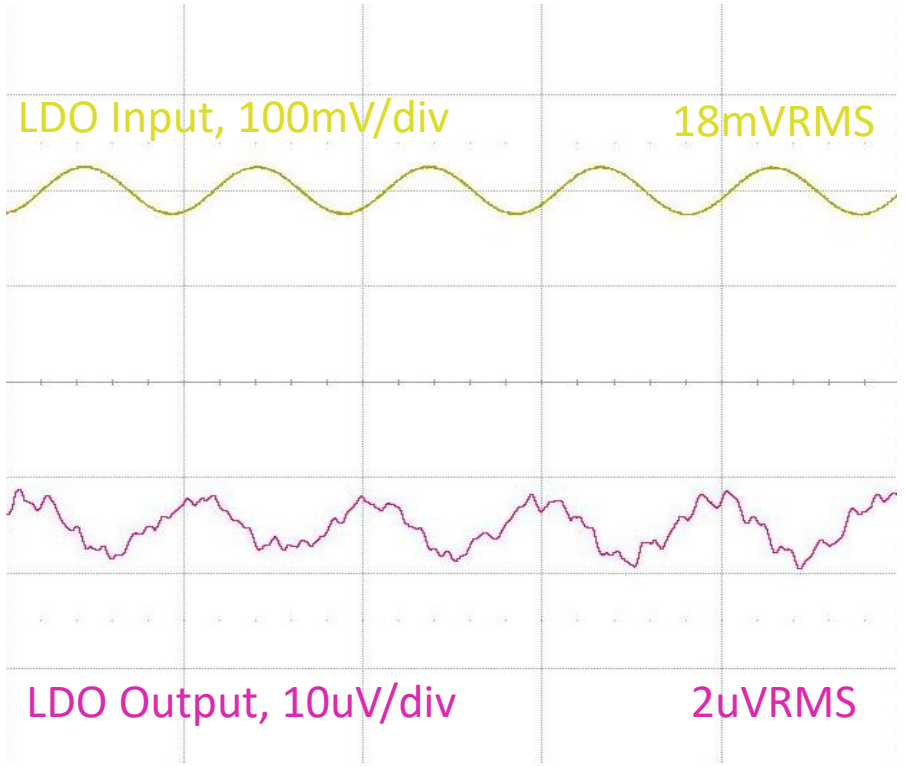
LT3045-1 Final Demo Board Top Silk Screen



LT3045-1 Final Demo Board Test Results: 4.7uF CIN on Back, Optimized PCB Layout





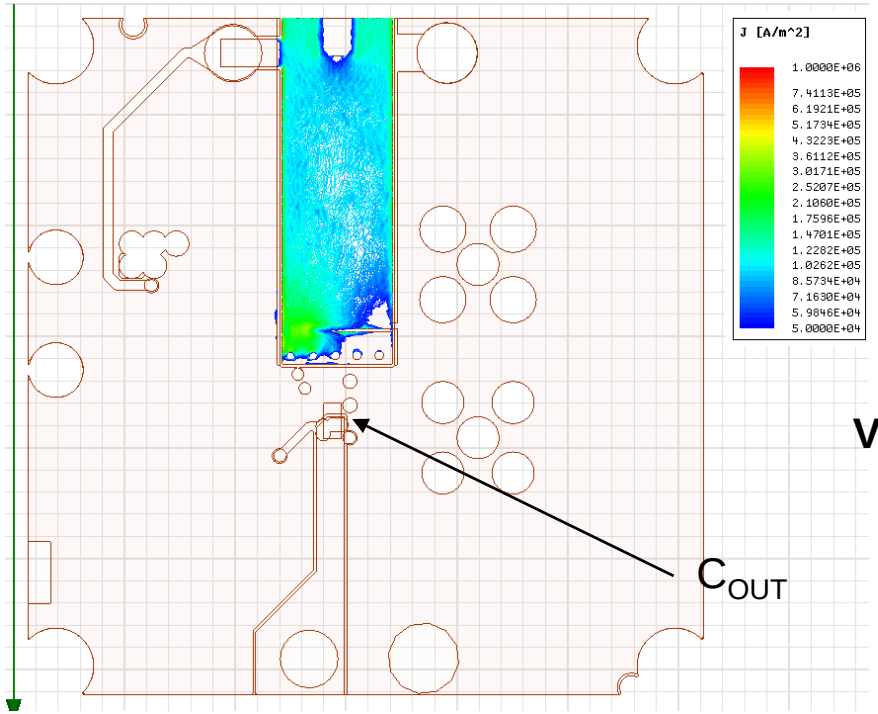


Time Scale: 1us/div

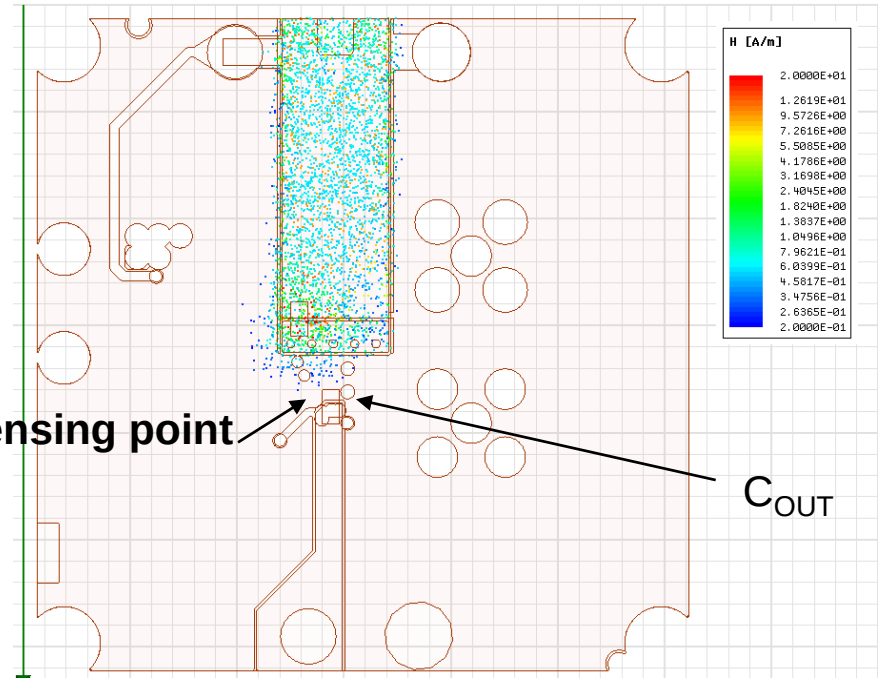
Now 76dB PSRR is Obtained
Yay! But Why?

Maxwell FEA Simulations: LT3045-1 Final Demo Board Analysis

100mA 1MHz AC current injection as I_{IN}



Input and return path of input current exactly overlap each other (CIN reoriented)



Nearly no flux around COUT and Vo sensing point (COUT reoriented)!

Magnetic Coupling from Input to Output is practically eliminated

Appendix

Ultralow Noise RF Linear Regulators

Part Number	I_{OUT} (A)	Noise, 10Hz to 100kHz, typ (μV_{RMS})	Typ PSRR @ 1MHz, (dB)	1k Price	Pkg (mm)	Noise Density, 10kHz (nV/√Hz)	V_{IN} (V), V_{OUT} Range
LT3042	0.2	0.8	79	$2.25	3x3 DFN-10, MSOP-10E	2	1.8 to **20**, 0 to 15
LT3045/-1	0.5	0.8	76	$2.80	3x3 DFN-10, MSOP-12E	2	1.8 to **20**, 0 to 15
ADM7154/ ADM7155	0.6	1.6	58 57	$2.14	3x3 LFCSP-8, SO-8	1.5	2.3 to 5.5 1.2 to 3.3 fixed /1.2 to 3.4 adj
ADM7150/ ADM7151	0.8	1.6	>60	$3.64	3x3 LFCSP-8, SO-8	1.7	4.5 to **16,** 1.8 to 5 fixed / 1.5 to 5.1 adj
ADP7156/ ADP7157	1.2	1.6	60 55	$2.69	3x3 LFCSP-10, SO-8	1.7	2.3 to 5.5 1.2 to 3.3 fixed / 1.2 to 3.3 adj
ADP7158/ ADP7159	2	1.6	50 45	$3.05	3x3 LFCSP-10, SO-8	1.7	2.3 to 5.5 1.2 to 3.3 fixed / 1.2 to 3.3 adj

Very Low Input Voltage, Low Noise LDOs

Part Number	I_{OUT} (A)	V_{IN} (V)	RMS Noise (µVrms)*	Package Options	1k Price Range	Key Features	Notes
ADP1761	1	1.1 to 1.98	12	3x3 LFCSP-16	$3.09	Ultralow noise (indep of V_{OUT}), 30mV to 85mV dropout, Fixed/adj V_{OUT}, PG, SS, REFCAP	Ideal for core and I/O power supplies, FPGA transceiver power & high performance, low noise power (HS ADC/DAC, RF, ASICs, etc.)
ADP1762	2	1.1 to 1.98	12	3x3 LFCSP-16	$3.49		
ADM7170/1/2	0.5, 1, 2	2.3 to 6.5	6	3x3 LFCSP-8	$0.88, $1.19, $1.79	Low noise (indep of V_{OUT}), SS, Ultra fast transient, QOD	
ADP1763	3	1.1 to 1.98	12	3x3 LFCSP-16	$3.99	Ultralow noise (indep of V_{OUT}), 30mV to 85mV dropout, Fixed/adj V_{OUT}, PG, SS, REFCAP	
ADP1764	4	1.1 to 1.98	3	3x3 LFCSP-16	$5.29		
ADP1765	5	1.1 to 1.98	3	3x3 LFCSP-16	$6.79		
LTC3070/ LTC3071	5	0.95 to 3.0	25	4x5 QFN-28	$4.20	85mV dropout, 0.8V to 1.8V Dig Prog V_{OUT}, Margining (3071)	

*10Hz to 100kHz

LDOs with Ultra Small Chip-Scale Package Options

Part Number	I_{OUT} Range (A)	V_{IN} (V)	RMS Noise (µVrms)	Package Options	1k Price Range	Key Features	Notes
ADP7112, ADP7118	0.05	3.3 to **20**	11	1x1.2 WLCSP, 2x2 LFCSP-6, TSOT-5, SOIC-8	$0.53 to $0.96	SS	20V max V_{IN}
ADP16x to ADP166	0.15	2.2 to 5.5	80	1x1 WLCSP-4, 2x2 LFCSP-6, TSOT-5	$0.34	Ultralow 560nA I_Q, Fixed/Adj V_{OUT}	Low I_Q targets portable applications
ADM7160, ADP150, ADP151	0.15, 0.2	2.2 to 5.5	9	TSOT-5, 2x2 LFCSP-6, 0.8x0.8 WLCSP-4	$0.34, $0.59	Low noise (indep of V_{OUT}), Fixed V_{OUT}	Low-noise performance for many signal-chain applications
ADP12x to ADP125	0.15 to 0.5	2.3 to 5.5	25~40	TSOT-5, 2x2 LFCSP-6, 0.8x0.8 WLCSP-4	$0.28 to $0.42	Fixed/Adj V_{OUT}	General purpose
ADP170/1/2	0.3	1.6 to 3.6	30	TSOT-5, WLCSP-4	$0.32, $0.34	Fixed/Adj V_{OUT}, wider V_{OUT} range	General purpose
ADP220 to ADP225	0.2 to 0.3	2.5 to 5.5	27	1x1.5 WLCSP, 2x2 LFCSP-8	$0.49, $0.58	Fixed/Adj V_{OUT}	General purpose

*10Hz to 100kHz

ANALOG DEVICES

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