



Title	<i>Reference Design Report for a 30 W Power Supply Using InnoSwitch™ 3-AQ INN3977CQ</i>
Specification	30 VDC – 550 VDC Input; 30 VDC – 12 V / 0.85 A; 60 VDC – 12 V / 1.25 A; 130-550 VDC – 12 V / 2.5 A Outputs
Application	Wide Input Range For Automotive
Author	Applications Engineering Department
Document Number	RDR-840Q
Date	August 31, 2020
Revision	1.3

Summary and Features

- Wide input voltage range: 30 VDC to 550 VDC
- InnoSwitch3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >85% efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
 - Insensitive to transformer variation
 - Extremely fast transient response independent of load timing

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.

Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

1	Introduction	4
2	Power Supply Specification	5
3	Schematic	6
3.1	SR FET Version	6
3.2	Qspeed Diode Version	6
4	Circuit Description	7
4.1	INN3977CQ IC Primary	7
4.2	INN3977CQ IC Secondary	7
5	PCB Layout	8
6	Bill of Materials	10
6.1	Main Board	10
6.2	Mechanical Parts	11
7	Transformer Design	12
7.1	Electrical Diagram	12
7.2	Electrical Specifications	12
7.3	Material List	12
7.4	Transformer Build Diagram	13
7.5	Transformer Instructions	13
7.6	Winding Illustrations	14
8	Performance Data with SR FET version	20
8.1	Average Efficiency	20
8.1.1	30 VDC, 12 V 0.85 A (10 W)	20
8.1.2	60 VDC, 12 V 1.25 A (15 W)	21
8.1.3	130 VDC, 12 V 2.5 A (30 W)	22
8.1.4	400 VDC, 12 V 2.5 A (30 W)	23
8.1.5	550 VDC, 12 V 2.5 A (30 W)	24
8.2	Efficiency vs. Load and Line	25
8.2.1	SR FET Version	25
8.2.2	Qspeed Version	26
8.3	No-Load Input Power	27
8.4	Load and Line Regulation	28
8.5	CV/CC	29
9	Waveforms	30
9.1	Switching Waveforms	30
9.1.1	Drain Voltage and Current, Steady-State.	30
9.1.2	Drain Voltage and Current, Start-up.	32
9.1.3	SR FET Waveforms, Steady-State	34
9.1.4	SR FET Waveforms, Start-up.	36
9.1.5	FWD Pin, Steady-State	38
9.1.6	FWD Pin, Start-up	40
9.1.7	Output Voltage and Current, Startup CR Load	42
9.2	Output Ripple Measurements (SR FET)	44
9.2.1	Ripple Measurement Technique	44



9.2.2	100% Loading Condition	45
9.2.3	75% Loading Condition	47
9.2.4	50% Loading Condition	49
9.2.5	25% Loading Condition	51
9.2.6	0% Loading Condition	53
9.3	<i>Output Ripple Measurements (Qspeed Diode)</i>	<i>55</i>
9.3.1	100% Loading Condition	55
9.3.2	75% Loading Condition	56
9.3.3	50% Loading Condition	57
9.3.4	25% Loading Condition	58
9.3.5	0% Loading Condition	59
9.4	<i>Output Load Transient</i>	<i>60</i>
9.4.1	Output Load Transient, 100% to 50% Load	60
9.4.2	Output Load Transient, 100% to 0% Load	62
9.5	<i>Output Short-Circuit Auto-Restart Test</i>	<i>64</i>
10	Thermal Performance (SR FET)	66
10.1	<i>INN3977CQ Temperature Rise vs. Output Power</i>	<i>68</i>
12	Thermal Performance (Qspeed Diode)	69
13	-40 °C and +85 °C operational test	71
15	Revision History	72

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 30 VDC to 550 VDC input, 12 V output, 30 W Power Supply utilizing INN3977CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

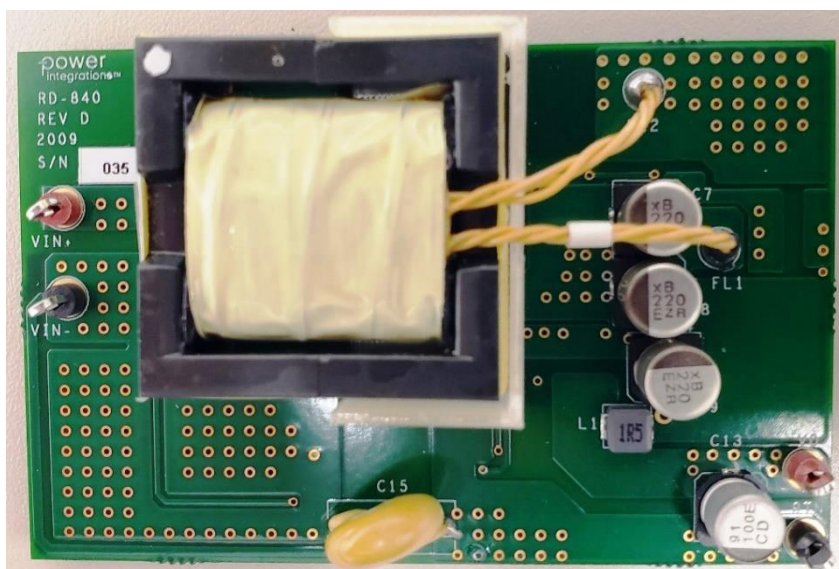


Figure 1 – Populated Circuit Board Photograph, Top.

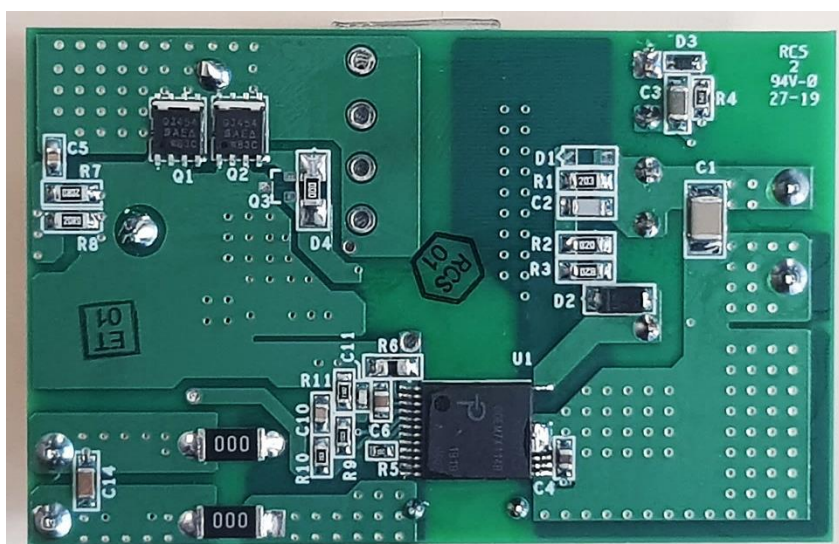


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	30	400	550	VDC	For Electric Vehicle Emergency PSU.
No-load Input Power (400VDC)				50	mW	@ 400 VDC.
Output						
Output Voltage	V_{OUT}		12		V	±5%
Output Current	I_{OUT}		2.33		A	
Output Ripple Voltage	V_{RIPPLE}			240	mV	On Board.
Total Output Power						
Continuous Output Power	P_{OUT}			30	W	V_{IN} 130 VDC to 550 VDC.
Continuous Output Power	P_{OUT}			15	W	V_{IN} of 60 VDC to 130 VDC.
Continuous Output Power	P_{OUT}			10	W	V_{IN} of 30 VDC to 60 VDC.
Isolation		Meets IEC 60664-1 as a minimum. Reinforce better				
Ambient Temperature	T_{AMB}	-40		85	°C	Inside Inverter.

3 Schematic

3.1 SR FET Version

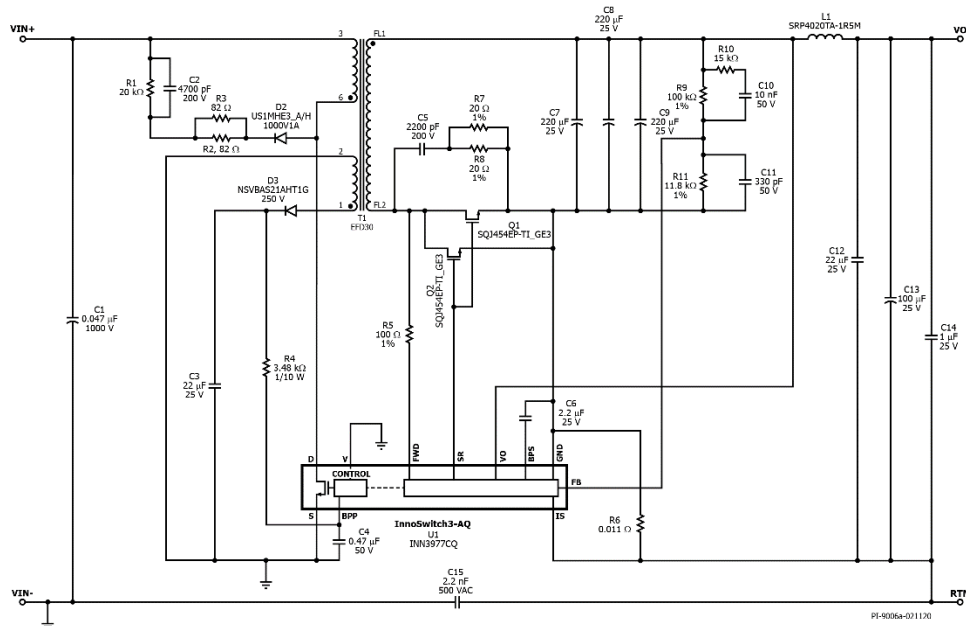


Figure 3 – Schematic with SR FET.

3.2 Qspeed Diode Version

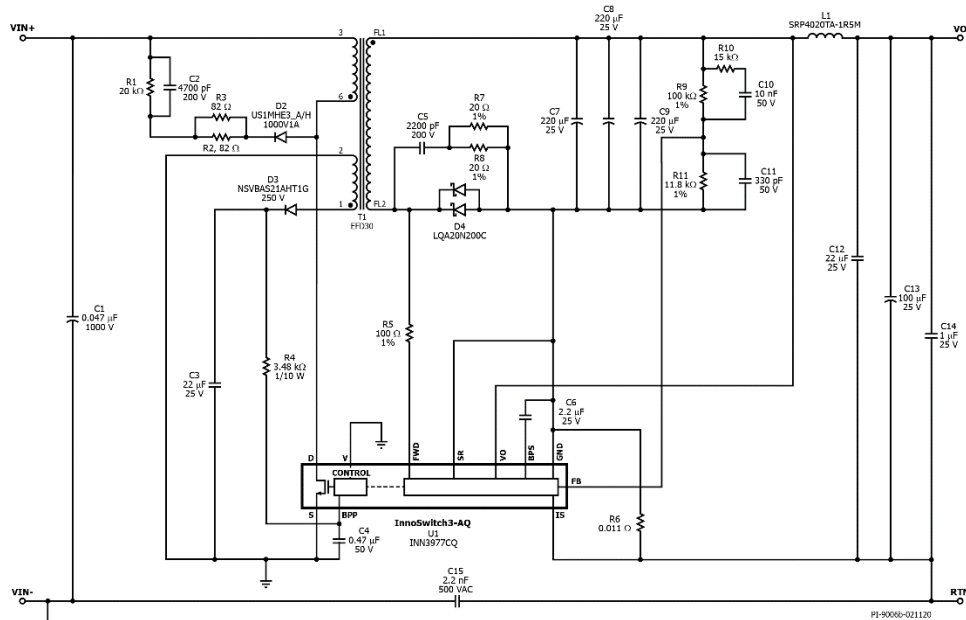


Figure 4 – Schematic with Qspeed Diode.

4 Circuit Description

4.1 *INN3977CQ IC Primary*

One end of the transformer primary is connected to the DC bus, the other is connected to the integrated power MOSFET inside the INN3977CQ IC (U1). High-voltage ceramic capacitor C1 is used for the decoupling capacitor for the DC input voltage, and a low cost RCD clamp formed by D2, R1, R2, R3, and C2 limits the peak Drain voltage due to the effects of transformer leakage inductance. Capacitor C15, Y capacitor, is used to attenuate the high frequency common mode noise on the output.

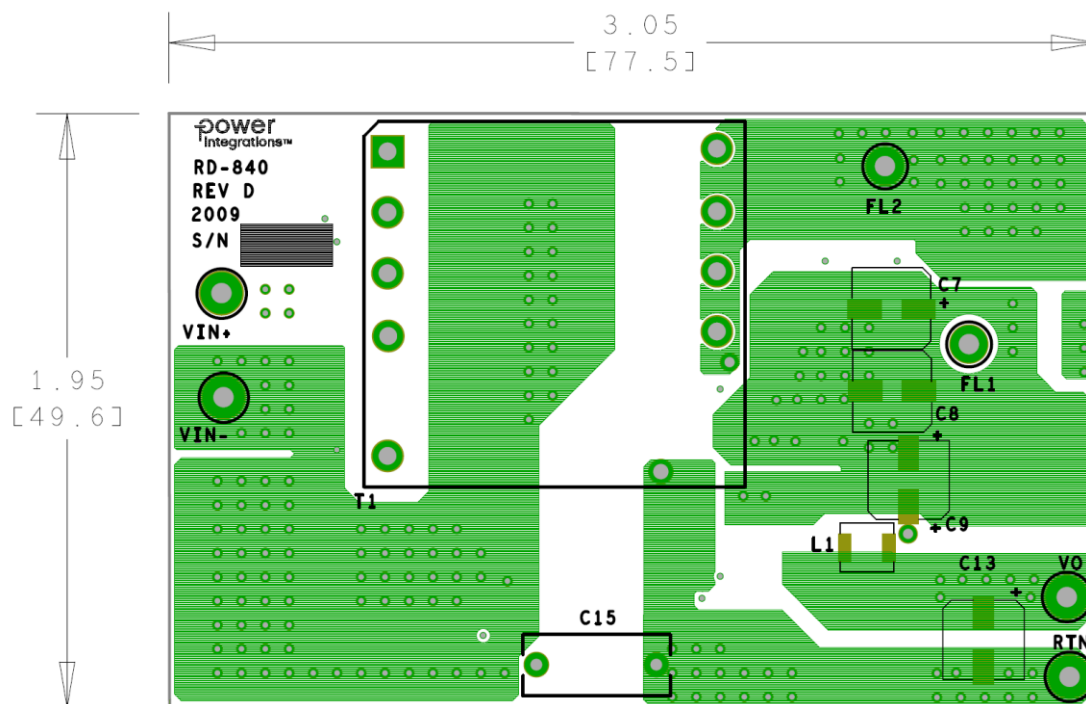
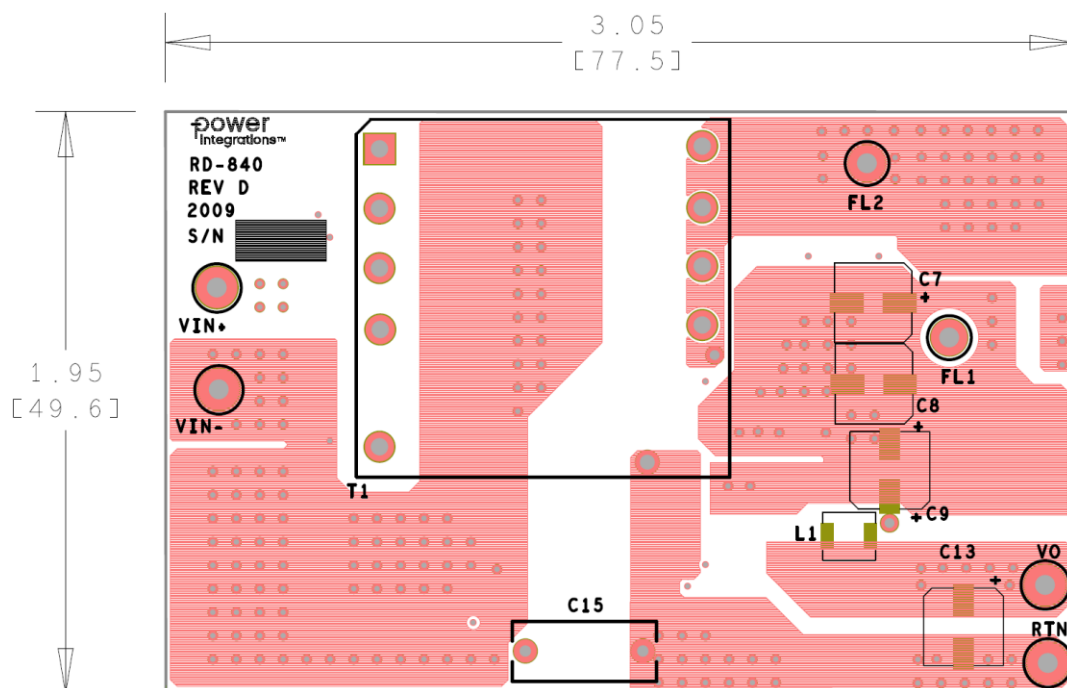
The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D3 and capacitor C3, and fed in the BPP pin via a current limiting resistor R4.

4.2 *INN3977CQ IC Secondary*

The secondary-side of the INN3977CQ IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 12 V output is provided by SR FETs Q1 and Q2. Low ESR capacitors, C7, C8, C9, C12, C13 and output inductor L1 provide filtering. Ceramic capacitor C15 attenuates high frequency noise on the output. RC snubber network comprising R7, R8 and C5 for Q1 and Q2 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R5 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin. It will charge the decoupling capacitor C6 via an internal regulator.

Resistors R9 and R11 form a voltage divider network that senses the output voltage. INN3977CQ IC has an internal reference of 1.265 V. Capacitor C11 provides decoupling from high frequency noise affecting power supply operation, and C10 and R10 is the feedforward networks to speed up the response time to lower the output ripple. The output current is sensed by R6 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

**Figure 7 – Printed Circuit Board Layout (Internal layer 1).****Figure 8 – Printed Circuit Board Layout (Internal layer 2).**

6 Bill of Materials

6.1 Main Board

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	0.047 μ F, $\pm$ 10%, 1000V (1kV), Ceramic, X7R, Automotive, AEC-Q200, 1812	1812Y1K00473KST	Knowles Syfer
2	1	C2	100 pF, $\pm$ 5%, 200 V, Ceramic, C0G/NP0, Automotive, AEC-Q200, 1206	CGJ5H3C0G2D472J115AA	TDK
3	1	C3	22 μ F, $\pm$ 20%, 25V, Ceramic, X5R, Automotive, AEC-Q200, 1206	12063D226MAT2A	AVX
4	1	C4	0.47 μ F, $\pm$ 10%, 50 V, Ceramic, X7R, AEC-Q200, Automotive, 0805, -55°C ~ 125°C	CGA4J3X7R1H474K125AB	TDK
5	1	C5	2200 pF, $\pm$ 10%, 200V, Ceramic, X7R, Automotive, AEC-Q200, 0805	08052C222K4T2A	AVX
6	1	C6	2.2 μ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
7	3	C7 C8 C9	220 μ F, 25 V, Electrolytic, Automotive, AEC-Q200, 0.260" L x 0.260" W (6.60 mm x 6.60 mm) x 0.315" H (8.00 mm), SMD	EMZR250ARA221MF80G	United Chemi-Con
8	1	C10	10 nF, 50 V, Ceramic, X7R, Automotive, AEC-Q200, 0805	C0805C103K5RACTU	Kemet
9	1	C11	330 pF, $\pm$ 5%, 50V, Ceramic, C0G, NP0, Automotive, AEC-Q200, 0603 (1608 Metric)	C0603C331J5GACAUTO	KEMET
10	1	C12	22 μ F, 25 V, Ceramic, X7R, 1210	GRM32ER71E226KE15L	Murata
11	1	C13	100 μ F, $\pm$ 20%, 25 V, Z=320 m Ω , Electrolytic, Automotive, AEC-Q200, 0.260" L x 0.260" W (6.60 mm x 6.60 mm) x 0.315" H (8.00mm), SMD	UCD1E101MCL1GS	Nichicon
12	1	C14	1 μ F, $\pm$ 10%, 25V, X7R, 1206, 1206 (3216 Metric)	C1206C105K3RACAUTO	Kemet
13	1	C15	CAP, CER, 2200pF, $\pm$ 20%, 760 VAC, Safety, Automotive, AEC-Q200, X1, Y1, Radial, Disc	AY1222M47Y5UC63L0	Vishay
14	1	D2	DIODE, GEN PURP, 1000V, 1A, Automotive, AEC-Q101, DO214AC, DO-214AC (SMA)	US1MHE3_A/H	Vishay
15	1	D3	Diode, General Purpose, 250 V, 200 mA, Automotive, AEC-Q101, SC-76, SOD-323	NSVBAS21AHT1G	ON Semi
16	2	FL1 FL2	Flying Lead, Hole size 70mils	N/A	N/A
17	1	L1	1.5 μ H, $\pm$ 20%, Shielded, Wirewound, Inductor, 4.5A, 42mOhm Max, Automotive, AEC-Q200, 2-SMD	SRP4020TA-1R5M	Bourns
18	2	Q1 Q2	MOSFET, N-Channel, 200 V, 13 A (Tc), 68 W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8, PowerPAK SO-8	SQJ454EP-T1_GE3	Vishay
19	1	R1	RES, 20 k Ω , 5%, 1/4 W, Automotive, AEC-Q200, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
20	2	R2 R3	RES, 82 Ω , 5%, 1/4 W, Automotive, AEC-Q200, Thick Film, 1206	ERJ-8GEYJ820V	Panasonic
21	1	R4	RES, 3.48 k Ω , 1%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805	ERJ-6ENF3481V	Panasonic
22	1	R5	RES, SMD, 100 Ω , 1%, 1/10W, $\pm$ 100ppm/ $^{\circ}$ C, -55°C ~ 155°C, 0603, Moisture Resistant, Thick Film	RC0603FR-07100RL	Yageo
23	1	R6	0.011 Ω , $\pm$ 1%, $\pm$ 75ppm/ $^{\circ}$ C, 1W, 1206, Automotive AEC-Q200, Current Sense, -55°C ~ 155°C	ERJ-8CWF011V	Panasonic
24	2	R7 R8	RES, 20 Ω , 1%, 1/4 W, Automotive, AEC-Q200, Thick Film, 1206	ERJ-8ENF20R0V	Panasonic
25	1	R9	RES, 100 k Ω , 1%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
26	1	R10	RES, 15 k Ω , 5%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
27	1	R11	RES, 11.8 k Ω , 1%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
28	1	T1	Bobbin, EFD30, Horizontal, 12 pins	B66424-B1012-D1	Epcos
29	1	U1	InnoSwitch3-AQ InSOP24D	INN3977CQ	Power Integrations



6.2 Mechanical Parts

Item	Qty	Ref Des	Value	Description	Mfg Part Number	Mfg	PI Part Number
30	2	RTN, VIN-	BLK	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone	35-00042-00
31	2	VIN+, VO	RED	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone	35-00043-00

7 Transformer Design

7.1 Electrical Diagram

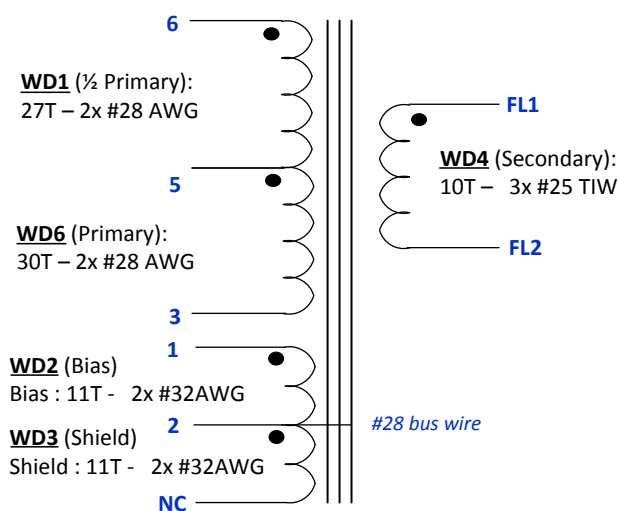


Figure 9 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 3 and 6, with all other windings open.	950 μ H $\pm$ 5%
Resonant Frequency	Between pin 3 and 6, other windings open	1,100 kHz (Min.)
Primary Leakage Inductance	Between pin 3 and 6, with pins:FL1-FL2 shorted	4.5 μ H (Max.)

7.3 Material List

Item	Description
[1]	Core: Ferroxcube-EFD30-3F3, PI#:99-00068-00.
[2]	Bobbin: EFD30-Hor-12pins (6/6), Thru Hole; PI#: 25-00026-00.
[3]	Cover: PI#: 61-00267-00.
[4]	Magnet Wire: #28 AWG, Double Coated.
[5]	Magnet Wire: #32 AWG, Double Coated.
[6]	Magnet Wire: #25 AWG, Triple Insulated Wire.
[7]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 20.4 mm Width.
[9]	Epoxy: Devcon, 5 mins Epoxy, Mfr#: 14270; or Equivalent.
[10]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

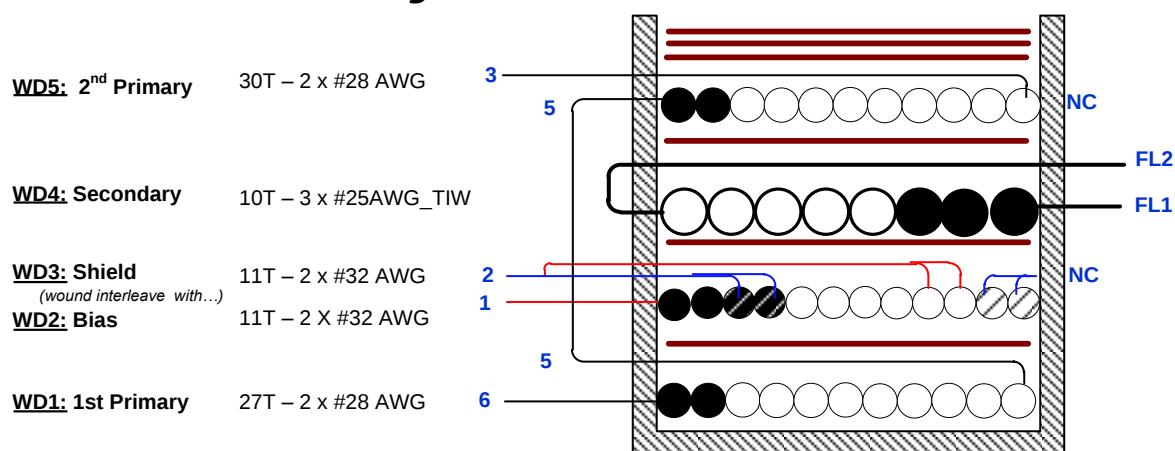
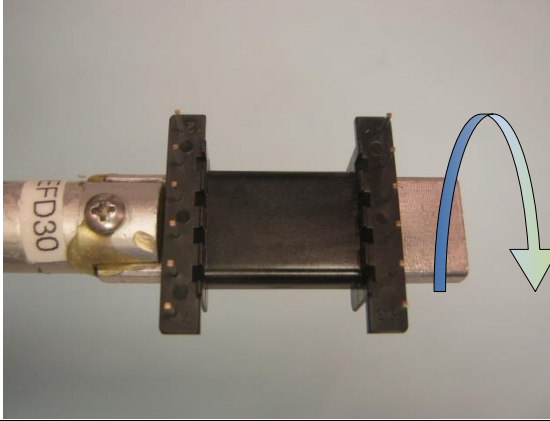
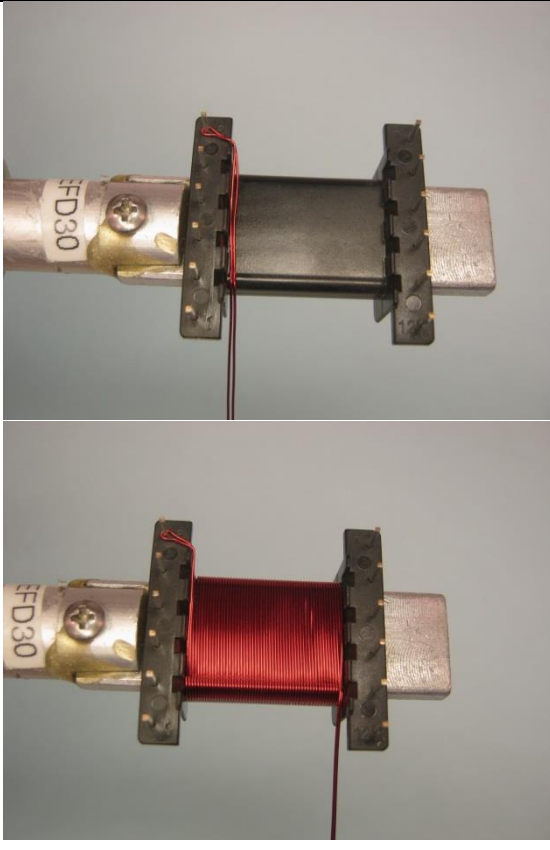


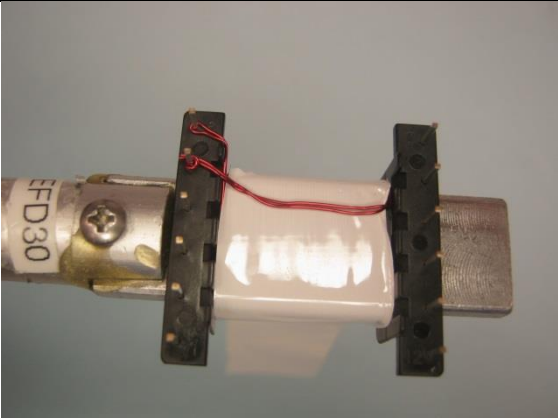
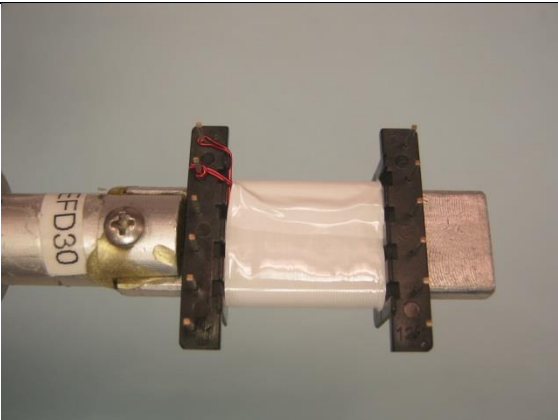
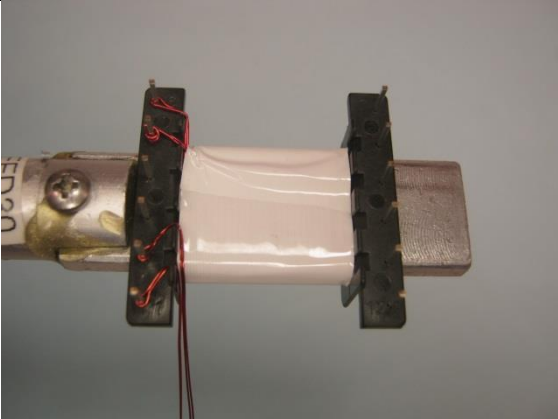
Figure 10 – Transformer Build Diagram.

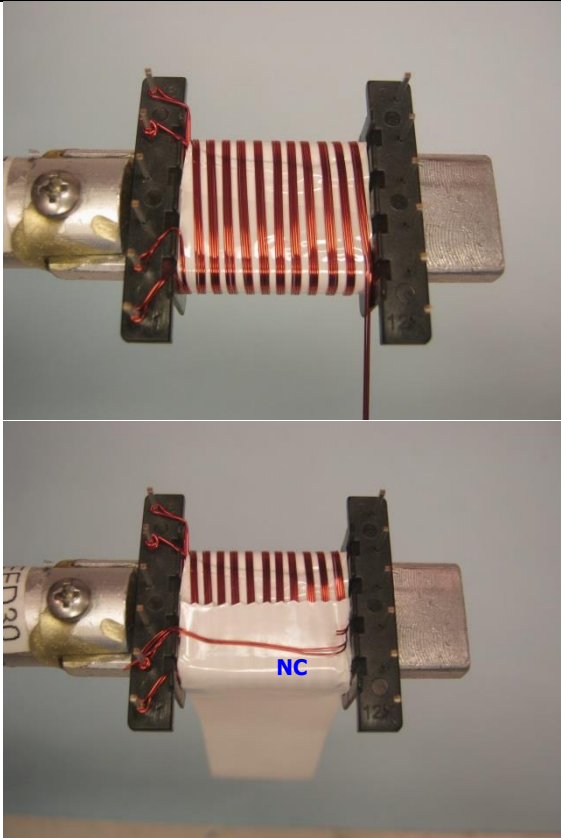
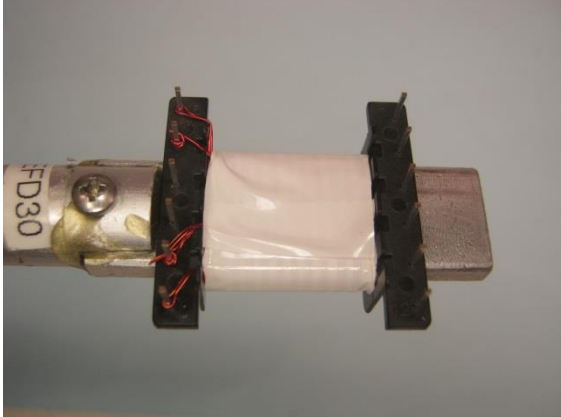
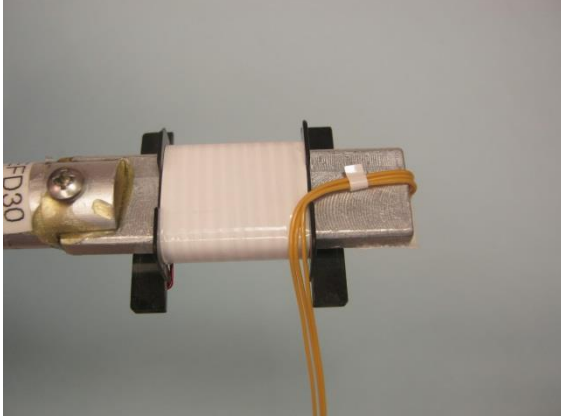
7.5 Transformer Instructions

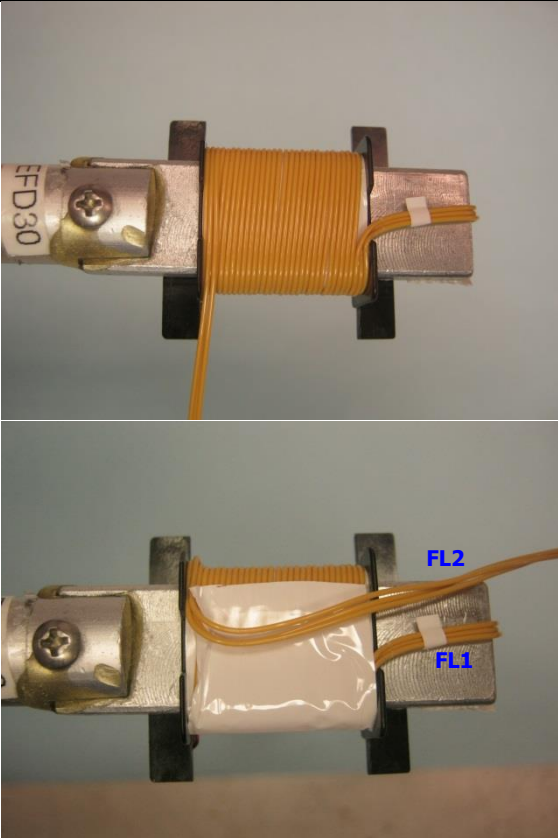
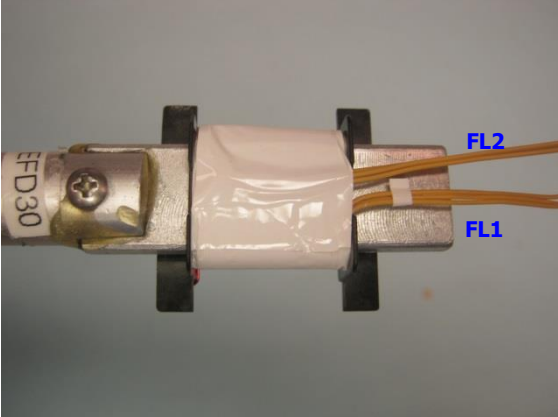
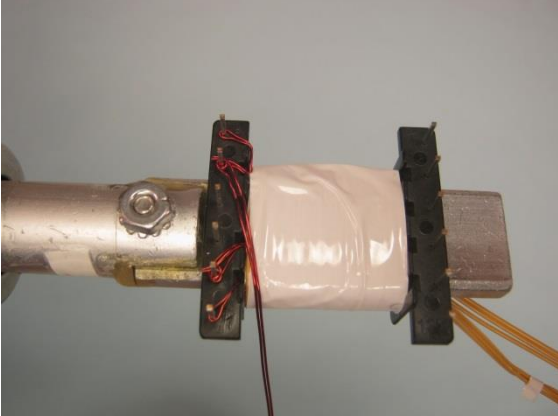
Winding Preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 6, wind 27 bifilar turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 5.
Insulation	1 layer of tape Item [8].
WD2: Bias & WD3: Shield	Use 2 wires Item [5] start at pin 1 for Bias winding, also use 2 wires same Item [5] start at pin 2 for Shield winding. Wind all 4 wires in parallel, at the 11 th turn: - bring 2 wires for Bias winding to the left and terminate at pin 2, - cut short 2 wires for Shield Winding as No-Connect.
Insulation	1 layer of tape Item [8].
WD4 Secondary	Start at right slot of secondary side on the top of bobbin, use 3 wires Item [6], leaving ~ 50.0mm floating, and mark as FL1. Wind 10 turns in 1 layer, from right to left, at the last turn bring the wires back to the right, also leaving ~ 50.0mm floating, and mark FL2.
Insulation	1 layer of tape Item [8].
WD5 2nd Primary	Start at pin 5, wind 27 tri-filar turns of wire Item [4], from left to right for the 1 st layer. Continue winding 3 more turns for the 2 nd layer, spreading from right to left and terminate at pin 3.
Insulation	2 layers of tape Item [8] to secure the windings.
Finish	Gap core halves to get 950 uH. Use 70mm of bus wire Item [7], solder to pin 2 then lean along core halves and secure with tape. Remove all secondary pins and cut short pin 5. Varnish with Item [11]. Place 2 beads of epoxy Item [9] at right and left, inside the cover Item [3]. Insert secondary side of the transformer into cover Item [3].

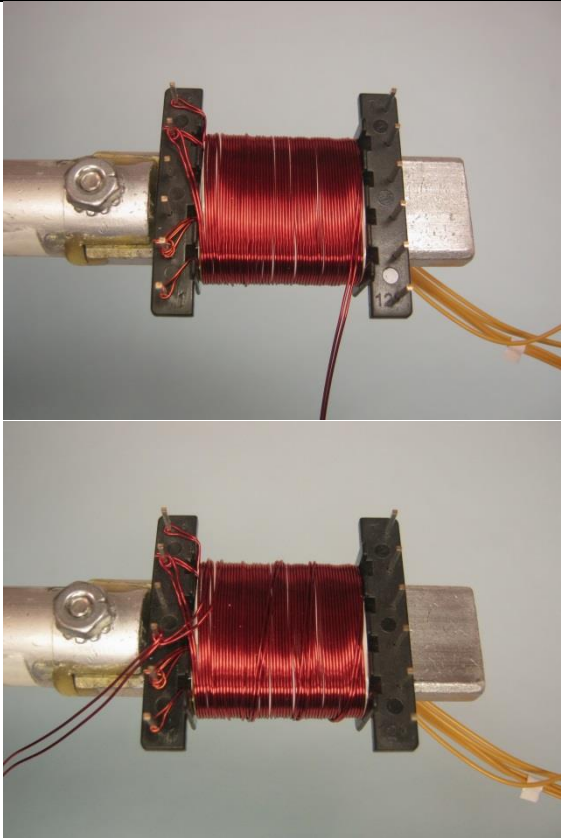
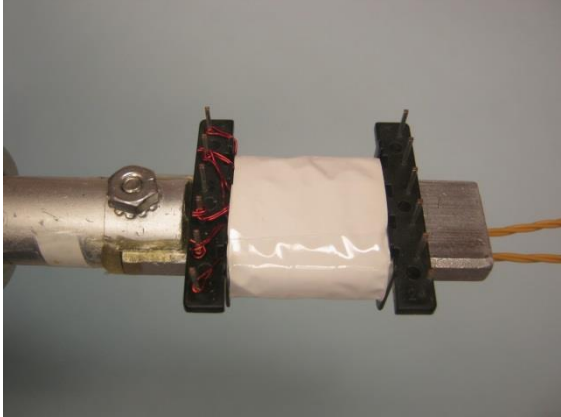
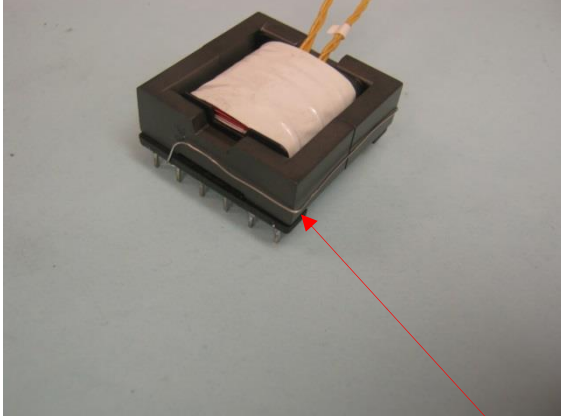
7.6 *Winding Illustrations*

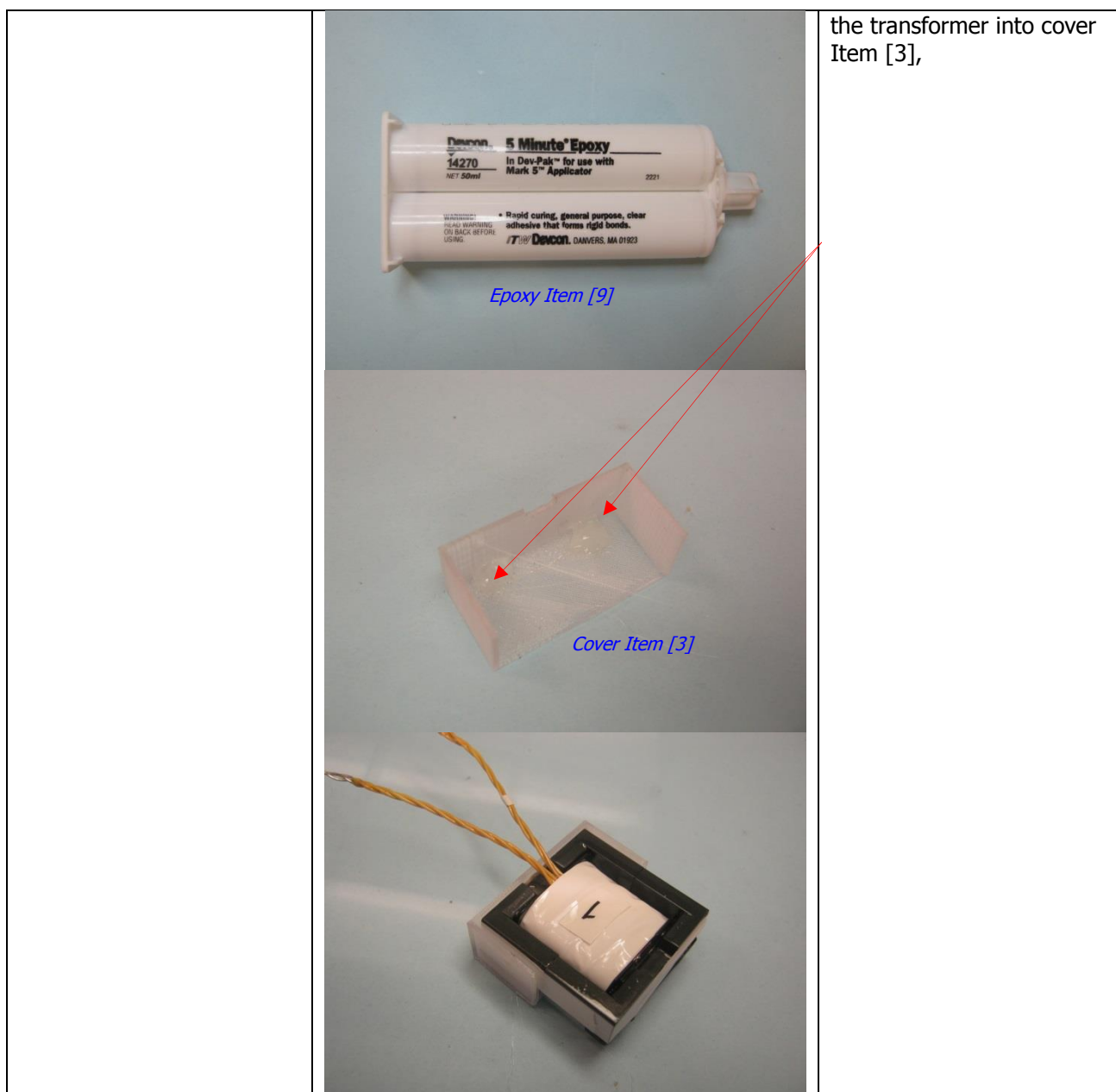
Winding Preparation	 A photograph of a bobbin assembly mounted on a metal mandrel. The bobbin is black with two copper-colored end plates. A blue wire is shown entering from the right, and a green arrow indicates a clockwise winding direction.	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction..
WD1 1st Primary	 Two photographs showing the winding process. The top photo shows the start of the winding with a red wire. The bottom photo shows the completed winding, which is a dense, multi-layered coil of red wire.	Start at pin 6, wind 27 bifilar turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 5.

		
Insulation		1 layer of tape Item [8].
WD2: Bias & WD3: Shield		Use 2 wires Item [5] start at pin 1 for Bias winding, also use 2 wires same Item [5] start at pin 2 for Shield winding. Wind all 4 wires in parallel, at the 11th turn: - bring 2 wires for Bias winding to the left and terminate at pin 2, - cut short 2 wires for Shield Winding as No-Connect.

		
Insulation		1 layer of tape Item [8].
WD4 Secondary		Start at right slot of secondary side on the top of bobbin, use 3 wires Item [6], leaving ~ 50.0mm floating, and mark as FL1. Wind 10 turns in 1 layer, from right to left, at the last turn bring the wires back to the right, also leaving ~ 50.0mm floating, and mark FL2.

		
Insulation		1 layer of tape Item [8].
WD5 2nd Primary		Start at pin 5, wind 27 tri-filar turns of wire Item [4], from left to right for the 1 st layer. Continue winding 3 more turns for the 2 nd layer, spreading from right to left and terminate at pin 3.

		
Insulation		2 layers of tape Item [8] to secure the windings.
Finish		Gap core halves to get 950uH. Use 70mm of bus wire Item [7], solder to pin 2 then <u>lean along core halves</u> and secure with tape. Remove all secondary pins and cut short pin 5. Varnish with Item [11]. <u>Place 2 beads of epoxy Item [9]</u> at right and left, inside the cover Item [3]. Insert secondary side of



8 Performance Data with SR FET version

All measurements performed with room ambient temperature. Measured at PCB output terminal.

8.1 *Average Efficiency*

8.1.1 30 VDC, 12 V 0.85 A (10 W)

8.1.1.1 SR FET Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.50	848.56	87.71
75%	11.60	636.59	87.93
50%	11.70	424.63	87.12
25%	11.84	212.31	84.49
10%	11.92	85.06	76.28
		Average	86.69

8.1.1.2 Qspeed Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.58	849.25	83.71
75%	11.68	635.63	83.96
50%	11.78	423.25	82.97
25%	11.91	209.63	79.90
10%	11.99	82.13	71.46
		Average	82.64

8.1.2 60 VDC, 12 V 1.25 A (15 W)

8.1.2.1 SR FET Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.79	1241.88	89.97
75%	11.81	929.38	90.48
50%	11.98	619.06	89.33
25%	11.96	305.94	87.86
10%	11.93	120.00	79.64
		Average	89.40

8.1.2.2 Qspeed Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.84	1250.25	85.65
75%	11.85	936.38	85.66
50%	12.01	623.88	84.86
25%	12.01	310.00	83.35
10%	11.99	122.13	76.00
		Average	84.88

8.1.3 130 VDC, 12 V 2.5 A (30 W)

8.1.3.1 SR FET Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.74	2498.75	88.56
75%	11.92	1873.75	90.63
50%	12.01	1250.00	90.36
25%	12.01	624.06	87.22
10%	11.95	250.00	82.59
		Average	89.19

8.1.3.2 Qspeed Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.77	2504.25	86.14
75%	11.94	1877.50	86.41
50%	12.05	1250.25	87.11
25%	12.04	623.88	84.63
10%	12.01	247.38	80.06
		Average	86.07

8.1.4 400 VDC, 12 V 2.5 A (30 W)

8.1.4.1 SR FET Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.98	2498.75	87.38
75%	12.08	1873.44	87.73
50%	12.07	1250.31	87.13
25%	12.02	624.69	83.36
10%	11.96	250.00	78.25
		Average	86.40

8.1.4.2 Qspeed Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.99	2504.25	87.69
75%	12.04	1877.50	83.91
50%	12.08	1250.25	83.73
25%	12.07	623.88	80.25
10%	12.01	247.38	73.92
		Average	83.89

8.1.5 550 VDC, 12 V 2.5 A (30 W)

8.1.5.1 SR FET Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.97	2504.38	86.30
75%	12.09	1877.50	84.98
50%	12.08	1250.38	83.51
25%	12.04	623.75	79.15
10%	11.99	247.38	72.54
		Average	83.49

8.1.5.2 Qspeed Version

Load	V _{OUT} (V)	I _{OUT} (mA)	Efficiency (%)
100%	11.94	2504.25	81.99
75%	12.09	1877.63	83.83
50%	12.09	1250.25	81.33
25%	12.06	623.75	78.06
10%	12.02	247.38	69.62
		Average	81.30

8.2 Efficiency vs. Load and Line

Measurements taken at 0% to 100% of rated load.

8.2.1 SR FET Version

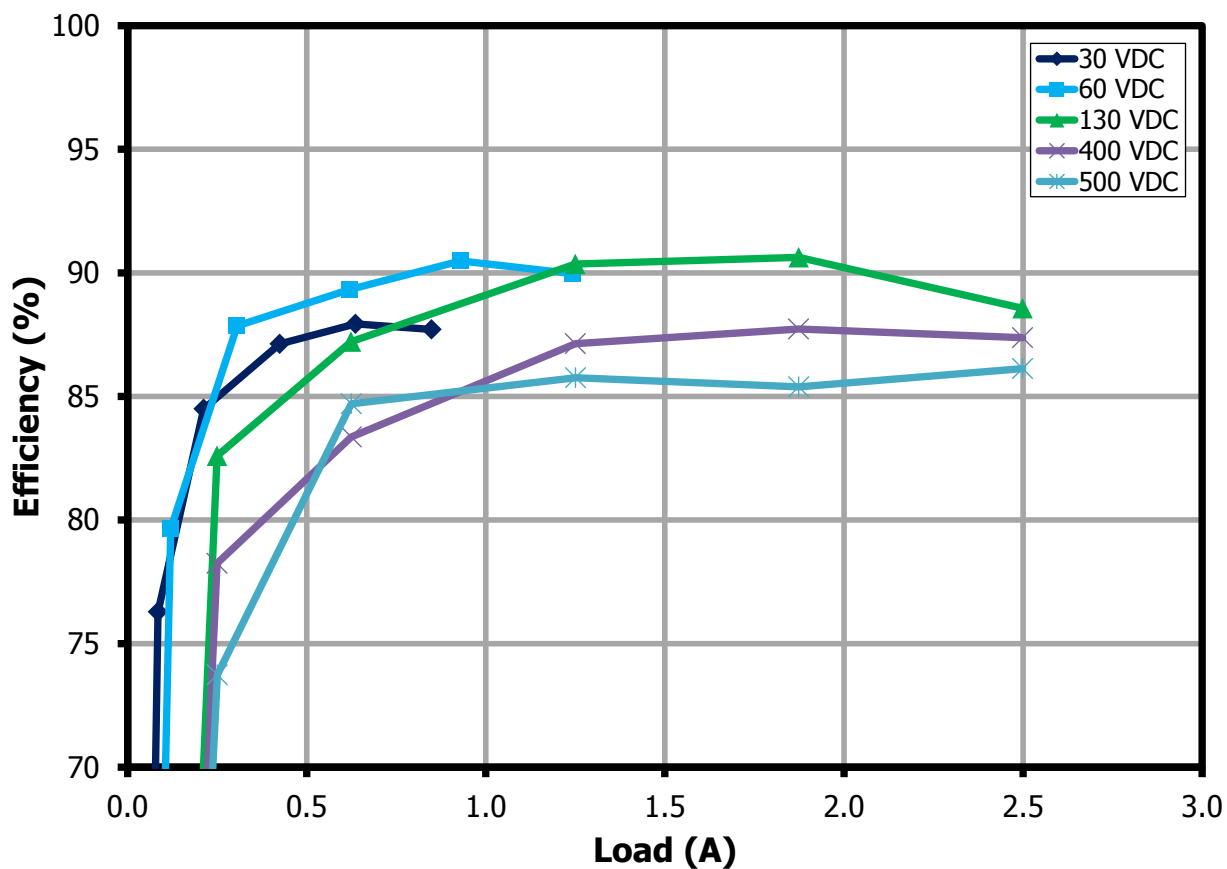


Figure 11 – Efficiency vs. Load and Line (VDC), Room Temperature – SR FET Version.

8.2.2 Qspeed Version

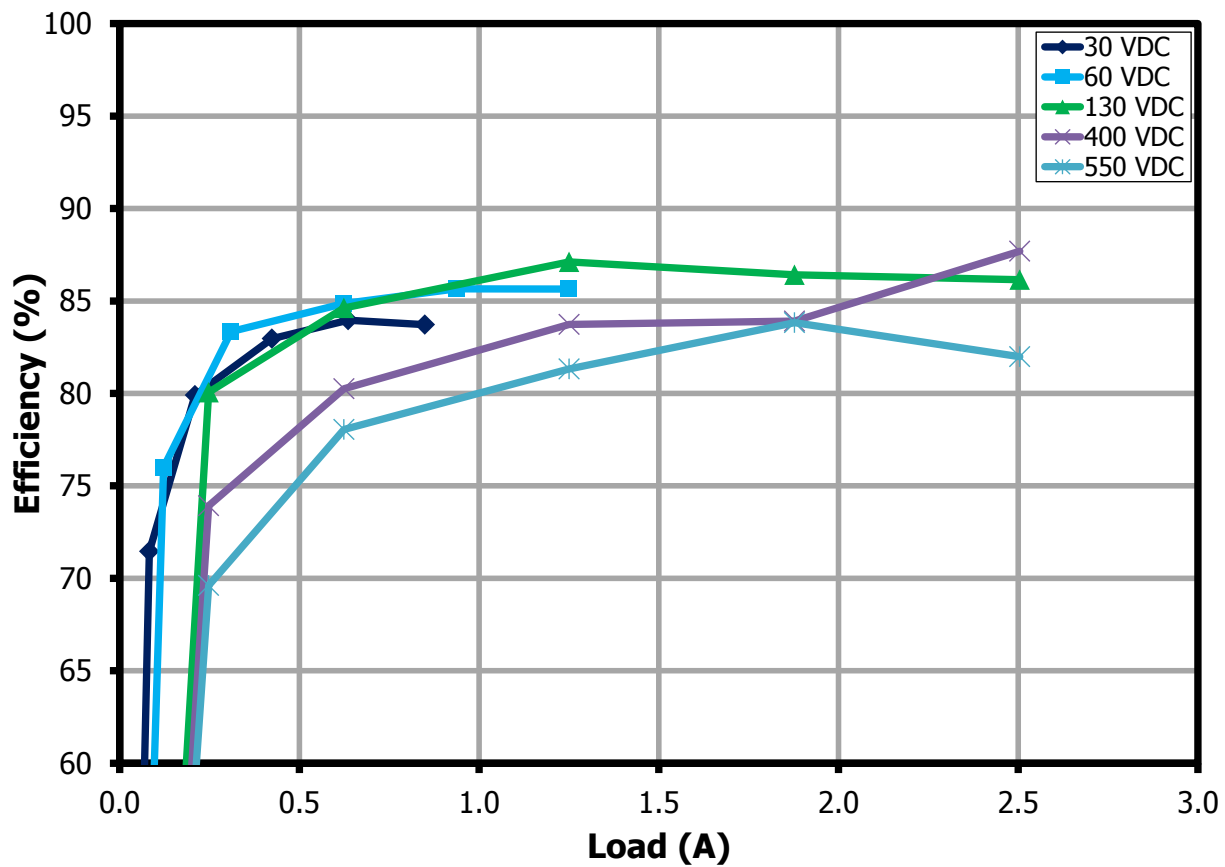


Figure 12 – Efficiency vs. Load and Line (VDC), Room Temperature – Qspeed Version.

8.3 *No-Load Input Power*

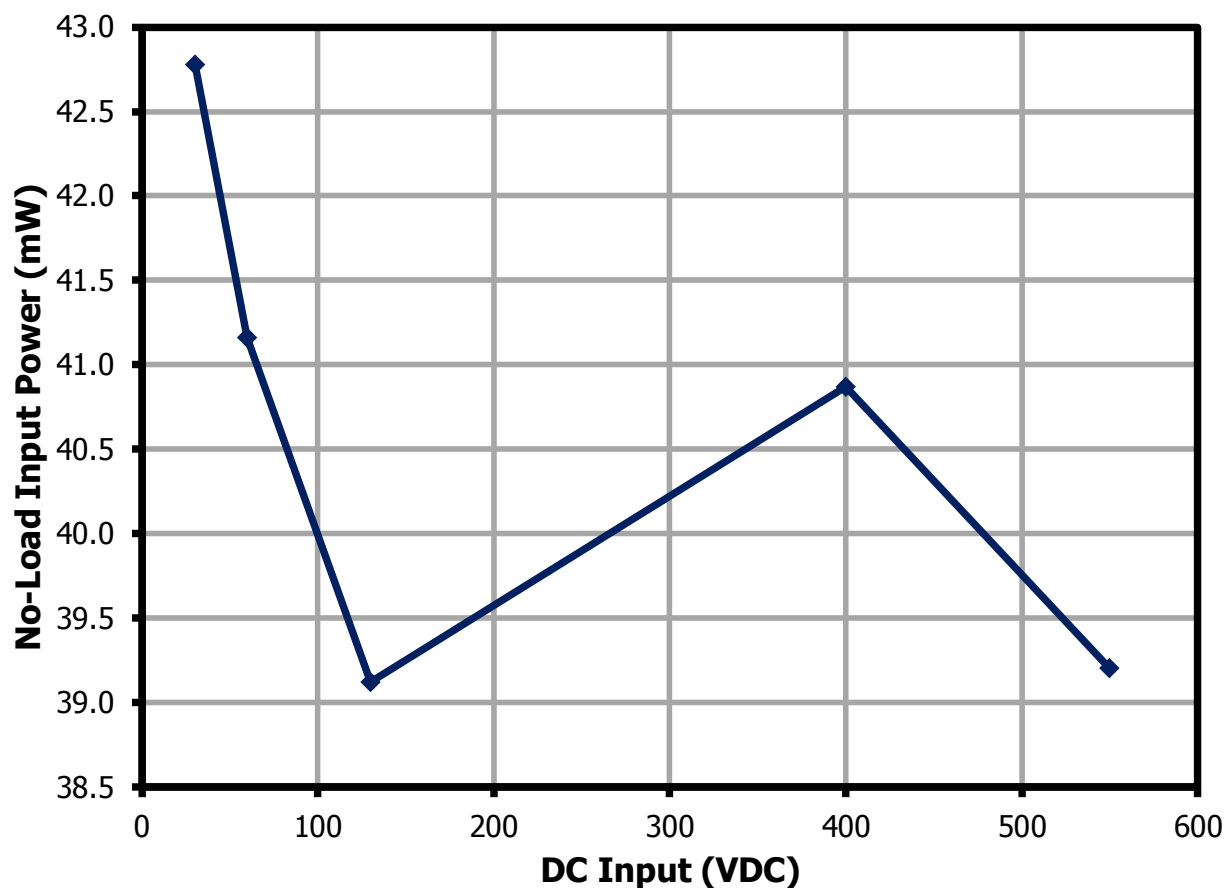


Figure 13 – No-Load Input Power, Room Temperature.

8.4 Load and Line Regulation

Measurements taken at 0% to 100% of rated load.

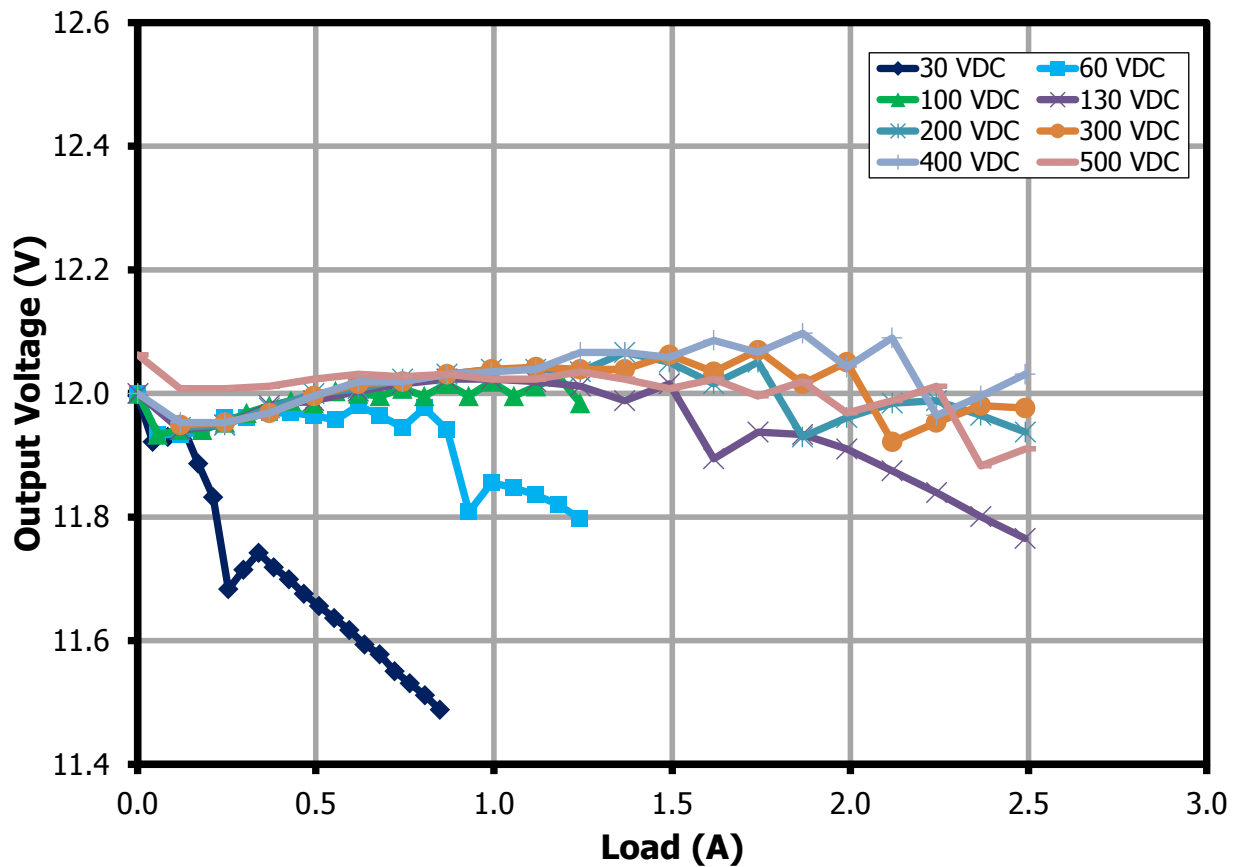


Figure 14 – Output Voltage vs. Output Current and Input Voltage (VDC), Room Temperature.

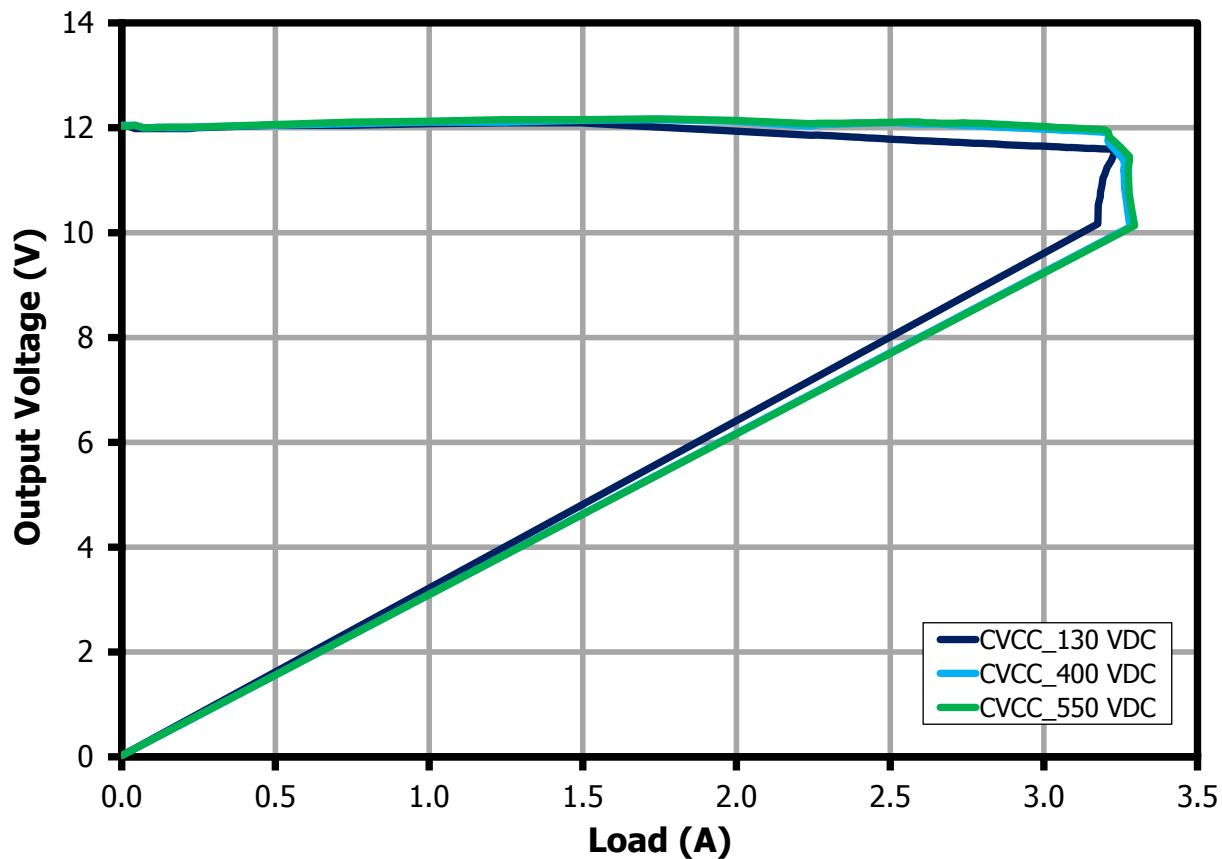
8.5 *CV/CC*

Figure 15 – CV/CC measured at PCB Output Terminal, Room Temperature.

9 Waveforms

9.1 Switching Waveforms

9.1.1 Drain Voltage and Current, Steady-State.

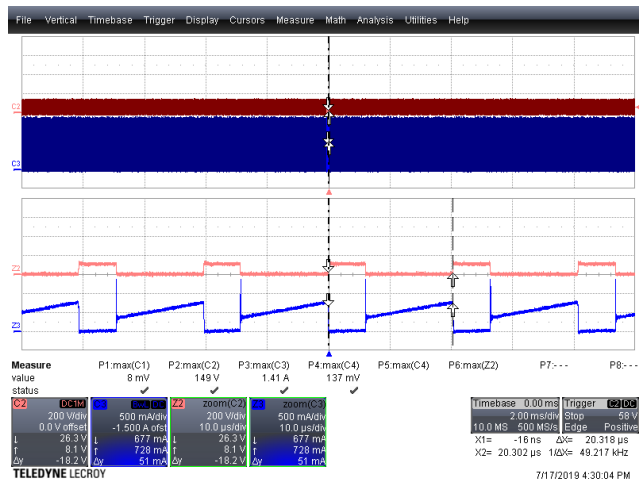


Figure 16 – Drain Voltage and Current Waveforms.
 $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 $V_{DS(\text{MAX})} = 149 \text{ V}$, $I_{DRAIN(\text{MAX})} = 1.41 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.
 Lower: I_{DRAIN} , 500 mA, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

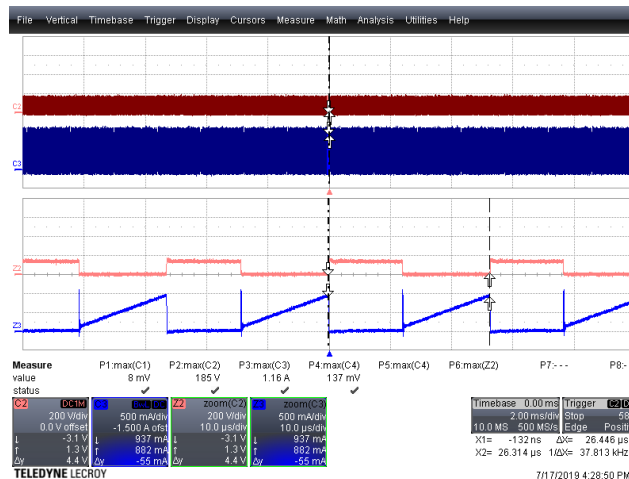


Figure 17 – Drain Voltage and Current Waveforms.
 $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 $V_{DS(\text{MAX})} = 185 \text{ V}$, $I_{DRAIN(\text{MAX})} = 1.16 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.
 Lower: I_{DRAIN} , 500 mA, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

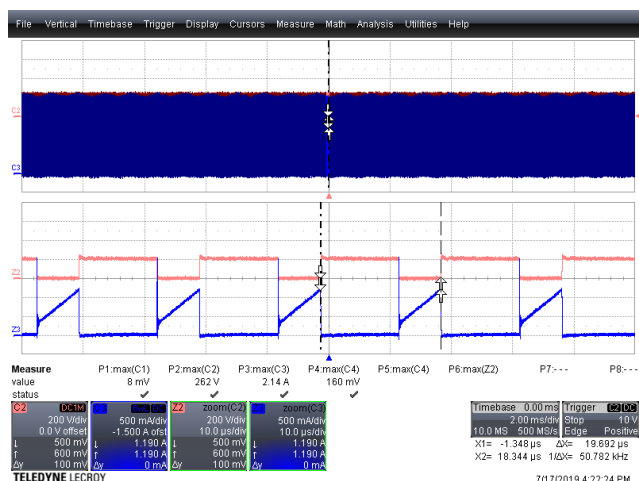


Figure 18 – Drain Voltage and Current Waveforms.
 $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(\text{MAX})} = 262 \text{ V}$, $I_{DRAIN(\text{MAX})} = 2.14 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.
 Lower: I_{DRAIN} , 500 mA, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

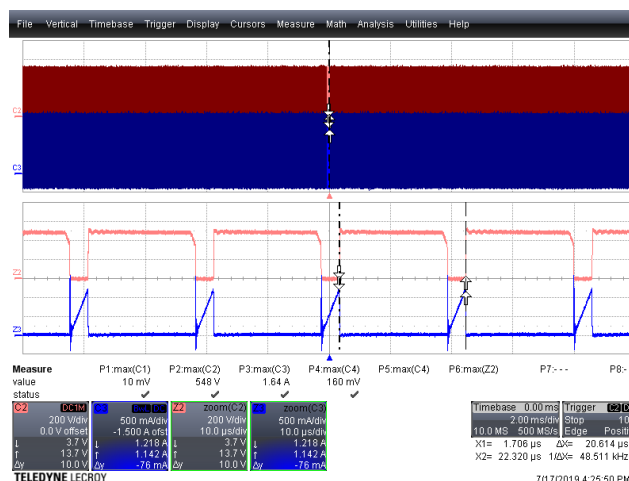


Figure 19 – Drain Voltage and Current Waveforms.
 $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(\text{MAX})} = 548 \text{ V}$, $I_{DRAIN(\text{MAX})} = 1.64 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.
 Lower: I_{DRAIN} , 500 mA, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

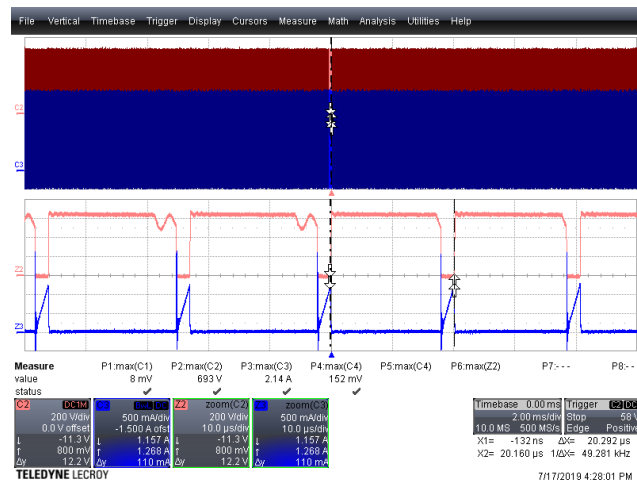


Figure 20 – Drain Voltage and Current Waveforms.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

$V_{DS(MAX)} = 693 \text{ V}$, $I_{DRAIN(MAX)} = 2.14 \text{ A}$.

Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.

Lower: I_{DRAIN} , 500 mA, 2 ms / div.

Bottom Half: Zoom @ 10 μ s / div.

9.1.2 Drain Voltage and Current, Start-up.

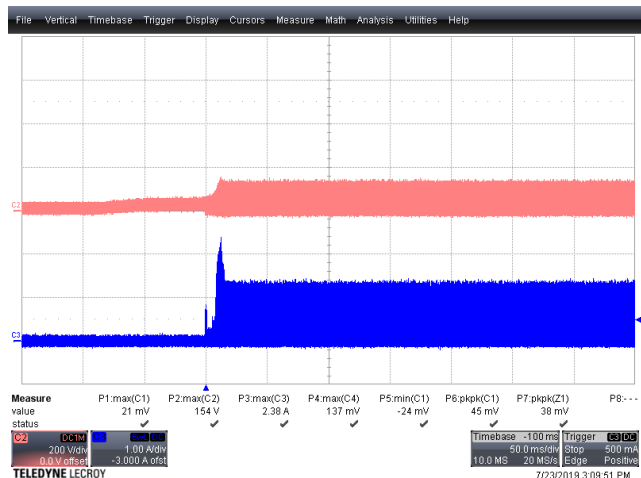


Figure 21 – Drain Voltage and Current Waveforms.
 $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 $V_{DS(MAX)} = 154 \text{ V}$, $I_{DRAIN(MAX)} = 2.38 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 50 ms / div.
 Lower: I_{DRAIN} , 1 A, 50 ms / div.

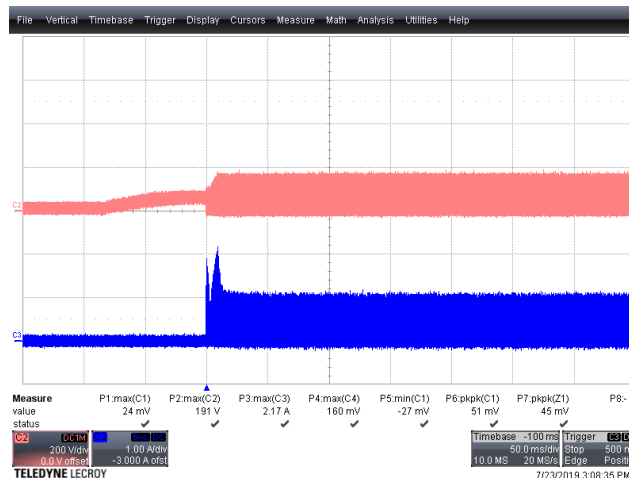


Figure 22 – Drain Voltage and Current Waveforms.
 $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 $V_{DS(MAX)} = 191 \text{ V}$, $I_{DRAIN(MAX)} = 2.17 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 50 ms / div.
 Lower: I_{DRAIN} , 1 A, 50 ms / div.

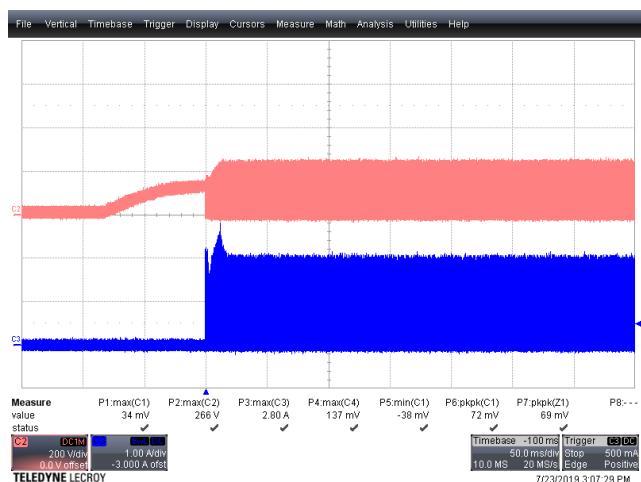


Figure 23 – Drain Voltage and Current Waveforms.
 $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(MAX)} = 266 \text{ V}$, $I_{DRAIN(MAX)} = 2.80 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 50 ms / div.
 Lower: I_{DRAIN} , 1 A, 50 ms / div.

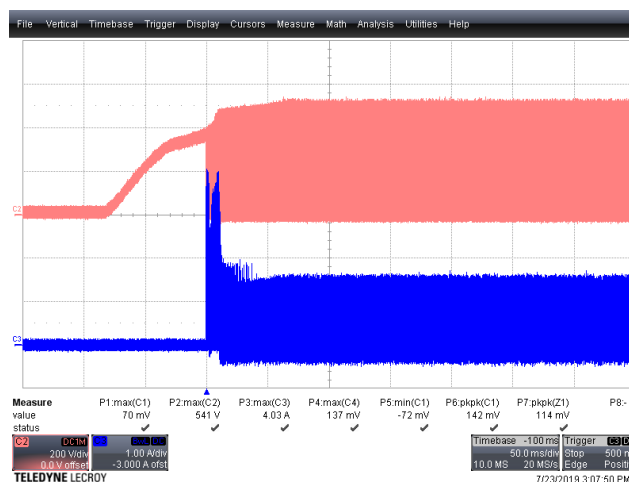


Figure 24 – Drain Voltage and Current Waveforms.
 $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(MAX)} = 541 \text{ V}$, $I_{DRAIN(MAX)} = 4.03 \text{ A}$.
 Upper: $V_{DRAIN-SOURCE}$, 200 V, 50 ms / div.
 Lower: I_{DRAIN} , 1 A, 50 ms / div.

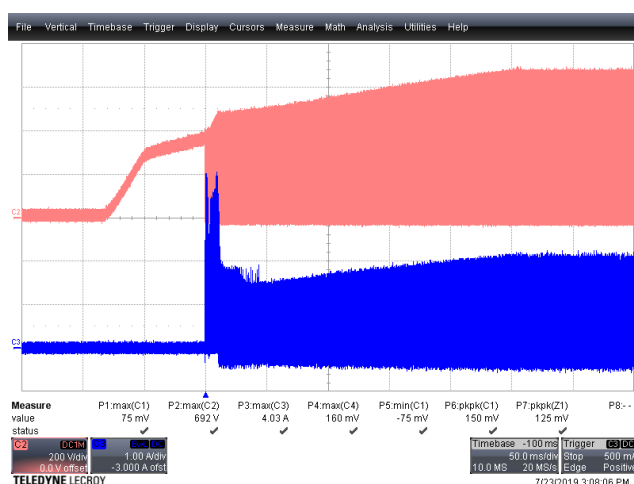


Figure 25 – Drain Voltage and Current Waveforms.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

$V_{DS(MAX)} = 692 \text{ V}$, $I_{DRAIN(MAX)} = 4.03 \text{ A}$.

Upper: $V_{DRAIN-SOURCE}$, 200 V, 50 ms / div.

Lower: I_{DRAIN} , 1 A, 50 ms / div.

9.1.3 SR FET Waveforms, Steady-State.

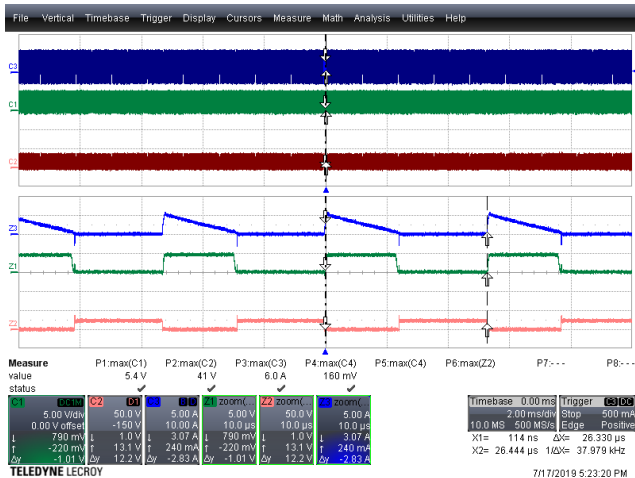


Figure 26 – Drain Voltage and Current Waveforms.
 $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 $V_{DS(MAX)} = 41 \text{ V}$, $I_{DRAIN(MAX)} = 6.0 \text{ A}$.
 Upper: I_{DRAIN} , 5 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

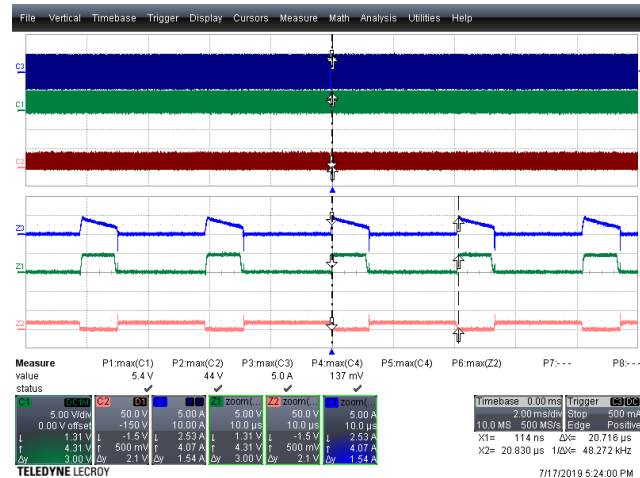


Figure 27 – Drain Voltage and Current Waveforms.
 $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 $V_{DS(MAX)} = 44 \text{ V}$, $I_{DRAIN(MAX)} = 5.0 \text{ A}$.
 Upper: I_{DRAIN} , 5 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

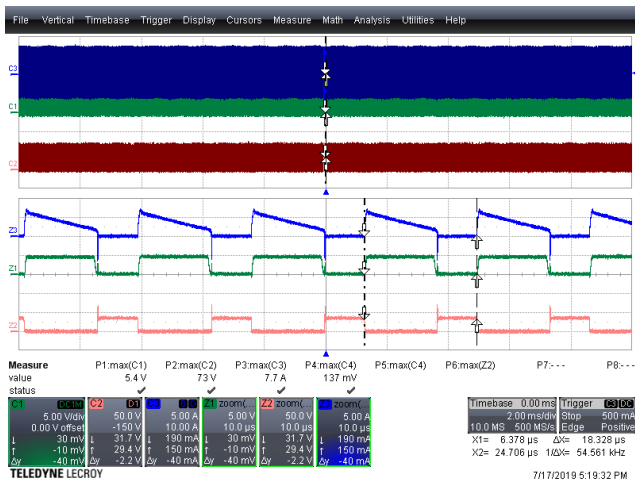


Figure 28 – Drain Voltage and Current Waveforms.
 $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(MAX)} = 73 \text{ V}$, $I_{DRAIN(MAX)} = 7.7 \text{ A}$.
 Upper: I_{DRAIN} , 5 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

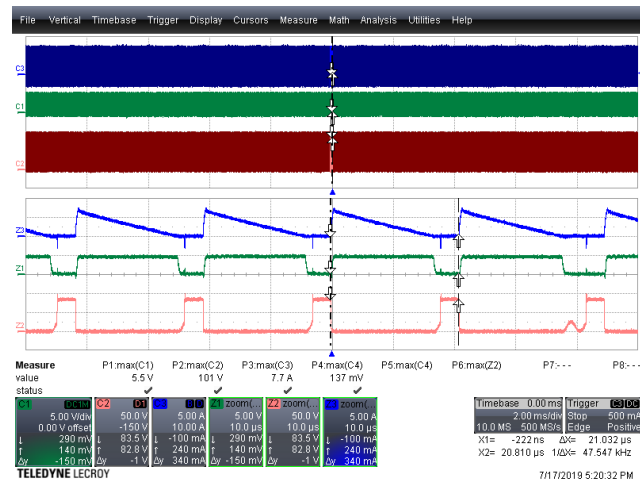


Figure 29 – Drain Voltage and Current Waveforms.
 $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(MAX)} = 101 \text{ V}$, $I_{DRAIN(MAX)} = 1.37 \text{ A}$.
 Upper: I_{DRAIN} , 5 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.
 Bottom Half: Zoom @ 10 μs / div.

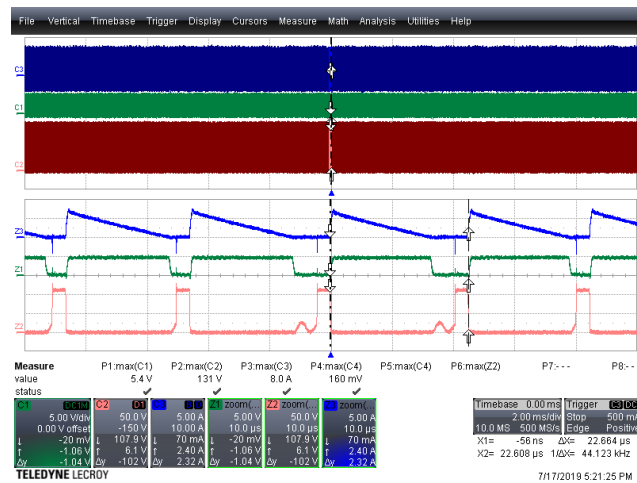


Figure 30 – Drain Voltage and Current Waveforms.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

$V_{DS(MAX)} = 131 \text{ V}$, $I_{DRAIN(MAX)} = 8.0 \text{ A}$.

Upper: I_{DRAIN} , 5 A, 2 ms / div.

Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.

Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.

Bottom Half: Zoom @ 10 μs / div.

9.1.4 SR FET Waveforms, Start-up.

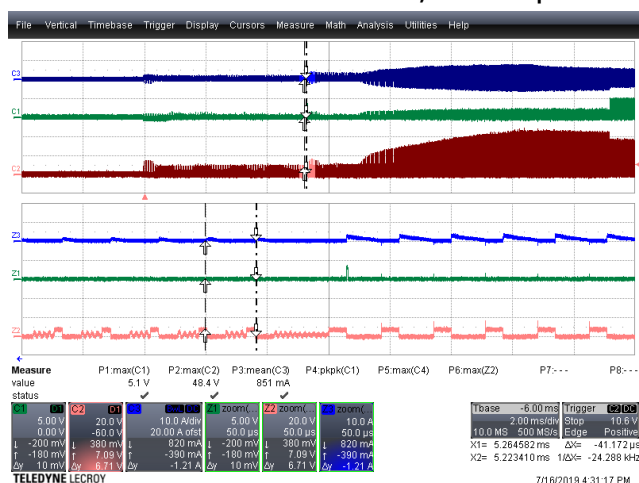


Figure 31 – Drain Voltage and Current Waveforms.
 $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 $V_{DS(MAX)} = 48.4 \text{ V}$, $I_{DRAIN(MAX)} = 0.851 \text{ A}$.
 Upper: I_{DRAIN} , 10 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 20 V, 2 ms / div.
 Bottom Half: Zoom @ 50 μs / div.

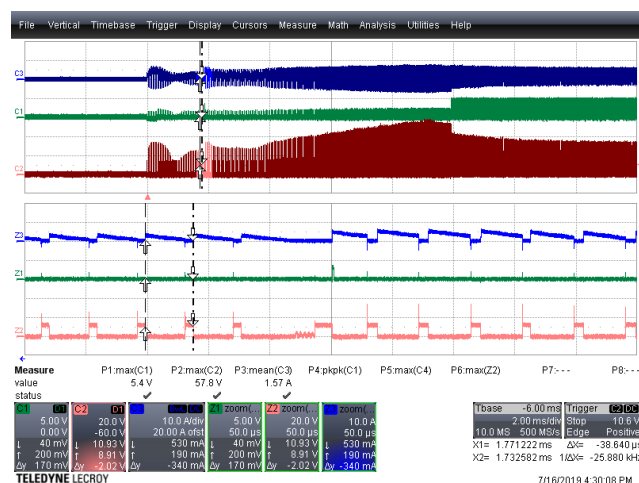


Figure 32 – Drain Voltage and Current Waveforms.
 $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 $V_{DS(MAX)} = 57.8 \text{ V}$, $I_{DRAIN(MAX)} = 1.57 \text{ A}$.
 Upper: I_{DRAIN} , 10 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 20 V, 2 ms / div.
 Bottom Half: Zoom @ 50 μs / div.

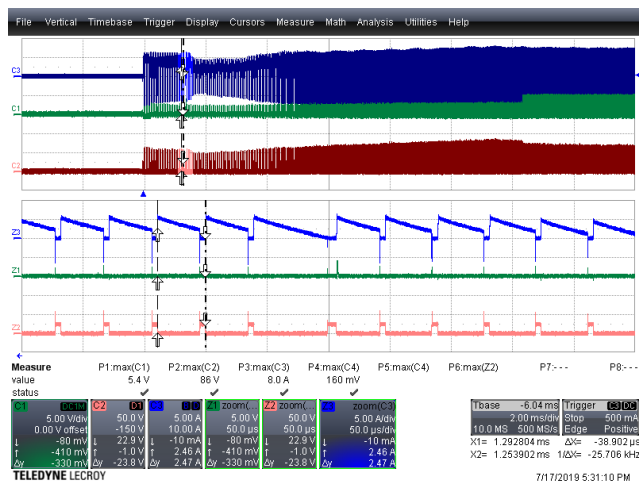


Figure 33 – Drain Voltage and Current Waveforms.
 $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(MAX)} = 86 \text{ V}$, $I_{DRAIN(MAX)} = 8.0 \text{ A}$.
 Upper: I_{DRAIN} , 5 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.
 Bottom Half: Zoom @ 50 μs / div.

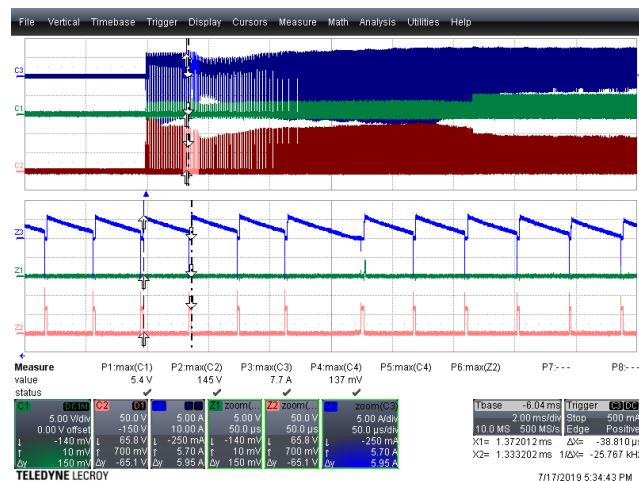


Figure 34 – Drain Voltage and Current Waveforms.
 $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 $V_{DS(MAX)} = 145 \text{ V}$, $I_{DRAIN(MAX)} = 7.7 \text{ A}$.
 Upper: I_{DRAIN} , 5 A, 2 ms / div.
 Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.
 Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.
 Bottom Half: Zoom @ 50 μs / div.

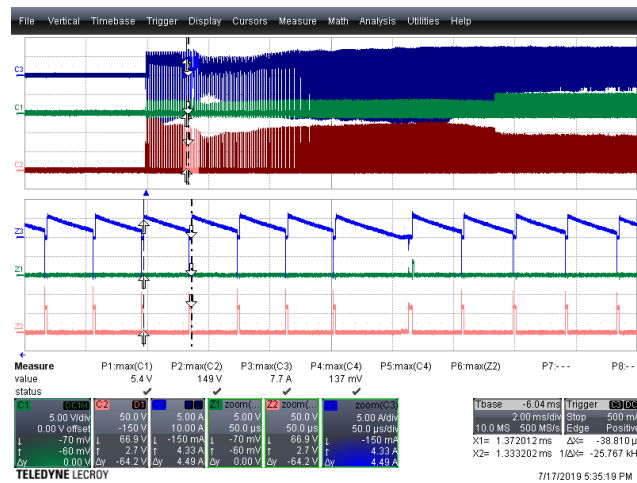


Figure 35 – Drain Voltage and Current Waveforms.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

$V_{DS(MAX)} = 149 \text{ V}$, $I_{DRAIN(MAX)} = 8.0 \text{ A}$.

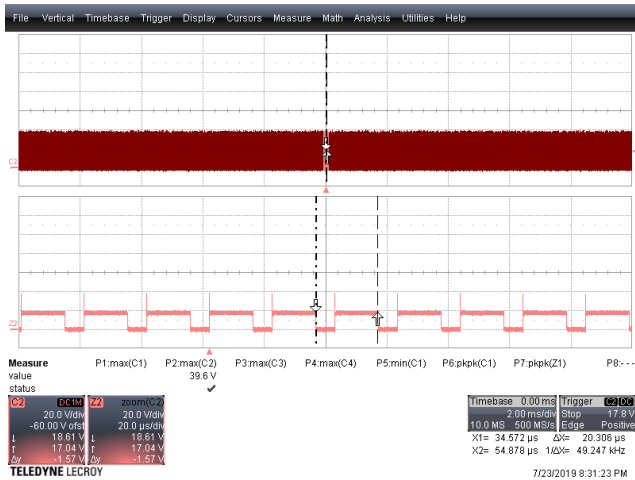
Upper: I_{DRAIN} , 10 A, 2 ms / div.

Middle: $V_{GATE-SOURCE}$, 5 V, 2 ms / div.

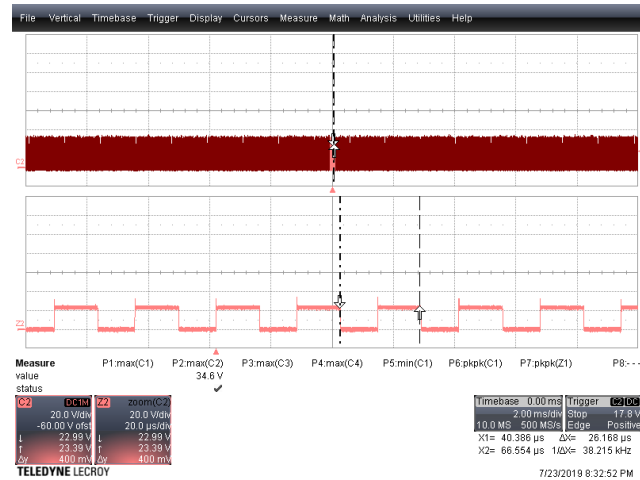
Lower: $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.

Bottom Half: Zoom @ 50 µs / div.

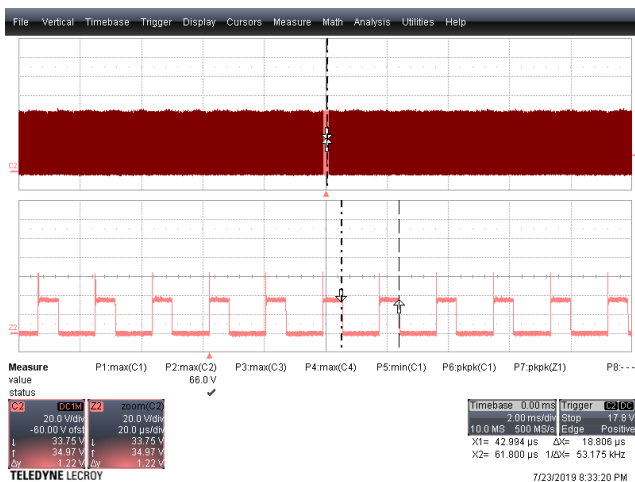
9.1.5 FWD Pin, Steady-State

**Figure 36** – Drain Voltage and Current Waveforms. $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$. $V_{FWD(MAX)} = 39.6 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.

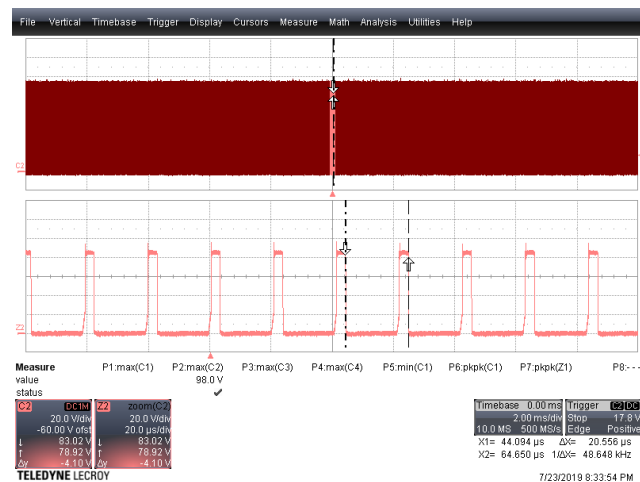
Bottom Half: Zoom @ 20 μs / div.

**Figure 37** – Drain Voltage and Current Waveforms. $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$. $V_{FWD(MAX)} = 34.6 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.

Bottom Half: Zoom @ 20 μs / div.

**Figure 38** – Drain Voltage and Current Waveforms. $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$. $V_{FWD(MAX)} = 66.0 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.

Bottom Half: Zoom @ 20 μs / div.

**Figure 39** – Drain Voltage and Current Waveforms. $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$. $V_{FWD(MAX)} = 98.0 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.

Bottom Half: Zoom @ 20 μs / div.

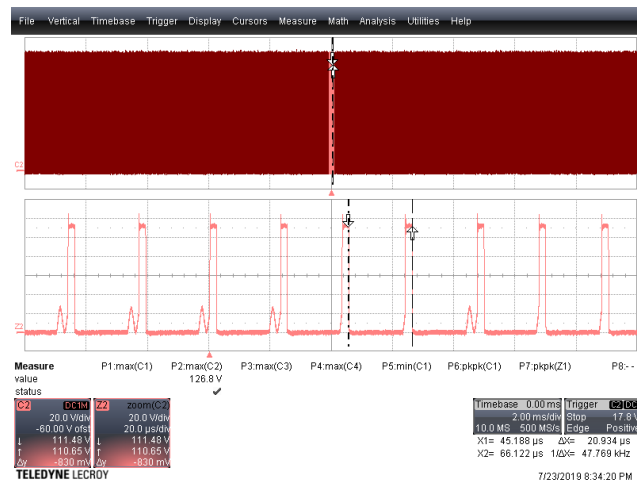


Figure 40 – Drain Voltage and Current Waveforms.

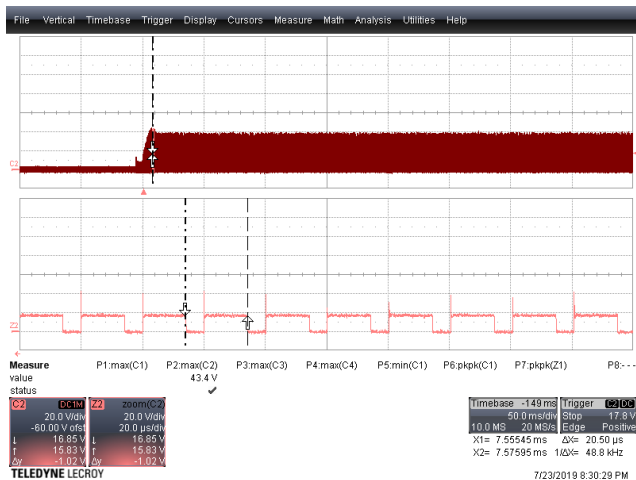
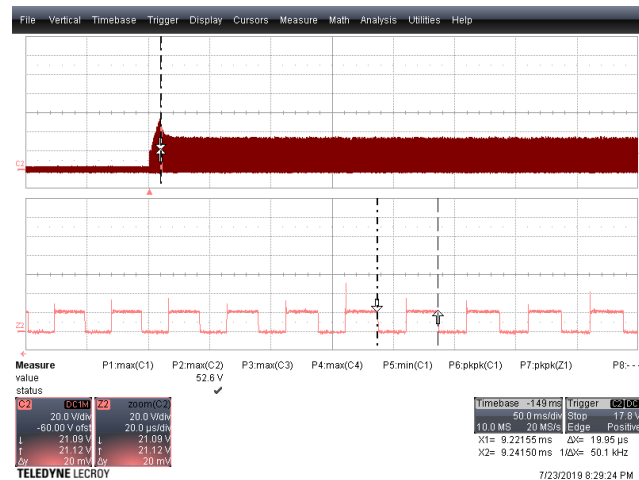
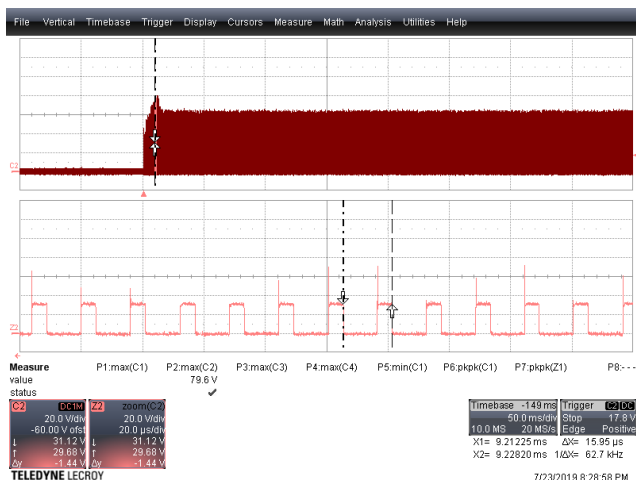
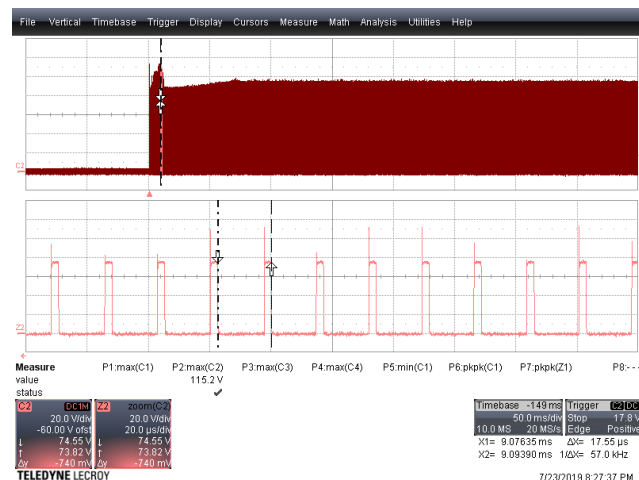
$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

$V_{FWD(MAX)} = 126.8 \text{ V}$

Upper: V_{FWD} , 20 V, 50 ms / div.

Bottom Half: Zoom @ 20 μs / div.

9.1.6 FWD Pin, Start-up

**Figure 41** – Drain Voltage and Current Waveforms. $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$. $V_{FWD(MAX)} = 43.4 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.Bottom Half: Zoom @ 20 μs / div.**Figure 42** – Drain Voltage and Current Waveforms. $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$. $V_{FWD(MAX)} = 52.6 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.Bottom Half: Zoom @ 20 μs / div.**Figure 43** – Drain Voltage and Current Waveforms. $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$. $V_{FWD(MAX)} = 79.6 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.Bottom Half: Zoom @ 20 μs / div.**Figure 44** – Drain Voltage and Current Waveforms. $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$. $V_{FWD(MAX)} = 115.2 \text{ V}$ Upper: V_{FWD} , 20 V, 50 ms / div.Bottom Half: Zoom @ 20 μs / div.

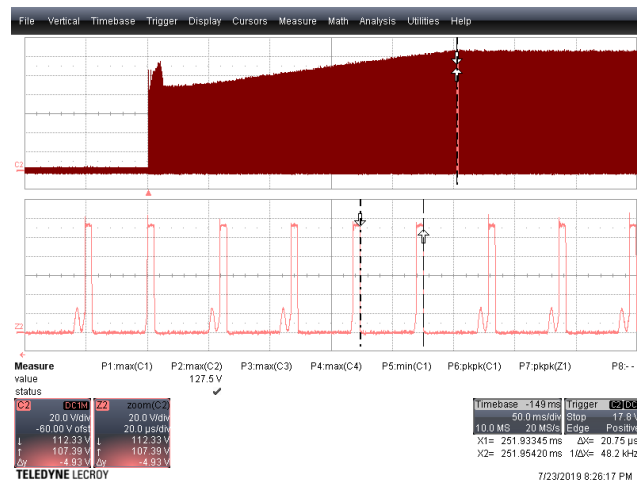


Figure 45 – Drain Voltage and Current Waveforms.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

$V_{FWD(MAX)} = 127.5 \text{ V}$

Upper: V_{FWD} , 20 V, 50 ms / div.

Bottom Half: Zoom @ 20 μs / div.

9.1.7 Output Voltage and Current, Startup CR Load

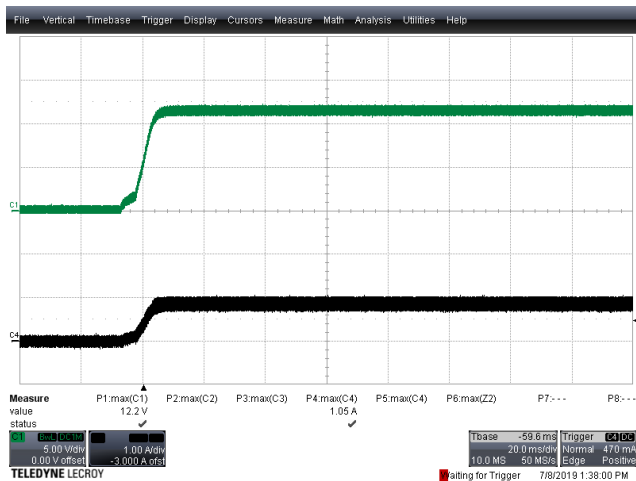


Figure 46 – Drain Voltage and Current Waveforms.
 $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$ CR Load.
 Upper: V_{OUT} , 5 V, 20 ms / div.
 Lower: I_{DRAIN} , 1 A, 20 ms / div.

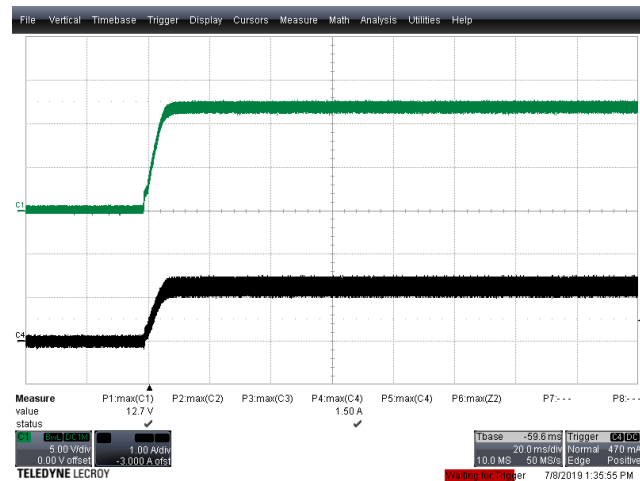


Figure 47 – Drain Voltage and Current Waveforms.
 $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$ CR Load.
 Upper: V_{OUT} , 5 V, 20 ms / div.
 Lower: I_{DRAIN} , 1 A, 20 ms / div.

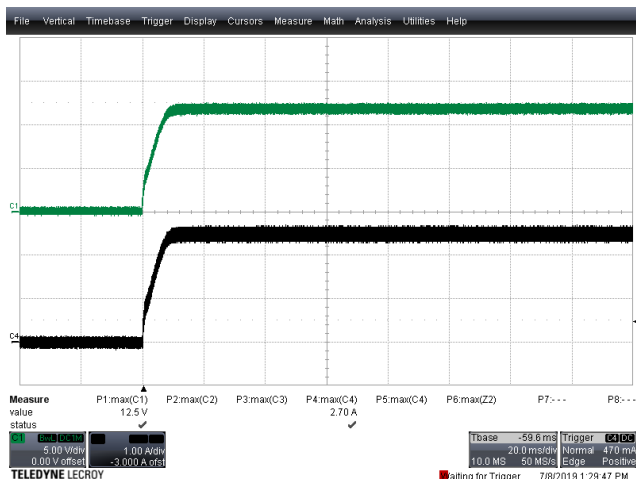


Figure 48 – Drain Voltage and Current Waveforms.
 $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$ CR Load.
 Upper: V_{OUT} , 5 V, 20 ms / div.
 Lower: I_{DRAIN} , 1 A, 20 ms / div.

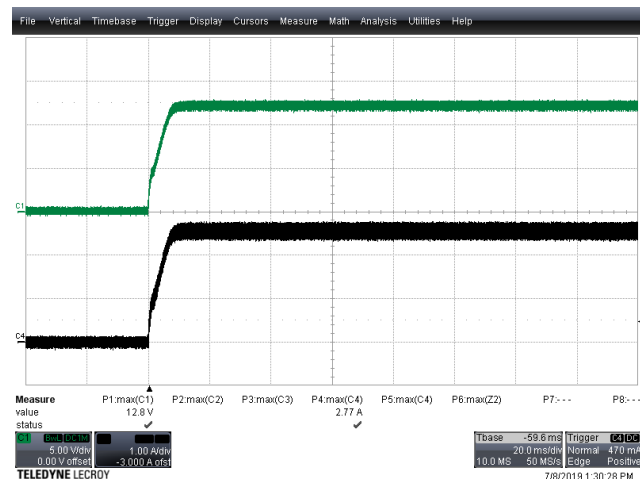


Figure 49 – Drain Voltage and Current Waveforms.
 $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$ CR Load.
 Upper: V_{OUT} , 5 V, 20 ms / div.
 Lower: I_{DRAIN} , 1 A, 20 ms / div.

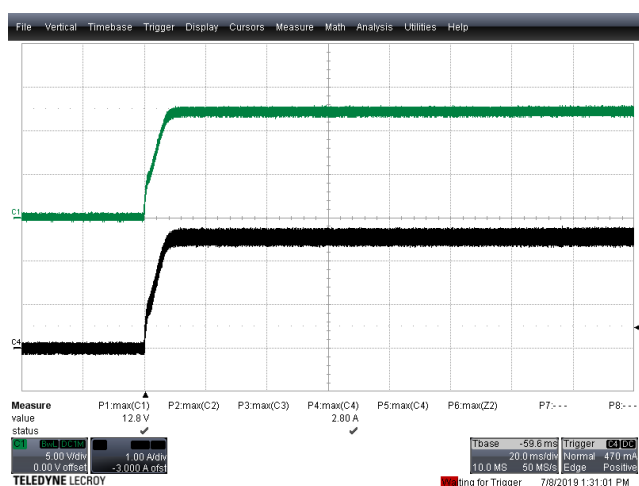


Figure 50 – Drain Voltage and Current Waveforms.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A CR Load}$.

Upper: V_{OUT} , 5 V, 20 ms / div.

Lower: I_{DRAIN} , 1 A, 20 ms / div.

9.2 ***Output Ripple Measurements (SR FET)***

9.2.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor include one (1) 1 μ F/50 V ceramic type.

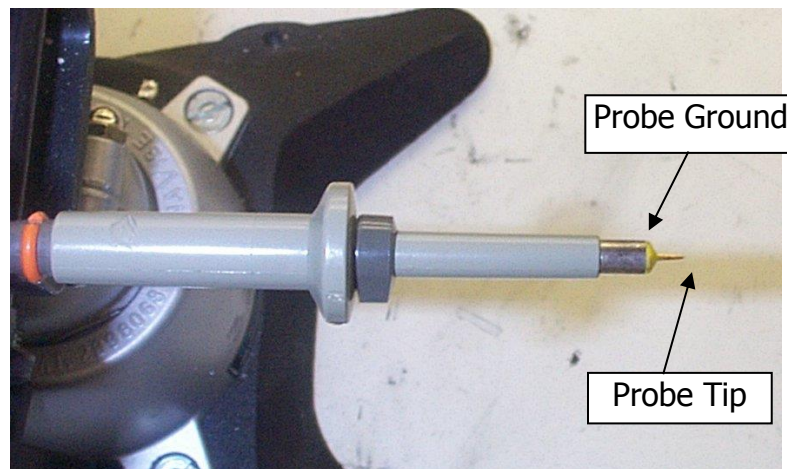
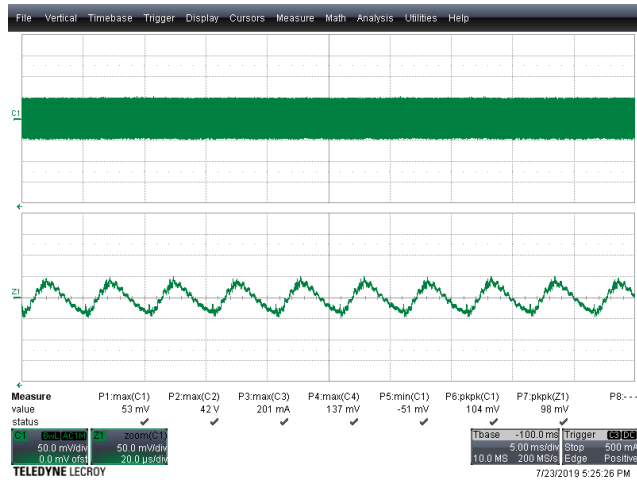
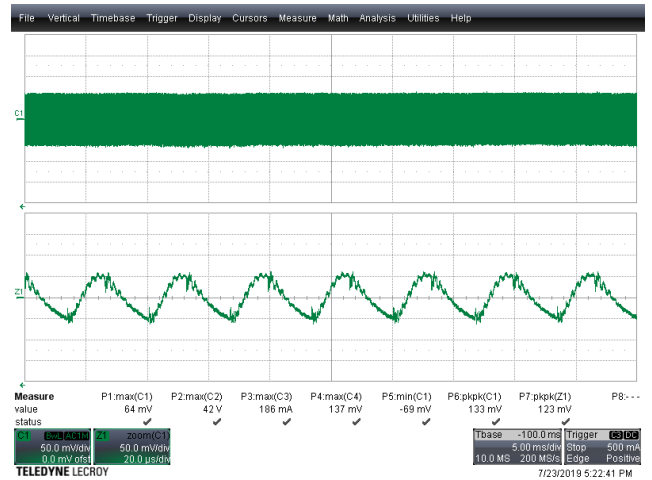
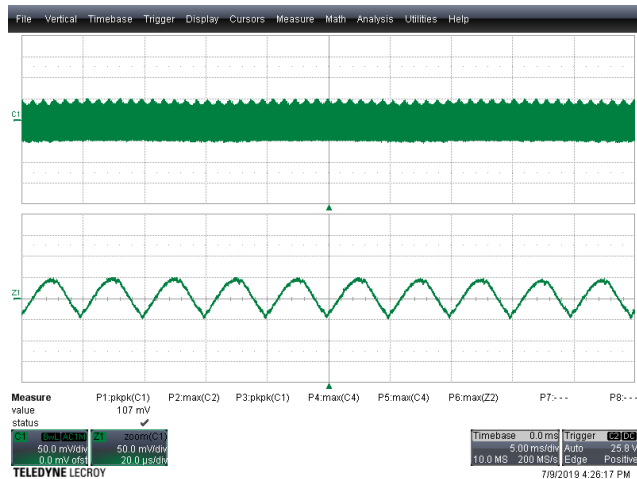
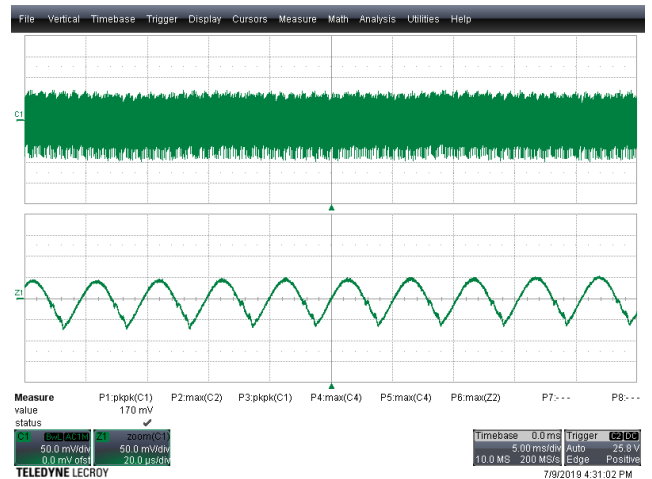


Figure 51 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 52 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)

9.2.2 100% Loading Condition

**Figure 53** – Output Voltage Ripple. $V_{IN} = 30$ VDC, $I_{OUT} = 0.85$ A.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μ s / div. $V_{RIPPLE} = 104$ mV_{p-p}**Figure 54** – Output Voltage Ripple. $V_{IN} = 60$ VDC, $I_{OUT} = 1.25$ A.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μ s / div. $V_{RIPPLE} = 133$ mV_{p-p}**Figure 55** – Output Voltage Ripple. $V_{IN} = 130$ VDC, $I_{OUT} = 2.5$ A.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μ s / div. $V_{RIPPLE} = 107$ mV_{p-p}**Figure 56** – Output Voltage Ripple. $V_{IN} = 400$ VDC, $I_{OUT} = 2.5$ A.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μ s / div. $V_{RIPPLE} = 170$ mV_{p-p}

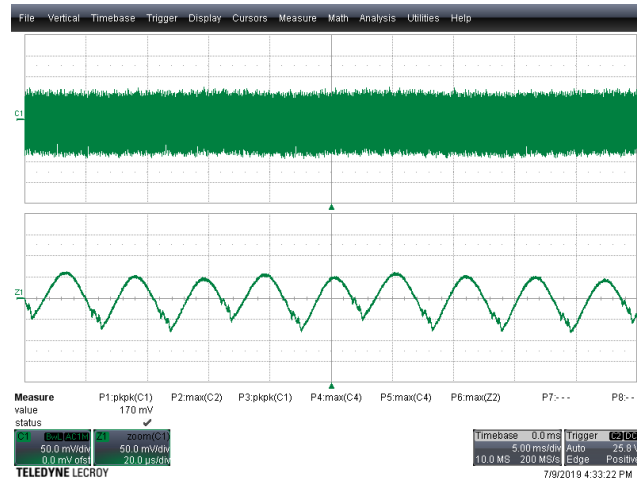


Figure 57 – Output Voltage Ripple.

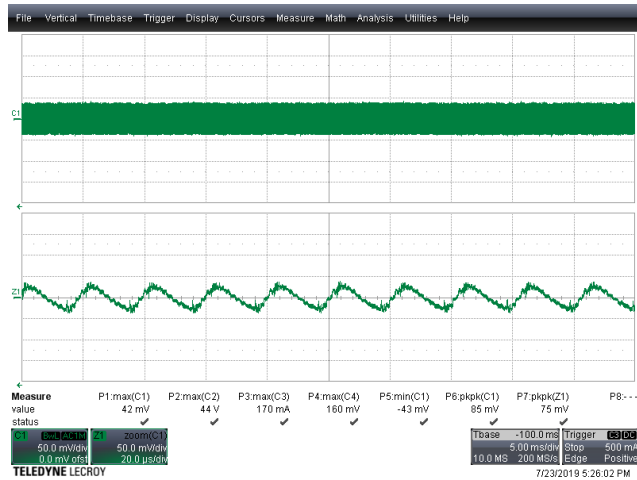
$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

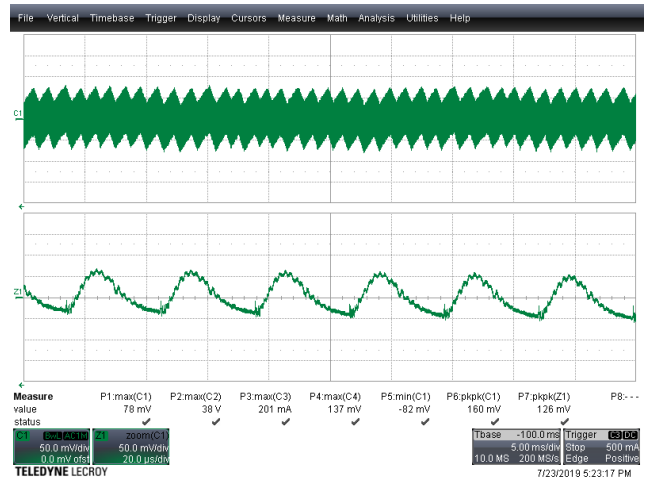
Bottom Half: Zoom @ 20 μs / div.

$V_{RIPPLE} = 170 \text{ mV}_{P-P}$

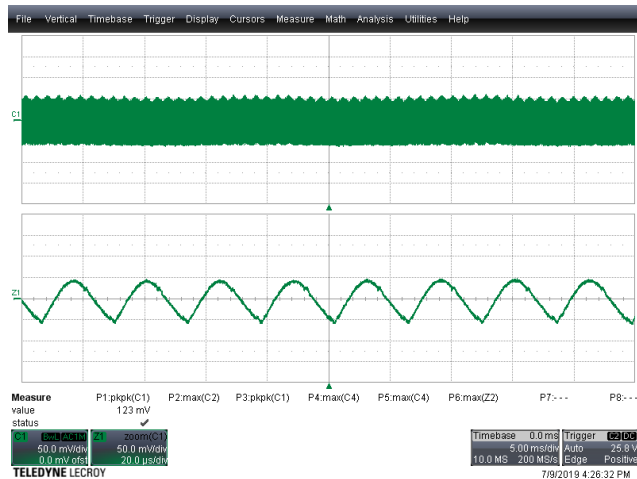
9.2.3 75% Loading Condition

**Figure 58** – Output Voltage Ripple.

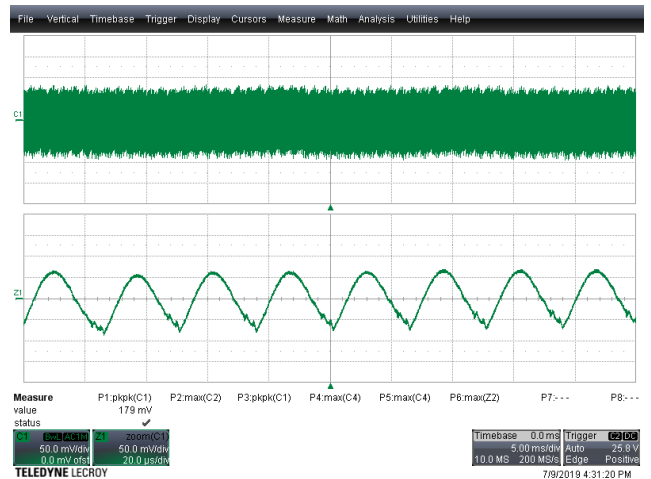
$V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 85 \text{ mV}_{p-p}$

**Figure 59** – Output Voltage Ripple.

$V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 160 \text{ mV}_{p-p}$

**Figure 60** – Output Voltage Ripple.

$V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 123 \text{ mV}_{p-p}$

**Figure 61** – Output Voltage Ripple.

$V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 179 \text{ mV}_{p-p}$

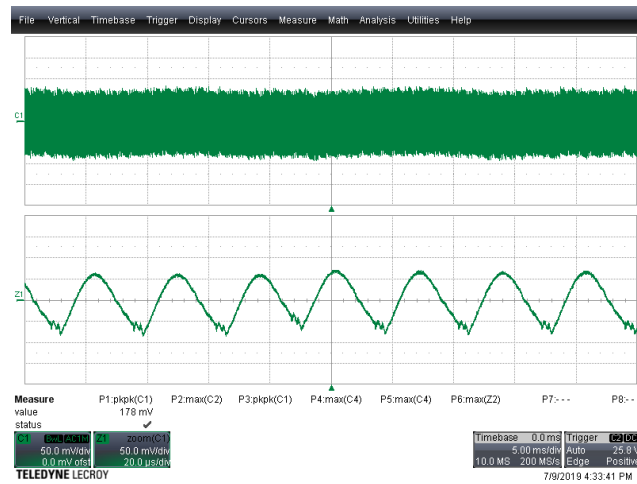


Figure 62 – Output Voltage Ripple.

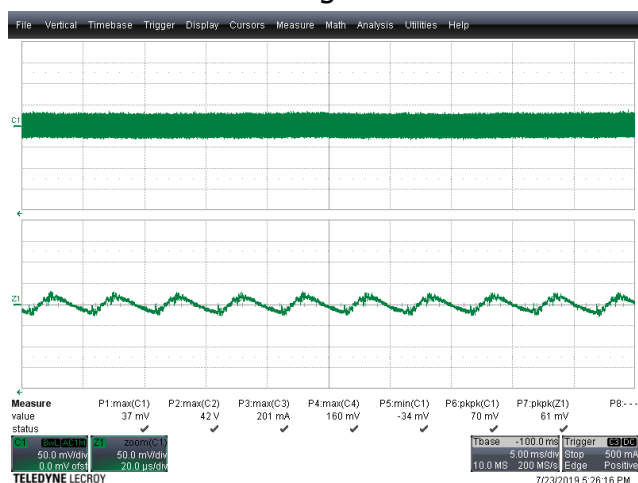
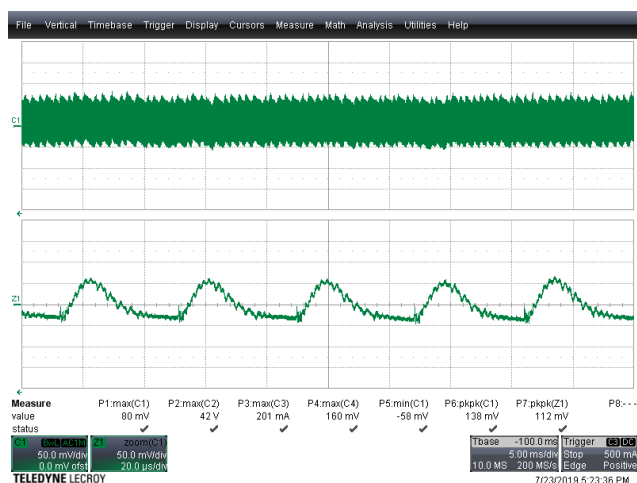
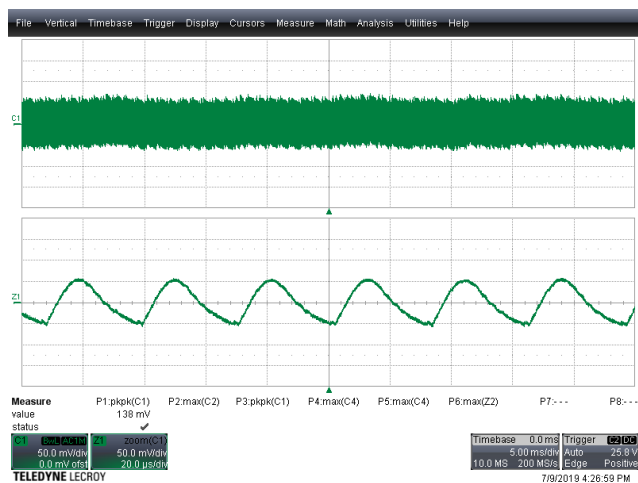
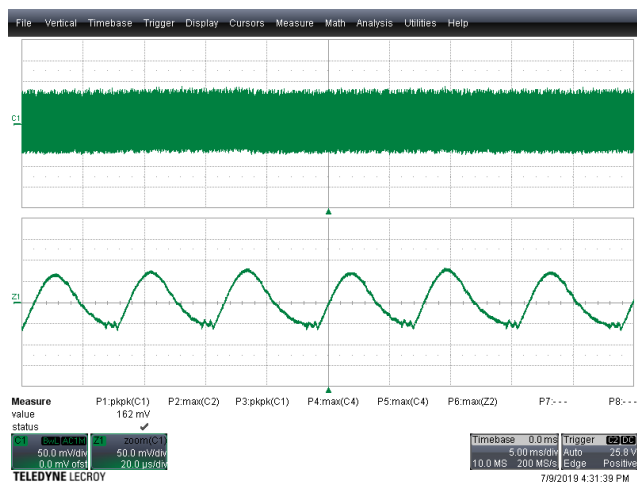
$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

Bottom Half: Zoom @ 20 μs / div.

$V_{RIPPLE} = 178 \text{ mV}_{P-P}$

9.2.4 50% Loading Condition

**Figure 63** – Output Voltage Ripple. $V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μs / div. $V_{RIPPLE} = 70 \text{ mV}_{P-P}$ **Figure 64** – Output Voltage Ripple. $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μs / div. $V_{RIPPLE} = 133 \text{ mV}_{P-P}$ **Figure 65** – Output Voltage Ripple. $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μs / div. $V_{RIPPLE} = 138 \text{ mV}_{P-P}$ **Figure 66** – Output Voltage Ripple. $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 20 μs / div. $V_{RIPPLE} = 162 \text{ mV}_{P-P}$

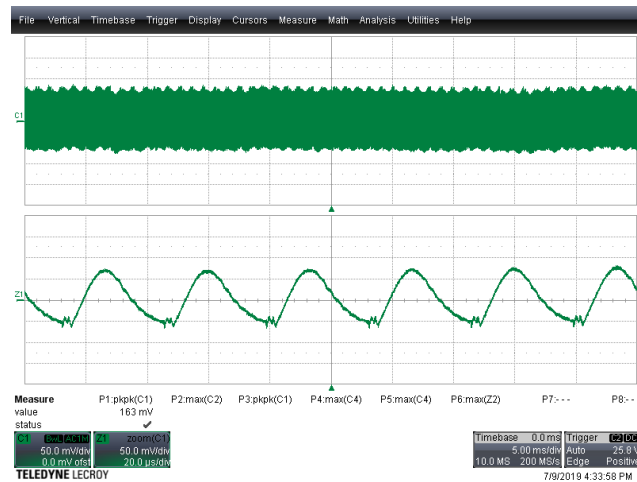


Figure 67 – Output Voltage Ripple.

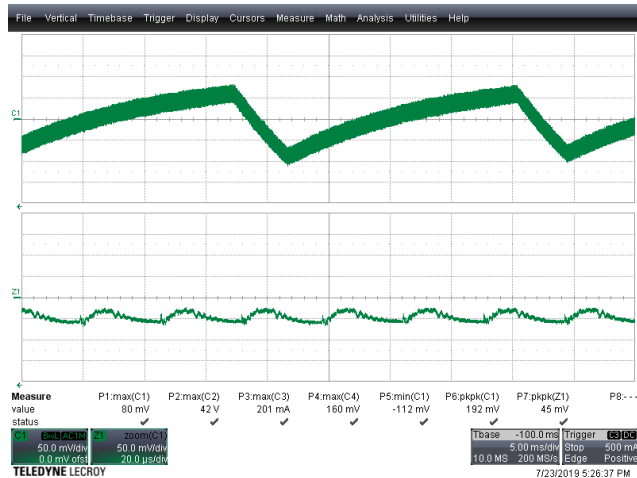
$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

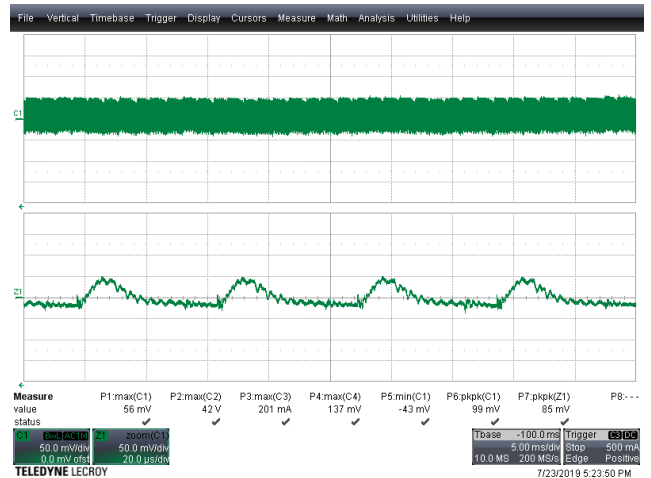
Bottom Half: Zoom @ 20 μs / div.

$V_{RIPPLE} = 163 \text{ mV}_{P-P}$

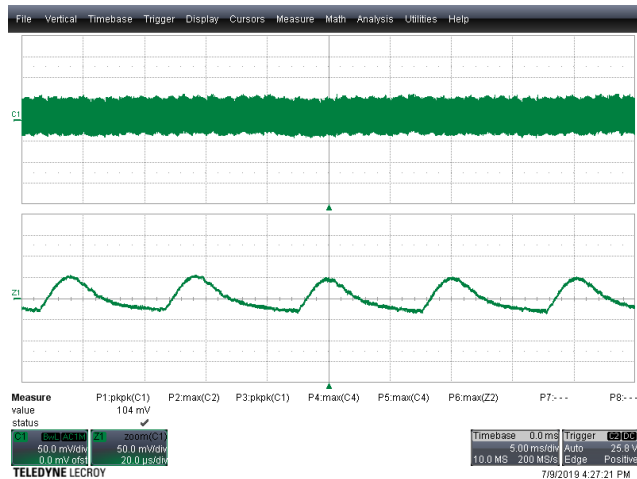
9.2.5 25% Loading Condition

**Figure 68** – Output Voltage Ripple.

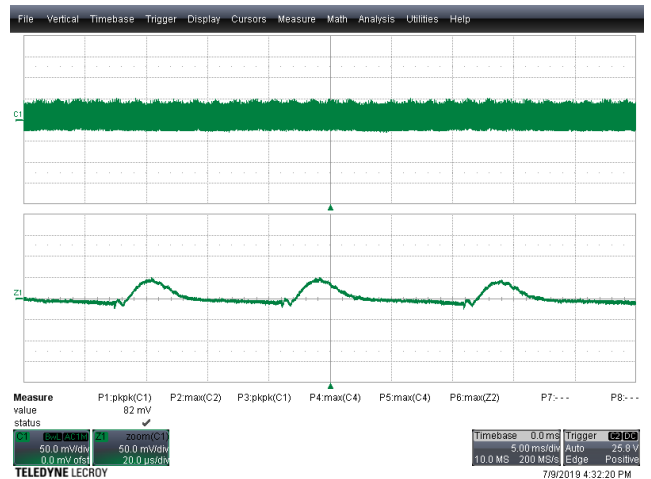
$V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 192 \text{ mV}_{P-P}$

**Figure 69** – Output Voltage Ripple.

$V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 99 \text{ mV}_{P-P}$

**Figure 70** – Output Voltage Ripple.

$V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 104 \text{ mV}_{P-P}$

**Figure 71** – Output Voltage Ripple.

$V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 82 \text{ mV}_{P-P}$

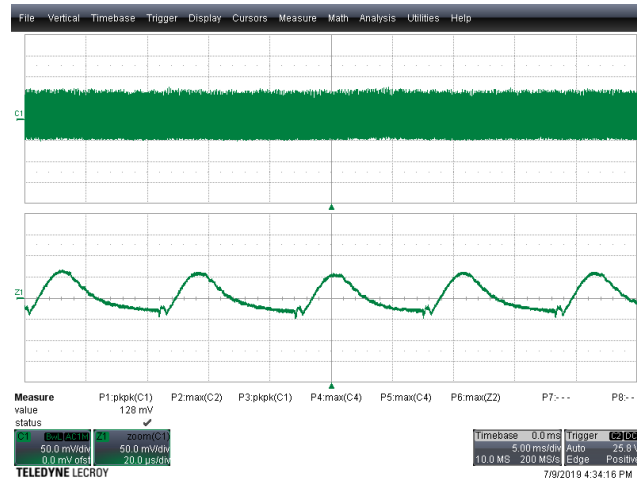


Figure 72 – Output Voltage Ripple.

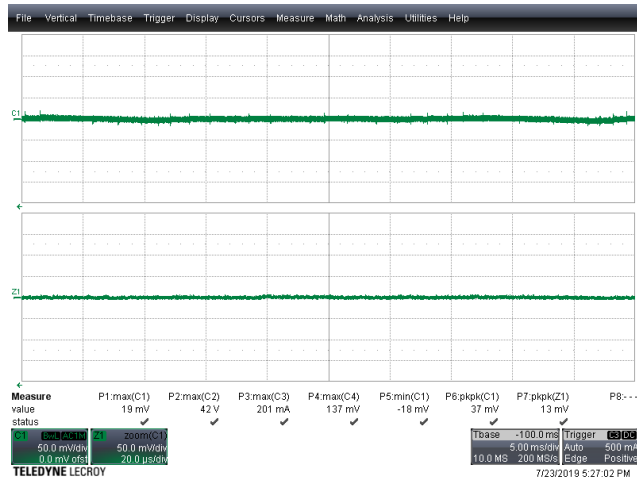
$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

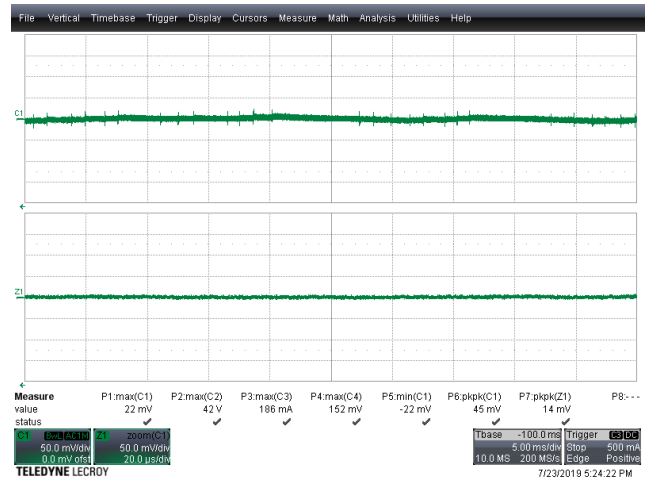
Bottom Half: Zoom @ 20 μs / div.

$V_{RIPPLE} = 128 \text{ mV}_{P-P}$

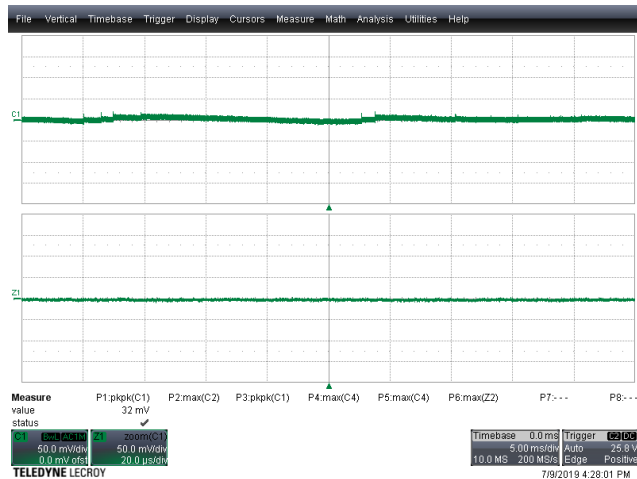
9.2.6 0% Loading Condition

**Figure 73** – Output Voltage Ripple.

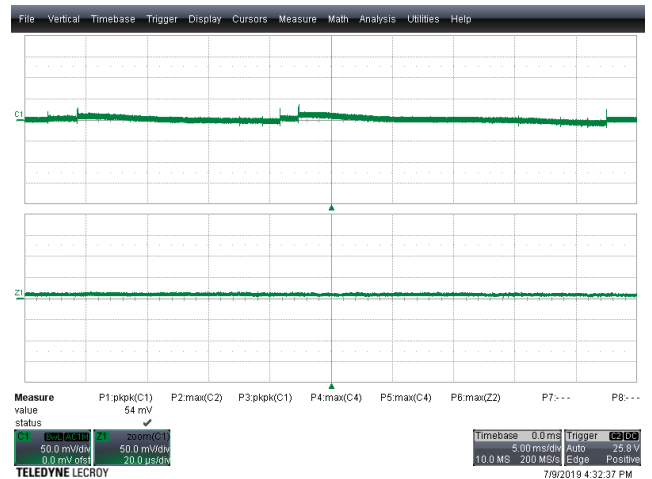
$V_{IN} = 30 \text{ VDC}$, $I_{OUT} = 0.85 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 37 \text{ mV}_{P-P}$

**Figure 74** – Output Voltage Ripple.

$V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 45 \text{ mV}_{P-P}$

**Figure 75** – Output Voltage Ripple.

$V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 32 \text{ mV}_{P-P}$

**Figure 76** – Output Voltage Ripple.

$V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 54 \text{ mV}_{P-P}$

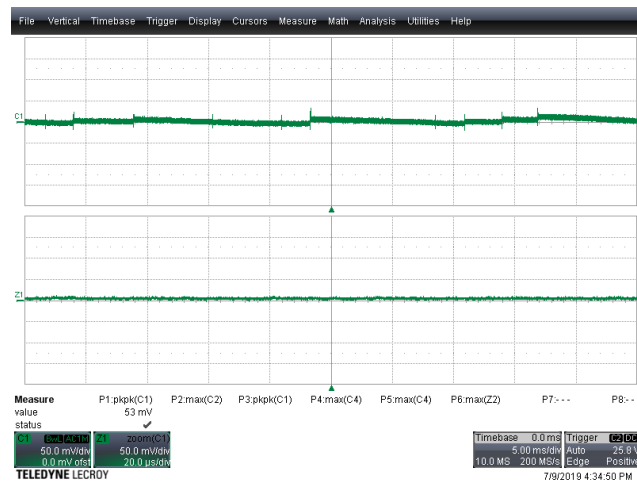


Figure 77 – Output Voltage Ripple.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

Bottom Half: Zoom @ 20 μs / div.

$V_{RIPPLE} = 53 \text{ mV}_{P-P}$

9.3 Output Ripple Measurements (Qspeed Diode)

9.3.1 100% Loading Condition

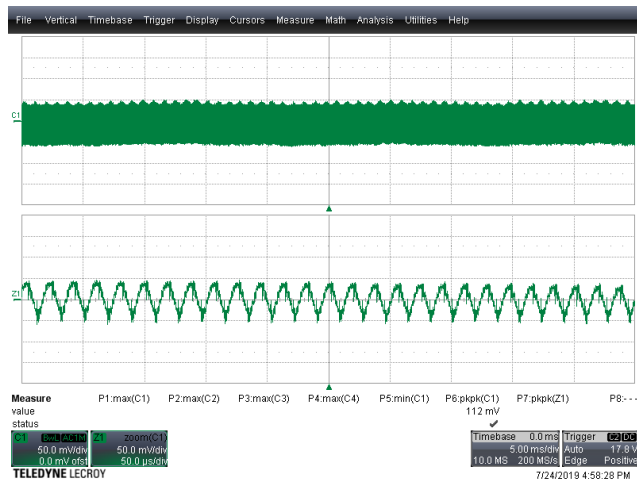


Figure 78 – Output Voltage Ripple.

$V_{IN} = 130$ VDC, $I_{OUT} = 2.5$ A.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

Bottom Half: Zoom @ 50 μ s / div.

$V_{RIPPLE} = 112$ mV_{P-P}

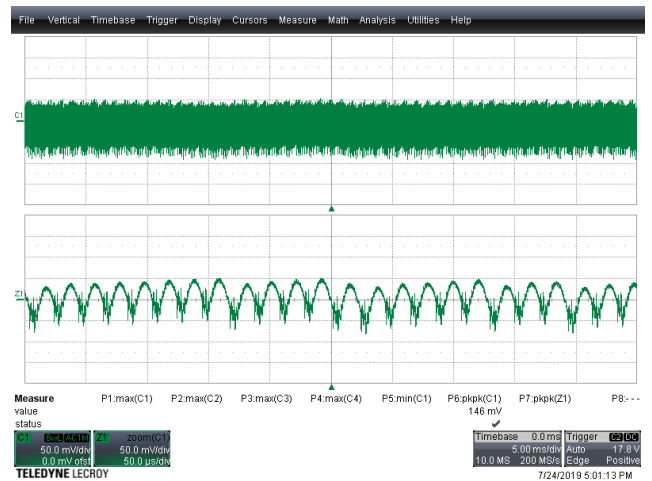


Figure 79 – Output Voltage Ripple.

$V_{IN} = 400$ VDC, $I_{OUT} = 2.5$ A.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

Bottom Half: Zoom @ 50 μ s / div.

$V_{RIPPLE} = 146$ mV_{P-P}

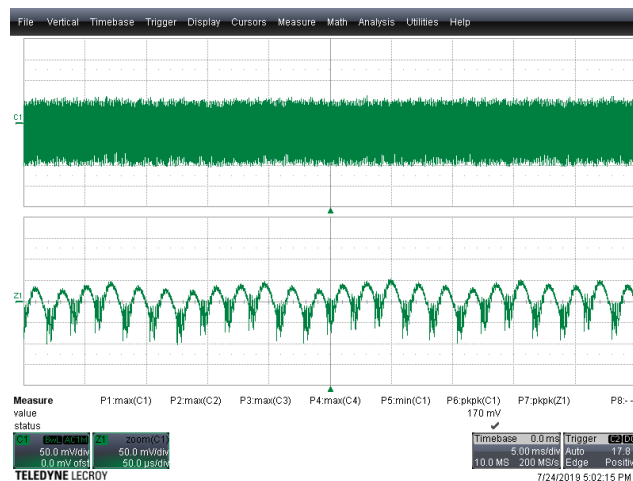


Figure 80 – Output Voltage Ripple.

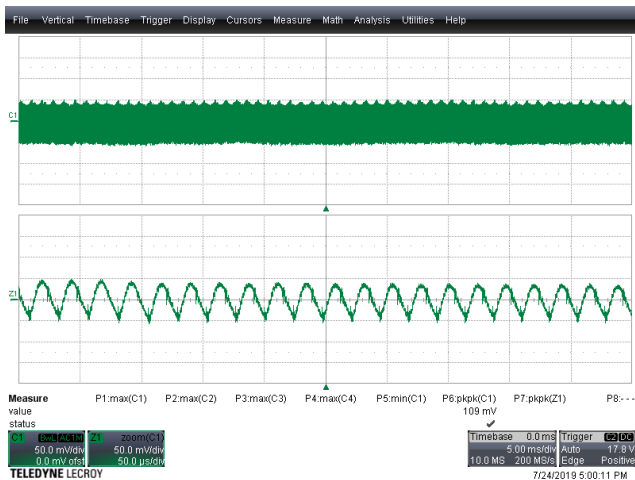
$V_{IN} = 550$ VDC, $I_{OUT} = 2.5$ A.

Top Half: V_{OUT} , 50 mV, 5 ms / div.

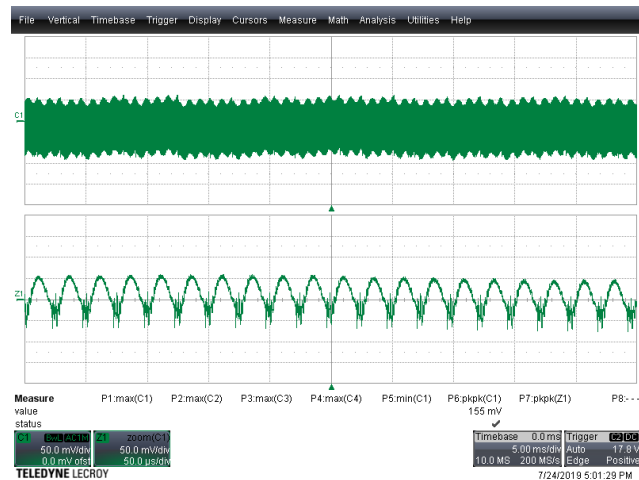
Bottom Half: Zoom @ 50 μ s / div.

$V_{RIPPLE} = 170$ mV_{P-P}

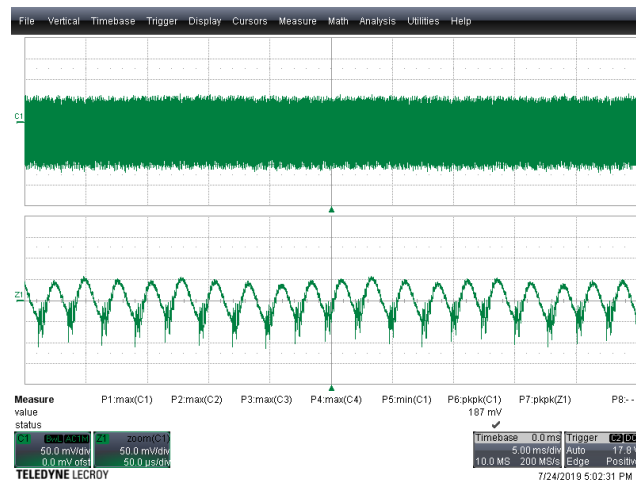
9.3.2 75% Loading Condition

**Figure 81** – Output Voltage Ripple.

$V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 1.875 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 109 \text{ mV}_{P-P}$

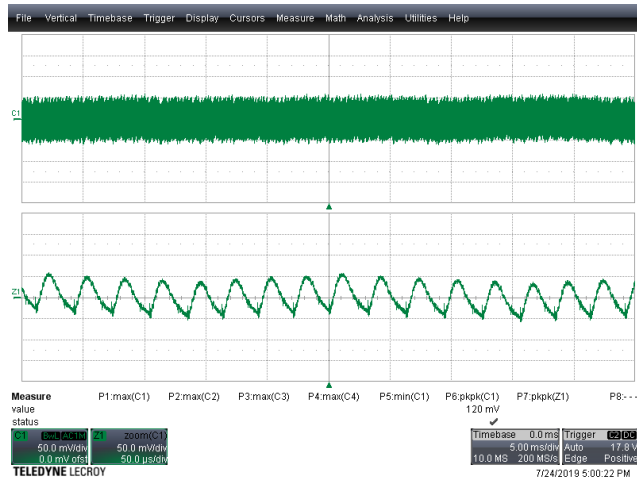
**Figure 82** – Output Voltage Ripple.

$V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 1.875 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 155 \text{ mV}_{P-P}$

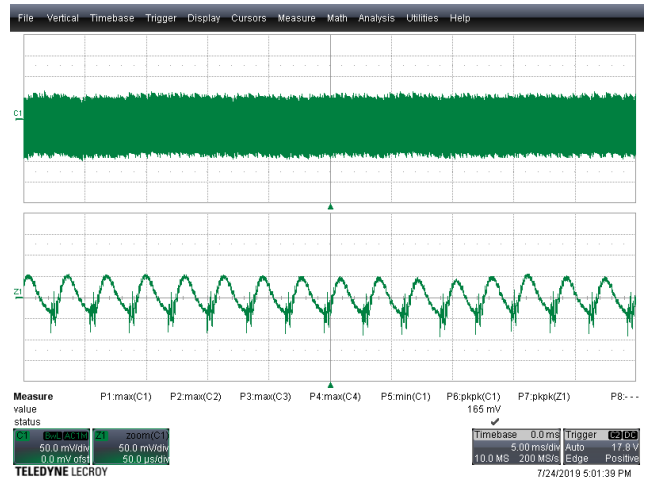
**Figure 83** – Output Voltage Ripple.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 1.875 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 187 \text{ mV}_{P-P}$

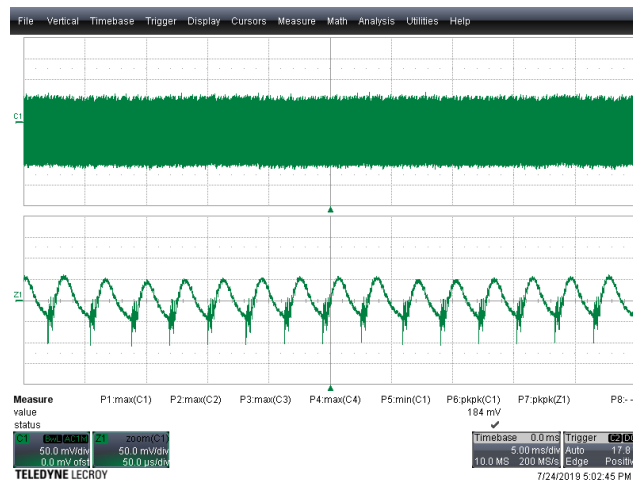
9.3.3 50% Loading Condition

**Figure 84** – Output Voltage Ripple.

$V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 120 \text{ mV}_{P-P}$

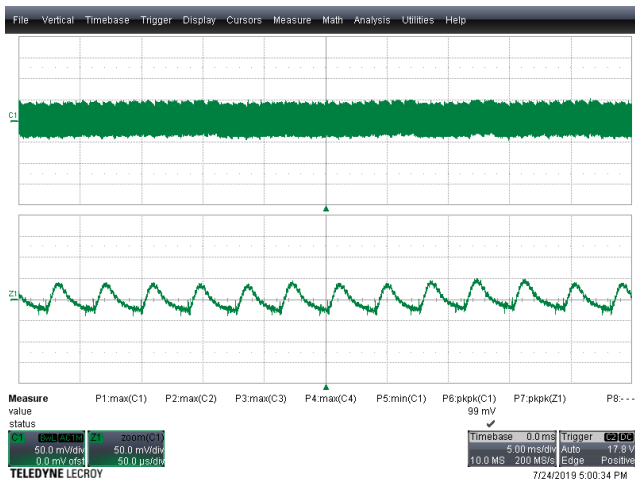
**Figure 85** – Output Voltage Ripple.

$V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 165 \text{ mV}_{P-P}$

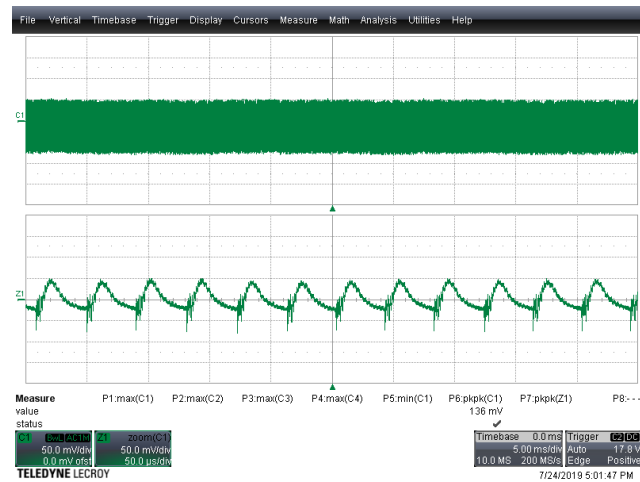
**Figure 86** – Output Voltage Ripple.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 184 \text{ mV}_{P-P}$

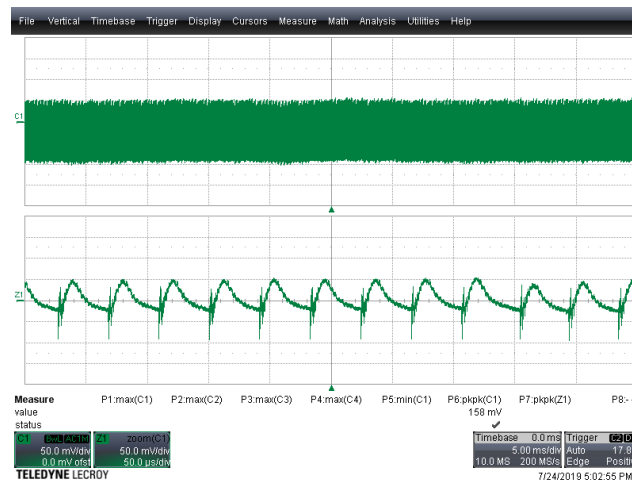
9.3.4 25% Loading Condition

**Figure 87** – Output Voltage Ripple.

$V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 0.625 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 99 \text{ mV}_{P-P}$

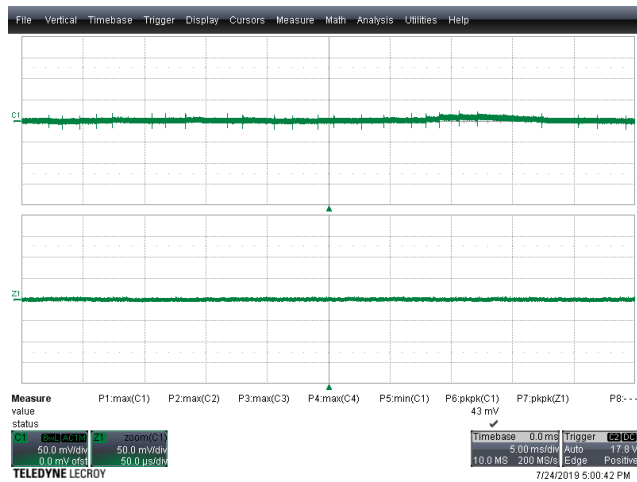
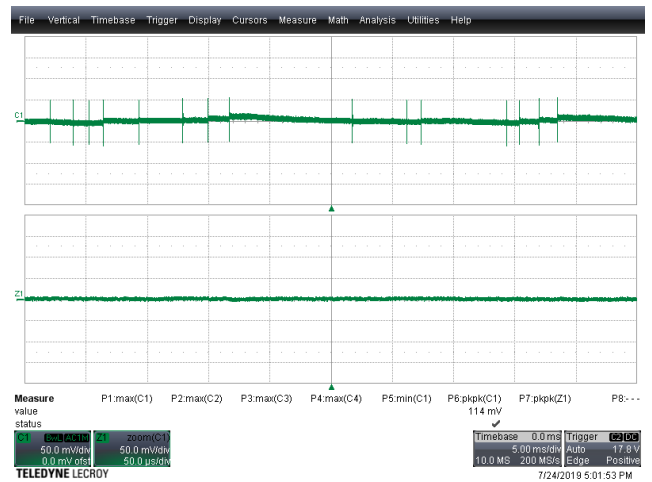
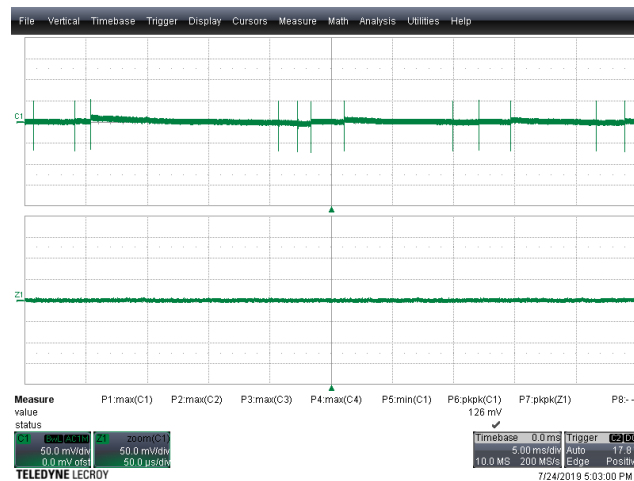
**Figure 88** – Output Voltage Ripple.

$V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 0.625 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 50 μs / div.
 $V_{RIPPLE} = 138 \text{ mV}_{P-P}$

**Figure 89** – Output Voltage Ripple.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 0.625 \text{ A}$.
 Top Half: V_{OUT} , 50 mV, 5 ms / div.
 Bottom Half: Zoom @ 20 μs / div.
 $V_{RIPPLE} = 158 \text{ mV}_{P-P}$

9.3.5 0% Loading Condition

**Figure 90** – Output Voltage Ripple. $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 0 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 50 μs / div. $V_{RIPPLE} = 43 \text{ mV}_{P-P}$ **Figure 91** – Output Voltage Ripple. $V_{IN} = 60 \text{ VDC}$, $I_{OUT} = 0 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 50 μs / div. $V_{RIPPLE} = 114 \text{ mV}_{P-P}$ **Figure 92** – Output Voltage Ripple. $V_{IN} = 130 \text{ VDC}$, $I_{OUT} = 0 \text{ A}$.Top Half: V_{OUT} , 50 mV, 5 ms / div.Bottom Half: Zoom @ 50 μs / div. $V_{RIPPLE} = 126 \text{ mV}_{P-P}$

9.4 Output Load Transient

9.4.1 Output Load Transient, 100% to 50% Load

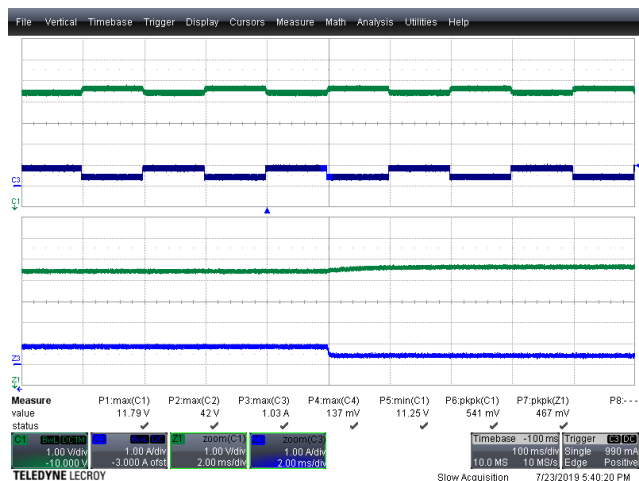


Figure 93 – Output Load Transient, 100% to 50% Load.

$V_{IN} = 30$ VDC, $I_{OUT} = 0.85$ A to 0.425 A

$V_{OUT(MAX)} = 11.79$ V, $V_{OUT(MIN)} = 11.25$ V.

Upper: V_{OUT} , 1 V, 100 ms / div.

Lower: I_{OUT} , 1 A, 100 ms / div.

Bottom Half: Zoom @ 2 ms / div.

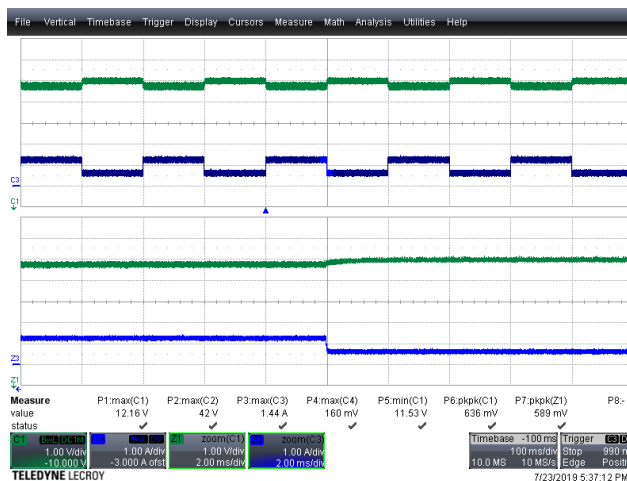


Figure 94 – Output Load Transient, 100% to 50% Load.

$V_{IN} = 60$ VDC, $I_{OUT} = 1.25$ A to 0.625 A.

$V_{OUT(MAX)} = 12.16$ V, $V_{OUT(MIN)} = 11.53$ V.

Upper: V_{OUT} , 1 V, 100 ms / div.

Lower: I_{OUT} , 1 A, 100 ms / div.

Bottom Half: Zoom @ 2 ms / div.

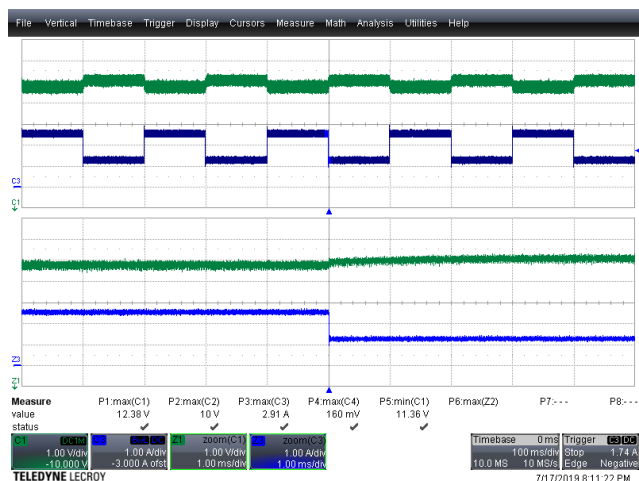


Figure 95 – Output Load Transient, 100% to 50% Load.

$V_{IN} = 130$ VDC, $I_{OUT} = 2.5$ A to 1.25 A.

$V_{OUT(MAX)} = 12.38$ V, $V_{OUT(MIN)} = 11.36$ V.

Upper: V_{OUT} , 1 V, 100 ms / div.

Lower: I_{OUT} , 1 A, 100 ms / div.

Bottom Half: Zoom @ 1 ms / div.

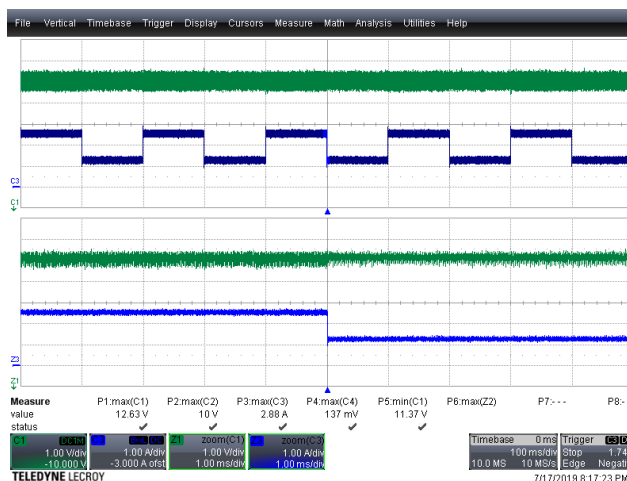


Figure 96 – Output Load Transient, 100% to 50% Load.

$V_{IN} = 400$ VDC, $I_{OUT} = 2.5$ A to 1.25 A.

$V_{OUT(MAX)} = 12.63$ V, $V_{OUT(MIN)} = 11.37$ V.

Upper: V_{OUT} , 1 V, 100 ms / div.

Lower: I_{OUT} , 1 A, 100 ms / div.

Bottom Half: Zoom @ 1 ms / div.

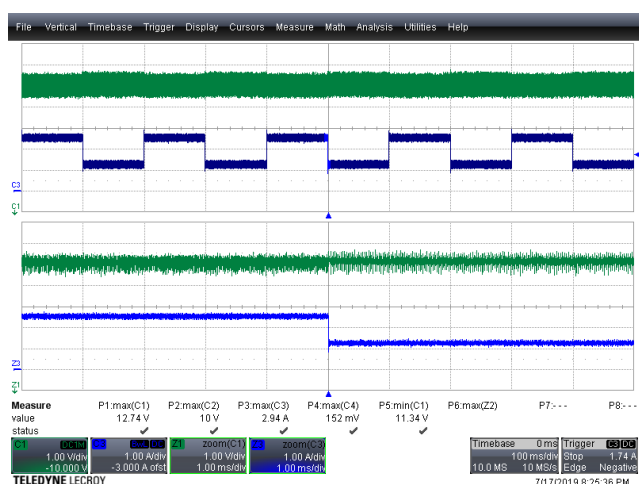


Figure 97 – Output Load Transient, 100% to 50% Load.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$ to 1.25 A .

$V_{OUT(MAX)} = 12.74 \text{ V}$, $V_{OUT(MIN)} = 11.34 \text{ V}$.

Upper: V_{OUT} , 1 V, 100 ms / div.

Lower: I_{OUT} , 1 A, 100 ms / div.

Bottom Half: Zoom @ 2 ms / div.

9.4.2 Output Load Transient, 100% to 0% Load

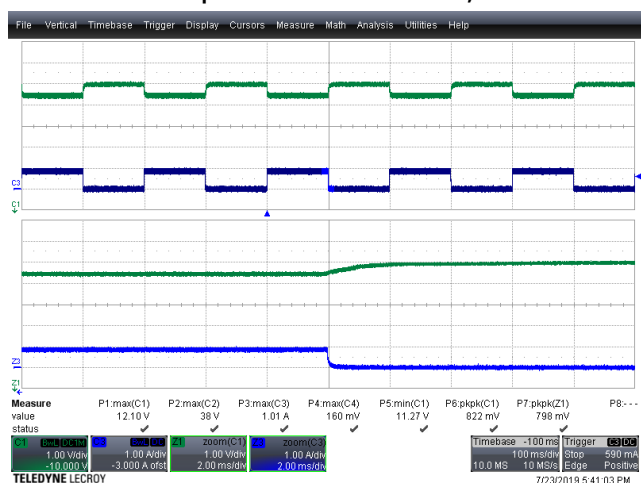


Figure 98 – Output Load Transient, 100% to 0% Load.
 $V_{IN} = 30$ VDC, $I_{OUT} = 0.85$ A to 0 A.
 $V_{OUT(MAX)} = 12.10$ V, $V_{OUT(MIN)} = 11.27$ V.
 Upper: V_{OUT} , 1 V, 100 ms / div.
 Lower: I_{OUT} , 1 A, 100 ms / div.
 Bottom Half: Zoom @ 2 ms / div.

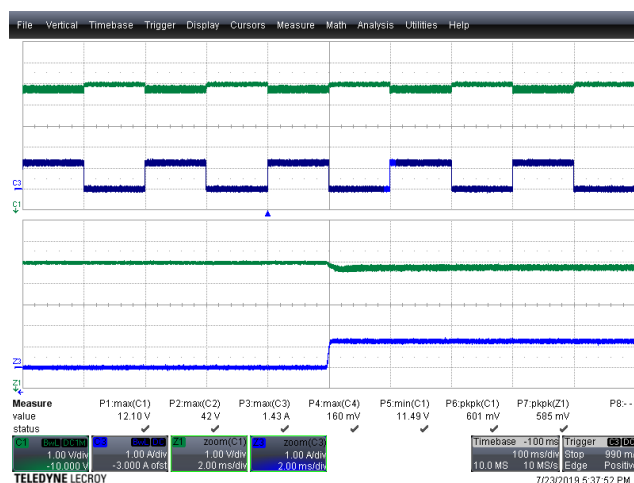


Figure 99 – Output Load Transient, 100% to 0% Load.
 $V_{IN} = 60$ VDC, $I_{OUT} = 1.25$ A to 0 A.
 $V_{OUT(MAX)} = 12.10$ V, $V_{OUT(MIN)} = 11.49$ V.
 Upper: V_{OUT} , 1 V, 100 ms / div.
 Lower: I_{OUT} , 1 A, 100 ms / div.
 Bottom Half: Zoom @ 2 ms / div.

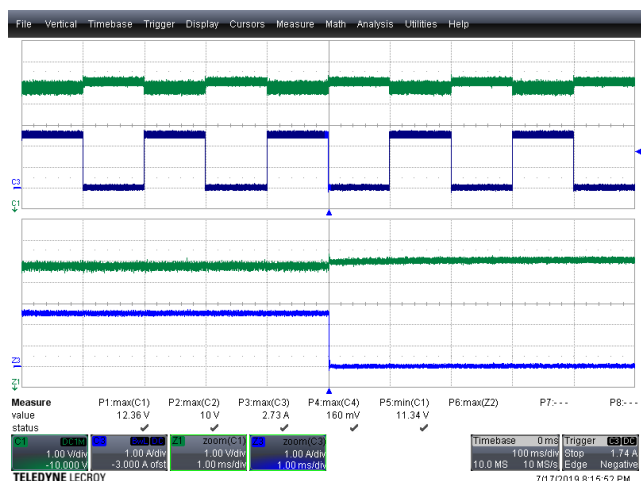


Figure 100 – Output Load Transient, 100% to 0% Load.
 $V_{IN} = 130$ VDC, $I_{OUT} = 2.5$ A to 0 A.
 $V_{OUT(MAX)} = 12.36$ V, $V_{OUT(MIN)} = 11.34$ V.
 Upper: V_{OUT} , 1 V, 100 ms / div.
 Lower: I_{OUT} , 1 A, 100 ms / div.
 Bottom Half: Zoom @ 1 ms / div.

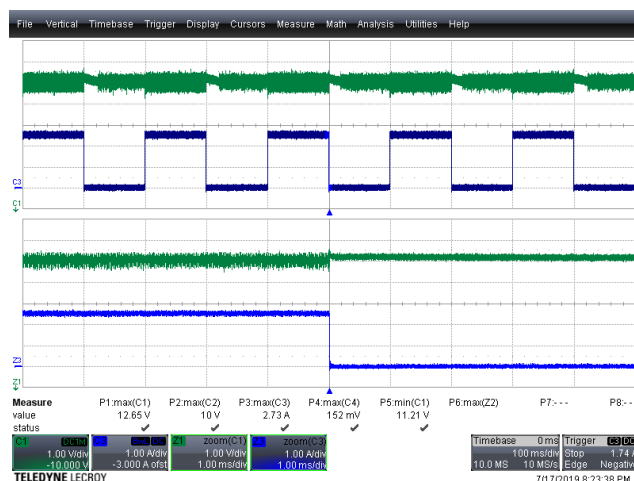


Figure 101 – Output Load Transient, 100% to 0% Load.
 $V_{IN} = 400$ VDC, $I_{OUT} = 2.5$ A to 0 A.
 $V_{OUT(MAX)} = 12.65$ V, $V_{OUT(MIN)} = 11.21$ V.
 Upper: V_{OUT} , 1 V, 100 ms / div.
 Lower: I_{OUT} , 1 A, 100 ms / div.
 Bottom Half: Zoom @ 1 ms / div.

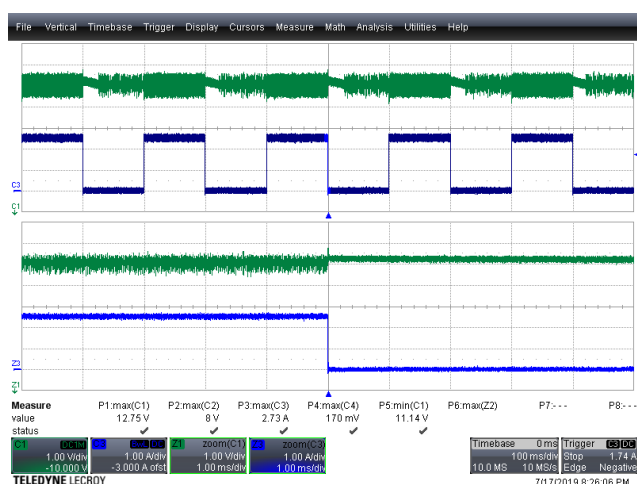


Figure 102 – Output Load Transient, 100% to 0% Load.

$V_{IN} = 550 \text{ VDC}$, $I_{OUT} = 2.5 \text{ A}$ to 1.25 A .

$V_{OUT(MAX)} = 12.75 \text{ V}$, $V_{OUT(MIN)} = 11.14 \text{ V}$.

Upper: V_{OUT} , 1 V, 100 ms / div.

Lower: I_{OUT} , 1 A, 100 ms / div.

Bottom Half: Zoom @ 2 ms / div.

9.5 Output Short-Circuit Auto-Restart Test



Figure 103 – 30 VDC, Output Shorted.
 $V_{IN} = 30$ VDC.
 $AR_{Ton} = 81$ ms, $AR_{Toff} = 1.88$ s.
 Upper: V_{OUT} , 1 V, 1 s / div.
 Lower: I_{OUT} , 1 A, 1 s / div.
 Bottom Half: Zoom @ 10 ms / div.

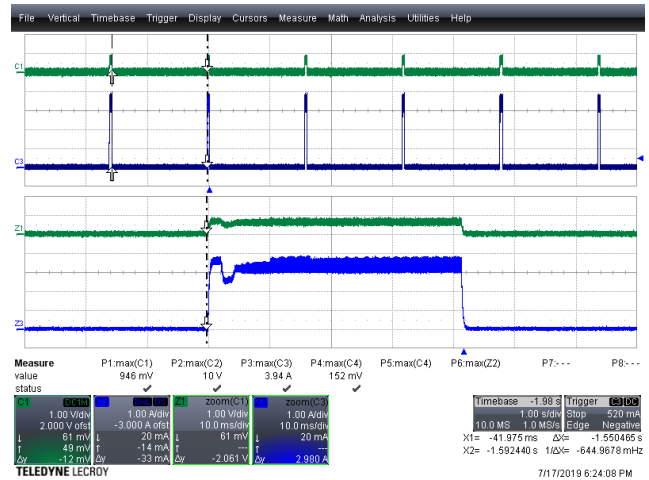


Figure 104 – 60 VDC, Output Shorted.
 $V_{IN} = 60$ VDC.
 $AR_{Ton} = 41$ ms, $AR_{Toff} = 1.55$ s.
 Upper: V_{OUT} , 1 V, 1 s / div.
 Lower: I_{OUT} , 1 A, 1 s / div.
 Bottom Half: Zoom @ 10 ms / div.

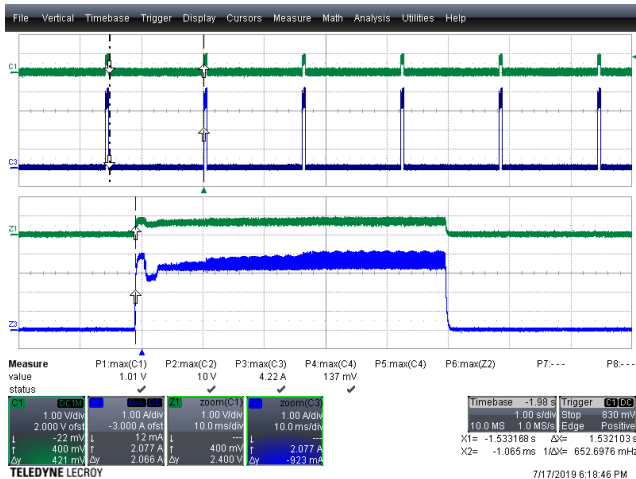


Figure 105 – 130 VDC, Output Shorted.
 $V_{IN} = 130$ VDC.
 $AR_{Ton} = 50$ ms, $AR_{Toff} = 1.53$ s.
 Upper: V_{OUT} , 1 V, 1 s / div.
 Lower: I_{OUT} , 1 A, 1 s / div.
 Bottom Half: Zoom @ 10 ms / div.

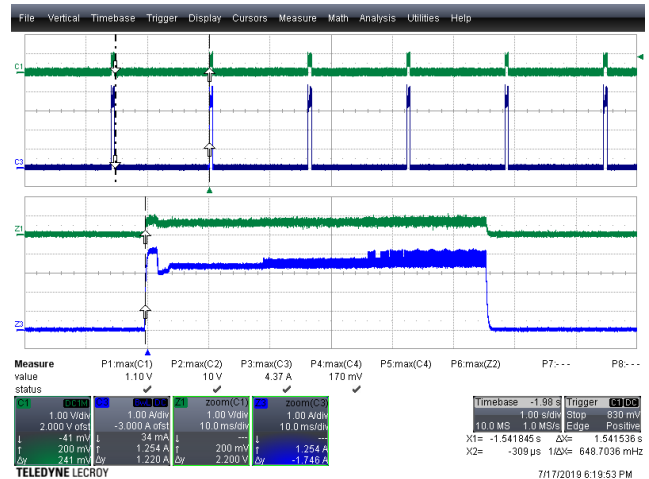


Figure 106 – 400 VDC, Output Shorted.
 $V_{IN} = 400$ VDC.
 $AR_{Ton} = 56$ ms, $AR_{Toff} = 1.54$ s.
 Upper: V_{OUT} , 1 V, 1 s / div.
 Lower: I_{OUT} , 1 A, 1 s / div.
 Bottom Half: Zoom @ 10 ms / div.

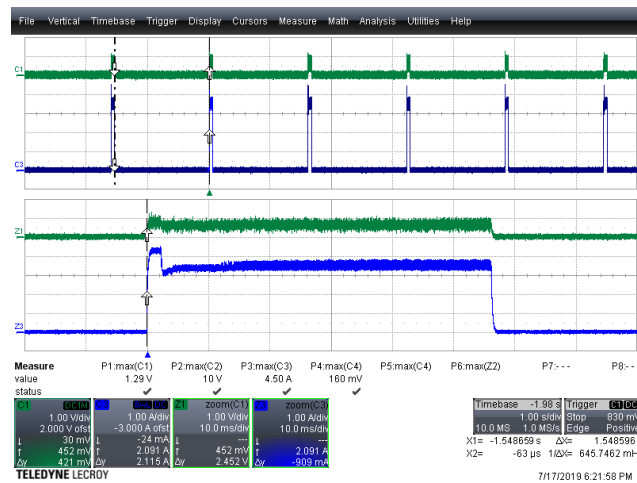


Figure 107 – 550 VDC, Output Shorted.

$V_{IN} = 550 \text{ VDC}$.

$AR_{Ton} = 56 \text{ ms}$, $AR_{Toff} = 1.54 \text{ s}$.

Upper: V_{OUT} , 1 V, 1 s / div.

Lower: I_{OUT} , 1 A, 1 s / div.

Bottom Half: Zoom @ 10 ms / div..

10 Thermal Performance (SR FET)

All measurements have been done at room ambient temperature after 2 hours of continuous operation.

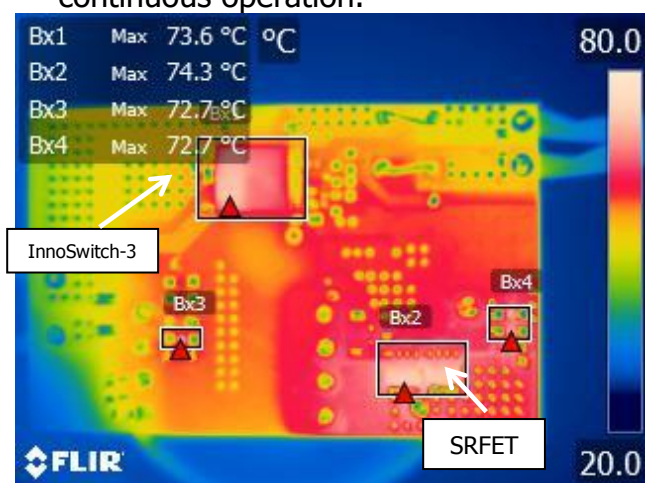


Figure 108 – 130 VDC 2.5 A Full Load.
Temperature of InnoSwitch3-AQ: 73.6 °C.
Temperature of SR FET: 74.3 °C.
Ambient Temperature: 28.5 °C.

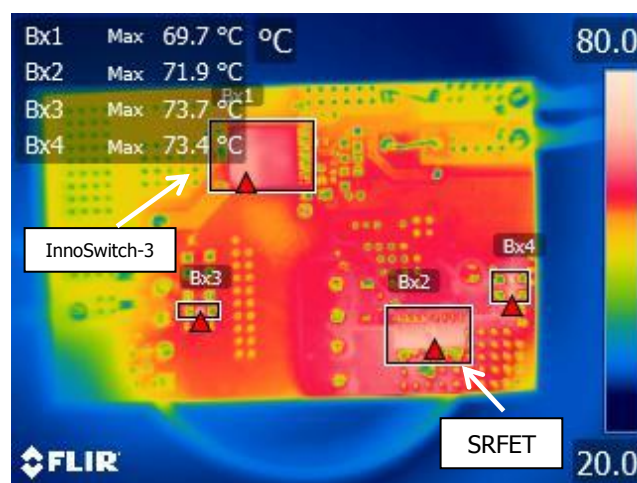


Figure 109 – 400 VDC 2.5 A Full Load.
Temperature of InnoSwitch3-AQ: 69.7 °C.
Temperature of SR FET: 71.9 °C.
Ambient Temperature: 26.8 °C.

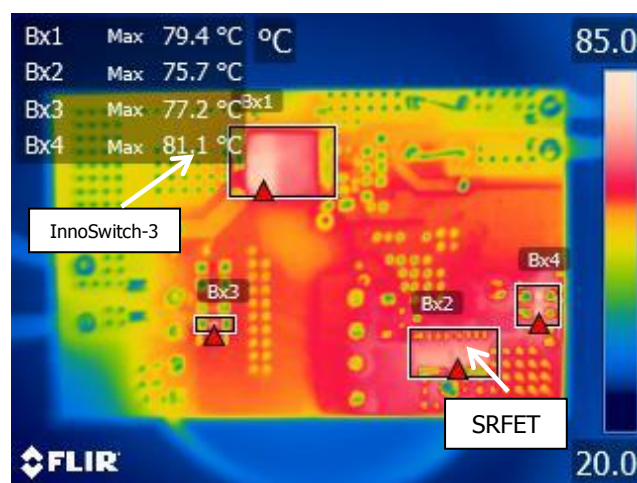
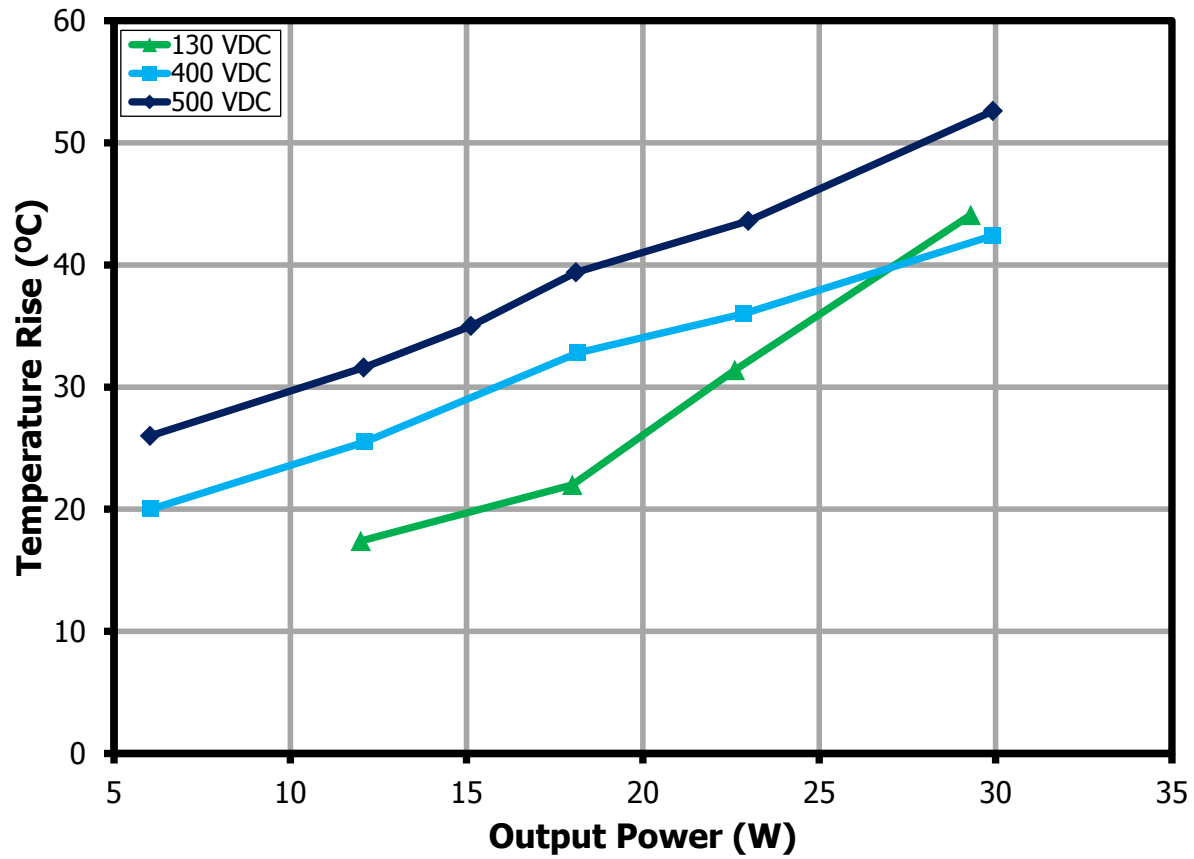


Figure 110 – 500 VDC 2.5 A Full Load.
Temperature of InnoSwitch3-AQ: 79.4 °C.
Temperature of SR FET: 75.7 °C.
Ambient Temperature: 28.2 °C.

Component	130 VDC Temperature (°C)	400 VDC Temperature (°C)	500 VDC Temperature (°C)
U1 (Primary Controller) – Bx1	73.6	69.7	79.4
Q1, Q2 (SR FET) – Bx2	74.3	71.9	75.7
Ambient	28.5	26.8	28.2
IC temperature rise vs. ambient (delta)	45.1	42.9	51.2

10.1 ***INN3977CQ Temperature Rise vs. Output Power*****Figure 111** – Output Power vs. InnoSwitch3-AQ Temperature Rise.

12 Thermal Performance (Qspeed Diode)

All measurements have been done at room ambient temperature after 2 hours of continuous operation.

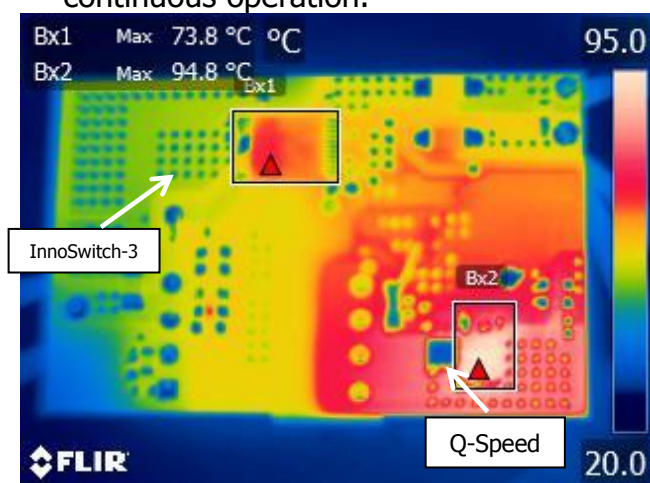


Figure 112 – 130 VDC 2.5A Full Load.
 Temperature of InnoSwitch3-AQ: 73.8 °C.
 Temperature of SR FET: 94.8 °C.
 Ambient Temperature: 27.3 °C.

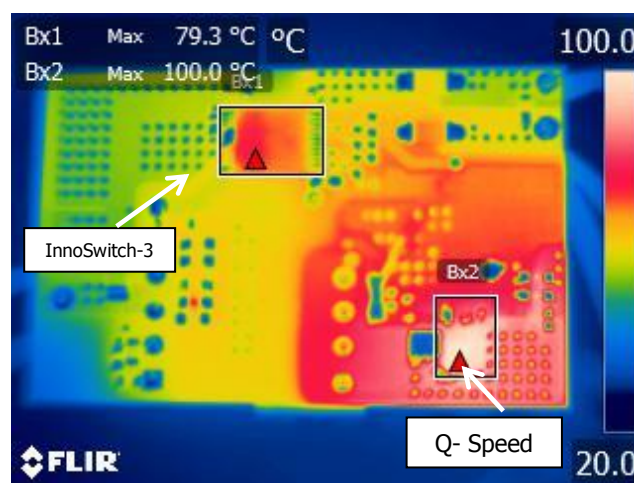


Figure 113 – 400 VDC 2.5A Full Load.
 Temperature of InnoSwitch3-AQ: 79.3 °C.
 Temperature of SR FET: 100 °C.
 Ambient Temperature: 28.3 °C.

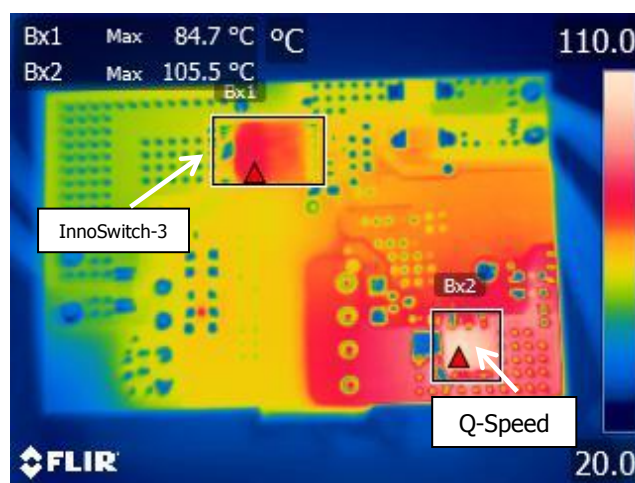


Figure 114 – 500 VDC 2.5A Full Load.
 Temperature of InnoSwitch3-AQ: 84.7 °C.
 Temperature of SR FET: 105.5 °C.
 Ambient Temperature: 27.3 °C .

Component	130 VDC Temperature (°C)	400 VDC Temperature (°C)	500 VDC Temperature (°C)
U1 (Primary Controller) – Bx1	73.8	79.3	84.7
Q1 (Qspeed Diode) – Bx2	94.8	100	105.5
Ambient	27.3	28.3	27.3
IC temperature rise vs. ambient (delta)	46.5	51	57.4

13 -40 °C and +85 °C operational test

Start-up at -40 °C full load						
Ambient (°C)	V_{IN} (VDC)	Input Power (W)	Input Current (mA)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)
-40 °C	30	11.3	505	11.2	0.9	83.7
	60	17.1	470	11.7	1.3	86.4
	130	33.6	518	11.8	2.5	87.8
	400	37.6	287	12.3	2.5	81.8
	550	37.9	239	12.3	2.5	81.1
After one hour running at full load, no OTP occurred						
Ambient (°C)	V_{IN} (VDC)	Input Power (W)	Input Current (mA)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)
85 °C	30	11.6	516	11.51	0.85	84.3
	60	16.5	455	11.66	1.25	88.3
	130	33.5	523	11.56	2.5	86.3
	400	33.5	298	11.74	2.5	87.6
	550	34.6	249	11.75	2.5	84.9

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
11-Feb-20	DK	1.0	Initial Release	Apps & Mktg
09-Apr-20	KM	1.1	Added Test Point Parts	Apps & Mktg
09-Jun-20	KM	1.2	Converted to RDR.	Apps & Mktg
31-Aug-20	KM	1.3	Updated Figure 13.	Apps & Mktg

For the latest updates, visit our website: www.power.com

Reference Designs are technical proposals concerning how to use Power Integrations' gate drivers in particular applications and/or with certain power modules. These proposals are "as is" and are not subject to any qualification process. The suitability, implementation and qualification are the sole responsibility of the end user. The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein. No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.power.com/ip.htm>.

Power Integrations, the Power Integrations logo, CAPZero, ChiPhy, CHY, DPA-Switch, EcoSmart, E-Shield, eSIP, eSOP, HiperPLC, HiperPFS, HiperTFS, InnoSwitch, Innovation in Power Conversion, InSOP, LinkSwitch, LinkZero, LYTSwitch, SENZero, TinySwitch, TOPSwitch, PI, PI Expert, PowiGaN, SCALE, SCALE-1, SCALE-2, SCALE-3 and SCALE-iDriver, are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©2019, Power Integrations, Inc.

Power Integrations Worldwide Sales Support Locations**WORLD HEADQUARTERS**

5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)

Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)

17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)

Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)

HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

INDIA

#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY

Via Milanese 20, 3rd Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN

Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA

RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE

51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN

5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK

Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com



Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Power Integrations:](#)

[RDK-840Q](#)