Boundary Devices
a Laird Connectivity™ company

Datasheet

Nitrogen8M Mini SMARC

Version 1.1

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	11 Jan 2024	Preliminary Release	Jody Van	Gary Bisson
1.1	23 Jan 2024	Update instruction to switch from LVDS to MIPI-DSI in MIPI-DSI vs. LVDS Options. Updated Ordering Information.	Jody Van	Gary Bisson

CONTENTS

1 SCOPE

This document describes key hardware aspects of Boundary Device's Nitrogen8M Mini SMARC system-on-module which is based on the i.MX 8M Mini processor family and the Sona NX611 Wi-Fi/BT combo radio. Data in this document is drawn from several sources and includes information found in the documentation for NXP's i.MX 8M Mini and our Sona NX611.

Note: Information in this document is subject to change. Contact us for the most updated version of this document.

2 INTRODUCTION

The Nitrogen8M Mini SMARC is an integrated platform solution with the NXP i.MX 8M MINI processor that integrates a dual Arm® Cortex®-A53 cluster operating up to 1.8 GHz, a 400 MHz Arm Cortex-M4 and pre-certified dual-band 802.11 a/b/g/n/ac/ax WLAN plus dual-mode Bluetooth® 5.3 Low Energy module.

The Arm® Cortex®-A53 cores bring best-in-class performance and energy efficiency to Linux-based edge applications and the Arm Cortex-M4 processor can perform time-critical real-time compute and control.

Additionally, it offers the latest high-speed interfaces for connectivity and fast data transfer with 2x USB 2.0, 3x SD/SDIO 3.01, 1x Gbit Ethernet with EEE, AVB, IEEE 1588, in addition to 3x UART modules. The memory interfaces supported are 16-bit LPDDR4X and eMMC 5.1.

The module also includes a 4-lane MIPI-CSI camera interface capable of supporting 1080p60 resolution as well as a 4-lane MIPI-DSI output capable of supporting 1080p60 resolution or a 4-lane LVDS one supporting 720p60 for multimedia applications.

The i.MX 8M Mini family implements security via NXP's Cryptographic Accelerator and Assurance Module (CAAM). CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Mini processors, the secure memory provided is 32 KB.

The Nitrogen8M Mini SMARC includes the Sona NX611 which is pre-calibrated and integrates the complete transmit/receive RF paths including diplexer, switches, reference crystal oscillator and power management units (PMU). Two RF connectors (MHF4) on the module provide the most flexibility for antenna selection, installation, and performance. Several high-performance antennas are certified with the Sona NX611 onboard the Nitrogen8M Mini SMARC. A detailed antenna list is shown in the Certified Antennas section.

The Nitrogen8M Mini SMARC has several product SKUs providing different eMMC and LPDDR4 memory configurations, see Ordering Information section.

3 NITROGEN8M MINI SMARC FEATURES SUMMARY

The Nitrogen8M Mini SMARC module complies with the SMARC v2.1 specification from SGET.

Key features of Nitrogen8M Mini SMARC are described in Table 1.

Table 1: Key Features of Nitrogen8M Mini SMARC

Feature	Description
CPU	Quad symmetric Cortex®-A53 processors operation up to 1.8 GHz ▪ 32 KB L1 Instruction Cache ▪ 32 KB L1 Data Cache ▪ 64-bit Armv8-A architecture ▪ 512 KB unified L2 cache Cortex®-M4 core platform operating up to 400 MHz ▪ 16 KB L1 Instruction Cache ▪ 16 KB L1 Data Cache ▪ 256 KB tightly coupled memory (TCM)
Memory interface	▪ On module: 16-bits LPDDR4 with inline ECC (size, please refer to Ordering Information) ▪ On module: 8-bits eMMC 5.1 with HS400 speed (size, please refer Ordering Information) ▪ On carrier: 1 SDXC (4-bit, with extended capacity)

Feature	Description
Video	Video Processing Unit: ▪ 1080p60 VP9 Profile 0, 2 (10-bit) ▪ 1080p60 HEVC/H.265 Decoder ▪ 1080p60 AVC/H.264 Baseline, Main, High decoder ▪ 1080p60 VP8 ▪ 1080p60 AVC/H.264 Encoder ▪ 1080p60 VP8
Graphics Engine	Graphic Processing Unit: ▪ GCNanoUltra for 3D acceleration ▪ GC320 for 2D acceleration
LCDIF Display Controller	The LCDIF can drive one display: ▪ Support up to 2 layers of overlay ▪ Support up to 1080p60 display through MIPI DSI
Display Interfaces	▪ LVDS output from SN65DSI83 ▪ 4-lane MIPI DSI interface (Optional)
Camera Interface	▪ 4-lane MIPI CSI
Audio	▪ Two SAI interface with 1 Tx and 1 Rx lane ▪ One PCM interface to the BT module for SCO operation (when supported by BT chip)
Connectivity	▪ One PCI Express (PCIe) ▪ One USB 2.0 OTG interface ▪ Three USB 2.0 Host interfaces ▪ One Ultra Secure Digital Host Controller (uSDHC) interface ▪ One Gigabit Ethernet controller ▪ Three Universal Asynchronous Receiver/Transmitter (UART) modules ▪ Four I2C modules ▪ Two SPI modules
Security	▪ Resource Domain Controller (RDC) ▪ Arm® TrustZone® (TZ) architecture ▪ On-chip RAM (OCRAM) secure region protection using OCRAM controller ▪ High Assurance Boot (HAB) ▪ Cryptographic acceleration and assurance (CAAM) module and Assurance Module: ▫ Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms ▫ Real-time integrity checker (RTIC) ▫ DRM support for RSA, AES, 3DES, DES ▫ Side channel attack resistance ▫ True random number generation (RNG) ▫ Manufacturing protection support ▪ Secure real-time clock (RTC)
Debug Interface	▪ Secure JTAG controller (SJC)

4 BLOCK DIAGRAM

The figure below shows the block diagram of the Nitrogen8M Mini SMARC which contains the NXP i.MX 8M Mini processor, PMIC and the Sona NX611 Wi-Fi/BT combo.

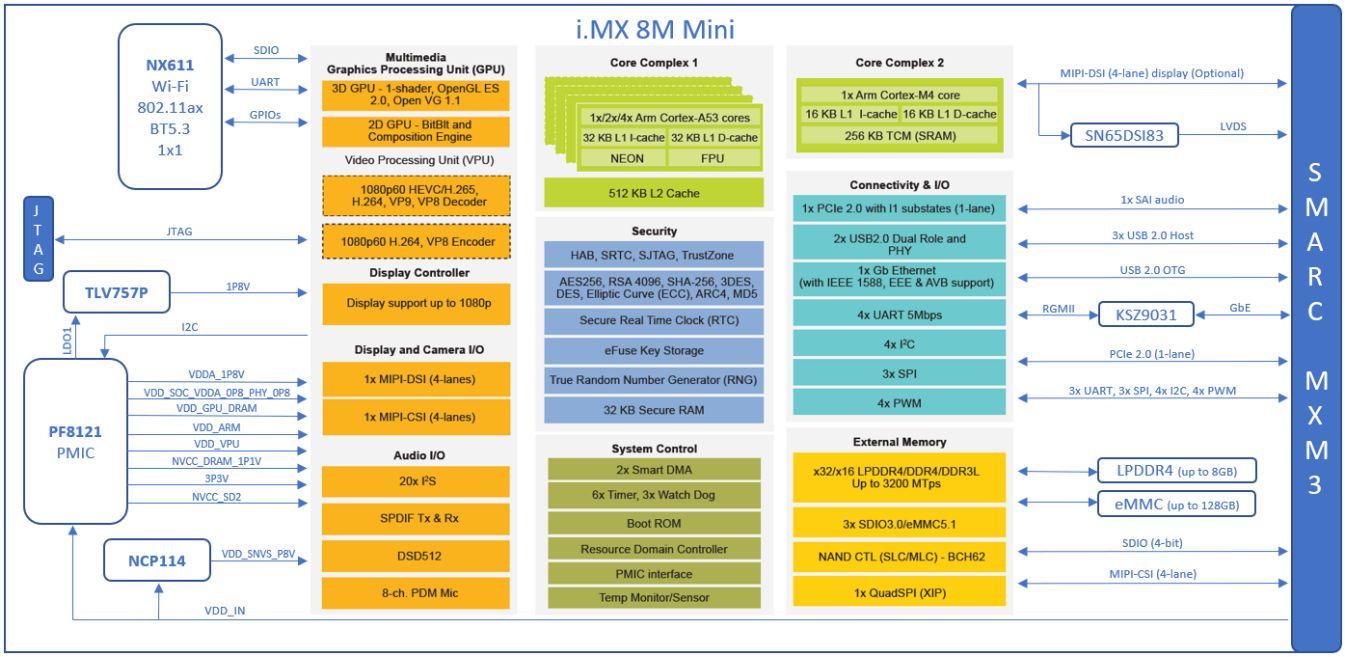


Figure *1*: Nitrogen8M Mini SMARC block diagram

Detailed connections between the NX611 and the i.MX 8M Mini are detailed in Table 2 below.

Table 2: Sona NX611 to i.MX 8M Mini Connections

	NX611	i.MX 8M Mini
SDIO	SDIO_CLK/CMD/DATA[0:3]	SD3
UART	UART_RX/UART_TX/UART_CTS/UART_RTS	UART3 (DAP_TCLK/TMS/TDI/TDO)
CLK	SUSCLK	GPIO1_IO00
BT_EN	W_DISABLE2#	GPIO1_IO05
BT_IRQ	UART_WAKE#	NAND_DQS
WL_EN	W_DISABLE1#	SAI2_RXFS
WL_IRQ	SDIO_WAKE#	GPI01_IO12

5 DC POWER TREE

The Nitrogen8M Mini SMARC requires a primary 5V power supply (VSYS) input. This supply is the main power domain to the on-module NXP PF8121 power management IC (PMIC), which generates all required supply voltages for the module.

Power Modes Diagram

NXP has ten power modes: OTP/TRIM, LP_OFF, QPU_OFF, PWRUP, RUN, STANDBY, WD_RESET, PWRDN, FAULT TRANSITION, AND COIN CELL. Below figure shows the state transition diagram showing the conditions to enter and exit each state.

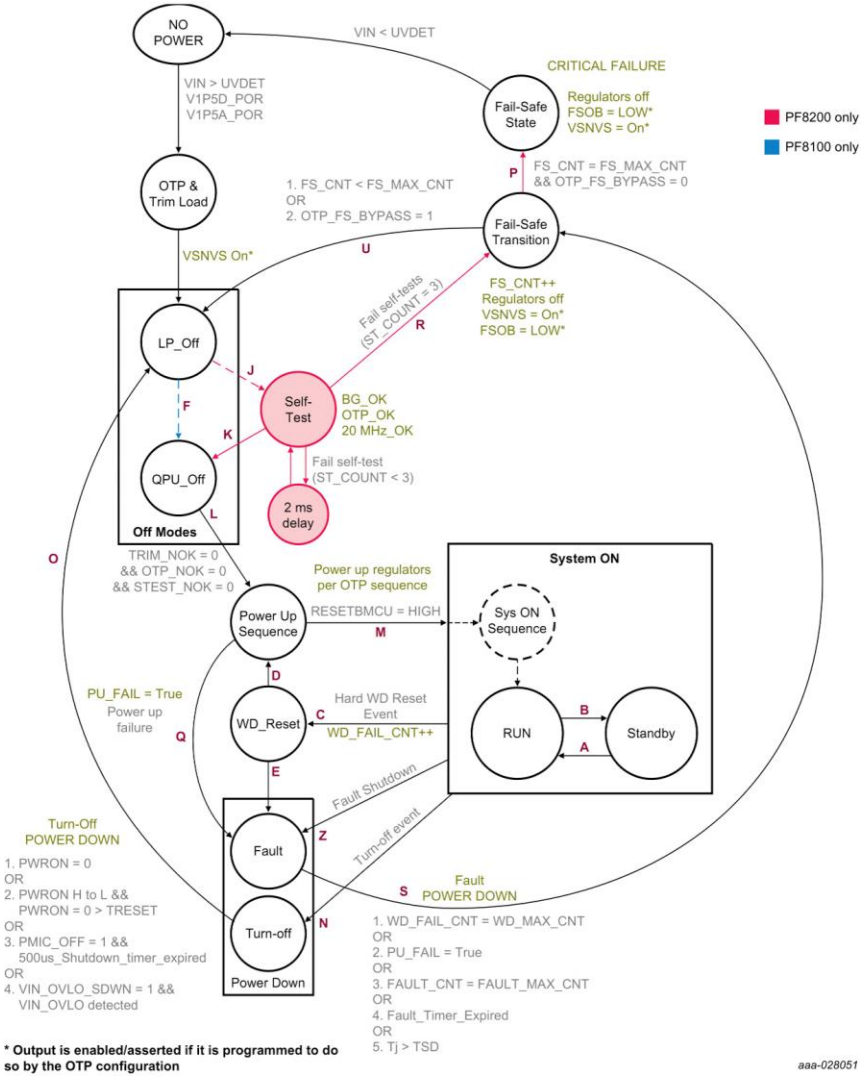


Figure 2: State transition diagram for PMIC

- **OTP/TRIM LOAD mode:**
  Upon VIN application V1P5D and V1P5A regulators are turned on automatically. Once the V1P5D and V1P5A cross their respective POR thresholds, the fuses (for trim and OTP) are loaded into the mirror registers and into the functional I2C registers if configured by the voltage on the VDDOTP pin.
- **LP_OFF Mode:**
  The LP_Off state is a low power off mode selectable by the LPM_OFF bit during the system on modes. By default, the LPM_OFF = 0. When LPM_OFF= 1, the state machine transitions automatically to the QPU_Off state if no power up event has been present and waits in the QPU_Off until a valid power up event is present.

- **QPU_OFF Mode:**
  The QPU_Off state is a higher power consumption off mode, in which all internal circuitry required for a power on is biased and ready to start a power up sequence.
- **PWRUP Mode:**
  During the power up sequence, the external regulators are turned on in a predefined order as programmed by the default (OTP or hardwire) sequence.
- **RUN Mode:**
  In this state, RESETBMCU is released high, and the MCU is expected to boot up and set up specific registers on the PMIC as required during the system boot up process.
- **STANDBY Mode:**
  In this state, the voltage regulators can be preset to a specific low power configuration to reduce the power consumption during system's sleep or state retention modes of operations. The standby state is entered when the STANDBY pin is pulled high or low as defined by the STANBYINV bit below:

STANDBY (pin)	STANDBYINV (I2C bit)	STANDBY control
0	0	Not in Standby Mode
0	1	In Standby Mode
1	0	In Standby Mode
1	1	Not in Standby Mode

- **WD_RESET Mode:**
  When a hard watchdog reset is present, the state machine increments the WD_EVENT_CNT[3:0] register and compares against the WD_MAX_CNT[3:0] register. If WD_EVENT_CNT[3:0] = WD_MAX_CNT[3:0], the state machine detects a cyclic watchdog failure, it powers down the external regulators and proceeds to the fault transition
- **PWRDN Mode:**
  All regulators except VSNVS are disabled as configured in the power down sequence. Two types of events may lead to the power down sequence:
  - Non faulty turn off events: move directly into LP_Off state as soon as power down sequence is finalized
  - Turn off events due to a PMIC fault: move to the fault transition as soon as the power down sequence is finalized
- **FAULT TRANSITION Mode:**
  The fault transition is entered if the PF8121 initiates a turn off event due to a PMIC fault. If the fault transition is entered, the PF8121 provides four FAIL bits to indicate the source of the failure:
  - The PU_FAIL is set to 1 when the device shuts down due to a power up failure
  - The WD_FAIL is set to 1 when the device shuts down due to a watchdog event counter max out
  - The REG_FAIL is set to 1 when the device shuts down due to a regulator failure (fault counter maxed out or fault timer expired)
  - The TSD_FAIL is set to 1 when the device shuts down due to a thermal shutdown
- **COIN CELL Mode:**
  When VIN is not present and LICELL pin has a valid voltage, the device is placed into a coin cell state. Only VSNVS remains on (if programmed to do so by the OTP_VSNVSVOTL[1:0] bits) and is expected to provide power to the SNVS domain on the MCU as long as the LICELL pin has a valid input suitable to supply the configured VSNVS output voltage.

6 Boot mode

The Nitrogen8M Mini SMARC is initialized by sampling the BOOT_MODE0 and BOOT_MODE1 inputs on the rising edge of the POR_B. BOOT_MODE0 goes to FORCE_RECOVERY# and BOOT_MODE1 goes to SMARC BOOT_SEL0.

Table 3: Boot mode combinations

BOOT_MODE [1:0]	BOOT CORE	BOOT MODE
00	Cortex-A53	Boot from Internal Fuses
01	Cortex-A53	Serial Download (USB1)
10	Cortex-A53	USDHC1 8-bit eMMC 5.1 (default)
11	Cortex-A53	Reserved

7 Electrical Characteristic and Power Consumption

Absolute Maximum Ratings

Table 4 summarizes the absolute maximum ratings and Table 5 lists the recommended operating conditions for the Nitrogen8M Mini SMARC product series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 4: Absolute maximum ratings

Symbol (Domain)	Parameter	Min.	Max	Unit
VSYS	Input voltage for the SOM	-0.5	+6.0	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	-0.3	+2.1	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	-0.3	+3.6	V
$T_{STORAGE}$	Storage Temperature Range	-40	+125	°C
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	NA	+10	dBm
ESD	Electrostatic discharge tolerance	-2000	+2000	V

Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VSYS	Input voltage for the SOM	3.3	3.8	5.5	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	1.71	1.8	1.89	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	3.0	3.3	3.6	V
T-ambient	Operating Ambient temperature	-40	25	85	°C

Note: The operating ambient temperature ratings are highly dependent on the design-case, such as the enclosure design, system design, processor activity, GPU/VPU activity, and peripherals used.

Running over 70° C ambient temperature typically requires the implementation of thermal management strategies such as passive (heatsink/spreader). Please contact Boundary Devices if you need information and guidance for thermal management.

DC current consumption

Several power saving modes are available and are listed in Table 6.

Note: These figures are estimates and subject to change.

Table 6: Typical current consumption

Mode	Description	Current (Avg)
Power Saving Mode	CPU is on, Stay on Wi-Fi connection only.	194mA
RAM Suspend Mode	CPU is on, memory and wireless connection are off	53mA
Stress Test	WiFi + Eth0 + GPU	760mA
Stress Test	WiFi + Eth0 + CPU/GPU/iperf	840mA

8 Module pin out and Pinmux table

Table 7 lists the pin multiplexing (PIN-MUX) of the Nitrogen8M Mini SMARC.

PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

NXP process has configurable internal Pull-up (PU) and pull-down (PD) resistor whose values are listed below. During a reset condition, the PU and PD state are pre-defined and cannot be changed.

Table 7: Resistor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Pull-up (PU) resistor	VDD=1.65 to 1.95V Temp=0 to 95℃	12	22	49	kΩ
Pull-down (PD) resistor		13	23	48	kΩ
Pull-up (PU) resistor	VDD=3.0 to 3.6V Temp=0 to 95℃	18	37	72	kΩ
Pull-down (PD) resistor		24	43	87	kΩ

Pin configuration for the i.MX is achieved using a suite of evaluation and configuration tools that assists users from initial evaluation to production software development. Users can download the tool from the NXP website: https://www.nxp.com/design/designs/config-tools-for-i-mx-applications-processors:CONFIG-TOOLS-IMX?tab=Design_Tools_Tab

Table 8: Pinout table for Nitrogen8M Mini SMARC edge connector (J2)

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P1	SMB_ALERT#	**SAI:** SAI5_RXD1 **SAI:** SAI1_TX_DATA3 **SAI:** SAI1_TX_SYNC **SAI:** SAI5_TX_SYNC **PDM:** PDM_DATA1 **GPIO:** GPIO3_IO22	DI	1.8 V	
P2	GND	NA	-	NA	
P3	CSI1_CK+	MIPI_CSI_CLK_P	DO	NA	
P4	CSI1_CK-	MIPI_CSI_CLK_N	DO	NA	
P5	GBE1_SDP	NA	-	NA	
P6	GBE0_SDP	**GPIO:** GPIO1_IO09 **ENET:** ENET1_1588_EVENT0_OUT **SDMA:** SDMA2_EXT_EVENT0 **CCM**: CCMSCPCMIX_STOP **NAND**: RAWNAND_TEST_TRIG	DI/O	3.3V	
P7	CSI1_D0+	MIPI_CSI_D0_P	DI	1.8V	
P8	CSI1_D0-	MIPI_CSI_D0_N	DI	1.8V	
P9	GND	NA	-	NA	
P10	CSI1_D1+	MIPI_CSI_D1_P	DI	1.8V	
P11	CSI1_D1-	MIPI_CSI_D1_N	DI	1.8V	
P12	GND	NA	-	NA	
P13	CSI1_D2+	MIPI_CSI_D2_P	DI	1.8V	
P14	CSI1_D2-	MIPI_CSI_D2_N	DI	1.8V	
P15	GND	NA	-	NA	
P16	CSI1_D3+	MIPI_CSI_D3_P	DI	1.8V	
P17	CSI1_D3-	MIPI_CSI_D3_N	DI	1.8V	
P18	GND	NA	-	NA	
P19	GBE0_MDI3-	TXRXM_D	DI/O	1.8V	From KSZ9031RN (U10)
P20	GBE0_MDI3+	TXRXP_D	DI/O	1.8V	From KSZ9031RN (U10)
P21	GBE0_LINK100#	LED2	DO	3.3V	From KSZ9031RN (U10)
P22	GBE0_LINK1000#	LED2	DO	3.3V	From KSZ9031RN (U10)
P23	GBE0_MDI2-	TXRXM_C	DI/O	1.8V	From KSZ9031RN (U10)
P24	GBE0_MDI2+	TXRXP_C	DI/O	1.8V	From KSZ9031RN (U10)
P25	GBE0_LINK#_ACT#	LED1	DO	3.3V	From KSZ9031RN (U10)
P26	GBE0_MDI1-	TXRXM_B	DI/O	1.8V	From KSZ9031RN (U10)
P27	GBE0_MDI1+	TXRXP_B	DI/O	1.8V	From KSZ9031RN (U10)
P28	GBE0_CTREF	TP9	-	NA	Test point

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P29	GBE0_MDI0-	TXRXM_A	DI/O	1.8V	From KSZ9031RN (U10)
P30	GBE0_MDI0+	TXRXP_A	DI/O	1.8V	From KSZ9031RN (U10)
P31	SPI0_CS1#	**SPDIF**: SPDIF1_OUT **PWM**: PWM3_OUT **GPIO**: GPIO5_IO3 **TPSMP**: TPSMP_HDATA5	DO	1.8V	
P32	GND	NA	-	NA	
P33	SDIO_WP	**USDHC**: USDHC2_WP **GPIO**: GPIO2_IO20 **SIM**: SIM_M_HMASTLOCK	DI	1.8 or 3.3V	
P34	SDIO_CMD	**USDHC**: USDHC2_CMD **GPIO**: GPIO2_IO14 **CCM**: CCMSRCGPCMIX_OBSERVE1 **OBSERVE**: OBSERVE_MUX_OUT1	DI/O	1.8 or 3.3V	
P35	SDIO_CD	**USDHC**: USDHC2_CD_B **GPIO**: GPIO2_IO12	DI	1.8 or 3.3V	
P36	SDIO_CLK	**USDHC**: USDHC2_CLK **GPIO**: GPIO2_IO13 **CCM**: CCMSRCGPCMIX_OBSERVE0 **OBSERVE**: OBSERVE_MUX_OUT0	DO	1.8 or 3.3V	
P37	SDIO_PWR_EN	**USDHC**: USDHC2_RESET_B **GPIO**: GPIO2_IO19 **CCM**: CCMSRCGPCMIX_SYSTEM_RESET	DO	1.8 or 3.3V	
P38	GND	NA	-	NA	
P39	SDIO_D0	**USDHC**: USDHC2_DATA0 **GPIO**: GPIO2_IO15 **CCM**: CCMSRCGPCMIX_OBSERVE2 **OBSERVE**: OBSERVE_MUX_OUT2	DI/O	1.8 or 3.3V	
P40	SDIO_D1	**USDHC**: USDHC2_DATA1 **GPIO**: GPIO2_IO16 **CCM**: CCMSRCGPCMIX_WAIT **OBSERVE**: OBSERVE_MUX_OUT3	DI/O	1.8 or 3.3V	
P41	SDIO_D2	**USDHC**: USDHC2_DATA2 **GPIO**: GPIO2_IO17 **CCM**: CCMSRCGPCMIX_STOP **OBSERVE**: OBSERVE_MUX_OUT4	DI/O	1.8 or 3.3V	
P42	SDIO_D3	**USDHC**: USDHC2_DATA3 **GPIO**: GPIO2_IO18 **CCM**: CCMSRCGPCMIX_EARLY_RESET	DI/O	1.8 or 3.3V	
P43	SPI0_CS0#	**SPI**: ECSPI2_SS0 **UART**: UART4_DCE_RTS_B **UART**: UART4_DTE_CTS_B **GPIO**: GPIO5_IO13 **TPSMP**: TPSMP_HDATA15	DO	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P44	SPI0_CK	**SPI**: ECSPI2_SCLK **UART**: UART4_DCE_RX **UART**: UART4_DTE_TX **GPIO**: GPIO5_IO10 **TPSMP**: TPSMP_HDATA12	DO	1.8V	
P45	SPIO_DIN	**SPI**: ECSPI2_MISO **UART**: UART4_DCE_CTS_B **UART**: UART4_DTE_RTS_B **GPIO**: GPIO5_IO12 **TPSMP**: TPSMP_HDATA14	DI	1.8V	
P46	SPIO_DO	**SPI**: ECSPI2_MOSI **UART**: UART4_DCE_TX **UART**: UART4_DTE_RX **GPIO**: GPIO5_IO11 **TPSMP**: TPSMP_HDATA13	DO	1.8V	
P47	GND	NA	-	NA	
P48	SATA_TX+	NA	-	NA	
P49	SATA_TX-	NA	-	NA	
P50	GND	NA	-	NA	
P51	SATA_RX+	NA	-	NA	
P52	SATA_RX-	NA	-	NA	
P53	GND	NA	-	NA	
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	**CE0**: RAWNAND_CE0_B **SPI**: QSPI_A_SS0_B **GPIO**: GPIO3_IO1 **SIM**: SIM_M_HPROT1	DO	1.8V	
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#1	**GPIO**: GPIO1_IO6 **ENET**: ENET1_MDC **USDHC**: USDHC1_CD_B **CCM**: CCMSRCGPCMIX_EXT_CLK3 **SPI**: ECSPI1_TEST_TRIG	DO	1.8V	
P56	SPI1_CK / ESPI_CK / QSPI_CK	**ALE**: RAWNAND_ALE **SPI**: QSPI_A_SCLK **GPIO**: GPIO3_IO0 **SIM**: SIM_M_HPROT0	DO	1.8V	
P57	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	**DATA**: RAWNAND_DATA00 **SPI**: QSPI_A_DATA0 **GPIO**: GPIO3_IO6 **SIM**: SIM_M_HADDR2	DI	1.8V	
P58	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	**DATA**: RAWNAND_DATA01 **SPI**: QSPI_A_DATA1 **GPIO**: GPIO3_IO7 **SIM**: SIM_M_HADDR3	DO	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P59	GND	NA	-	NA	
P60	USB0+	USB1_DP	DI/O	3.3V	
P61	USB0-	USB1_DN	DI/O	3.3V	
P62	USB0_EN_OC	**GPIO**: GPIO1_IO13 **USB**: USB1_OTG_OC **PWM**: PWM2_OUT **CCM**: CCMSRCGPCMIX_OUT2 **CSU**: CSU_CSU_ALARM_AUT1	DO	3.3V	
P63	USB0_VBUS_DET	USB1_VBUS	DI	5V	
P64	USB0_OTG_ID	USB1_ID	DI	3.3V	
P65	USB1+	BDP_DN1	DI/O	3.3V	From USB2513B (U12)
P66	USB1-	BDM_DN1	DI/O	3.3V	From USB2513B (U12)
P67	USB1_EN_OC	PRTPWR1	DI	3.3V	From USB2513B (U12)
P68	GND	NA	-	NA	
P69	USB2+	BDP_DN2	DI/O	3.3V	From USB2513B (U12)
P70	USB2-	BDM_DN2	DI/O	3.3V	From USB2513B (U12)
P71	USB2_EN_OC	PRTPWR2	DI	3.3V	From USB2513B (U12)
P72	RSVD_01	CLKOUT1	DI	1.8V	
P73	RSVD_02	CLKOUT2	DI	1.8V	
P74	USB3_EN_OC	PRTPWR3	DI	3.3V	From USB2513B (U12)
P75	PCIE_A_RST	**CE**: RAWNAND_CE1_B **SPI**: QSPI_A_SS1_B **USD**: USDHC3_STROBE **GPIO**: GPIO3_IO2 **SIM**: SIM_M_HPROT2	DI/O	3.3V	
P76	USB4_EN_OC#	NA	-	NA	
P77	PCIE_B_CKREQ-	NA	-	NA	
P78	PCIE_CLK_REQ	**SAI**: SAI3_RX_BCLK **GPT**: GPT1_CLK **SAI**: SAI5_RX_BCLK **UART**: UART2_DCE_CTS_B **UART**: UART2_DTE_RTS_B **GPIO**: GPIO4_IO29 **TPSMP**: TPSMP_HTRANS1	DI/O	3.3V	
P79	GND	NA	-	NA	
P80	PCIE_C_REFCK+	NA	-	NA	
P81	PCIE_C_REFCK-	NA	-	NA	
P82	GND	NA	-	NA	
P83	PCIE_A_REFCK+	PCIE_CLK_P			
P84	PCIE_A_REFCK-	PCIE_CLK_N			

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P85	GND	NA	-	NA	
P86	PCIE_A_RX+	PCIE_RXN_P			
P87	PCIE_A_RX-	PCIE_RXN_N			
P88	GND	NA	-	NA	
P89	PCIE_A_TX+	PCIE_TXN_P			
P90	PCIE_A_TX-	PCIE_TXN_N			
P91	GND	NA	-	NA	
P92	HDMI_D2+ / DP1_LANE0+	NA	-	NA	
P93	HDMI_D2- / DP1_LANE0-	NA	-	NA	
P94	GND	NA	-	NA	
P95	HDMI_D1+ / DP1_LANE1+	NA	-	NA	
P96	HDMI_D1- / DP1_LANE1-	NA	-	NA	
P97	GND	NA	-	NA	
P98	HDMI_D0+ / DP1_LANE2+	NA	-	NA	
P99	HDMI_D0- / DP1_LANE2-	NA	-	NA	
P100	GND	NA	-	NA	
P101	HDMI_CK+ / DP1_LANE3+	NA	-	NA	
P102	HDMI_CK- / DP1_LANE3-	NA	-	NA	
P103	GND	NA	-	NA	
P104	HDMI_HPD / DP1_HPD	NA	-	NA	
P105	HDMI_CTRL_CK / DP1_AUX+	NA	-	NA	
P106	HDMI_CTRL_DAT / DP1_AUX-	NA	-	NA	
P107	DP1_AUX_SEL	NA	-	NA	
P108	GPIO0 / CAM0_PWR	**SAI**: SAI5_RX_DATA0 **SAI**: SAI1_TX_DATA2 **PDM**: PDM_DATA0 **GPIO**: GPIO3_IO21	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P109	GPIO1 / CAM1_PWR	**SAI**: SAI1_TX_DATA7 **SAI**: SAI6_MCLK **PDM**: PDM_CLK **TRACE**: CORESIGHT_TRACE15 **GPIO**: GPIO4_IO19 **CCM**: CCMSRCGPCMIX_BOOT_CFG15 **SIM**: SIM_M_HBURST2	DI/O	1.8V	
P110	GPIO2 / CAM0_RST	**SAI**: SAI1_RX_SYNC **SAI**: SAI5_RX_SYNC **TRACE**: CORESIGHT_TRACE_CLK **GPIO**: GPIO4_IO0 **SIM**: SIM_M_HADDR15	DI/O	1.8V	
P111	GPIO3 / CAM1_RST	**SAI**: SAI1_RX_BCLK **SAI**: SAI5_RX_BCLK **TRACE**: CORESIGHT_TRACE_CTL **GPIO**: GPIO4_IO1 **SIM**: SIM_M_HADDR16	DI/O	1.8V	
P112	GPIO4 / HDA_RST#	**SAI**: SAI1_RX_DATA1 **SAI**: SAI5_RX_DATA1 **PDM**: PDM_DATA1 **TRACE**: CORESIGHT_TRACE1 **GPIO**: GPIO4_IO3 **CCM**: CCMSRCGPCMIX_BOOT_CFG1 **SIM**: SIM_M_HADDR18	DI/O	1.8V	
P113	GPIO5 / PWM_OUT	**SAI**: SAI3_MCLK **PWM**: PWM4_OUT **SAI**: SAI5_MCLK **GPIO**: GPIO5_IO2 **TPSMP**: TPSMP_HDATA4	DI/O	1.8V	
P114	GPIO6 / TACHIN	**SAI**: SAI1_RX_DATA2 **SAI**: SAI5_RX_DATA2 **PDM**: PDM_DATA2 **TRACE**: CORESIGHT_TRACE2 **GPIO**: GPIO4_IO4 **CCM**: CCMSRCGPCMIX_BOOT_CFG2 **SIM**: SIM_M_HADDR19	DI/O	1.8V	
P115	GPIO7	**SAI**: SAI1_RX_DATA3 **SAI**: SAI5_RX_DATA3 **PDM**: PDM_DATA3 **TRACE**: CORESIGHT_TRACE3 **GPIO**: GPIO4_IO5 **CCM**: CCMSRCGPCMIX_BOOT_CFG3 **SIM**: SIM_M_HADDR20	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P116	GPIO8	**SAI**: SAI1_RX_DATA4 **SAI**: SAI6_TX_BCLK **SAI**: SAI6_RX_BCLK **TRACE**: CORESIGHT_TRACE4 **GPIO**: GPIO4_IO6 **CCM**: CCMSRCGPCMIX_BOOT_CFG4 **SIM**: SIM_M_HADDR21	DI/O	1.8V	
P117	GPIO9	**SAI**: SAI1_RX_DATA5 **SAI**: SAI6_TX_DATA0 **SAI**: SAI6_RX_DATA0 **SAI**: SAI1_RX_SYNC **TRACE**: CORESIGHT_TRACE5 **GPIO**: GPIO4_IO7 **CCM**: CCMSRCGPCMIX_BOOT_CFG5 **SIM**: SIM_M_HADDR22	DI/O	1.8V	
P118	GPIO10	**SAI**: SAI1_RX_DATA6 **SAI**: SAI6_TX_SYNC **SAI**: SAI6_RX_SYNC **TRACE**: CORESIGHT_TRACE6 **GPIO**: GPIO4_IO8 **CCM**: CCMSRCGPCMIX_BOOT_CFG6 **SIM**: SIM_M_HADDR23	DI/O	1.8V	
P119	GPIO11	**SAI**: SAI1_RX_DATA7 **SAI**: SAI6_MCLK **SAI**: SAI1_TX_SYNC **SAI**: SAI1_TX_DATA4 **TRACE**: CORESIGHT_TRACE7 **GPIO**: GPIO4_IO9 **CCM**: CCMSRCGPCMIX_BOOT_CFG7 **SIM**: SIM_M_HADDR24	DI/O	1.8V	
P120	GND	NA	-	NA	
P121	I2C_PM_CK	**I2C**: I2C4_SC **PWM**: PWM2_OUT **PCIE**: PCIE1_CLKREQ_B **GPIO**: GPIO5_IO20 **TPSMP**: TPSMP_HDATA22	DI/O	1.8V	
P122	I2C_PM_DAT	**I2C**: I2C4_SDA **PWM**: PWM1_OUT **PCIE**: PCIE2_CLKREQ_B **GPIO**: GPIO5_IO21 **TPSMP**: TPSMP_HDATA23	DI/O	1.8V	
P123	BOOT_SEL0#	BOOT_MODE1	DI	1.8V	
P124	BOOT_SEL1#	NA	-	NA	
P125	BOOT_SEL2#	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P126	RESET_OUT#	**SAI**: SAI2_RX_BCLK **SAI**: SAI5_TX_BCLK **UART**: UART1_DCE_RX **UART**: UART1_DTE_TX **GPIO**: GPIO4_IO22 **SIM**: SIM_M_HSIZE1	DI/O	1.8V	
P127	RESET_IN#	POR_B	DI	1.8V – 5V	
P128	POWER_BTN#	ONOFF	DI	1.8	
P129	SER0_TX	**UART**: UART1_DCE_TX **UART**: UART1_DTE_RX **SPI**: ECSPI3_MOSI **GPIO**: GPIO5_IO23 **TPSMP**: TPSMP_HDATA25	DO	1.8V	
P130	SER0_RX	**UART**: UART1_DCE_RX **UART**: UART1_DTE_TX **SPI**: ECSPI3_SCLK **GPIO**: GPIO5_IO22 **TPSMP**: TPSMP_HDATA24	DI	1.8V	
P131	SER0_RTS#	**UART:** UART3_DCE_TX **UART**: UART3_DTE_RX **UART**: UART1_DCE_RTS_B **UART**: UART1_DTE_CTS_B **GPIO**: GPIO5_IO27 **TPSMP**: TPSMP_HDATA29	DI	1.8V	
P132	SER0_CTS#	**UART:** UART3_DCE_RX **UART**: UART3_DTE_TX **UART**: UART1_DCE_CTS_B **UART**: UART1_DTE_RTS_B **GPIO**: GPIO5_IO26 **TPSMP**: TPSMP_HDATA28	DO	1.8V	
P133	GND	NA	-	NA	
P134	SER1_TX	**UART**: UART2_DCE_TX **UART**: UART2_DTE_RX **SPI**: ECSPI3_SS0 **GPIO**: GPIO5_IO25 **TPSMP**: TPSMP_HDATA27	DO	1.8V	
P135	SER1_RX	**UART**: UART2_DCE_RX **UART**: UART2_DTE_TX **SPI**: ECSPI3_MISO **GPIO**: GPIO5_IO24 **TPSMP**: TPSMP_HDATA26	DI	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P136	SER2_TX	**UART**: UART4_DCE_TX **UART**: UART4_DTE_RX **UART**: UART2_DCE_RTS_B **UART**: UART2_DTE_CTS_B **PCIE**: PCIE2_CLKREQ_B **GPIO**: GPIO5_IO29 **TPSMP**: TPSMP_HDATA31	DO	1.8V	
P137	SER2_RX	**UART**: UART4_DCE_RX **UART**: UART4_DTE_TX **UART**: UART2_DCE_CTS_B **UART**: UART2_DTE_RTS_B **PCIE**: PCIE1_CLKREQ_B **GPIO**: GPIO5_IO28 **TPSMP**: TPSMP_HDATA30	DI	1.8V	
P138	SER2_RTS#	NA	-	NA	
P139	SER2_CTS#	NA	-	NA	
P140	SER3_TX	NA	-	NA	
P141	SER3_RX	NA	-	NA	
P142	GND	NA	-	NA	
P143	CAN0_TX	NA	-	NA	
P144	CAN0_RX	NA	-	NA	
P145	CAN1_TX	NA	-	NA	
P146	CAN1_RX	NA	-	NA	
P147	VDD_IN	VSYS	A	3.0 - 5.25V	
P148	VDD_IN	VSYS	A	3.0 - 5.25V	
P149	VDD_IN	VSYS	A	3.0 - 5.25V	
P150	VDD_IN	VSYS	A	3.0 - 5.25V	
P151	VDD_IN	VSYS	A	3.0 - 5.25V	
P152	VDD_IN	VSYS	A	3.0 - 5.25V	
P153	VDD_IN	VSYS	A	3.0 - 5.25V	
P154	VDD_IN	VSYS	A	3.0 - 5.25V	
P155	VDD_IN	VSYS	A	3.0 - 5.25V	
P156	VDD_IN	VSYS	A	3.0 - 5.25V	
S1	CSI1_TX+ / I2C_CAM1_CK	**I2C**: I2C2_SCL **ENET**: ENET1_1588_EVENT1_IN **GPIO**: GPIO5_IO16 **TPSMP**: TPSMP_HDATA18	DO	1.8V	
S2	CSI1_TX- / I2C_CAM1_DAT	**I2C**: I2C2_SDA **ENET**: ENET1_1588_EVENT1_OUT **GPIO**: GPIO5_IO17 **TPSMP**: TPSMP_HDATA19	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S3	GND	NA	-	NA	
S4	RSVD_05	**GPIO**: GPIO1_IO14 **USB**: USB2_OTG_PWR **PWM**: PWM3_OUT **CCM**: CCMSRCGPCMIX_CLKO1 **CSU**: CSU_CSU_ALARM_AUT2	DI	1.8V	
S5	CSI0_TX- / I2C_CAM0_CK	SC0	DO	1.8V	From PCA9546APW (U8)
S6	CAM_MCK	**GPIO**: GPIO1_IO15 **USB**: USB2_OTG_OC **PWM**: PWM4_OUT **CCM**: CCMSRCGPCMIX_CLKO2 **CSU**: CSU_CSU_INT_DEB	DO	1.8V	
S7	CSI0_TX+ / I2C_CAM0_DAT	SD0	DI/O	1.8V	From PCA9546APW (U8)
S8	CSI0_CK+	NA	-	NA	
S9	CSI0_CK-	NA	-	NA	
S10	GND	NA	-	NA	
S11	CSI0_RX0+	NA	-	NA	
S12	CSI0_RX0-	NA	-	NA	
S13	GND	NA	-	NA	
S14	CSI0_RX1+	NA	-	NA	
S15	CSI0_RX1-	NA	-	NA	
S16	GND	NA	-	NA	
S17	GBE1_MDI0+	NA	-	NA	
S18	GBE1_MDI0-	NA	-	NA	
S19	GBE1_LINK	NA	-	NA	
S20	GBE1_MDI1+	NA	-	NA	
S21	GBE1_MDI1-	NA	-	NA	
S22	GBE1_LINK1000#	NA	-	NA	
S23	GBE1_MDI2+	NA	-	NA	
S24	GBE1_MDI2-	NA	-	NA	
S25	GND	NA	-	NA	
S26	GBE1_MDI3+	NA	-	NA	
S27	GBE1_MDI3-	NA	-	NA	
S28	GBE1_CTREF	NA	-	NA	
S29	PCIE_D_TX+	NA	-	NA	
S30	PCIE_D_TX-	NA	-	NA	
S31	GBE1_LINK_ACT#	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S32	PCIE_D_RX+	NA	-	NA	
S33	PCIE_D_RX-	NA	-	NA	
S34	GND	NA	-	NA	
S35	USB4_D+	NA	-	NA	
S36	USB4_D-	NA	-	NA	
S37	USB3_VBUS_DET	NA	-	NA	
S38	AUDIO_MCK	**SAI**: SAI2_MCLK **SAI**: SAI5_MCLK **GPIO**: GPIO4_IO27 **TPSMP**: TPSMP_HDATA_DIR	DO	1.8V	
S39	I2S0_LRCK	**SAI**: SAI2_TX_SYNC **SAI**: SAI5_TX_DATA1 **UART**: UART1_DCE_CTS_B **UART**: UART1_DTE_RTS_B **GPIO**: GPIO4_IO24 **SIM**: SIM_M_HWRITE	DI/O	1.8V	
S40	I2S0_SDOUT	**SAI**: SAI2_TX_DATA0 **SAI**: SAI5_TX_DATA3 **GPIO**: GPIO4_IO26 **TPSMP**: TPSMP_CLK	DO	1.8V	
S41	I2S0_SDIN	**SAI**: SAI2_RX_DATA0 **SAI**: SAI5_TX_DATA0 **UART**: UART1_DCE_RTS_B **UART**: UART1_DTE_CTS_B **GPIO**: GPIO4_IO23 **SIM**: SIM_M_HSIZE2	DI	1.8V	
S42	I2S0_CK	**SAI**: SAI2_TX_BCLK **SAI**: SAI5_TX_DATA2 **GPIO**: GPIO4_IO25 **TPSMP**: SIM_M_HREADYOUT	DI/O	1.8V	
S43	ESPI_ALERT0#	**GPIO**: GPIO1_IO10 **USB**: USB1_OTG_ID **OCOTP**: OCOTP_CTRL_WRAPPER_FUSE_LATCHED	DI/O	1.8V	
S44	ESPI_ALERT1#	NA	-	NA	
S45	MDIO_CLK	NA	-	NA	
S46	MDIO_DAT	NA	-	NA	
S47	GND	NA	-	NA	
S48	I2C_GP_CK	**I2C:** I2C3_SCL **PWM**: PWM4_OUT **GPT**: GPT2_CLK **GPIO**: GPIO5_IO18 **TPSMP**: TPSMP_HDATA20	DO	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S49	I2C_GP_DAT	**I2C:** I2C3_SDA **PWM**: PWM3_OUT **GPT**: GPT3_CLK **GPIO**: GPIO5_IO19 **TPSMP**: TPSMP_HDATA21	DI/O	1.8V	
S50	I2S2_LRCK / HDA_SYNC	**SAI:** SAI1_TX_SYNC **SAI**: SAI5_TX_SYNC **CORESIGHT**: CORESIGHT_EVENTO **GPIO**: GPIO4_IO10 **SIM**: SIM_M_HADDR25	DI/O	1.8V	
S51	I2S2_SDOUT / HDA_SDO	**SAI:** SAI1_TX_DATA0 **SAI**: SAI5_TX_DATA0 **CORESIGHT**: CORESIGHT_TRACE8 **GPIO**: GPIO4_IO12 **CCM**: CCMSRCGPCMIX_BOOT_CFG8 **SIM**: SIM_M_HADDR27	DO	1.8V	
S52	I2S2_SDIN / HDA_SDI	**SAI:** SAI1_RX_DATA0 **SAI**: SAI5_RX_DATA0 **PDM**: PDM_DATA0 **CORESIGHT**: CORESIGHT_TRACE0 **GPIO**: GPIO4_IO2 **CCM**: CCMSRCGPCMIX_BOOT_CFG0 **SIM**: SIM_M_HADDR17	DI	1.8V	
S53	I2S2_CK / HDA_CK	**SAI:** SAI1_TX_BCLK **SAI**: SAI5_TX_BCLK **CORESIGHT**: CORESIGHT_EVENTI **GPIO**: GPIO4_IO11 **SIM**: SIM_M_HADDR26	DI/O	1.8V	
S54	SATA_ACT#	NA	-	NA	
S55	USB5_EN_OC-	NA	-	NA	
S56	ESPI_IO_2	**DATA:** RAWNAND_DATA02 **SPI**: QSPI_A_DATA2 **GPIO**: GPIO3_IO8 **SIM**: SIM_M_HADDR4	DI/O	1.8V	
S57	ESPI_IO_3	**DATA:** RAWNAND_DATA03 **SPI**: QSPI_A_DATA3 **GPIO**: GPIO3_IO9 **SIM**: SIM_M_HADDR5	DI/O	NA	
S58	ESPI_RESET#	**SPDIF:** SPDIF1_IN **PWM**: PWM2_OUT **GPIO**: GPIO5_IO4 **TPSMP**: TPSMP_HDATA6	DI/O	1.8V	
S59	USB5_D+	NA	-	NA	
S60	USB5_D-	NA	-	NA	
S61	GND	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S62	USB3_SSTX+	NA	-	NA	
S63	USB3_SSTX-	NA	-	NA	
S64	GND	NA	-	NA	
S65	USBSSRX+	NA	-	NA	
S66	USBSSRX-	NA	-	NA	
S67	GND	NA	-	NA	
S68	USB3_D+	BDP_DN3	DI/O	3.3V	From USB2513B (U12)
S69	USB3_D-	BDM_DN3	DI/O	3.3V	From USB2513B (U12)
S70	GND	NA	-	NA	
S71	USB2_SSTX+	NA	-	NA	
S72	USB2_SSTX-	NA	-	NA	
S73	GND	NA	-	NA	
S74	USB2_SSRX+	NA	-	NA	
S75	USB2_SSRX-	NA	-	NA	
S76	PCIE_B_RST#	NA	-	NA	
S77	PCIE_C_RST#	NA	-	NA	
S78	PCIE_C_RX+	NA	-	NA	
S79	PCIE_C_RX-	NA	-	NA	
S80	GND	NA	-	NA	
S81	PCIE_C_TX+	NA	-	NA	
S82	PCIE_C_TX-	NA	-	NA	
S83	GND	NA	-	NA	
S84	PCIE_B_REFCK+	NA	-	NA	
S85	PCIE_B_REFCK-	NA	-	NA	
S86	GND	NA	-	NA	
S87	PCIE_B_RX+	NA	-	NA	
S88	PCIE_B_RX-	NA	-	NA	
S89	GND	NA	-	NA	
S90	PCIE_B_TX+	NA	-	NA	
S91	PCIE_B_TX-	NA	-	NA	
S92	GND	NA	-	NA	
S93	DP0_LANE0+	NA	-	NA	
S94	DP0_LANE0-	NA	-	NA	
S95	DP0_AUX_SEL	NA	-	NA	
S96	DP0_LANE1+	NA	-	NA	
S97	DP0_LANE1-	NA	-	NA	
S98	DP0_HPD	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S99	DP0_LANE2+	NA	-	NA	
S100	DP0_LANE2-	NA	-	NA	
S101	GND	NA	-	NA	
S102	DP0_LANE3+	NA	-	NA	
S103	DP0_LANE3-	NA	-	NA	
S104	USB3_OTG_ID	NA	-	NA	
S105	DP0_AUX+	NA	-	NA	
S106	DP0_AUX-	NA	-	NA	
S107	LCD1_BKLT_EN	NA	DI/O	1.8V	
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	NA	-	NA	
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	NA	-	NA	
S110	GND	NA	-	NA	
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	NA	-	NA	
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	NA	-	NA	
S113	eDP1_HPD	NA	-	NA	
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	NA	-	NA	
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	NA	-	NA	
S116	LCD1_VDD_EN	NA	DI/O	1.8V	
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	NA	-	NA	
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	NA	-	NA	
S119	GND	NA	-	NA	
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	NA	-	NA	
S122	LCD1_BKLT_PWM	NA	-	NA	
S123	GPIO13	**GPIO:** GPIO1_IO11 **USB**: USB2_OTG_ID **CCM**: CCMSRCGPCMIX_PMIC_READY **CCM**: CCMSRCGPCMIX_OUT0 **CAAM**: CAAM_WRAPPER_RNG_OSC_OBS	DI/O	1.8V	
S124	GND	NA	-	NA	
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS A_Y0_P	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS A_Y0_N	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S127	LCD0_BKLT_EN	**GPIO:** GPIO1_IO1 **PWM**: PWM1_OUT **AMAIX**: ANAMIX_REF_CLK_24M **CCM**: CCMSRCGPCMIX_EXT_CLK2 **SJC**: SJC_ACTIVE	DO	1.8V	
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS A_Y1_P	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS A_Y1_N	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S130	GND	NA	-	NA	
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS A_Y2_P	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS A_Y2_N	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S133	LCD0_VDD_EN	**GPIO:** GPIO1_IO3 **USDHC**: USDHC1_VSELECT **SDMA**: SDMA1_EXT_EVENT0 **ANAMIX**: ANAMIX_XTAL_OK **SJC**: SJC_DONE	DO	1.8V	
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS A_CLK_P	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS A_CLK_N	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S136	GND	NA	-	NA	
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS A_Y3_P	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS A_Y3_N	DO	1.8V	From SN65DSI83ZXHR (U6) or MIPI_DSI_D0_P (optional)
S139	I2C_LCD_CK	SC1	DO	1.8V	From PCA9546APW (U8)
S140	I2C_LCD_DAT	SD1	DO	1.8V	From PCA9546APW (U8)
S141	LCD0_BKLT_PWM	**SPDIF**: SPDIF1_EXT_CLK **PWM**: PWM1_OUT **GPIO**: GPIO5_IO5 **TPSMP**: TPSMP_HDATA7	DI/O	1.8V	
S142	GPIO12	**SAI**: SAI5_RX_DATA2 **SAI**: SAI1_TX_DATA4 **SAI**: SAI1_TX_SYNC **SAI**: SAI5_TX_BCLK **PDM**: PDM_DATA2 **GPIO**: GPIO3_IO23	DI/O	1.8V	
S143	GND	NA	-	NA	
S144	eDP0_HPD	NA	-	NA	
S145	WDT_TIME_OUT#	**GPIO**: GPIO1_IO2 **WDOG**: WDOG1_WDOG_B **WDOG**: WDOG1_WDOG_ANY **SJC**: SJC_DE_B	DO	1.8V	
S146	PCIE_WAKE#	**SAI**: SAI1_MCLK **SAI**: SAI5_MCLK **SAI**: SAI1_TX_BCLK **PDM**: PDM_CLK **GPIO**: GPIO4_IO20 **SIM**: SIM_M_HRESP	DI	1.8V	
S147	VDD_RTC	NVCC_BBSM	A	1.8V	
S148	LID#	**SAI**: SAI1_TX_DATA3 **SAI**: SAI5_TX_DATA3 **CORESIGHT**: CORESIGHT_TRACE11 **GPIO**: GPIO4_IO15 **CCM**: CCMSRCGPCMIX_BOOT_CFG11 **SIM**: SIM_M_HADDR30	DI	1.8 - 5V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S149	SLEEP#	**SAI**: SAI1_TX_DATA1 **SAI**: SAI5_TX_DATA1 **CORESIGHT**: CORESIGHT_TRACE9 **GPIO**: GPIO4_IO15 **CCM**: CCMSRCGPCMIX_BOOT_CFG11 **SIM**: SIM_M_HADDR30	DI	1.8 - 5V	
S150	VIN_PWR_BAD#	**SAI**: SAI1_TX_DATA2 **SAI**: SAI5_TX_DATA2 **CORESIGHT**: CORESIGHT_TRACE10 **GPIO**: GPIO4_IO14 **CCM**: CCMSRCGPCMIX_BOOT_CFG10 **SIM**: SIM_M_HADDR29	DI	VDD_IN	
S151	CHARGING#	**SAI**: SAI1_TX_DATA4 **SAI**: SAI6_RX_BCLK **SAI**: SAI6_TX_BCLK **CORESIGHT**: CORESIGHT_TRACE12 **GPIO**: GPIO4_IO16 **CCM**: CCMSRCGPCMIX_BOOT_CFG12 **SIM**: SIM_M_HADDR31	DI	1.8 - 5V	
S152	CHARGER_PRSNT#	**SAI**: SAI1_TX_DATA5 **SAI**: SAI6_RX_DATA0 **SAI**: SAI6_TX_DATA0 **CORESIGHT**: CORESIGHT_TRACE13 **GPIO**: GPIO4_IO17 **CCM**: CCMSRCGPCMIX_BOOT_CFG13 **SIM**: SIM_M_HBURST0	DI	1.8 - 5V	
S153	CARRIER_STBY#	**SAI**: SAI5_RX_DATA3 **SAI**: SAI1_TX_DATA5 **SAI**: SAI1_TX_SYNC **SAI**: SAI5_TX_DATA0 **PDM**: PDM_DATA3 **GPIO**: GPIO3_IO24	DO	1.8V	
S154	CARRIER_PWR_ON	**SAI**: SAI3_RX_SYNC **GPT**: GPT1_CAPTURE1 **SAI**: SAI5_RX_SYNC **GPIO**: GPIO4_IO28 **TPSMP**: TPSMP_HTRANS0	DO	1.8V	
S155	FORCE_RECOV#	BOOT_MODE0	DI	1.8V	
S156	BATLOW#	**SAI**: SAI1_TX_DATA6 **SAI**: SAI6_RX_SYNC **SAI**: SAI6_TX_SYNC **CORESIGHT**: CORESIGHT_TRACE14 **GPIO**: GPIO4_IO18 **CCM**: CCMSRCGPCMIX_BOOT_CFG14 **SIM**: SIM_M_HBURST	DI	1.8 - 5V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S157	TEST#	**SAI**: SAI5_RX_SYNC **SAI**: SAI1_TX_DATA0 **GPIO**: GPIO3_IO19	DI	1.8 - 5V	
S158	GND	NA	-	NA	

Table 9: Pinout table for Nitrogen8M Mini SMARC JTAG connector (J1)

Pin #	Pin Name	CPU PIN / Multiplexing	I/O	I/O Level	Comments
1	VDD_JTAG	1P8V	DO	1.8V	
2	JTAG_TRST#	TP2	-	NA	Test point
3	JTAG_TMS	JTAG_TMS	DI	1.8V	
4	JTAG_TDO	JTAG_TDO	DO	1.8V	
5	JTAG_TDI	JTAG_TDI	DI	1.8V	
6	JTAG_TCK	JTAG_TCK	DI	1.8V	
7	JTAG_RTCK	TP4	-	NA	Test point
8	JTAG_NTRST	JTAG_TRST_B	DO	1.8V	
9	JTAG_MOD	JTAG_MOD	DI	1.8V	
10	GND	GND	-	NA	

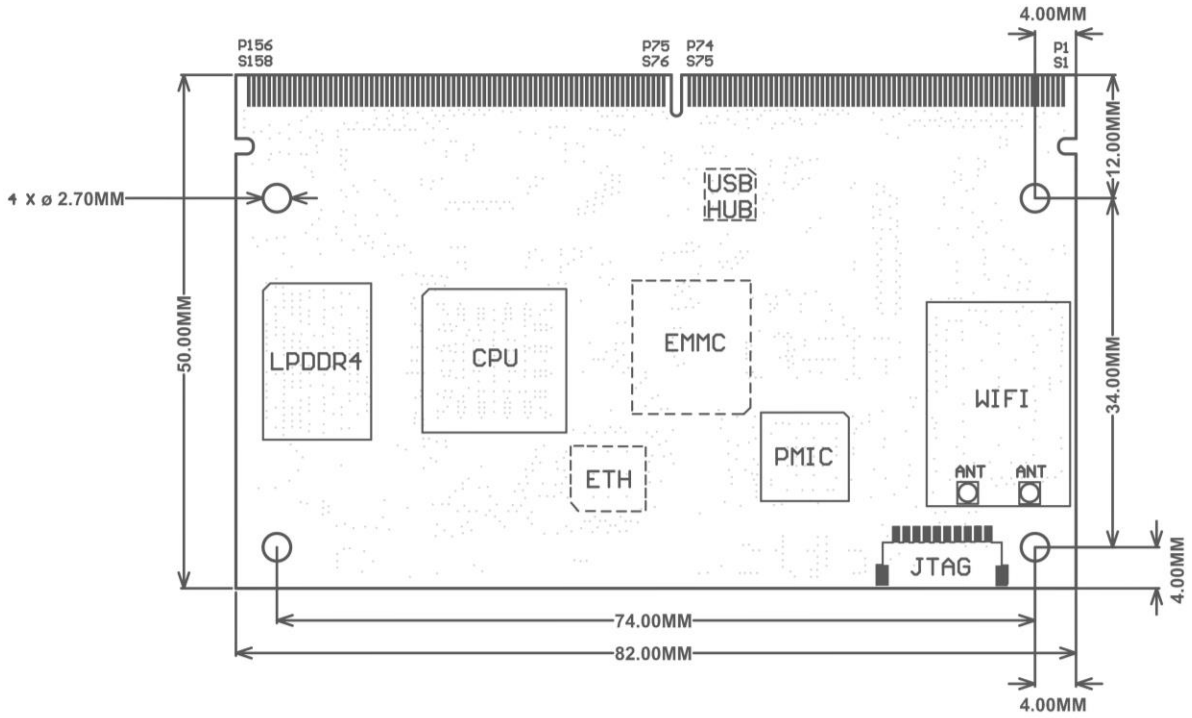
8.1 MIPI-DSI vs. LVDS Options

For the switch from LVDS to MIPI-DSI, you will need to:

- **Populate:** R97, R98, R99, R100, R101, R105, R118, R119, R121 and R122 (0 ohm)
- **Depopulate:** R123, R124, R125, R126, R127, R128, R129, R130, R131 and R132
- **Optionally:** Depopulate U6 (not strictly necessary)

9 MECHANICAL AND PCB FOOTPRINT SPECIFICATION

Module dimensions of the Nitrogen8M Mini SMARC are 82 x 50 mm. Detail drawings are shown below.



Note: ETH, EMMC and USB HUB are on the bottom side

10 STORAGE INSTRUCTIONS

Required Storage Conditions:

- **Prior to Opening the Dry Packing**
  The following are required storage conditions prior to opening the dry packing:
  - Normal temperature: 5~40℃
  - Normal humidity: 80% (Relative humidity) or less
  - Storage period: One year or less

11 REGULATORY

Regulatory IDs Summary

Model	US/FCC	Canada/IC	Japan
Nitrogen8M Mini SMARC	TBD		

12 CERTIFIED ANTENNAS

The Nitrogen8M Mini SMARC contains the Sona NX611 module, which was certified with the following antennas.

Manufacturer	Model	Laird Connectivity Part Number	Type	Connector	Peak Gain (dBi)		
					2.4 GHz	5 GHz	6 GHz
Laird Connectivity	FlexMIMO 6E	EFD2471A3S-10MH4L	PIFA	MHF4L	2.2	3.8	3.3
Laird Connectivity	FlexPIFA 6E	EFB2471A3S-10MH4L	PIFA	MHF4L	2.2	3.9	3.8
Laird Connectivity	Mini NanoBlade Flex 6 GHz	EMF2471A3S-10MH4L	PCB Dipole	MHF4L	2.4	4.4	5.2
JOYMAX	Dipole 6E	TWX-100BRSAX-2001	Dipole	RS-SMA	2	4.0	4.0
Laird Connectivity	FlexPIFA	001-0022	PIFA	MHF4L	2	–	–

13 Ordering Information

Order Model	Description
8MM_SMARC_SOM_1r16e	SMARC SOM: i.MX8M MINI Quad / 1GB / 16GB eMMC
8MM_SMARC_SOM_2r16e	SMARC SOM: i.MX8M MINI Quad / 2GB / 16GB eMMC
8MM_SMARC_SOM_4r16e	SMARC SOM: i.MX8M MINI Quad / 4GB / 16GB eMMC
8MM_SMARC_SOM_1r16eWB	SMARC SOM: i.MX 8M Mini Dual / 1GB / 16GB eMMC / NX611
8MM_SMARC_SOM_2r16eWB	SMARC SOM: i.MX 8M Mini Dual / 2GB / 16GB eMMC / NX611
8MM_SMARC_SOM_1r16e_i	SMARC SOM: i.MX8M MINI Quad / 1GB / 16GB eMMC / -40 to +85C
8MM_SMARC_SOM_2r16e_i	SMARC SOM: i.MX8M MINI Quad / 2GB / 16GB eMMC / -40 to +85C
8MM_SMARC_SOM_4r16e_i	SMARC SOM: i.MX8M MINI Quad / 4GB / 16GB eMMC / -40 to +85C
8MM_SMARC_SOM_1r16eWB_i	SMARC SOM: i.MX 8M Mini Dual / 1GB / 16GB eMMC / NX611 / Industrial Temp
8MM_SMARC_SOM_2r16eWB_i	SMARC SOM: i.MX 8M Mini Dual / 2GB / 16GB eMMC / NX611 / Industrial Temp
SMARC_CAR_BRD	Universal Carrier Board - SMARC (Note - SOM sold separately)

14 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Boundary Devices Support Center: https://boundarydevices.com/support/
Email: support@boundarydevices.com
Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852-2762-4823
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.

Laird Connectivity's products are subject to standard Terms & Conditions.

sales@lairdconnect.com
support@lairdconnect.com
www.lairdconnect.com