11. Power Requirements for Cyclone IV Devices

CYIV-51011-1.3

This chapter describes information about external power supply requirements, hot-socketing specifications, power-on reset (POR) requirements, and their implementation in Cyclone IV devices.

This chapter includes the following sections:

External Power Supply Requirements

This section describes the different external power supplies required to power Cyclone IV devices. Table 11–1 and Table 11–2 list the descriptions of external power supply pins for Cyclone IV GX and Cyclone IV E devices, respectively.

For each Altera recommended power supply's operating conditions, refer to the *Cyclone IV Device Datasheet* chapter.

For power supply pin connection guidelines and power regulator sharing, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

Table 11–1. Power Supply Descriptions for the Cyclone IV GX Devices (Part 1 of 2)

Power Supply Pin	Nominal Voltage Level (V)	Description
VCCINT	1.2	Core voltage, PCI Express (PCIe) hard IP block, and transceiver physical coding sublayer (PCS) power supply
VCCA (1)	2.5	PLL analog power supply
VCCD_PLL	1.2	PLL digital power supply
VCCIO (2)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	I/O banks power supply
VCC_CLKIN (3), (4)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	Differential clock input pins power supply
VCCH_GXB	2.5	Transceiver output (TX) buffer power supply
VCCA_GXB	2.5	Transceiver physical medium attachment (PMA) and auxiliary power supply

Table 11–1. Power Supply Descriptions for the Cyclone IV GX Devices (Part 2 of 2)

Power Supply Pin	Nominal Voltage Level (V)	Description
VCCL_GXB	1.2	Transceiver PMA and auxiliary power supply

Notes to Table 11–1:

(1) You must power up VCCA even if the phase-locked loop (PLL) is not used.

(2) I/O banks 3, 8, and 9 contain configuration pins. You can only power up the V_{CCIO} level of I/O banks 3 and 9 to 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V. For Fast Passive Parallel (FPP) configuration mode, you must power up the V_{CCIO} level of I/O bank 8 to 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V.

(3) All device packages of EP4CGX15, EP4CGX22, and device package F169 and F324 of EP4CGX30 devices have two VCC_CLKIN dedicated clock input I/O located at Banks 3A and 8A. Device package F484 of EP4CGX30, all device packages of EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have four VCC_CLKIN dedicated clock input I/O bank located at banks 3A, 3B, 8A, and 8B.

(4) You must set VCC_CLKIN to 2.5V if the CLKIN is used as a high-speed serial interface (HSSI) transceiver refclk. When not used as a transceiver refclk, VCC_CLKIN supports 1.2 V/ 1.5 V/ 1.8 V/ 2.5 V/ 3.0 V/ 3.3V voltages.

Table 11–2. Power Supply Descriptions for the Cyclone IV E Devices

Power Supply Pin	Nominal Voltage Level (V)	Description
VCCINT	1.0, 1.2	Core voltage power supply
VCCA (1)	2.5	PLL analog power supply
VCCD_PLL	1.0, 1.2	PLL digital power supply
VCCIO (2)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	I/O banks power supply

Notes to Table 11–2:

(1) You must power up VCCA even if the PLL is not used.

(2) I/O banks 1, 6, 7, and 8 contain configuration pins.

Hot-Socketing Specifications

Cyclone IV devices are hot-socketing compliant without the need for any external components or special design requirements. Hot-socketing support in Cyclone IV devices has the following advantages:

- You can drive the device before power up without damaging the device.
- I/O pins remain tri-stated during power up. The device does not drive out before or during power-up. Therefore, it does not affect other buses in operation.

Devices Driven Before Power-Up

You can drive signals into regular Cyclone IV E I/O pins and transceiver Cyclone IV GX I/O pins before or during power up or power down without damaging the device. Cyclone IV devices support any power-up or power-down sequence to simplify system-level designs.

I/O Pins Remain Tri-stated During Power-Up

The output buffers of Cyclone IV devices are turned off during system power up or power down. Cyclone IV devices do not drive out until the device is configured and working in recommended operating conditions. The I/O pins are tri-stated until the device enters user mode.

The user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are always enabled (after POR) before and during configuration. The weak pull up resistors are not enabled prior to POR.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch up. Latch up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the V_{CC} of the device and ground planes. This condition can lead to latch up and cause a low-impedance path from V_{CC} to GND in the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

The design of the I/O buffers and hot-socketing circuitry ensures that Cyclone IV devices are immune to latch up during hot-socketing.

For more information about the hot-socketing specification, refer to the *Cyclone IV Device Datasheet* chapter and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices* white paper.

Hot-socketing Feature Implementation

The hot-socketing circuit does not include the CONF_DONE, nCEO, and nSTATUS pins to ensure that they are able to operate during configuration. The expected behavior for these pins is to drive out during power-up and power-down sequences.

Altera uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, Altera recommends connecting the GND between boards before connecting the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND can otherwise cause an out-of-specification I/O voltage or current condition with the Altera device.

Power-On Reset Circuitry

Cyclone IV devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power up. During POR, all user I/O pins are tri-stated until the power supplies reach the recommended operating levels. In addition, the POR circuitry also ensures the V_{CCIO} level of I/O banks that contain configuration pins reach an acceptable level before configuration is triggered.

The POR circuit of the Cyclone IV device monitors the V_{CCINT}, V_{CCA}, and V_{CCIO} that contain configuration pins during power-on. You can power up or power down the V_{CCINT}, V_{CCA}, and V_{CCIO} pins in any sequence. The V_{CCINT}, V_{CCA}, and V_{CCIO} must have a monotonic rise to their steady state levels. All V_{CCA} pins must be powered to 2.5V (even when PLLs are not used), and must be powered up and powered down at the same time.

After the Cyclone IV device enters the user mode, the POR circuit continues to monitor the V_{CCINT} and V_{CCA} pins so that a brown-out condition during user mode is detected. If the V_{CCINT} or V_{CCA} voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the V_{CCIO} voltage sags during user mode, the POR circuit does not reset the device.

In some applications, it is necessary for a device to wake up very quickly to begin operation. Cyclone IV devices offer the Fast-On feature to support fast wake-up time applications. The MSEL pin settings determine the POR time (t_{POR}) of the device.

For more information about the MSEL pin settings, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

For more information about the POR specifications, refer to the *Cyclone IV Device Datasheet* chapter.

Document Revision History

Table 11–3 lists the revision history for this chapter.

Table 11–3. Document Revision History

Date	Version	Changes
May 2013	1.3	Updated Note (4) in Table 11–1.
July 2010	1.2	■ Updated for the Quartus II software version 10.0 release. ■ Updated "I/O Pins Remain Tri-stated During Power-Up" section. ■ Updated Table 11–1.
February 2010	1.1	Updated Table 11–1 and Table 11–2 for the Quartus II software version 9.1 SP1 release.
November 2009	1.0	Initial release.