TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

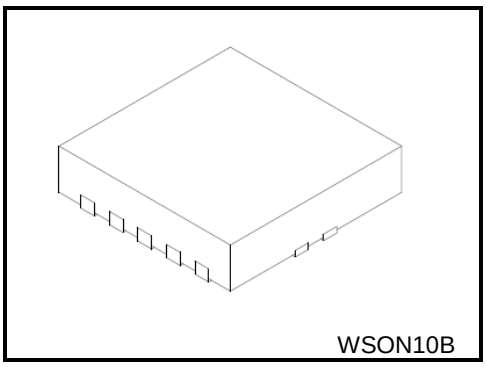
TCKE805 Series

18 V, 5A eFuse with Adjustable Over Current Protection and Reverse Blocking FET Control

The TCKE805 series are 18 V high input voltage Single Inputs－Single Output eFuse IC. It can be used as a reusable fuse, and other protection features like adjustable over current limit by an external resistor, short circuit protection, over voltage clamp, adjustable slew rete control by an external capacitance, under voltage protection, thermal shutdown and reverse current blocking by external MOSFET control circuit.

Switch ON resistance is only 28 mΩ, high output current is up to 5.0A, and wide input voltage operation characteristics makes this product ideal for power management such as in the Power Stage of Hard disk drive and Battery Charge applications.

This device is available in 0.4mm pitch small package WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ)). Thus this devices is ideal for various application such as portable applications that require high-density board.



WSON10B

Weight : 19.3mg (typ.)

Feature

- High input voltage: $V_{IN\ max}$ = 18 V
- High output current: $I_{OUT\ (DC)}$ = 5.0 A
- Low ON resistance : R_{ON} = 28 mΩ (typ.)
- Adjustable overcurrent limit : up to 5.0 A
- Fixed over voltage clamp
  5V power rail : 6.04 V (typ.)
- Programmable slew rate control by external capacitance for Inrush current reduction
- Programmable under voltage lockout by external resistor
- Reverse current blocking support by built in MOSFET Driver
- Adjustable under voltage lockout(UVLO) by external resistor
- Thermal shutdown
- Auto-discharge
- Small package:
  WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ))

Notice

This device is sensitive to electrostatic discharge.

Please ensure equipment and tools are adequately earthed when handling.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Input voltage	V_{IN}	-0.3 to 18	V
ILIM voltage	V_{ILIM}	-0.3 to 6	V
dV/dT voltage	$V_{dV/dT}$	-0.3 to 6	V
Control voltage	$V_{EN/UVLO}$	-0.3 to 18	V
Output voltage	V_{OUT}	-0.3 to V_{IN} + 0.3 or 18 V which is smaller	V
External MOSFET voltage	V_{EFET}	-0.3 to 30	V
Power dissipation	P_D	2.4 (Note 1)	W
Junction temperature	Tj	150	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

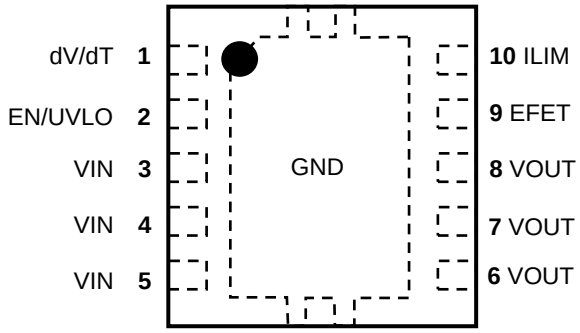
Note1: Rating at mounting on a board: FR4 board. (76.2mm * 114.3mm * 1.6mm, 4 layer)

Operating Ranges

Characteristics	Symbol	Ranges		Unit
Input voltage	V_{IN}	4.4 to 18		V
Output current	I_{OUT}	Continuous output current	0 to 5.0	A
I_{LIM} External resistance	R_{ILIM}	20 to 300		kΩ
Control voltage	$V_{EN/UVLO}$	0 to 18		V
External MOSFET voltage	V_{EFET}	0 to V_{IN} + 4.9		V
Operating Ambient temperature range	$Ta_{\_opr}$	−40 to 85		°C
External capacitance	$C_{dV/dT}$	1 (typ), 100 (max)		nF

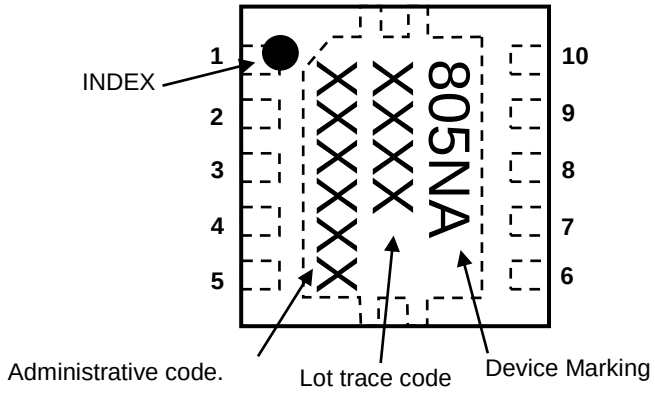
Pin Assignment (Top view)

WSON10B



Top Marking (Top view)

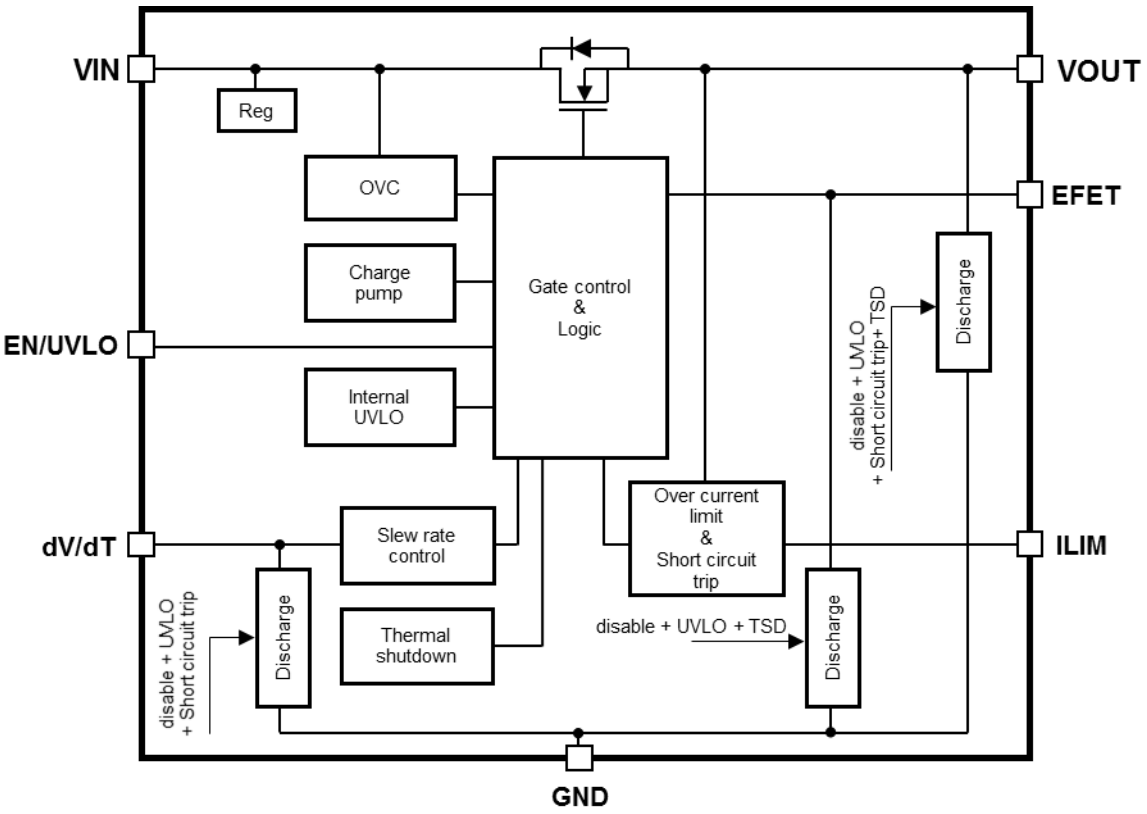
Example: TCKE805NA



Product list

Part number	Over voltage Clamp	CE function	Fault Response	Top Marking	Package
TCKE805NA	6.04V (typ)	Active High	Auto-retry	805NA	WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ))
TCKE805NL	6.04V (typ)	Active High	Latched	805NL	WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ))

Block Diagram



PIN Description

PIN Name	Description
EN/UVLO	This pin has two functions. One function turns on the output voltage of the internal MOSFET and EFET terminal as an enable signal. Another function can be used as a UVLO trip point with external resistors.
ILIM	Current limit set input. A resistor between I_{LIM} terminal and GND set the current limit.
dV/dT	Rise time set input. A capacitor between dV/dT terminal and GND set the slew rate of VOUT when the device turns on.
EFET	Connect this pin to the gate of a blocking Nch MOSFET. This pin can be left floating if it is not used
VIN	Supply Input. Input to the power switch and the supply voltage for the device.
GND	Ground.
VOUT	Output. Output of the power switch.

Operation Logic Table

	EN/UVLO “Low”	EN/UVLO “ High”
Output	**OFF**	**ON**

TCKE805 series DC Characteristics
(Unless otherwise specified, Ta = -40 to 85°C, V_{IN} = 5V, R_{ILIM} = 20kΩ)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = −40 to 85°C		Unit
			Min.	Typ.	Max.	Min.	Max.	
Basic operation								
VIN under voltage lockout (UVLO) threshold, rising	V_{IN_UVLO}		—	4.15	—	4.00	4.4	V
VIN under voltage lockout (UVLO) hysteresis	V_{IN_UVhyst}		—	5	—	—	—	%
EN/UVLO threshold voltage, rising	V_{ENR}	—	—	1.1	—	1.0	1.2	V
EN/UVLO threshold voltage, falling	V_{ENF}	—	—	0.96	—	0.89	1.01	V
On resistance	R_{ON}	I_{OUT} = 1.5 A	—	28	—	—	38	mΩ
Quiescent current (ON state)	I_Q	V_{EN} = 3 V, R_{ILIM} = 120 kΩ, I_{OUT} = 0 A	—	0.46	—	—	0.61	mA
Quiescent current (OFF state)	$I_{Q(OFF)}$	EN = 0V	—	33	—	—	48	μA
dV/dT control								
Capacitor Voltage	$V_{dV/dT}$	—	—	3	—	—	—	V
Charging Current	$I_{dV/dT}$	$V_{dV/dT}$ =0V	—	250	—	—	—	nA
Discharge resistance	$R_{dV/dT}$	V_{EN} = 0 V, $I_{dV/dT}$ =10 mA	—	5	—	3	9	Ω
dV/dT to OUT gain	$GAIN_{dV/dT}$	(Note2) $V_{dV/dT}$ = 0.3 V	—	10.5	—	—	—	V/V
External FET Gate driver								
Charging Current	I_{EFET}	V_{EFET} = 5 V (Note2)	—	2	—	—	—	μA
Output voltage	V_{EFET}	(Note2)	—	VIN+4.9	—	VIN+4.4	VIN+5.3	V
Discharge resistance	R_{EFET}	V_{EN} = 0 V, I_{EFET} = 20 mA	—	24	—	12	40	Ω
Over-voltage Protection								
Over voltage clamp (OVC)	V_{OVC}	V_{IN} = 7 V, I_{OUT} = 1 A	—	6.04	—	5.62	6.45	V
Over-current Protection								
Over current limit (Note3)	I_{LIM} (I_{OUT_CL})	R_{ILIM} = 20 kΩ, V_{IN} - V_{OUT} = 1 V	—	5.15	—	4.44	5.87	A
		R_{ILIM} = 24 kΩ, V_{IN} - V_{OUT} = 1 V	—	4.38	—	3.88	4.88	
		R_{ILIM} = 35.1 kΩ, V_{IN} - V_{OUT} = 1 V	—	3.06	—	2.70	3.41	
		R_{ILIM} = 62 kΩ, V_{IN} - V_{OUT} = 1 V	—	1.78	—	1.52	2.04	
		R_{ILIM} = 120 kΩ, V_{IN} - V_{OUT} = 1 V	—	0.96	—	0.76	1.16	
		R_{ILIM} = 250 kΩ, V_{IN} - V_{OUT} = 1 V	—	0.5	—	0.35	0.65	
		R_{ILIM} = 0 Ω, V_{IN} - V_{OUT} = 1 V	—	0.64	—	—	—	
		R_{ILIM} = OPEN, V_{IN} - V_{OUT} = 1 V	—	0.64	—	—	—	
Short-circuit current limit	I_{SCL}	(Note2),(Note4)	—	0.15	—	0.05	0.5	A
Fast trip comparator level	$I_{FASTTRIP}$ (I_{SHORT_TRIP})	—	—	I_{LIM} × 1.6	—	—	—	A
ILIM short resistor detect Threshold	$R_{SHORTLIM}$	—	—	11	—	—	—	kΩ
Thermal Protection								
Thermal shut down Threshold	T_{SD}	Tj	—	160	—	—	—	°C
Thermal shut down Hysteresis	T_{SDH}	Tj	—	20	—	—	—	°C

Note2: This parameter is warranted by design.

Note3: Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

Note4: Hard short less than 10 mΩ.

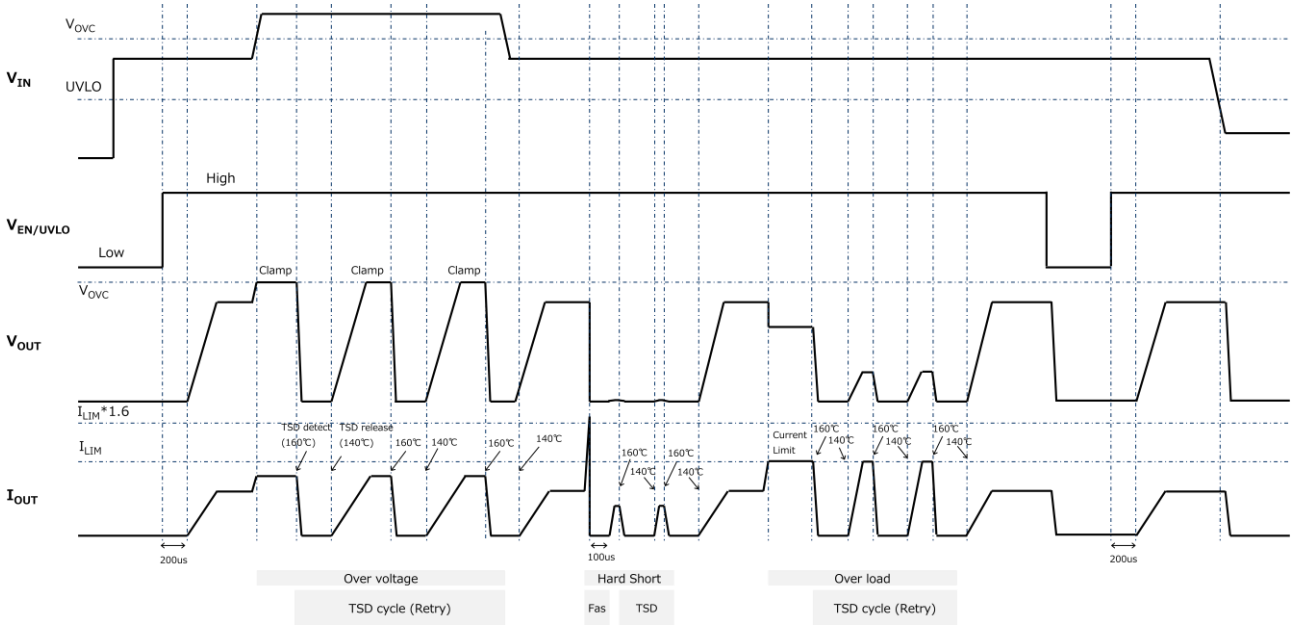
TCKE805 AC Characteristics
(Unless otherwise specified, Ta = -40 to 85°C, V_{IN} = 5V, R_{ILIM} = 20kΩ, R_{LOAD}=5Ω, C_{IN} = C_{OUT} = 1μF)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{OUT} on time	t_{ON}	V_{EN}↑ to I_{IN} = 100 mA, 1 A resistive load at V_{OUT}, $C_{dV/dT}$ = OPEN (Note5)	—	330	—	μs
V_{OUT} off time	t_{OFF}	V_{EN}↓ to V_{EFET}↓, C_{EFET} = OPEN (Note5)	—	0.96	—	μs
Output ramp time	$t_{dV/dT}$	V_{EN}↑ to V_{OUT} become V_{IN}* 90%, $C_{dV/dT}$ = OPEN (Note6)	200	400	700	μs
		V_{EN}↑ to V_{OUT} become V_{IN}* 90%, $C_{dV/dT}$ = 1 nF (Note5)	—	2.3	—	ms
Fast trip comparator delay	$t_{FastOffDly}$	I_{OUT} > $I_{FASTTRIP}$ to I_{OUT} = 0 (Switch off) (Note5)	—	150	—	ns
EFET on time	$t_{EFET-ON}$	V_{EN}↑ to V_{EFET} = V_{IN}, C_{EFET} = 1 nF(Note5)	—	2.6	—	ms
		V_{EN}↑ to V_{EFET} = V_{IN}, C_{EFET} = 10 nF(Note5)	—	25	—	ms
EFET off time	$t_{EFET-OFF}$	V_{EN}↓ to V_{EFET} = 1 V, C_{EFET} = 1 nF(Note5)	—	1.2	—	μs
		V_{EN}↓ to V_{EFET} = 1 V, C_{EFET} = 10 nF(Note5)	—	2.9	—	μs

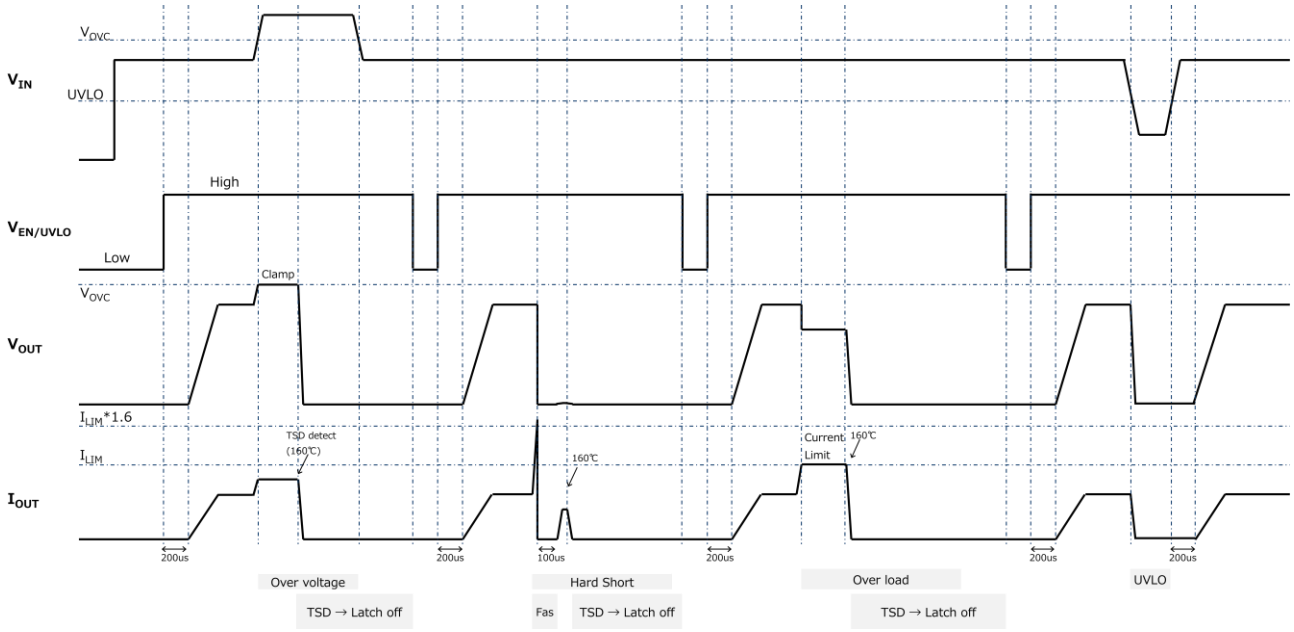
Note5: This parameter is reference only.
Note6: This parameter is warranted by design.

Timing chart

Example 1(Auto-retry type)

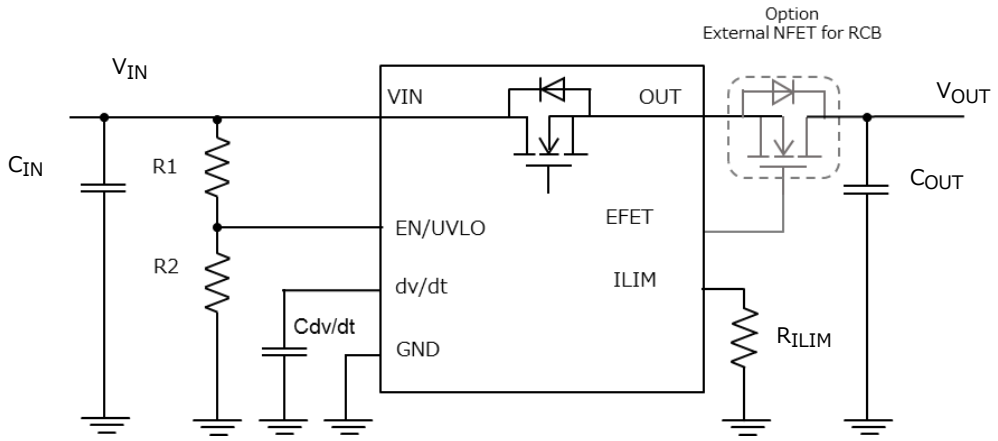


Example 2(Latched type)



Application Note

1. Application circuit example (top view)



1) Input and Output capacitor

An input capacitor (C_{IN}) and an output capacitor (C_{OUT}) are necessary for the stable operation of TCKE8xx series. And it is effective to reduce voltage overshoot or undershoot due to sharp changes in output current and also for improved stability of the power supply. When used, place C_{IN} and C_{OUT} more than 1.0μF as close to V_{IN} pin to improve stability of the power supply.

2) EN/UVLO pin

If you want to change the under voltage lockout function (UVLO) setting with an external resistor, it can be calculated by the following formula. If this UVLO setting is not required, the EN/UVLO pin features an 18V tolerance, so there is no problem with connecting this pin directly to the input voltage. However, please be careful that the input voltage does not exceed the absolute maximum rating.

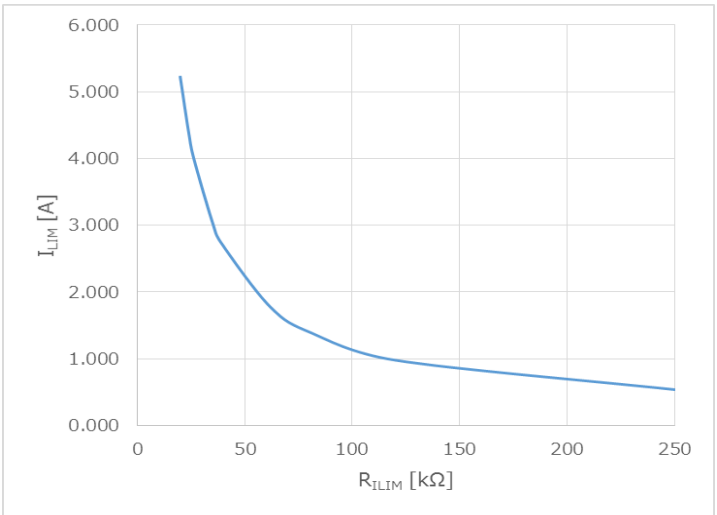
$UVLO(rise) = (R1+R2)/R2 \times V_{ENR}$

*Valid only at voltages higher than the internal UVLO threshold.

3) I_{LIM} Current Limit setting by External resistance

I_{LIM} is calculated by below formula. Please use high accuracy resistance to reduce variation of I_{LIM}. In addition, please select resistance value with reference to ILIM of electrical characteristics. The short protection function (Fast Trip) of this product operates when the output current exceeds 1.6 times of I_{LIM}. If I_{LIM} is set to 1A or less, the difference between the following formula and the actual measurement value may increase, so be careful when designing.

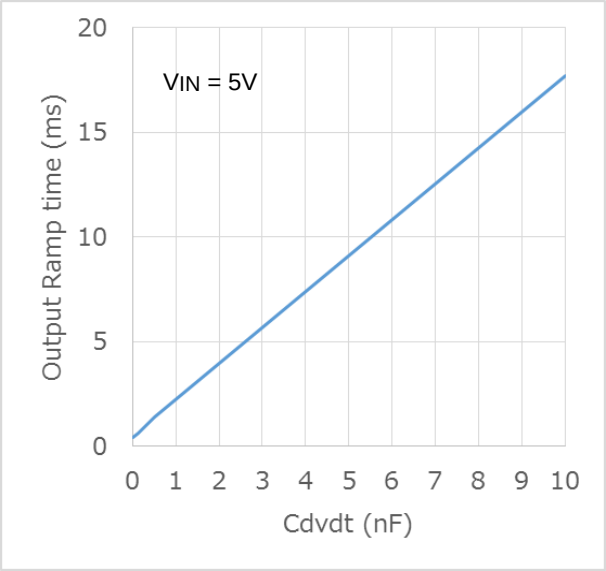
$$I_{LIM}\,(A) = 0.13+101800/R_{ILIM}\,(\Omega)$$



3) $t_{dv/dt}$ Slew rate control by External Capacitance

I_{LIM}, dv/dt parameters are calculated by below formula. Please use high accuracy capacitance to reduce variation of I_{LIM}. When selecting $C_{dv/dt}$ value, please use under 100nF so that the slew rate will not be too slow.

$$t_{dv/dt}\,(s) = 0.36 \times 10^{6} \times V_{IN}(C_{dVdT}+50pF)+3.0\times 10^{-4}$$



2. Reverse current blocking support by built in MOSFET Driver

Reverse current blocking function is designed by built in MOSFET Driver. This function is active at external output n-ch MOSEFT turned off.

However these does not assure for the suppression of uprising device operation. In use of these products, please read through and understand dissipation idea for absolute maximum ratings from the above mention or our ‘Semiconductor Reliability Handbook’. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommend inserting failsafe system into the design.

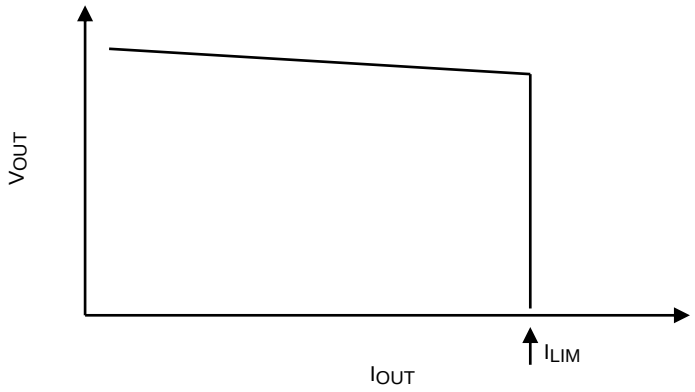
3. Thermal shut down function, Over current protection

Thermal shutdown function and over current protection is designed in these products, but these does not assure for the suppression of uprising device operation. In use of these products, please read through and understand dissipation idea for absolute maximum ratings from the above mention or our ‘Semiconductor Reliability Handbook’. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommend inserting failsafe system into the design.

4. Over current limit

Both of the constant type and latched type operates identically during the initial onset of an overcurrent event. During current limit operation, output current is limited by threshold that is set by R_{ILIM}.

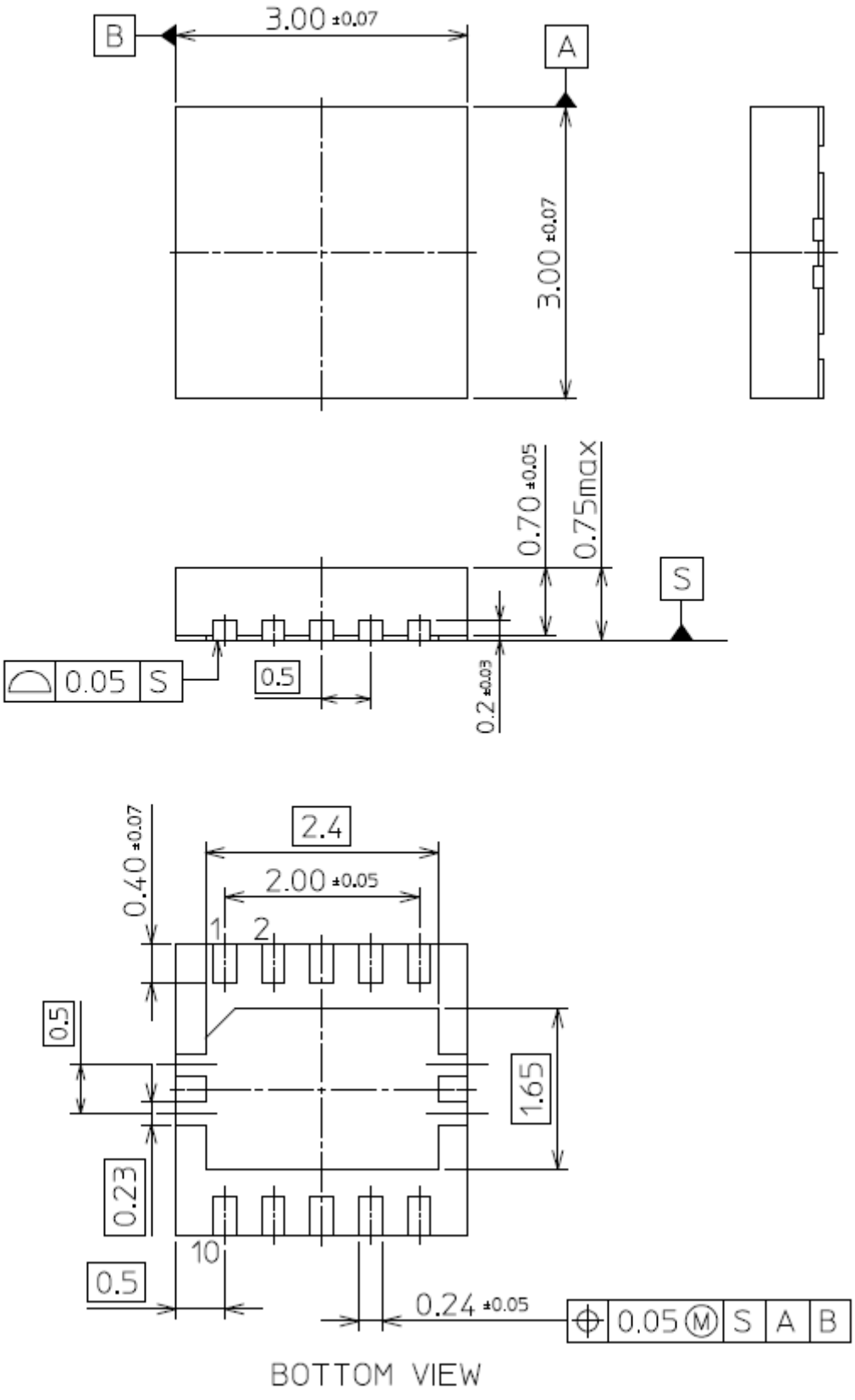
Output voltage – current limit threshold



Package Dimensions

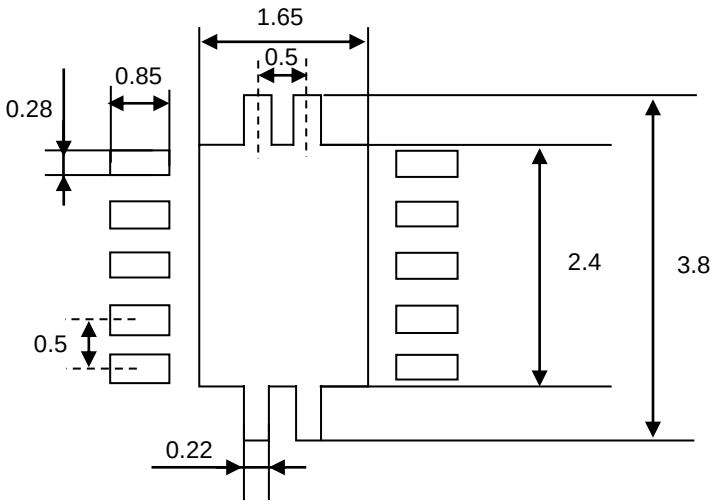
WSON10B

Unit: mm



Weight : 19.3 mg (typ.)

Land pattern dimensions for reference only



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