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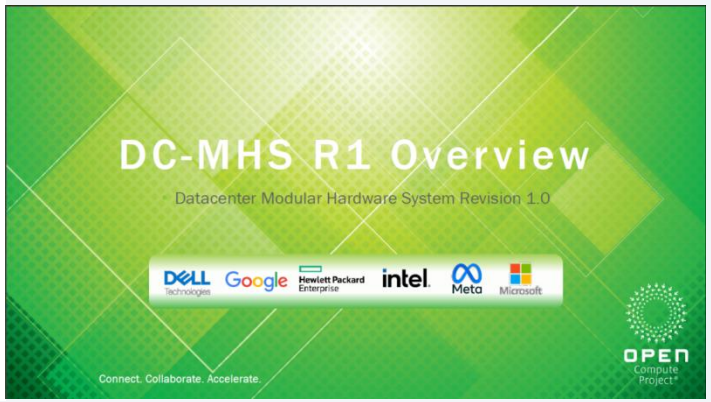
COMMUNICATIONS SOLUTIONS

Solutions for
OCP Related Applications

Oct, 2022

Commercial IO

OCP DC-MHS



OCP DC-MHS Summary

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DC-MHS Specifications --- 2022 Q2 released

1. Modular FulL Width HPMs (M-FLW)
2. Modular DeNsity Optimized HPMs (M-DNO)
3. Modular Peripheral Infrastructure Connectivity (M-PIC)
4. Modular Common Redundant Power Supply (M-CRPS)
5. Modular eXtensible I/O (M-XIO)
6. Modular PEripheral Sideband Tunneling Interface (M-PESTI)

HPM =
Host
Processor
Module

Type	Description	Version	Submit Date	Contributor	License	Notes
Specification	DC-MHS v1.0 specifications M-FLW_R1_v1p0 M-DNO_R1_v1p0 M-PESTI_R1_v1p0 M-PIC_R1_v1p0 M-XIO_R1_v1p0 M-CRPS_R1_v1p0	R1-v1.0_RC	9/28/2022	DC-MHS CLA group	OWF	For Review Send feedback to: dcmhs@opencompute.org

Introduction of DC-MHS

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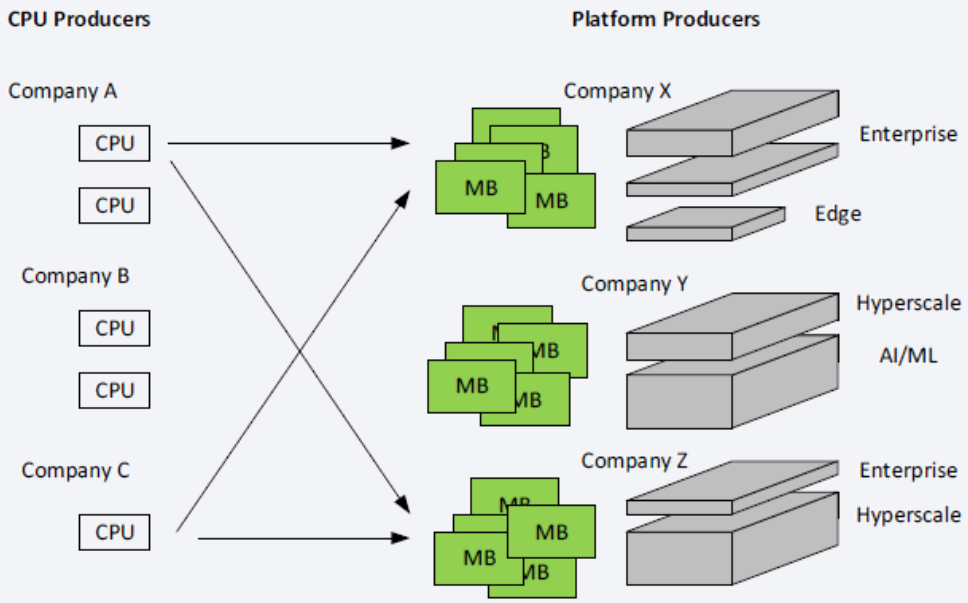
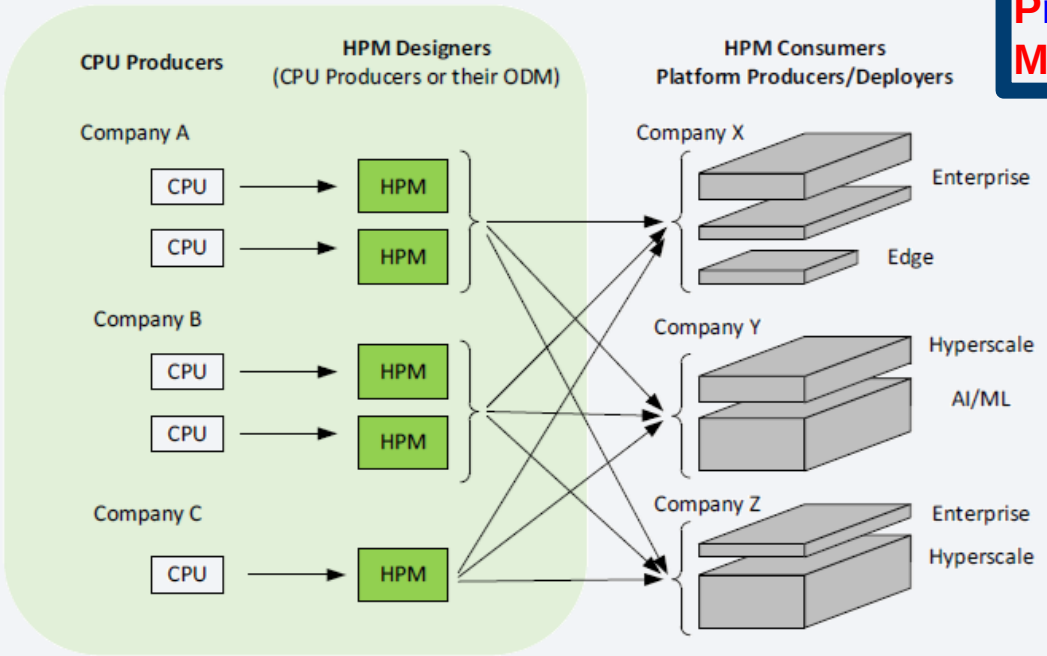
Today's Model



New Model w/ DC-MHS

HPM = Host Processor Module

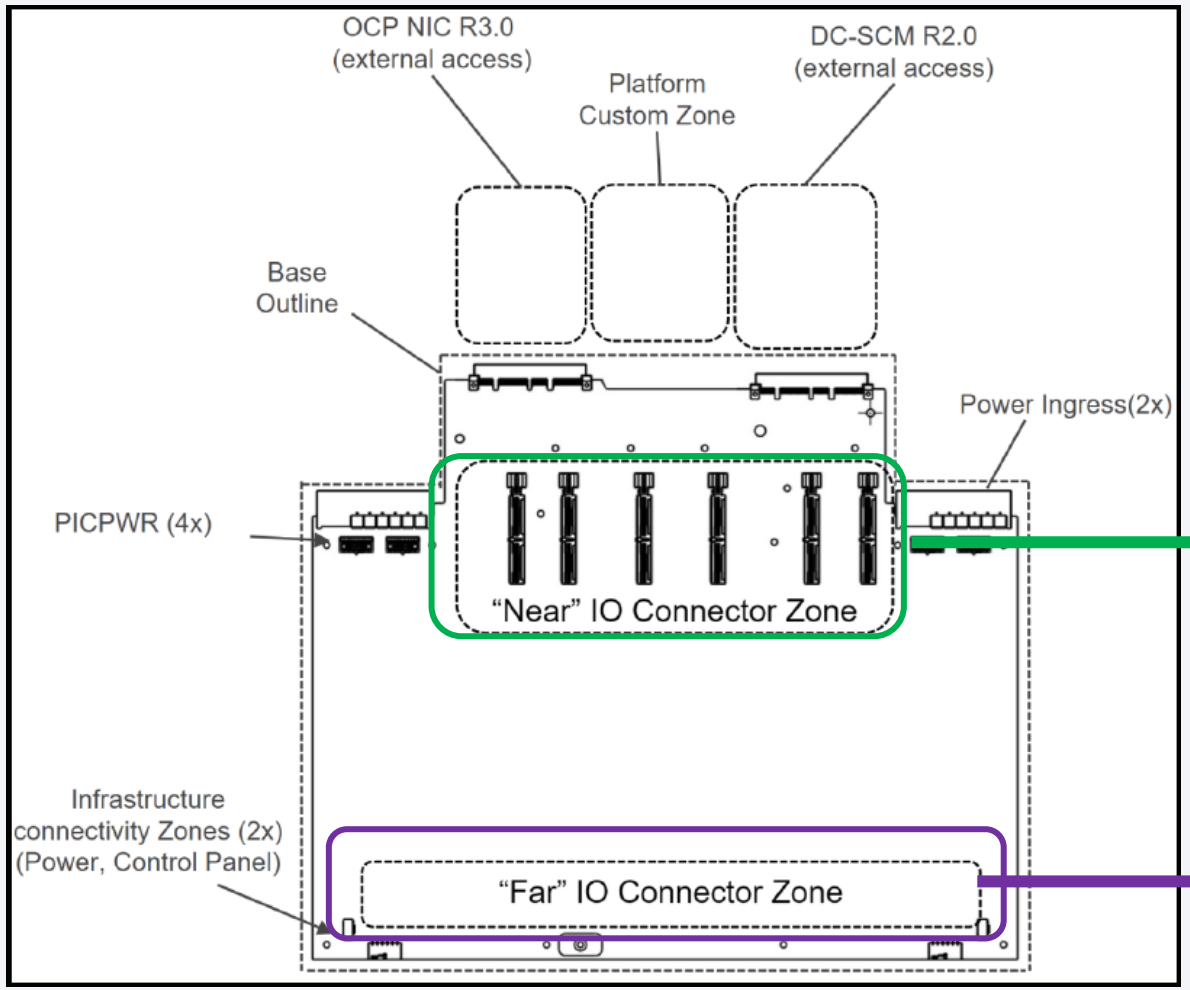


Connect. Collaborate. Accelerate.

Data Center – Modular Hardware System Revision 1.0

- DC-MHS R1 provide **consistent interface and form factors** among modular building blocks to realize **interoperability** between datacenter, edge and enterprise infrastructure.
- DC-MHS R1 standardizes a **collection of HPM (Host Processor Modules)** form-factors and supporting ingredients to allow interoperability of HPMs and platforms.

CMIO Solutions for OCP DC-MHS



Solutions for Near End IO Connector

Multi-Trak™ (SFF-TA-1033)
16x+Power/8x+Power/Power Only….

Solutions for Far End IO Connector

MCIO (SFF-TA-1016) VT/RA

NearStack (SFF-TA-1026) VT

Swift/Swift DE/Swift LP VT

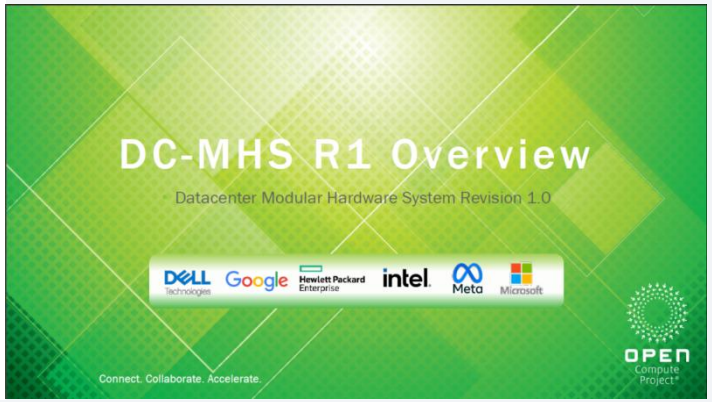
For Release	ID	Title	Published Revision	Draft Revision	Status
2022-08-12	SFF-TA-1033	Internal High-Speed Cable / Modular Connector System	-	-	New Project Initiated

Multi-Trak™ is associated with SFF-TA-1033.

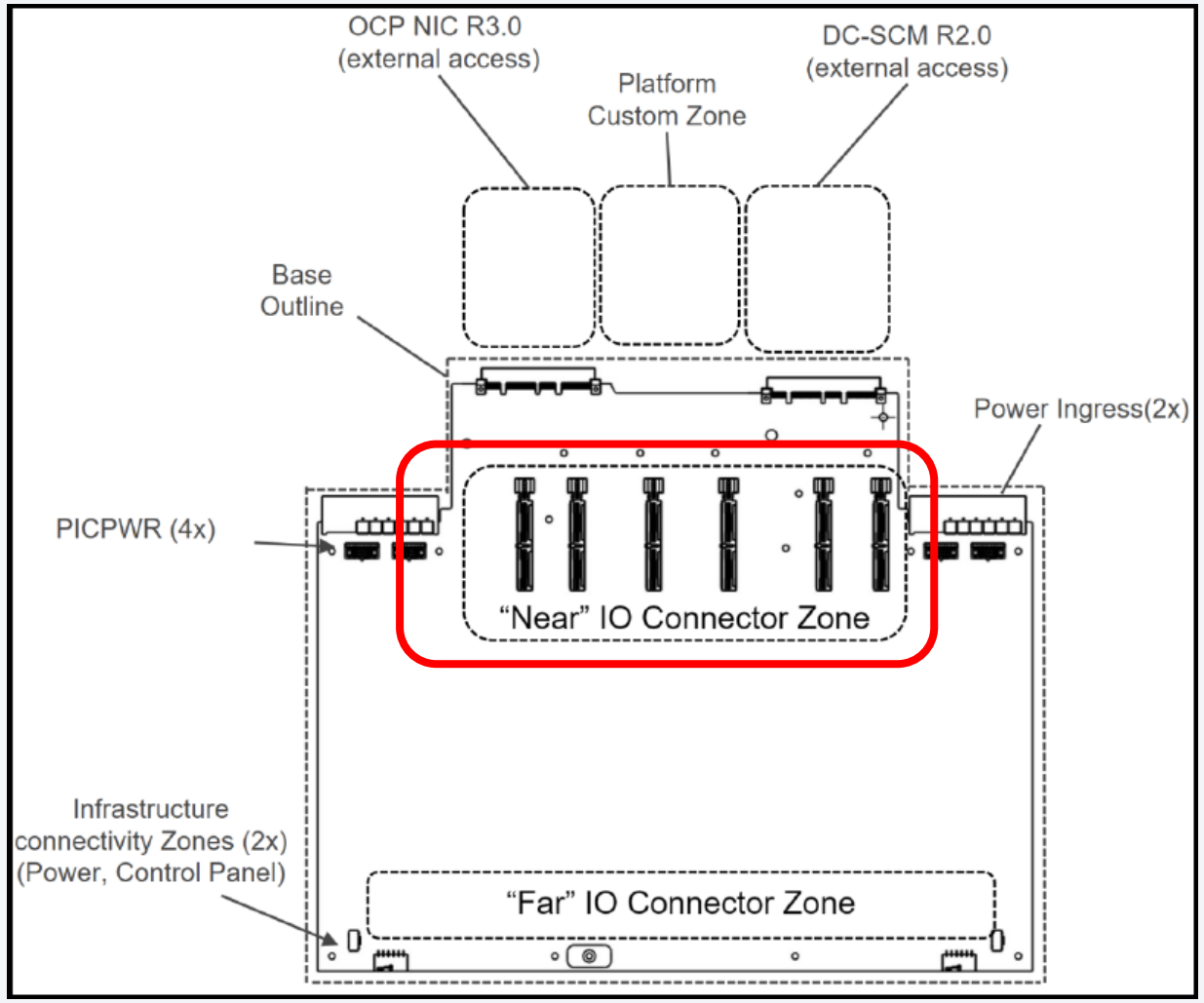
Multi-Trak™

SFF-TA-1033/OCP-MHS

OCP official released DC-MHS spec and use Multi-Trak™ as Near end side M-XIO solutions.



OCP DC-MHS Application



- **Near End side**

  Suggest to use Amphenol's **Multi-Trak™**.

1) *The required connector for Near IO Riser positions shall be SFF-TA-1033.*
   a) This Near IO connector can support either rigid or cabled riser connections.

Table 3. Table of IO allocation and connector priorities for Near IO connector SFF-TA-1033

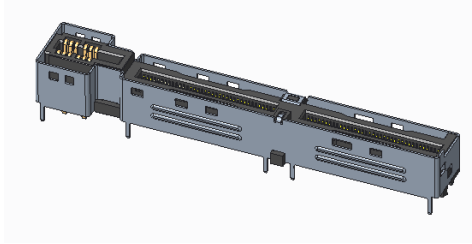
Recommended Priority	High speed connector housing	High speed routing	Power bay
1	X16	X16	power
2	X16	X8	power
3	X8	X8	Power
4	None	None	Power
5	Depopulate all connectors		

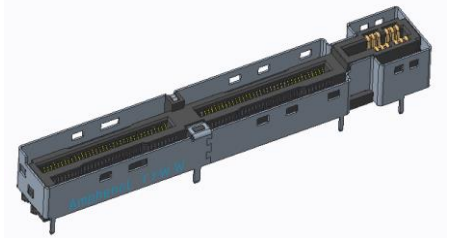
Multi-Trak™ Introduction
(SFF-TA-1033)

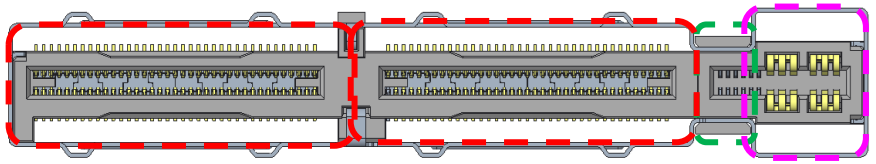
Amphenol CS introduces to the market the next generation interconnect solution – **Multi-Trak™**, which is a combo connector that includes two standard MCIO, 12Pins of SB, and 4Pins of Power to support the combined function to reduce the limited space.

0.60 mm pitch for STD MCIO and SB, combination form factor capable of transmitting high-speed signal up to **PCIe Gen 5** and target for **PCIe Gen6.**

Total support ***21A power*** per current design, modularized expansion for SB and Power.





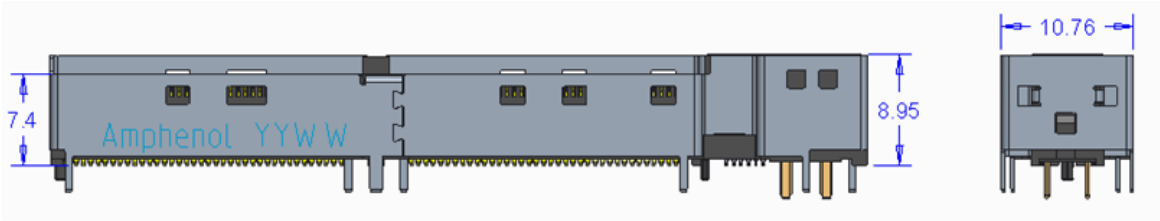


4 pins of Power solution DIP type, Total 21A

MCIO 74Pins
Gen 5 solution
X8+20pins SB

MCIO 74Pins
Gen 5 solution
X8+20pins SB

12 pins SB
Pitch:0.6mm
SMT type



32Gbps

NRZ (Ready)

Upgrade to PCIe GEN6

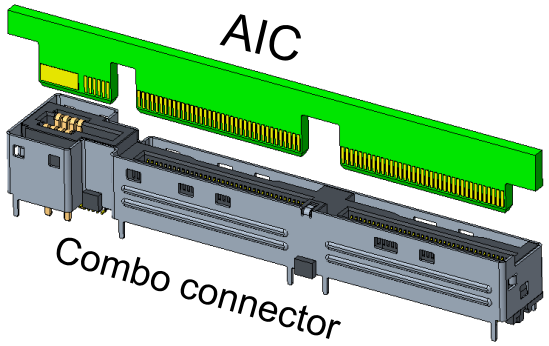
64Gbps

PAM4(developing)

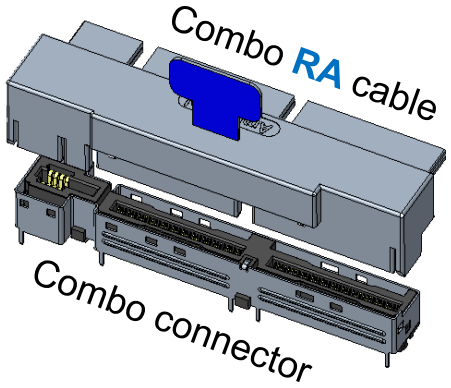
Features	Benefits
・Pitch 0.60 mm, combo connector	・Providing enhanced flexibility in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
・Up to PAM4 56Gbps, over 1 m transmission distance	
・Dual-use, supporting both cable and card edge connection with one identical connector	・Real economic choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses
・Target to standard form factor, covering most common uses applications in data centers such as PCIe/NVMe/OCP NIC…etc.	

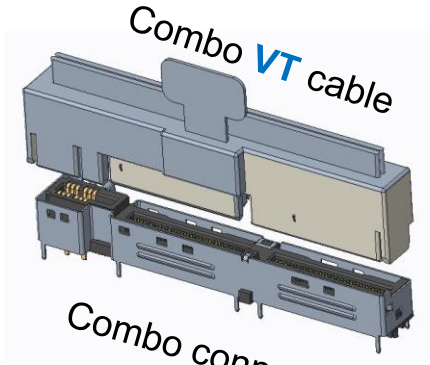
Design Concept

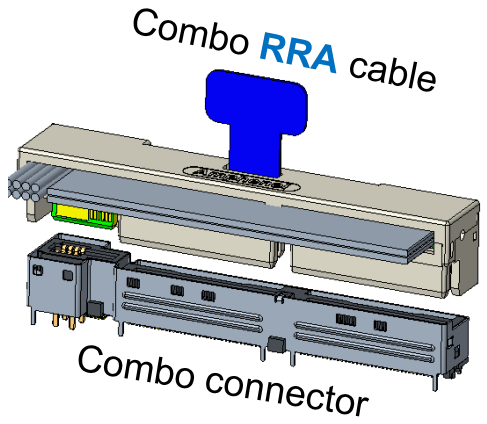
Application 1:
One AIC plug in a combo connector

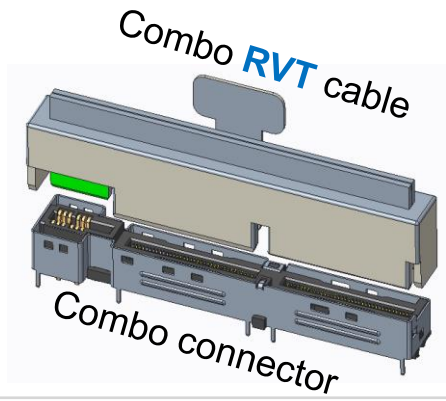


Application 2:
Combo cable

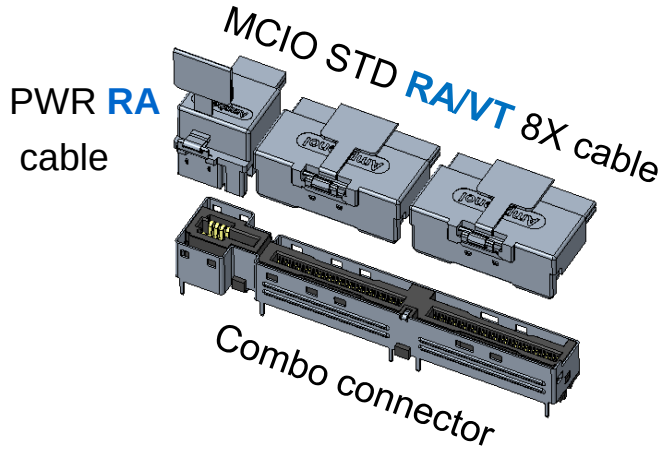


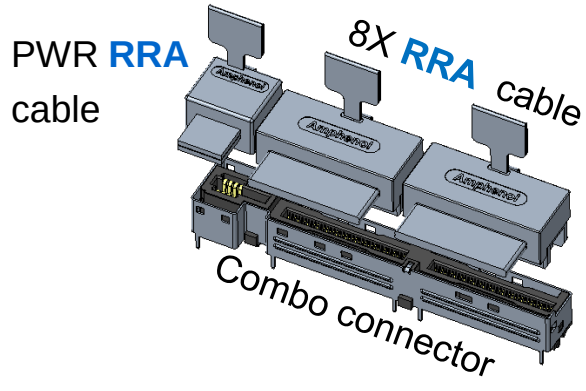




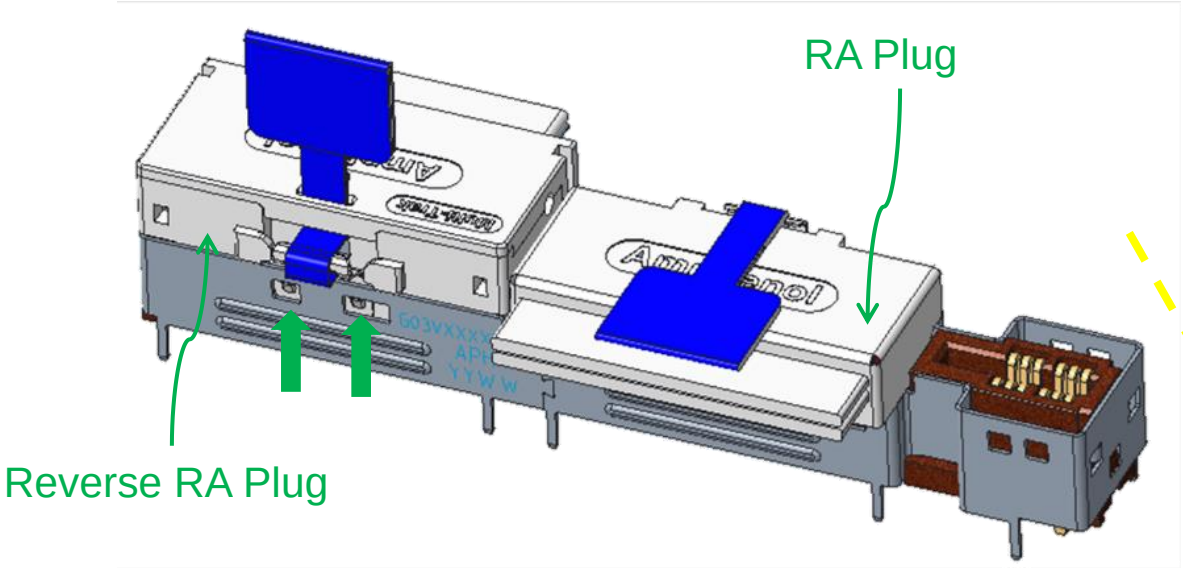


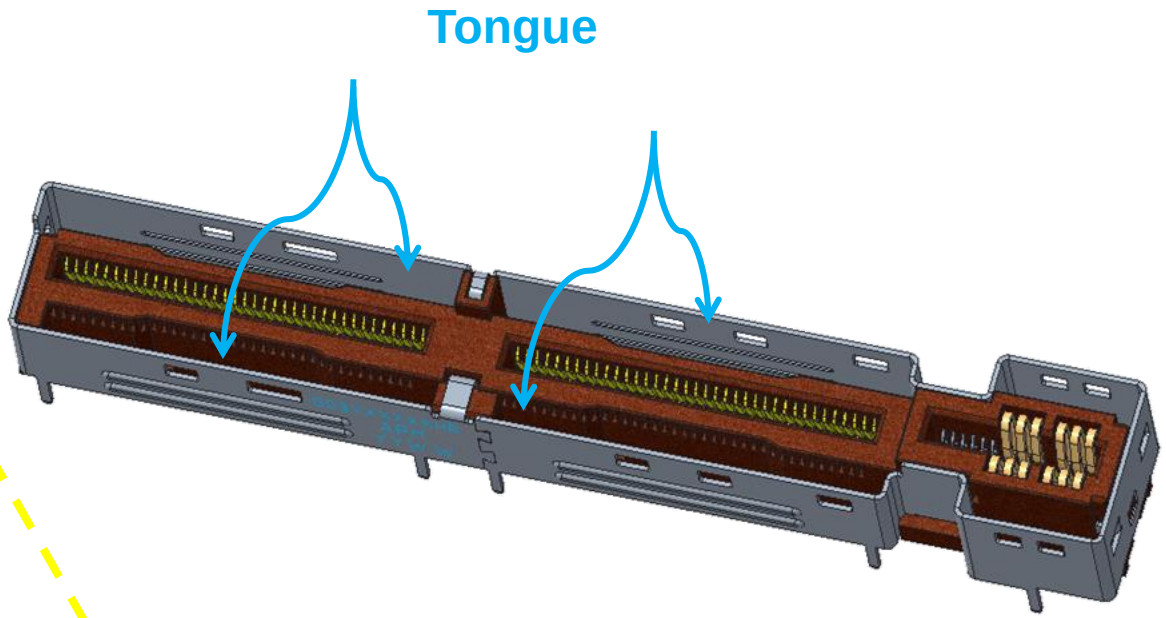
Application 3:
STD MCIO 2*8X cable



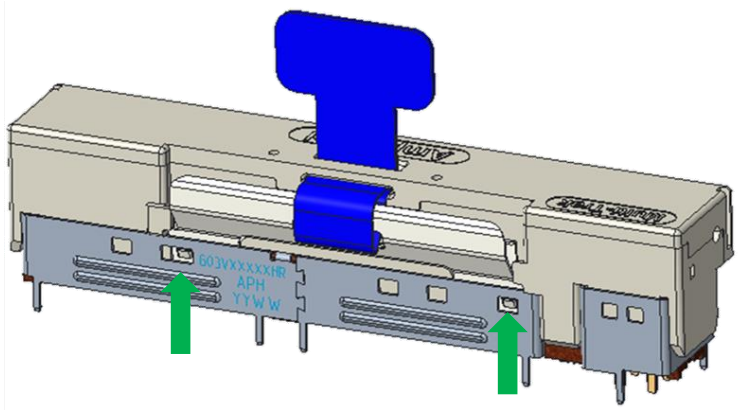


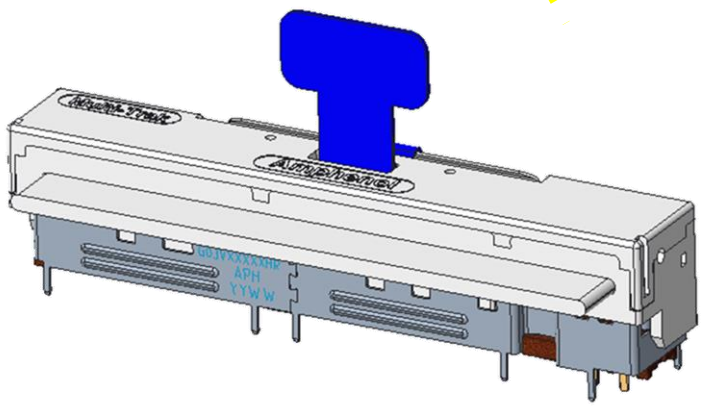
Design Concept





latch holes



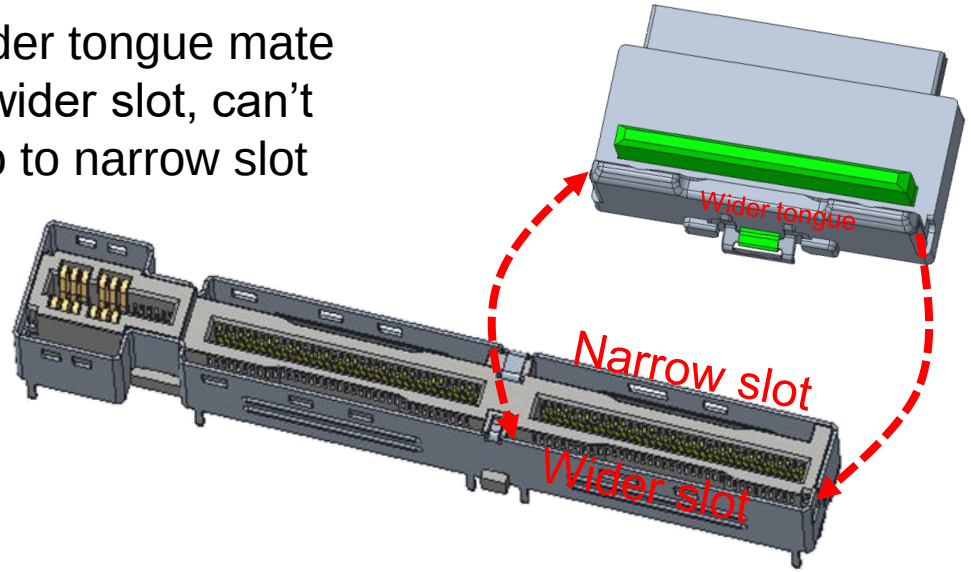
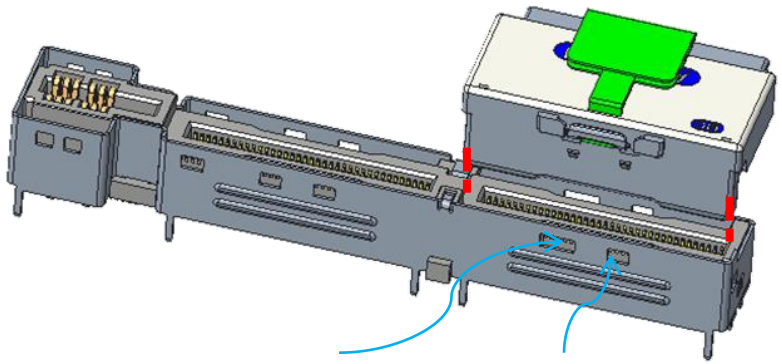
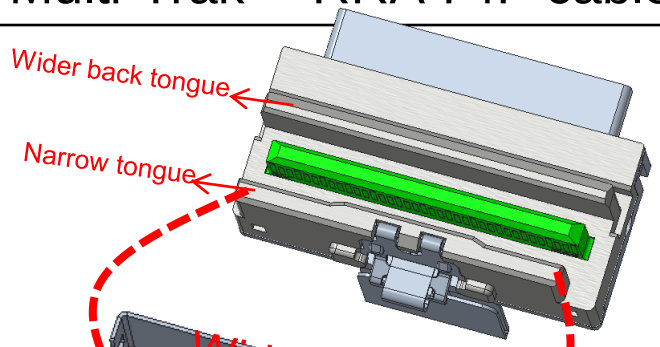
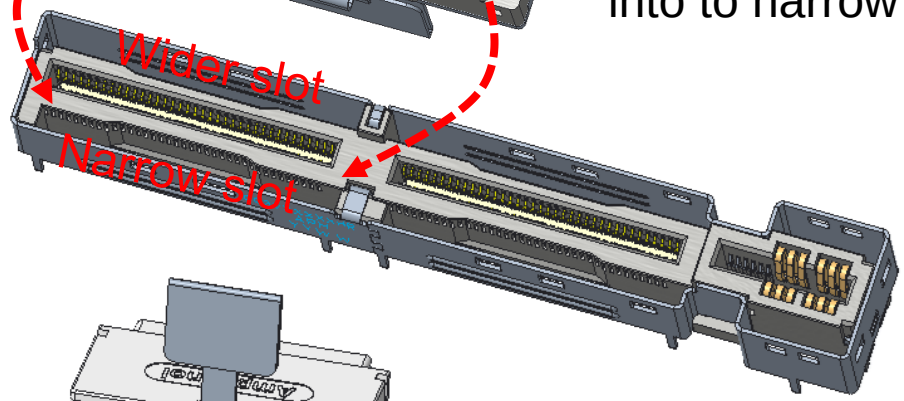
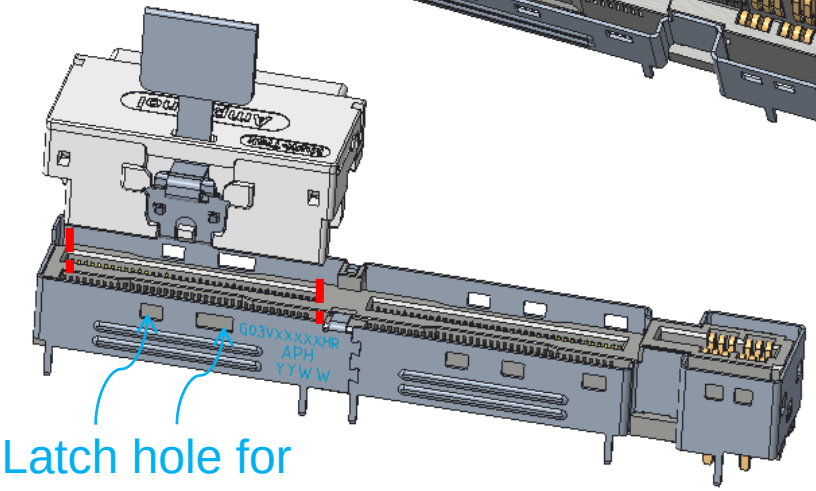


Fool-proof design features for plugs mating:

Latch holes & Tongue

Receptacle connector and two kinds of plug (RA & Reverse RA) have fool-proof design features, which can avoid two kinds of plug misuse.

Design Concept

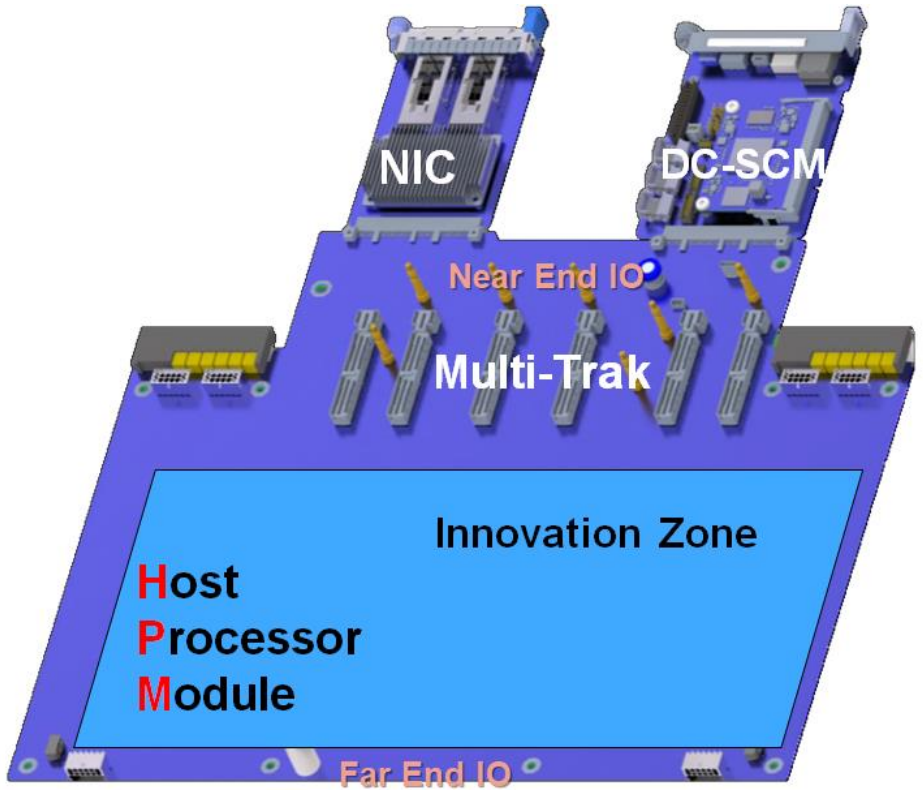
	MCIO RA cable	Multi-Trak™ RRA 74P cable
cable insert **correctly**	Wider tongue mate to wider slot, can't into to narrow slot  The tongue can enter the corresponding slot. 	 Wider back tongue mate to wider slot, can't into to narrow slot  

Multi-Trak™ Introduction

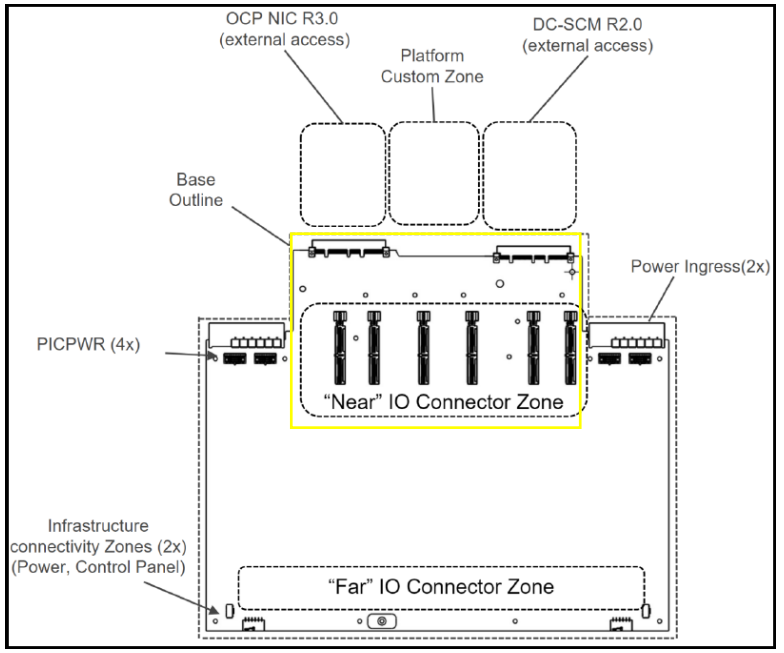
OCP (DC-MHS)

Data Center - Modular Hardware System

suggest Multi-Trak™ use to Near End side.



15	The Required connector for Near IO positions shall be SFF-TA-1033.



10.12.1. Location of Near Side M-XIO Connectors

Note, that Near IO Requirements are mechanically focused to enable reuse of chassis and IO subsystems.

1) *The required connector for Near IO Riser positions shall be SFF-TA-1033.*
   a) This Near IO connector can support either rigid or cabled riser connections.

2) An HPM might not use all 6x Near IO positions, but designers are recommended to use maximum number of possible positions. *For Near IO implemented positions, the Near IO Connector shall be placed at locations defined in* ***Figure 18.***

3) Additional and/or Alternate connectors used within the Near IO zone are allowed.
   - Alternate connector types, location and use cases are outside the scope of this specification.

4) Adoption of the following allocation priority in is recommended. Following this recommendation may result in increased applicability and interoperability of the HPM.

Application: Traditional Server layout reference

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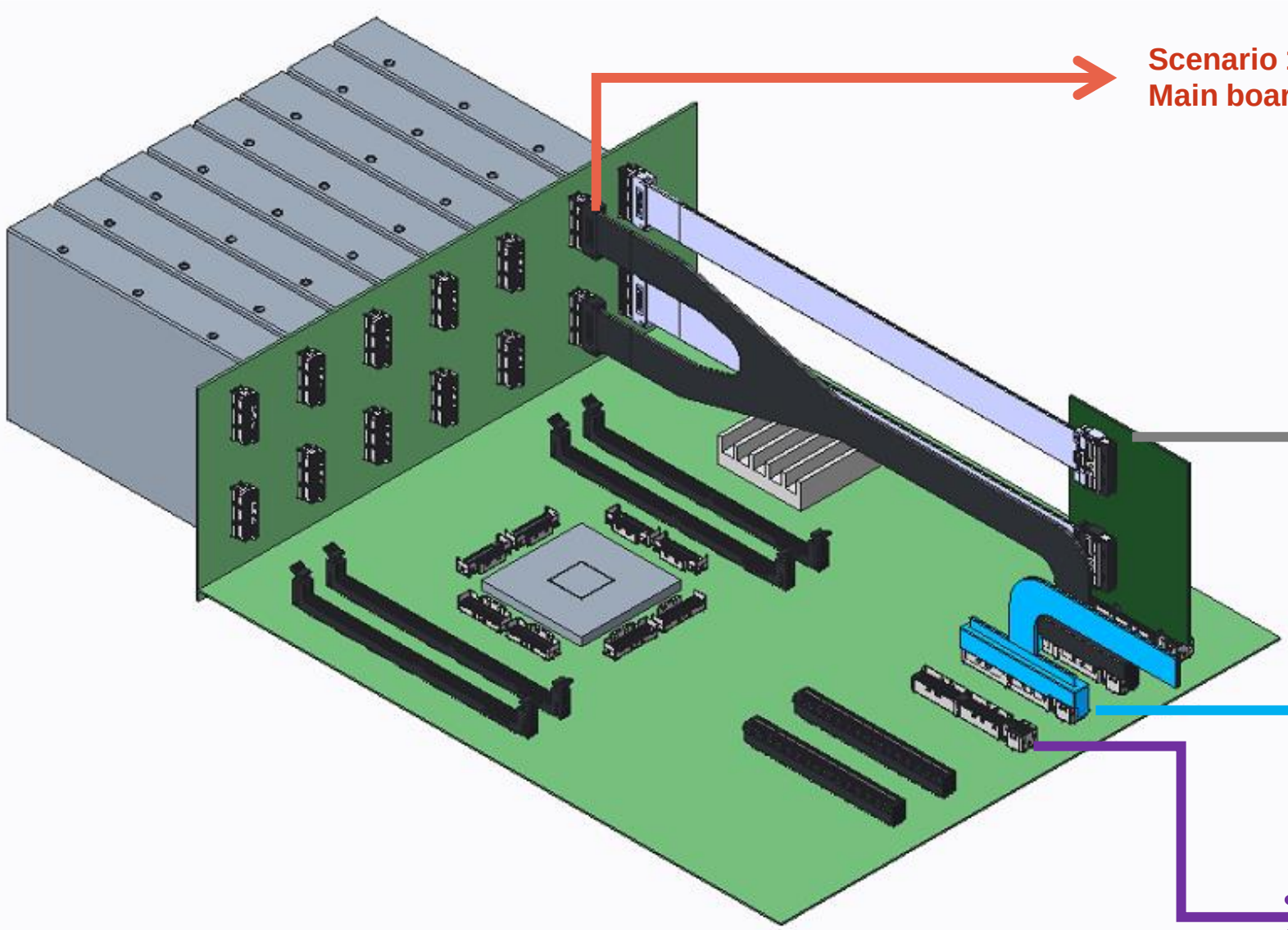
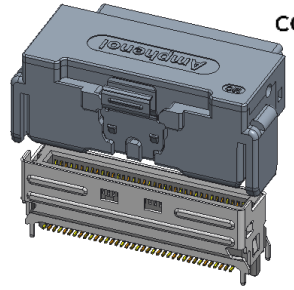
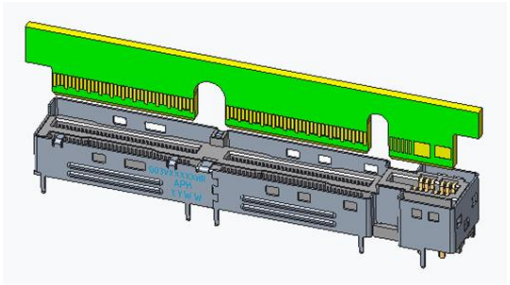


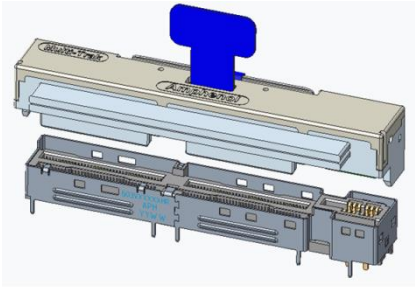
Scenario 1:
Main board to mid plane



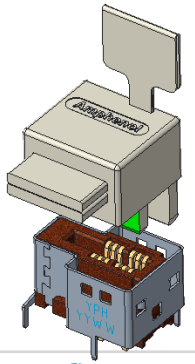
Scenario 2:
Riser expansion



Scenario 3:
Main board to IO

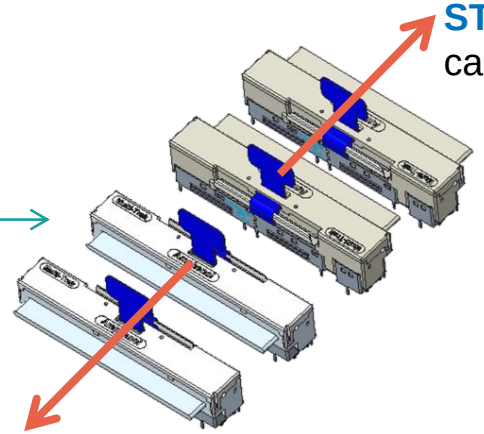


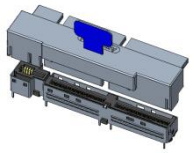
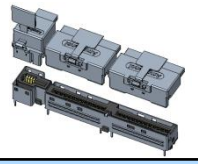
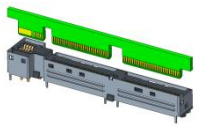
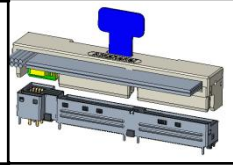
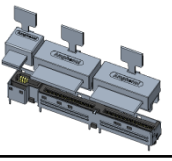
Scenario 4:
Power transmission



Benefit to customer

- ✓Combine original PCIE and MCIO to be one connector, include POWER and high/low speed signal.
- ✓Reverse cable for easy to organize the layout.
- ✓ Variety of plugs to support different routing requirement.
- ✓Modularized design for further expansion, card and cable interactive support.
- ✓Upgrade to **Gen6** version and apply to **PCI SIG** to be a standard connector.
- ✓Support different applications for **AIC**, **Combo cable** and **MCIO STD cable**.



	Combo cable	STD Cable
		
AIC	Reverse combo cable	Reverse cable
		

Roadmap

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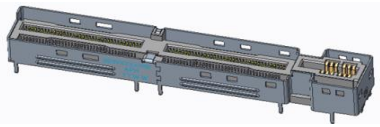
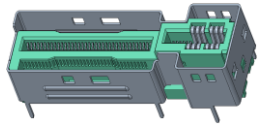
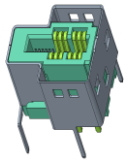
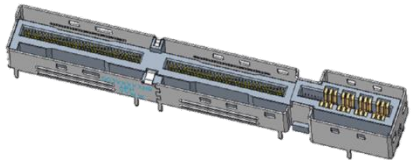
Tooled up

Type	Current Rating	Sample schedule
16X+Power(STD) (SFF-TA-1033) 	21A	Oct-mid
8X+Power(STD) (SFF-TA-1033) 	21A	End of Nov
Power(STD) (SFF-TA-1033) 	21A	Oct-end

Design Ready

Type	Status
16X+high power (Customized) 	Tool up per request
High Power (Customized) 	Tool up per request
RA type 8X+Power(STD) 	Tool up per request

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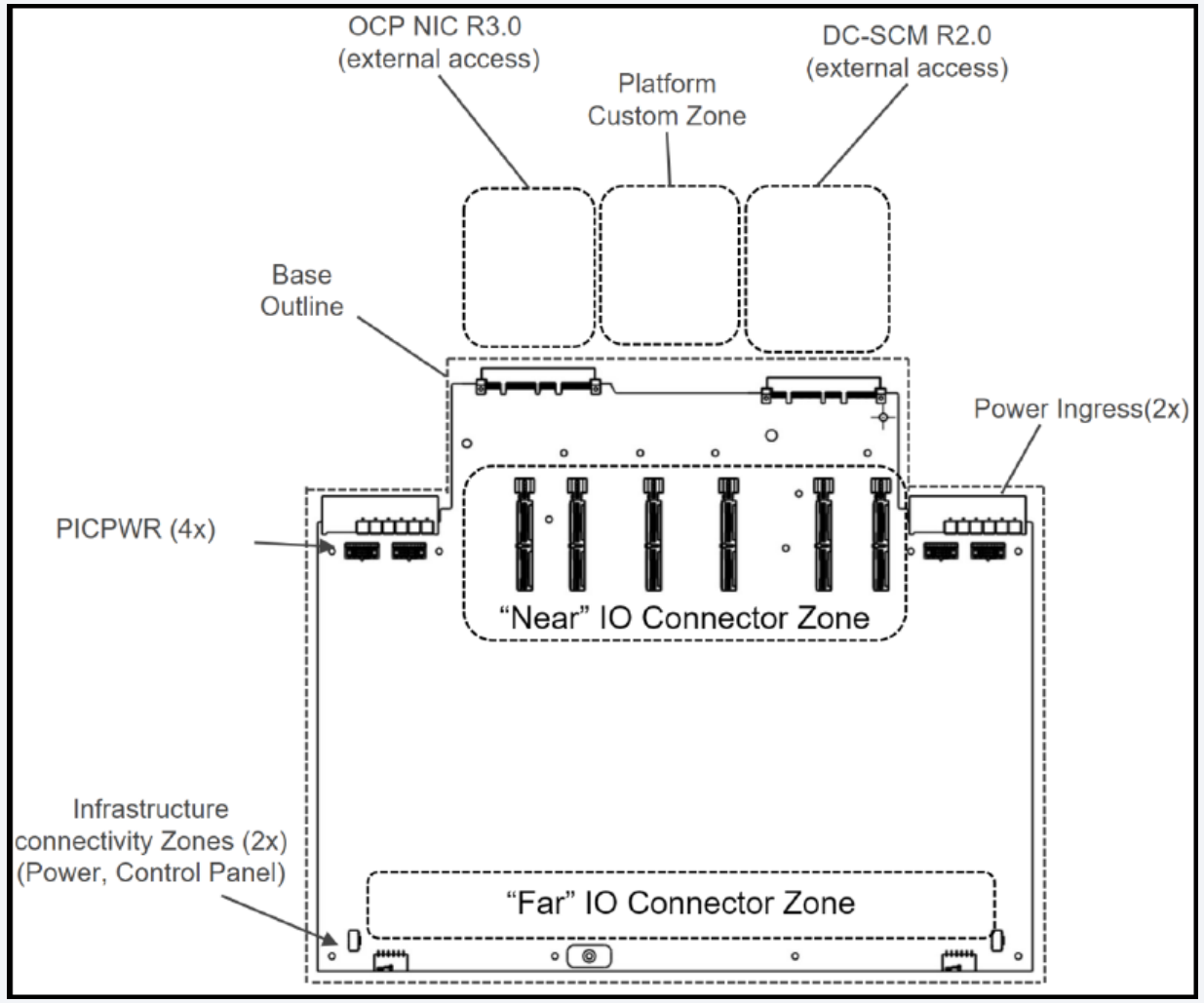
Mini Cool Edge IO

SFF-TA-1016, PCI SIG Gen5/Gen6, OCP DC-MHS

Commercial IO

OCP DC-MHS Application



- **Near End side**

  Suggest to use Amphenol's **Multi-Trak™**

- **Far End side**

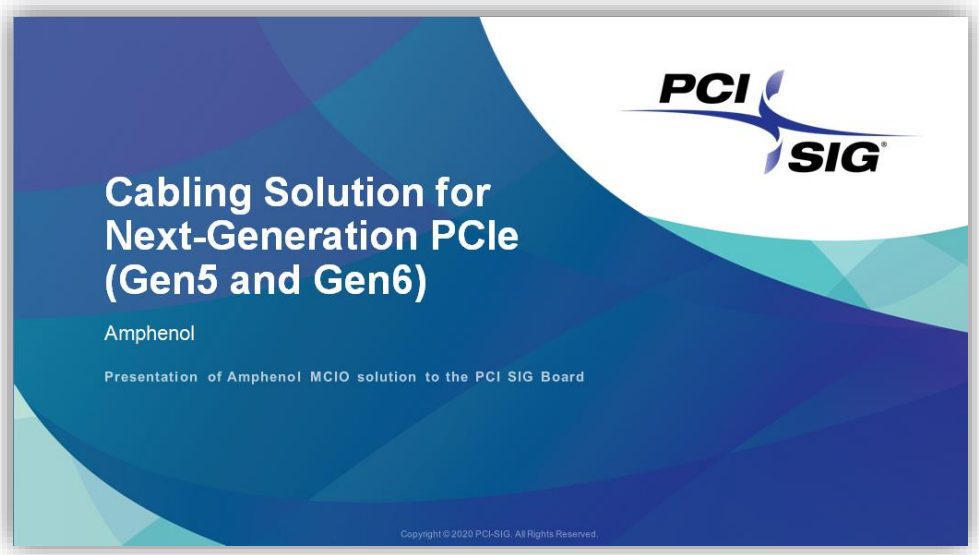
  Recommend to use Amphenol's **MCIO** to support.

Table 4. Far Side HSIO Recommended Connectors

Recommended Connector	Note
SFF-TA-1016	Must choose low profile variant
SFF-TA-1026	Appropriate due to low profile and ability to fit under thermal solutions

What is MCIO for standard?

PCIe SIG official released APH MCIO connector & cable are PCIe Gen5 internal link industrial standard.



DRAFT

SFF-TA-1016 Rev 0.0.3
Template Rev 1.0

SNIA
SFF TWG
Technology Affiliate

SFF-TA-1016

Specification for

Internal Unshielded High Speed Connector System

Rev 0.0.3 August 31, 2020.

SECRETARIAT: SFF TA TWG

This specification is made available for public review at http://www.snia.org/sff/specifications. Comments may be submitted at http://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

The description of the connector in this specification does not assure that the specific component is available from connector suppliers. If such a connector is supplied, it should comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines the mechanical specifications and general performance requirements for an Internal Unshielded High Speed Connector System that is designed for use in high speed serial interconnect applications. One such use may be as a 4, 8, or 16 lane (or more) receptacle and the mating cable plug for multiple generations of internal high speed applications.

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Chairman SFF TA TWG
Email: SFF-Chair@snia.org

DRAFT

MCIO is associated for SFF-TA-1016.

Mini Cool Edge IO
(SFF-TA-1016)

Amphenol COMMUNICATIONS SOLUTIONS

Amphenol CS introduces to the market **SFF-TA-1016** standard interconnect solution – **Mini Cool Edge IO**, which is 0.60 mm pitch, slim form factor design yet capable of transmitting high-speed signal up to **PAM4 56G** over the distance overwhelming the conventional routings.

The Mini Cool Edge IO provides not only a SI performance ready signal transmission media but also a new way of system design thinking that will lead your electronic system to a completely ***cost effective***, ***highly modularized & scalable***, and extremely ***easy repairing*** masterpiece.

Features

- Pitch **0.60 mm**, both V/T & R/A form factors
- Up to **PAM4 56Gbps**, over **1 m** transmission distance
- **Dual-use**, supporting both **cable and card** connection with one identical connector
- Optional **85Ω or 100Ω** impedance and variety of pin no. options – covering most common uses applications in data centers such as PCIe/NVMe/SAS/SFP(+)/SFP 28/…

Benefits

- Providing enhanced **flexibility** in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
- Real **economic** choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses

32Gbps
NRZ

56Gbps
PAM4

Internal
Connection
Blind Mate
(Floating) Connection

Multiple Form Factor
Wide Variety Solution Supported

Data Center Applications Supported:

- ✓ **PCI-Express**
- ✓ **NVMe**
- ✓ **SFP/SFP+/SFP28**
- ✓ **SAS**

Product Details – MCIO

PCIe Gen 5 & UPI 2.0 Series (G97)

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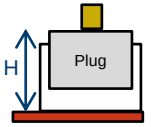
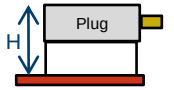
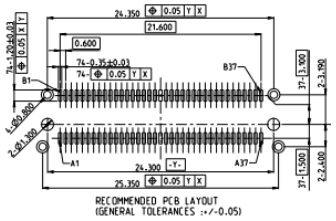
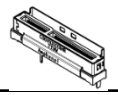
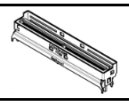
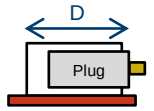
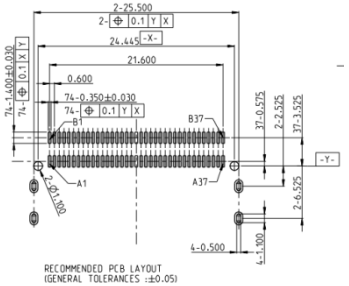
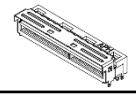
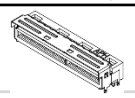
Spec	Form Factor	Pin	Recommended Channel: with Sideband	Recommended Channel: w/o Sideband	Pic	Width (mm)	Mating Height (mm)	Footprint
• NRZ 32G, 85Ω • Supports both Card (T 1.57 mm) & Cable connection) • Pitch 0.60 mm • Voltage Rating: 30V_{DC} • Operating Temperature: -25℃ ~ 60℃ • Storage Temperature: -40℃ ~ 85℃ • Ambient Humidity: 80% R.H. Maximum	V/T	38	4x + Sideband	6x		15.00	Straight Exit: 15.90 mm  Right Angle Exit: 13.95 mm 	
		50	6x + Sideband	8x		18.60		
		74	8x + Sideband	12x		25.80		
		84	8x + Sideband	13x		35.60		
		124	16x + Sideband	20x		42.00		
		148	20x + Sideband	24x		49.20		
	R/A	38	4x + Sideband	6x		15.00	Straight Exit: 18.50 mm 	
		74	8x + Sideband	12x		25.80		
		84	8x + Sideband	13x		35.,60		
		124	16x + Sideband	20x		42.00		
		148	20x + Sideband	24x		49.20		

Commercial IO

Product Features:
Internal Type

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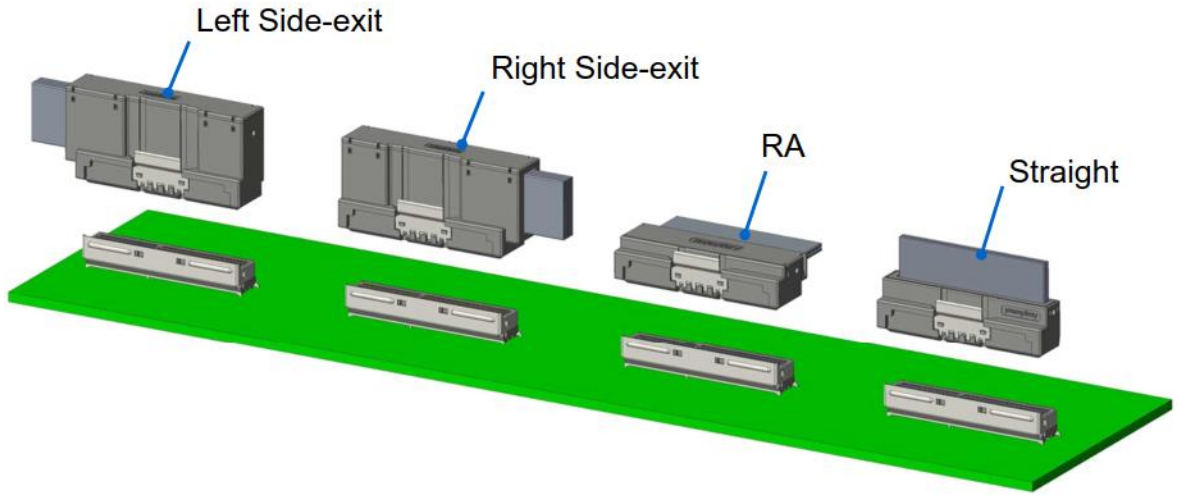
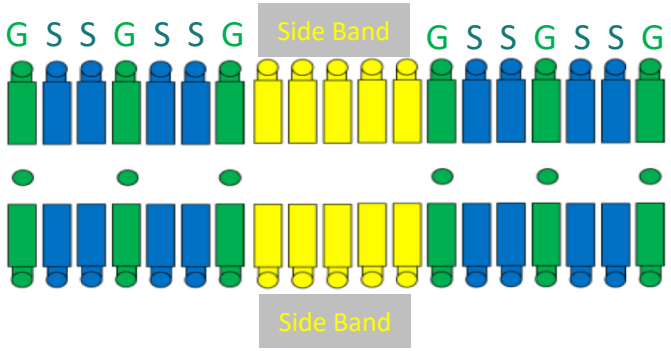
COMMUNICATIONS SOLUTIONS

***Multiple cable types** to support wide variety of mechanical requirement.*





Ex. 38PIN
Option 1: 4 pair HS channel + side band
Option 2: 6 pair HS channel
Option 3…..

For 92ohm and 85ohm MCIO,
We have full high-speed to different side band choices – extreme flexible on customization pin define.

PCIe Develop Roadmap Trend–MCIO

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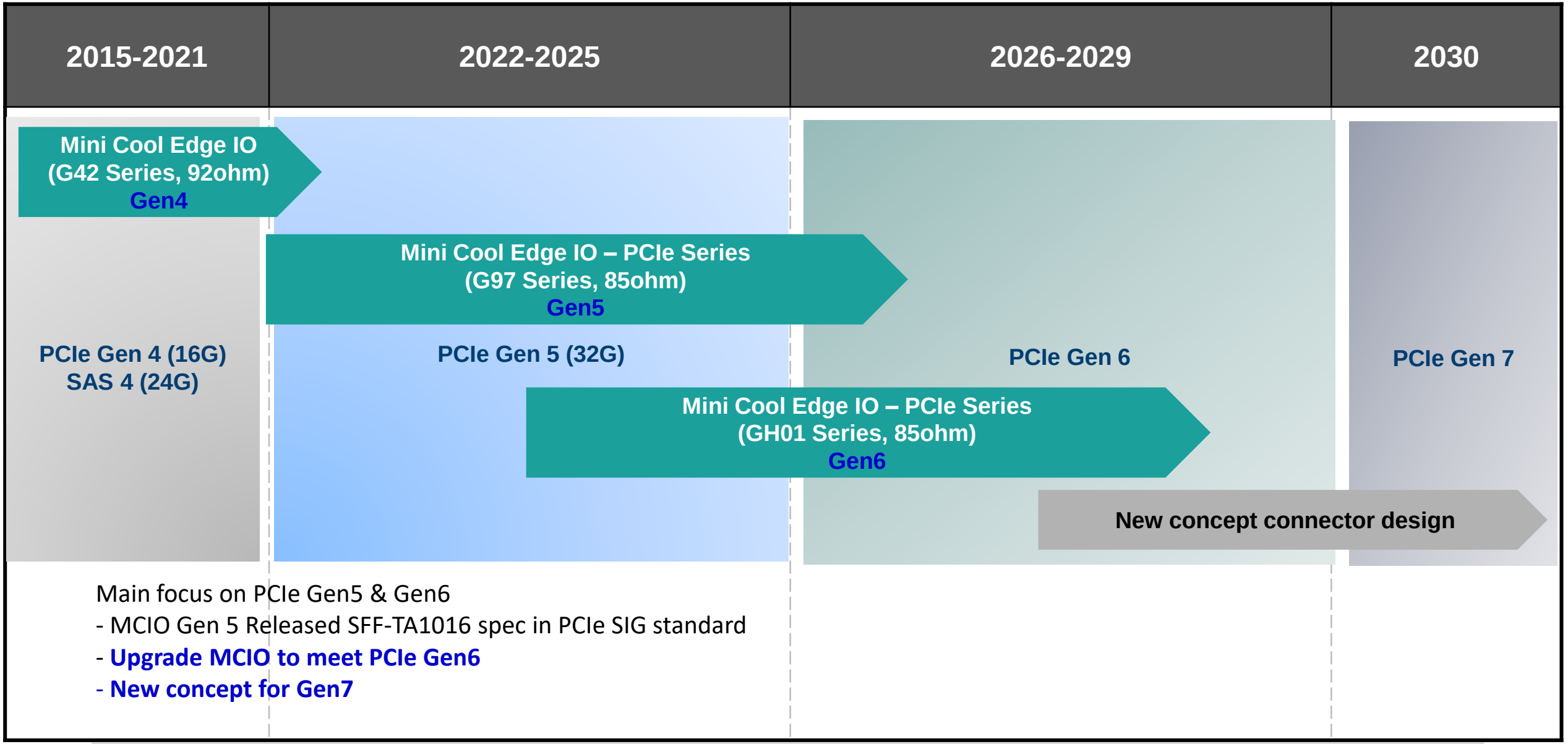

Main focus on PCIe Gen5 & Gen6
- MCIO Gen 5 Released SFF-TA1016 spec in PCIe SIG standard
- **Upgrade MCIO to meet PCIe Gen6**
- **New concept for Gen7**

Commercial IO

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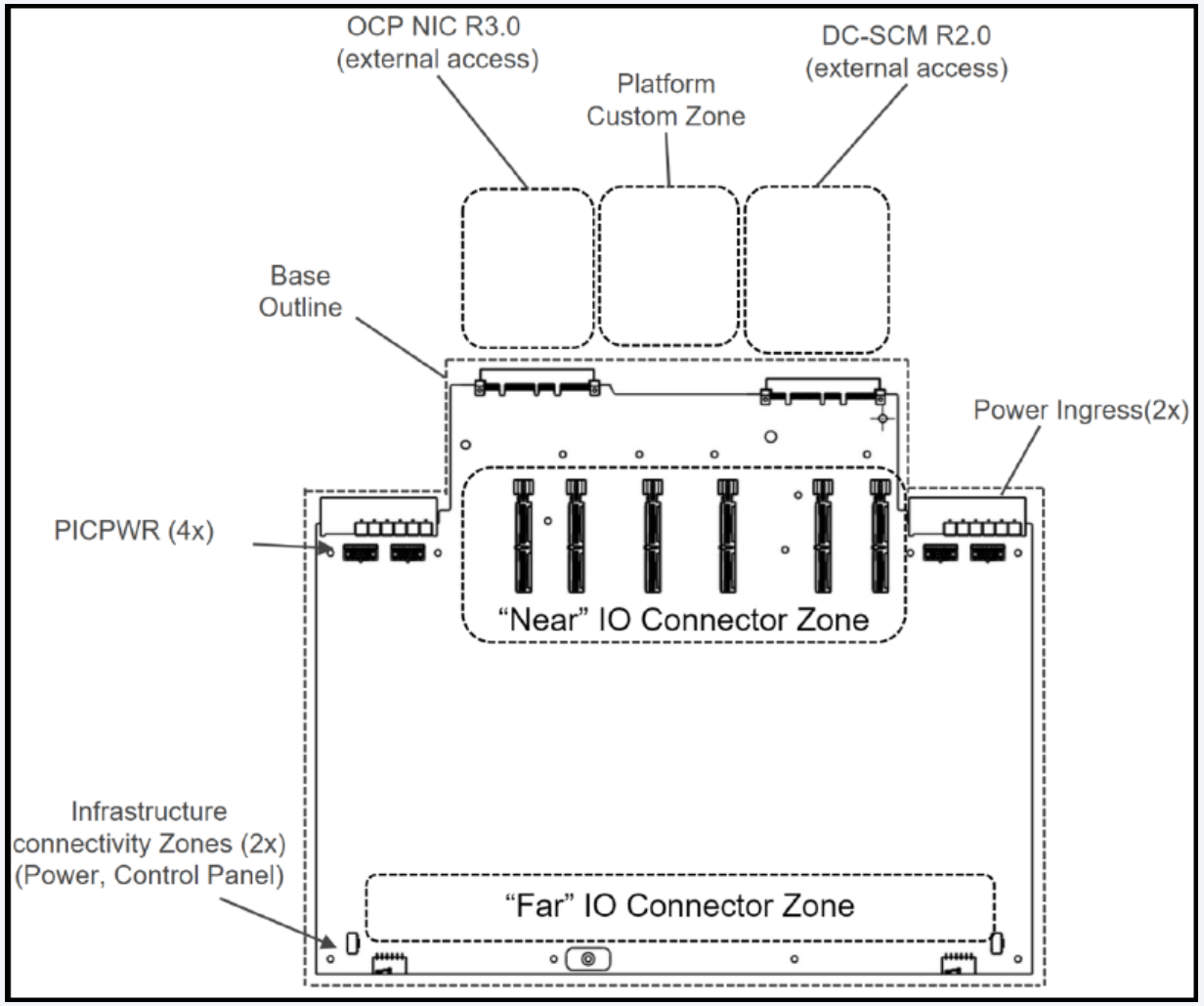
COMMUNICATIONS SOLUTIONS

OFS-IO (NearStack)

SFF-TA-1026/OCP DC-MHS

Commercial IO

OCP DC-MHS Application



- **Near End side**

  Suggest to use Amphenol's **Multi-Trak™**

- **Far End side**

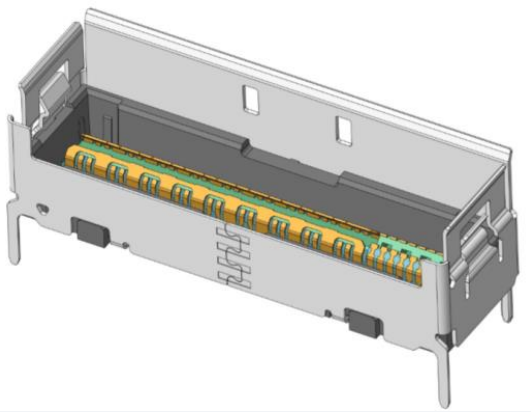
  We have **OFS-IO (Nearstack)** compatible products to support.

Table 4. Far Side HSIO Recommended Connectors

Recommended Connector	Note
SFF-TA-1016	Must choose low profile variant
SFF-TA-1026	Appropriate due to low profile and ability to fit under thermal solutions

OFSIO(NearStack)

OFSIO(NearStack) series is the next generation of interconnect solution, with 0.6mm pitch and is capable with signal up to PCIe Gen5 NRZ 32GT/s and PAM4 56GT/s. Compatible to SFF-TA-1026 industry standard.



Specification:

32Gbps
NRZ

56Gbps
PAM4

Features:

- Pitch 0.6mm with VT form factors
- Up to NRZ 32GT/s, over 1m transmission distance
- Covering most common uses applications in server/data center applications such as PCIe/NVMe/SAS/SFP/…

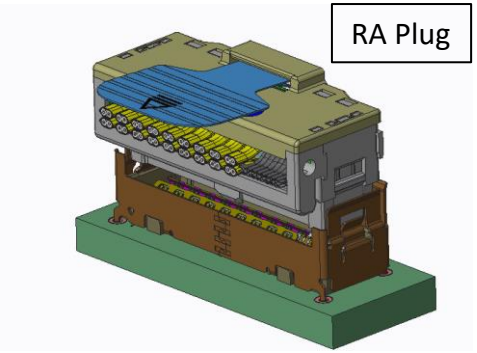
Target Market:

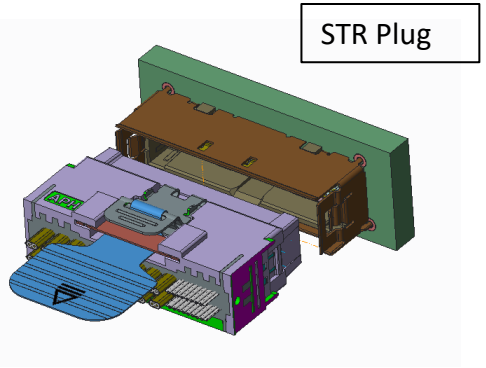
Baseband
Commercial Systems
Networking
Radio Units

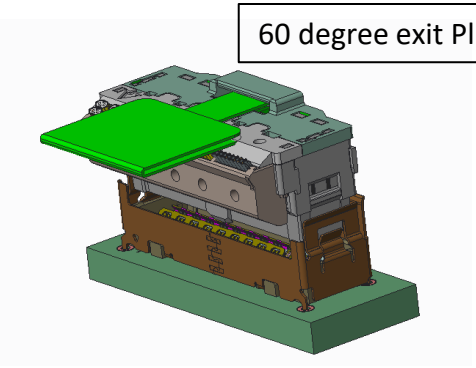
High-end
Computing system
Server/Storage

OFSIO(Nearstack) Product Roadmap

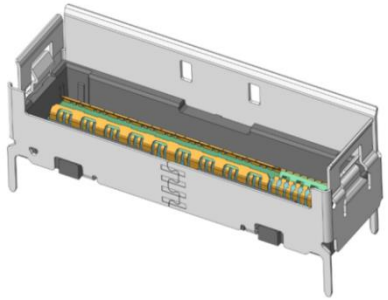
- **For Cable Assembly, now we can provide RA, STR and 60 degree exit in Q2 2021.**







- **For Receptacle, we can provide 8x 72 pin for 85 ohm product.**



OFSIO(NearStack) Product Roadmap

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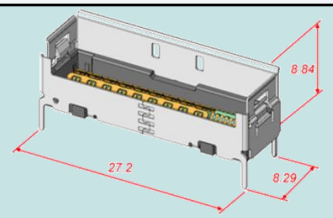
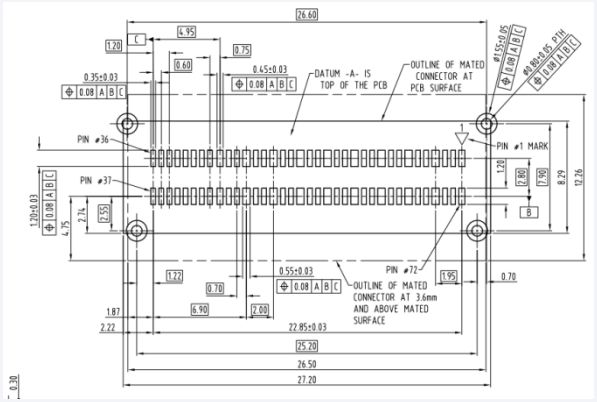
NearStack							
Configuration		Plug				Receptacle	
Type	Positions	Impedance	Straight	Right Angle	60 degree Exit	Impedance	Vertical
8X	72	85	Q2	Q2	Q2	85	Available

Category	Receptacle Dimension	Mating Dimension
Dimension	27.2*8.29*8.84 	27.2*11.27*12.35  

- **Footprint:**



- **Pin Assignment:**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	S	S	S	S	S	S
G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	S	S	S	S	S	S
72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37

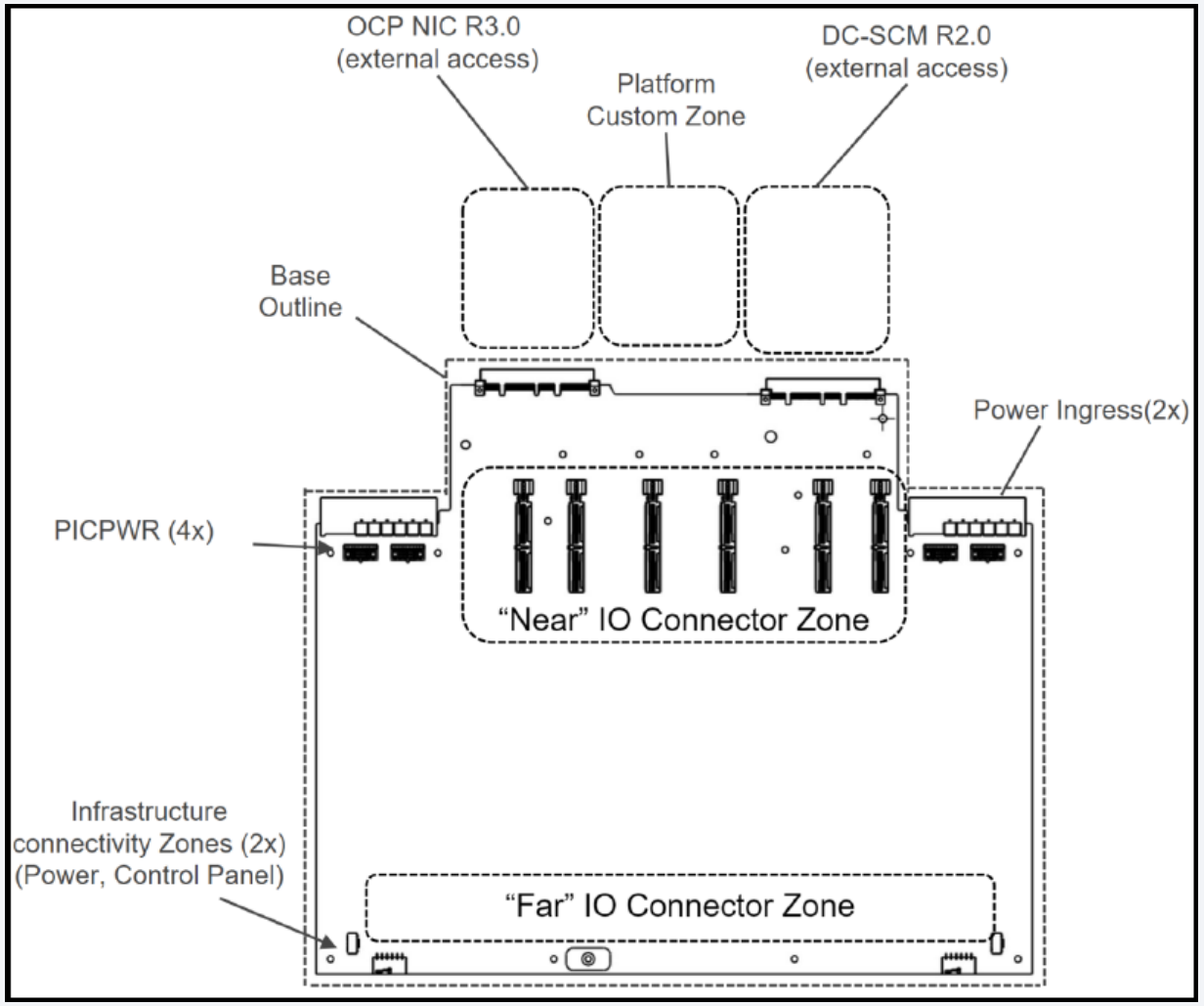
Commercial IO

Amphenol
COMMUNICATIONS SOLUTIONS

ExtremePort™ Swift Series

Commercial IO

OCP-MHS Application



- **Near End side**

  Suggest to use Amphenol's **Multi-Trak™**

- **Far End side**

  No specified in M-FLW, but need to meet the requirement of low profile and cable mating solutions(Under 12mm)

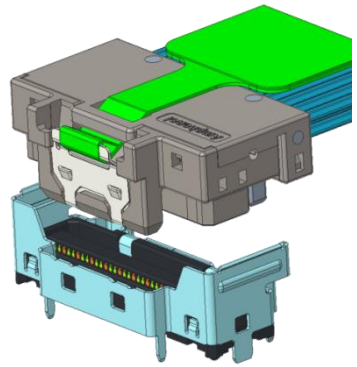
  Suggest to use Amphenol's **Swift series for ultra low profile requirement**

18	High Speed IO connector choices for the Far Side Shall meeting the Height Restriction requirements	Section 10.13
19	Primary side component height restriction zone shall be implemented	Figure 20, Section 10.14

For thermal solutions, one must consider the allowable variance in numbers, types, and location of Compute Core items. Thus, a fixed 12mm for component height restriction in the Compute Core area is intended to allow air cooling heatsinks or liquid cooling hardware of any variance. DIMM sockets are exempt from the 12mm component height restriction. All other soldered

ExtremePort™ Swift Series

Amphenol COMMUNICATIONS SOLUTIONS



Amphenol CS introduces to the market the next generation interconnect solution – **ExtremePort™ Swift**, which is 0.60 mm pitch, extreme low profile factor yet capable of transmitting high-speed signal up to **PCIe Gen 5** and target for **PCIe Gen6** under extreme mechanical condition.

The ExtremePort™ Swift provides not only a SI performance ready signal transmission media but also a new way of system design thinking that will lead your electronic system to a completely ***cost effective***, ***highly modularized & scalable***, and extremely ***easy repairing*** masterpiece.

32Gbps
NRZ (Ready)

64Gbps
PAM4(Tooling)

112Gbps
PAM4(Future development)

High Density
on one identical connection

Data Center Applications Supported:

- ✓ **PCI-Express**
- ✓ **NVMe**
- ✓ **UPI**
- ✓ **Ethernet**
- ✓ **SAS**

Features

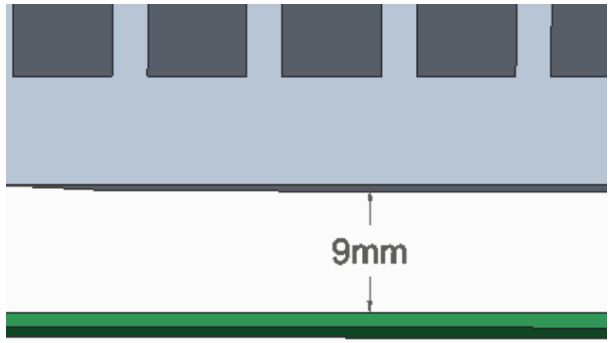
- Pitch 0.60 mm with V/T low profile form factors
- Up to NRZ 32G, over 1 m transmission distance
- Covering most common uses applications in data centers such as PCIe/NVMe/UPI/SAS/Ethernet/…

Benefits

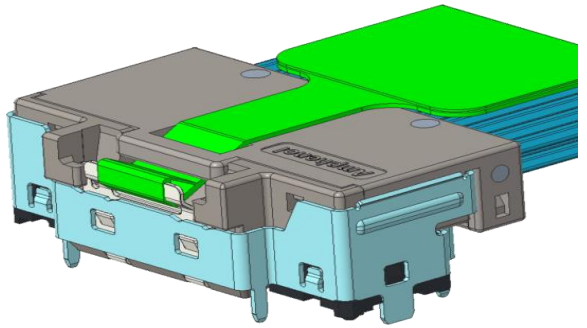
- Providing enhanced flexibility in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
- Real economic choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses

Commercial IO

Product Features

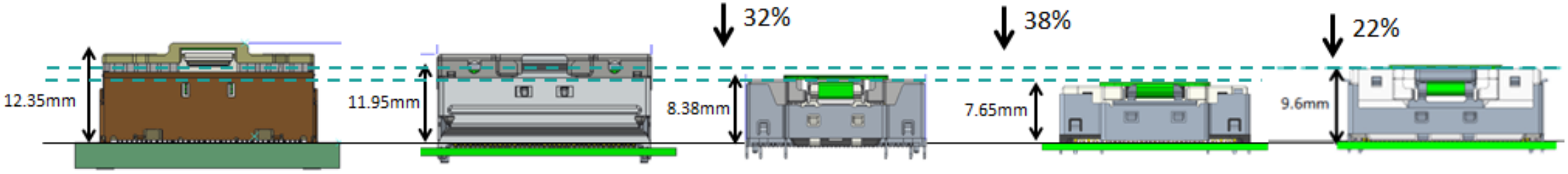


Near the chip applications

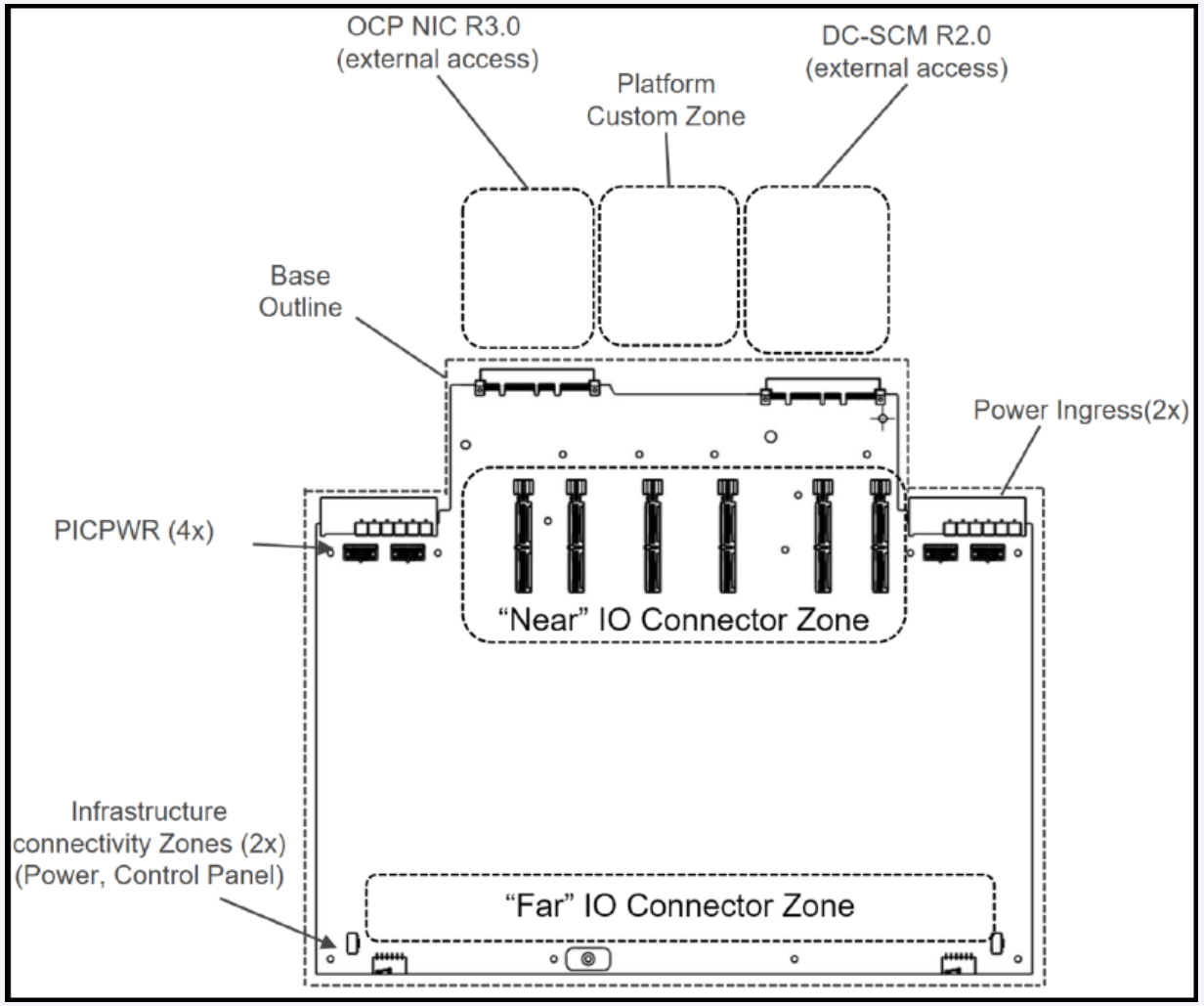


Space Limitation applications
Ex: **Under Heatsink applications**

- Mating height comparison: Nearstack(12.35mm) > MCIO(11.95mm) >Swift DE(9.6mm)>Swift(8.38mm)>Swift LP(7.65mm)



OCP DC-MHS Application



- **Near End side**

  Suggest to use Amphenol's **Multi-Trak™**

- **Far End side**

  Need to meet the requirement of low profile and cable mating solutions(Under 12mm)

  Suggest to use Amphenol's **Swift series**

Table 4. Far Side HSIO Recommended Connectors

Recommended Connector	Note
SFF-TA-1016	Must choose low profile variant
SFF-TA-1026	Appropriate due to low profile and ability to fit under thermal solutions

18	High Speed IO connector choices for the Far Side Shall meeting the Height Restriction requirements	Section 10.13
19	Primary side component height restriction zone shall be implemented	Figure 20, Section 10.14

For thermal solutions, one must consider the allowable variance in numbers, types, and location of Compute Core items. Thus, a fixed 12mm for component height restriction in the Compute Core area is intended to allow air cooling heatsinks or liquid cooling hardware of any variance. DIMM sockets are exempt from the 12mm component height restriction. All other soldered

Product Roadmap --- Swift series

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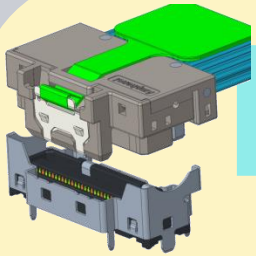
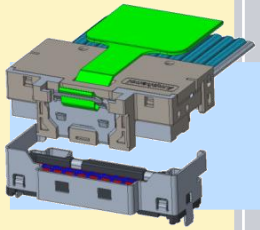
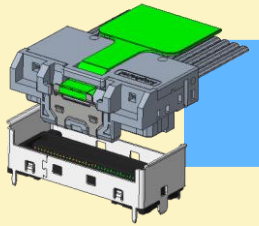
Product Supported RoadMap with PCIe Generations



Swift
Mating Height 8.95mm



Swift LP (Gen 5/Gen 6)
Mating Height 7.65mm



Swift DE
Mating Height 9.65mm

PCIe Gen5
NRZ 32G

PCIe Gen6
PAM4 64G

- Swift is target for **near the chip and under heatsink** solution with mating height mating height 8.95mm.
- Swift LP is under modifying SI for PCIe Gen 6 spec with extra low profile function **(mating height 7.65 mm)**.
- Swift DE is our new concept for supporting **customer flexible cable layout solutions**

ExtremePort™ Swift

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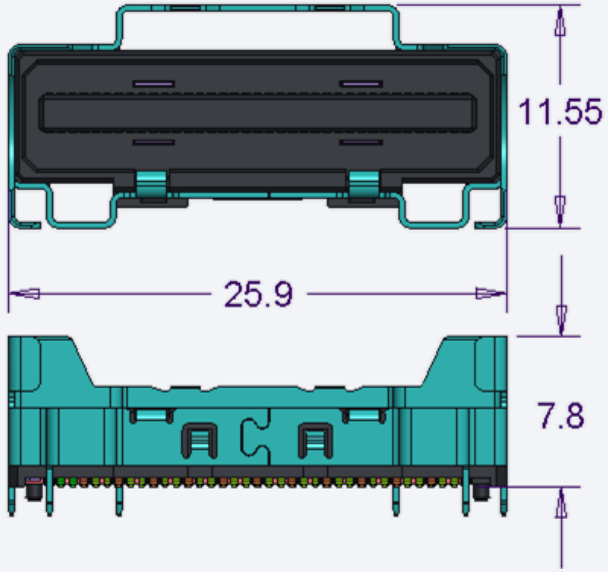
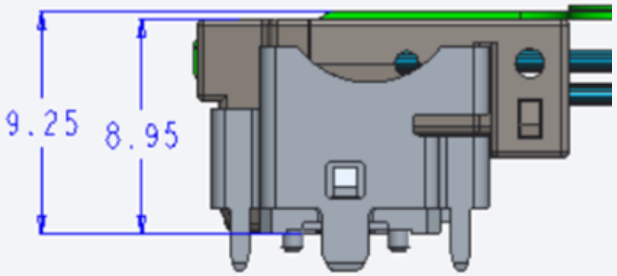
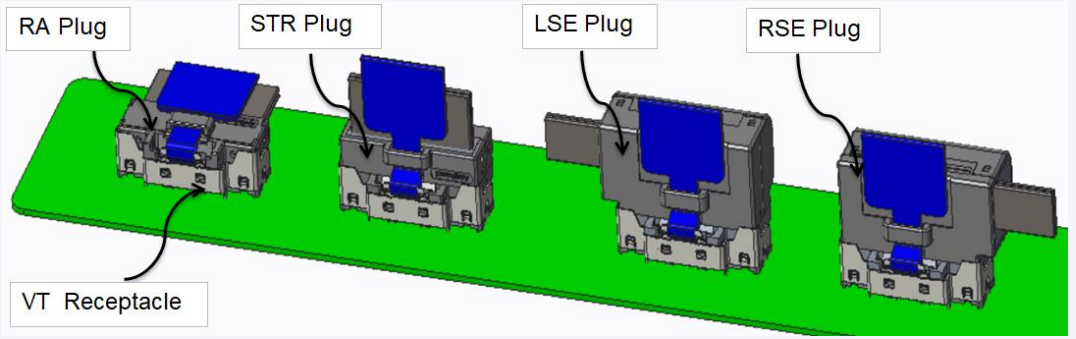
Outline Dimension:



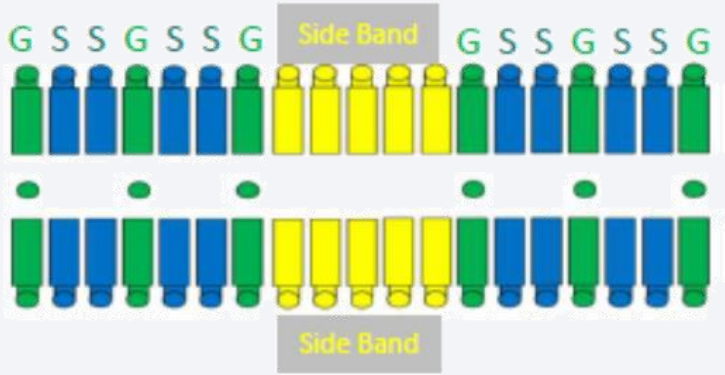
Mating Dimension:



- Swift Connector only have VT parts, but have various Plug side types to support different situations

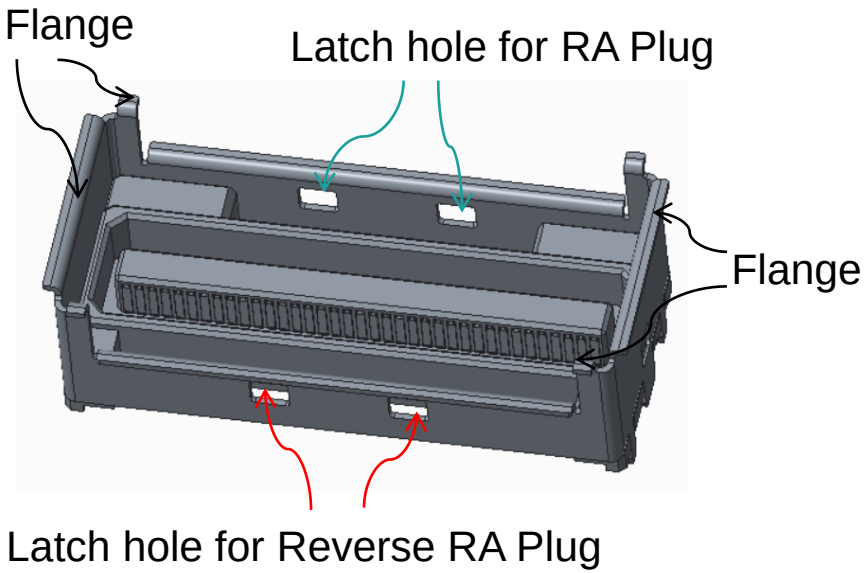


- Swift Ground Pin are connected together, but can be chosen as x4 + sideband or x6 w/o sideband (Take 38pin as example)

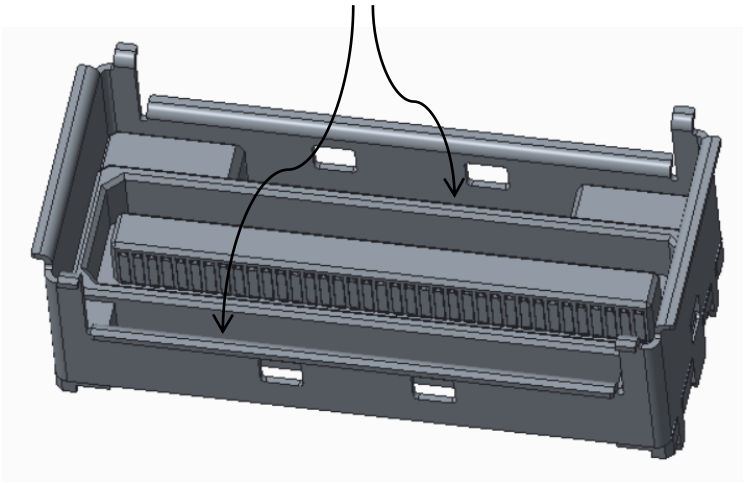


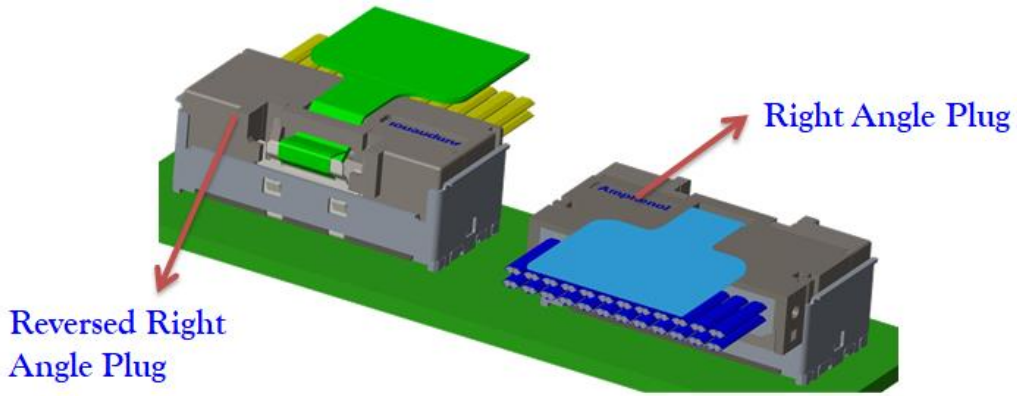
ExtremePort™ Swift DE

Amphenol
COMMUNICATIONS SOLUTIONS



Fool-proof design features for plugs mating





Comment:

1.Receptacle connector and two kinds of plug(RA & Reverse RA) have fool-proof design features, which can avoid two kinds of plug misuse.

2. Receptacle metal shell have flange that it can be used for blind mating application.

ExtremePort™ Swift LP

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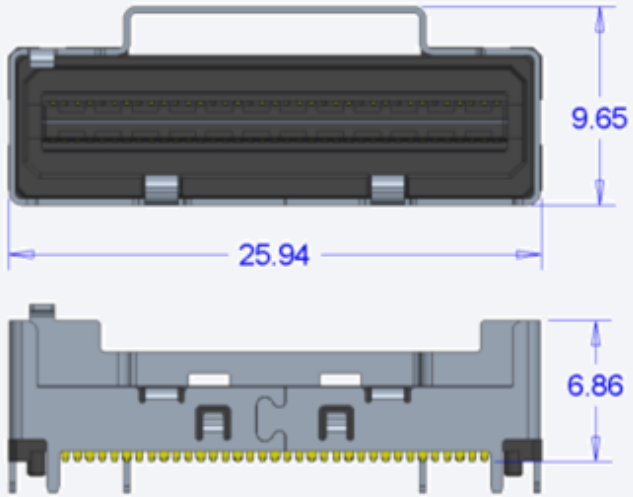
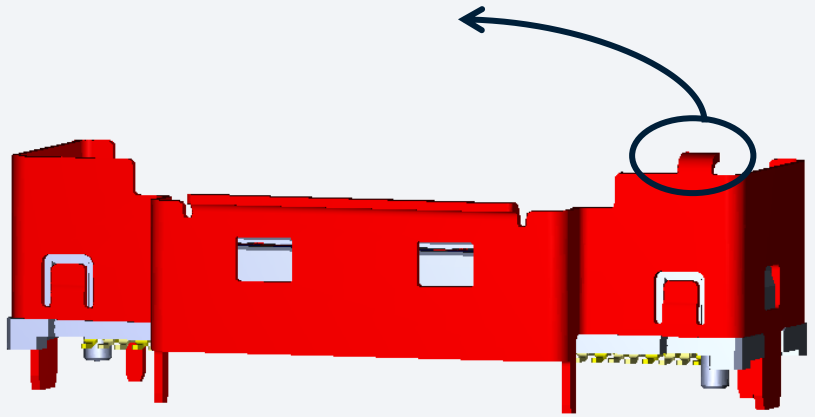
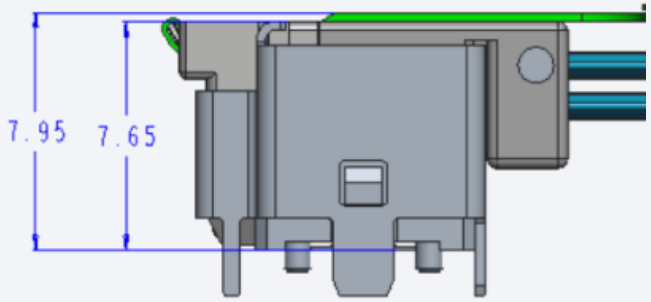
Outline Dimension:



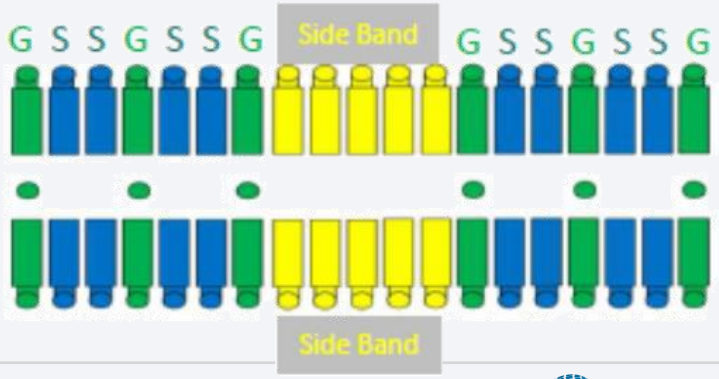
Fool-proof design features for plugs mating



Mating Dimension:



- Swift LP Ground Pin are connected together, but can be chosen as x4 + sideband or x6 w/o sideband (Take 38pin as example)



Product Roadmap

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Product RoadMap		Swift (Under 9mm)			Swift DE (Flexible cable layout)			Swift LP (Under 8mm)		
		Plug		Receptacle	Plug		Receptacle	Plug		Receptacle
Type	Positions	Straight	Right Angle	Vertical	Right Angle	Reverse Right Angle	Vertical	Straight	Right Angle	Vertical
4x+Sideband or 6x w/o Sideband	38	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Design Stage	Target 2022 Q4	Target 2022 Q4
8x+Sideband or 12x w/o Sideband	74	Available	Available	Available	Available	Available	Available	Design Stage	Available	Available
16x+Sideband or 20x w/o Sideband	124	Tool on request	Available	Available	Tool on request	Tool on request	Tool on request	Design Stage	Target 2022 Q4	Target 2022 Q4
20x+Sideband or 24x w/o Sideband	148	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Tool on request	Design Stage	Target 2023 Q1	Target 2023 Q1
Wire Gauge Supported		29~34 AWG (Prefer 30~32 AWG, 34AWG is expensive due to lower yield rate and heavier labor)								
Termination Process		Support Lase Welding, Resistance Welding and Hot Bar								
Wiping Length		0.88mm								

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ExtremePort™ Z-Link

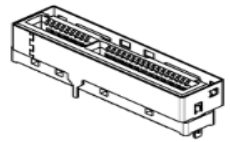
SFF-TA-1002/1020, GenZ

Commercial IO

ExtremePort™ Z-Link

Amphenol COMMUNICATIONS SOLUTIONS

Amphenol CS introduces to the market **SFF-TA-1002** standard interconnect solution – **ExtremPort™ Z-Link**, which is 0.60 mm pitch, dual-use connector capable of transmitting high-speed signal up to **PAM4 56G** over the distance overwhelming the conventional routings.



The ExtremePort™ Z-Link provides not only a SI performance ready signal transmission media but also a new way of system design thinking that will lead your electronic system to a completely ***cost effective***, ***highly modularized & scalable***, and extremely ***easy repairing*** masterpiece.

Features

- Pitch 0.60 mm, both V/T & R/A form factors
- Up to PAM4 56Gbps, over 1 m transmission distance
- Dual-use, supporting both cable and card edge connection with one identical connector
- SFF-TA-1002 standard form factor, with variety of pin no. options – covering most common uses applications in data centers such as PCIe/NVMe/OCP NIC/GenZ/…

Benefits

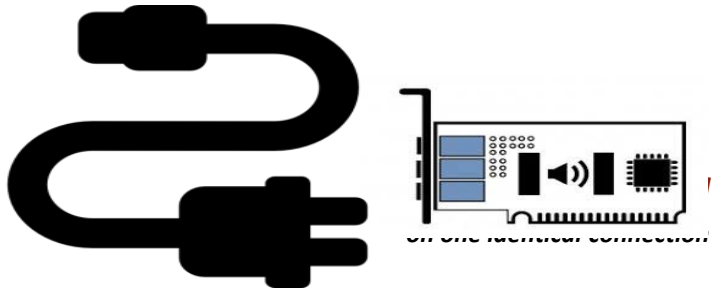
- Providing enhanced flexibility in system design to meet highly modularized, highly scalable, and easy repairing requirement simultaneously
- Real economic choice for not only save system material cost but also show high succession of system electrical design that saves both engineering and certification expenses

32G_{bps}

NRZ

56Gbps

PAM4



Industrial Standard of:

- ✓ **PCI-Express**
- ✓ **OCP NIC 3.0**
- ✓ **EDSFF**
- ✓ **GenZ**

Product Details – ExtremePort™ Z-Link
PCIe Gen 5, EDSFF & OCP NIC 3.0(Also standard for GenZ)

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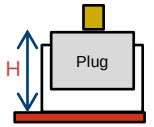
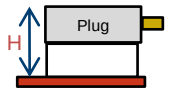
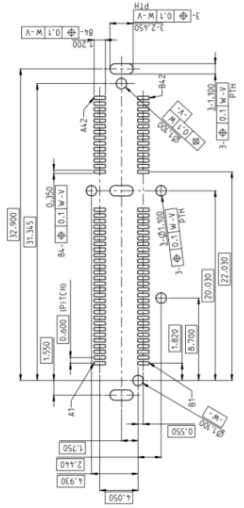
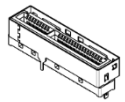
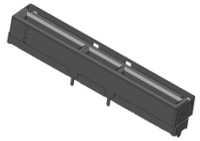
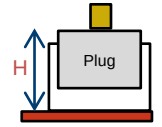
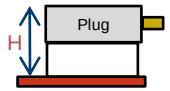
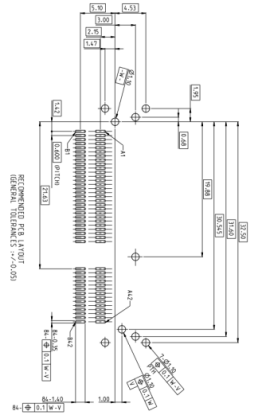
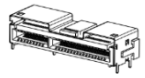
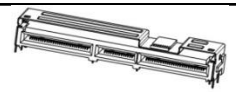
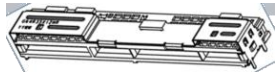
Spec	Form Factor	Pin	Recommended Channel: SFF-TA-1002 Standard	Pic	Width (mm)	Mating Height (mm)	Reference Footprint
• PAM4 56G, 85 Ω • Supports both cable & board connections • Pitch 0.60 mm • Voltage Rating: 30V_{DC} • Operating Temperature: -25℃ ~ 85℃ • Storage Temperature: -40℃ ~ 85℃ • Ambient Humidity: 80% R.H. Maximum	V/T	56 (1C)	9x		22.98	**Standard Version:** *2Straight Exit: 23.00 mm  *3Right Angle Exit: 22.80 mm 	
		84 (2C)	13x		34.70		
		140 (4C)	22x		57.20		
		168 (4C+)	24X		69.29		
	R/A	56 (1C)	9x		22.98	**Low Profile Version:** *2Straight Exit: 17.62 mm  *3Right Angle Exit: 15.87 mm 	
		84 (2C)	13x		34.70		
		140 (4C)	22x		57.20		
		168 (4C+)	24X		69.29		

Product Feature

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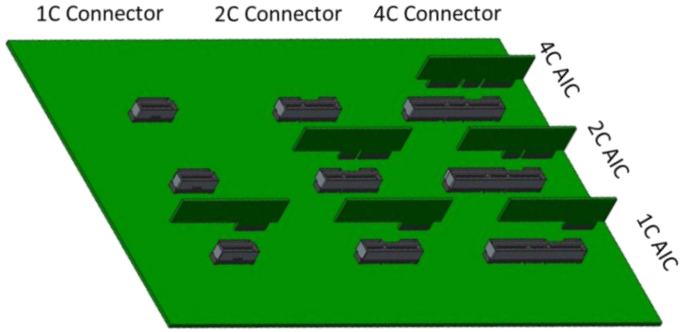
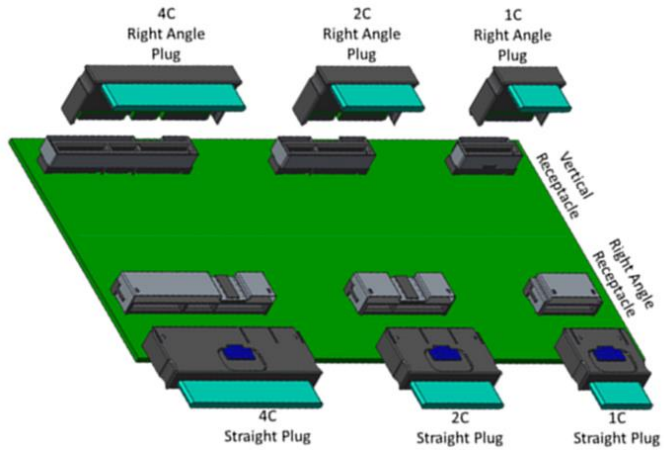
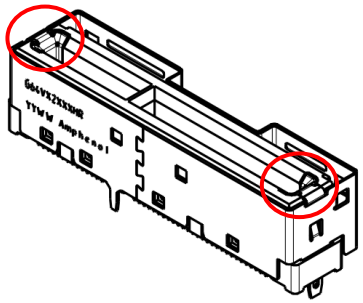
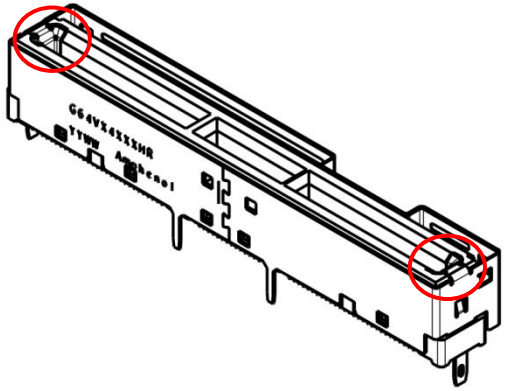
Supporting both cable and card connection with on identical connector.





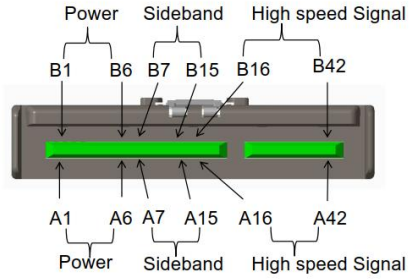


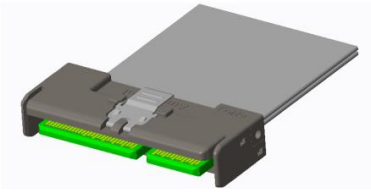


Metal protection at mating interface – protecting damage to plastic housing while card or plug inserted.

Benefit: Power+signal

Pin Assignment has combine Power and Signal





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Stack USB

OCP DC-SCM

Commercial IO

USB3.2, GEN2, A, Stack Sink, Right Angle, DIP

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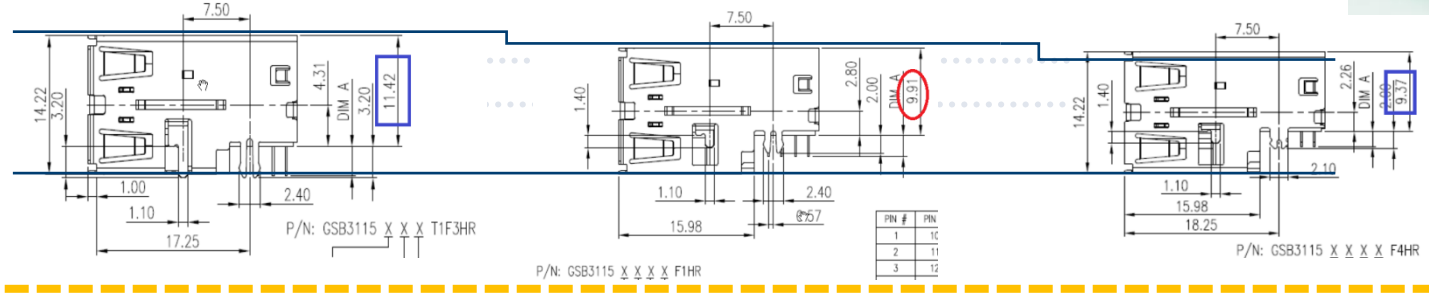
OCP Standardization

Server Standard

Since 2009, USB3.2,GEN1, A Type Standard Stack Sink has been selling more than 25KK in Server market.
Amphenol has three kind of different height to fulfill Server market needs.

- ✓ **Application: Server**
- ✓ **Customer: HP, Dell, Lenovo, SuperMicro, Cisco, Inspur, Sugon**
- ✓ **Capacity: 500K / monthly**

GSB3115XXXT1F3HR ***GSB3115XXXXF1HR*** ***GSB3115XXXXF4HR***



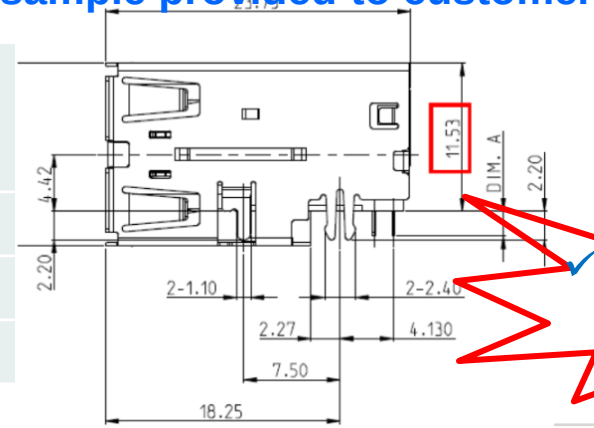
OCP Server Standard

In 2022, three key customers including Lenovo, Hp, Dell approach USB, Gen2, A, Stack Sink Right Angle Dip, Center Height @ " 11.53mm" as an Open Compute Project of Server standard.

Product Status: Approval sheet, SI report Done, sample provided to customers for validation.

OPEN Compute Project®

End Customer	Project Name	PN	EAU (Kpcs)	Usage	MP schedule
Lenovo	Ocracoke	GSB41153421A1 HR	300	1	2023 Q2
HP	Gen12_OCP rack server	GSB41153421A1 HR	250	1	2023 Q2
Dell	17G	GSB41153412A1 HR	200	1	2024 Q1



New Product Release

Commercial IO

Thank you!

For more information, please visit https://www.amphenol-cs.com

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