

Low Input / Output 1.5 A LDO Regulator

No.EA-585-210825

OVERVIEW

The RP120Z001D is a very low dropout LDO which operates from input voltage as low as 0.768 V (@ $V_{SET} = 0.6$ V, $V_{BIAS} = 3.3$ V, $I_{OUT} = 1.5$ A). The LDO uses an internal low on-resistance (67 m Ω @ $V_{SET} = 0.6$ V, $V_{BIAS} = 3.3$ V, $I_{OUT} = 1$ A) NMOS transistor as the driver. The VBIAS pin provides the higher supply necessary for the LDO circuitry while the output current comes directly from the VIN input for high efficiency regulation.

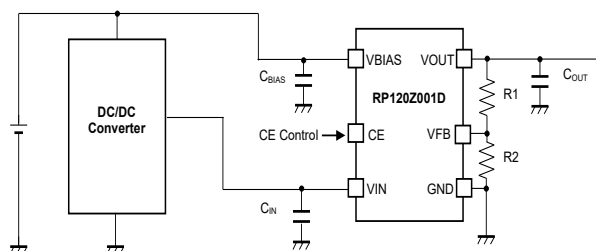
KEY BENEFITS

- High PSRR, high output current, and fast response characteristics.
- Suitable for sensitive sensors, high-quality audio, and RF devices.
- Very small WLCSP package (1.2 mm x 0.8 mm x 0.29 mm).

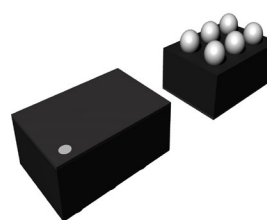
KEY SPECIFICATIONS

- Input Voltage Range :
 $V_{IN} = V_{SET} + V_{DIFF}$ to V_{BIAS}
 (Ex. Min. 0.768 V @ $V_{SET} = 0.6$ V, $V_{BIAS} = 3.3$ V, $I_{OUT} = 1.5$ A)
 $V_{BIAS} = 2.4$ V to 5.5 V
- External setting range of output voltage:
 0.6 V to 3.6 V
- Output Current: $I_{OUTMAX} = 1.5$ A
- Supply Current: Typ. 35 μ A
- Output Noise: Typ. 50 μ Vrms ($V_{SET} = 0.6$ V)
- Power Supply Ripple Rejection:
 Typ. 90 dB ($f = 1$ kHz, Ripple in V_{IN})
 Typ. 60 dB ($f = 100$ kHz, Ripple in V_{IN})
- Dropout Voltage: Typ. 67 mV
 ($I_{OUT} = 1$ A, $V_{SET} = 0.6$ V, $V_{BIAS} = 3.3$ V)
- Inrush Current Limit: Typ. 600 mA
- Short Circuit Current Protection: Typ. 600 mA
- Thermal Shutdown: Typ. 165 $^{\circ}$ C
- Ceramic Capacitor: C_{OUT} 4.7 μ F

TYPICAL APPLICATION



PACKAGE (unit: mm)



WLCSP-6-P11
1.2 x 0.8 x 0.29

APPLICATIONS

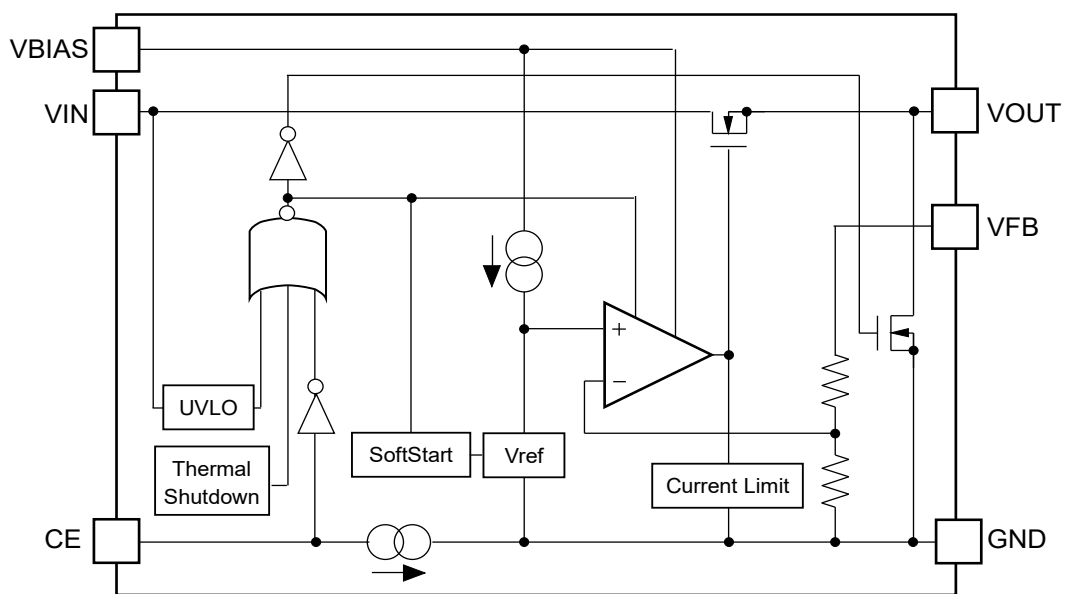
- Portable communication devices, battery-powered devices, camera, video, audio.
- Communication devices such as RF modules, clock generation devices such as VCOs and PLLs.
- Constant voltage source for analog circuits of FPGA and SoC.

SELECTION GUIDE

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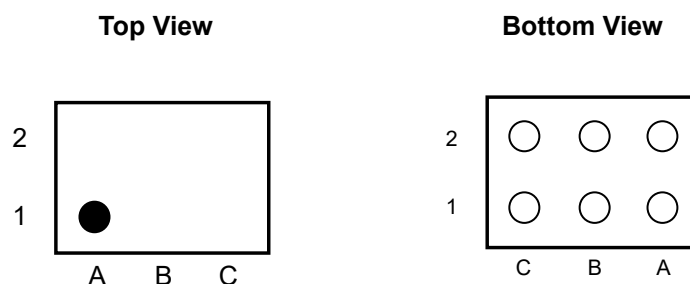
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP120Z001D-E2-F	WLCSP-6-P11	5,000 pcs	YES	YES

BLOCK DIAGRAM



RP120Z001D Block Diagram

PIN DESCRIPTIONS



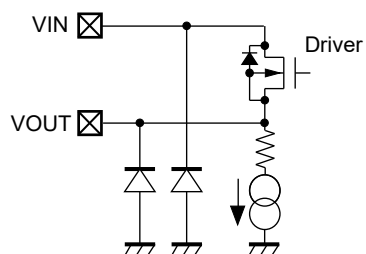
WLCSP-6-P11 Pin Configuration

RP120Z(WLCSP-6-P11) Pin Description

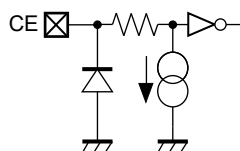
Symbol	Pin No.	I/O	Description
VOUT	A1	O	Output voltage pin. The VOUT pin supplies power to the load. A minimum output capacitance shown in “Phase Compensation” section is required to ensure stability. See the “Phase Compensation” section for more information on output capacitance.
VFB	B1	I	Output Feedback Pin This is the input to the error amplifier. The output voltage typically set be connecting VFB pin to a resistor divider from VOUT pin to GND.
GND	C1	-	Ground pin of the internal circuit.
VIN	A2	I	Power supply pin of the NMOS driver. Input Supply Voltage. Output load current is supplied directly from VIN. The VIN pin should be locally bypassed to GND.
CE	B2	I	Chip Enable Pin. Logic "High" input : LDO is active, Logic “Low” input: the LDO into shutdown. This pin is pulled down internally.
VBIAS	C2	I	Analog Power Supply Pin Must be connected to an external supply voltage. The VBIAS pin should be locally bypassed to GND.

Please refer to “TYPICAL APPLICATION CIRCUITN” or “OPERATION” for details.

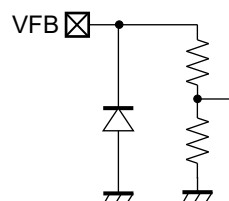
Internal Equivalent Circuit Diagram of Pin



Internal equivalent circuit diagram of VIN and VOUT pin



Internal equivalent circuit diagram of CE pin



Internal equivalent circuit diagram of VFB pin

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Unit
V_{BIAS}	Analog Power Supply Voltage	−0.3 to 6.5	V
V_{IN}	NMOS driver power input voltage	−0.3 to $V_{BIAS} + 0.3 \leq 6.5$	V
V_{CE}	Input Voltage (CE pin)	−0.3 to 6.5	V
V_{OUT}	Output Voltage	−0.3 to $V_{IN} + 0.3 \leq 6.5$	V
V_{FB}	VFB pin Voltage	−0.3 to $V_{OUT} + 0.3 \leq 6.5$	V
P_D	Power Dissipation	Refer to Appendix “POWER DISSIPATION”	
T_j	Junction Temperature Range	−40 to 125	°C
T_{stg}	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

ELECTROSTATIC DISCHARGE(ESD) RATINGS

Symbol	Conditions	Ratings	Unit
V_{HBM}	HBM C=100pF、R=1.5k Ω	± 2000	V
V_{CDM}	CDM	± 1000	

Electrostatic Discharge Ratings

The electrostatic discharge test is done based on JESD47.
In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

RECOMMENDED OPERATING CONDITIONS

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Symbol	Item	Ratings	Unit
V_{BIAS}	Input Voltage	2.4 to 5.5 ($V_{SET} < 0.9$)	V
V_{IN}		$V_{SET} + 1.5V$ to 5.5 ($V_{SET} \geq 0.9$)	V
T_a	Operating Temperature Range	$V_{SET} + V_{DIF}$ to V_{BIAS} (Max. 5.5)	°C
		-40 to 85	

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

$V_{BIAS} = V_{CE} = 3.6V$, $V_{IN} = 1.1V$, $I_{OUT} = 1mA$, $C_{BIAS} = C_{IN} = 1.0\mu F$, $C_{OUT} = 4.7\mu F$

unless otherwise specified.

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 85^{\circ}C$.

RP120Z001D

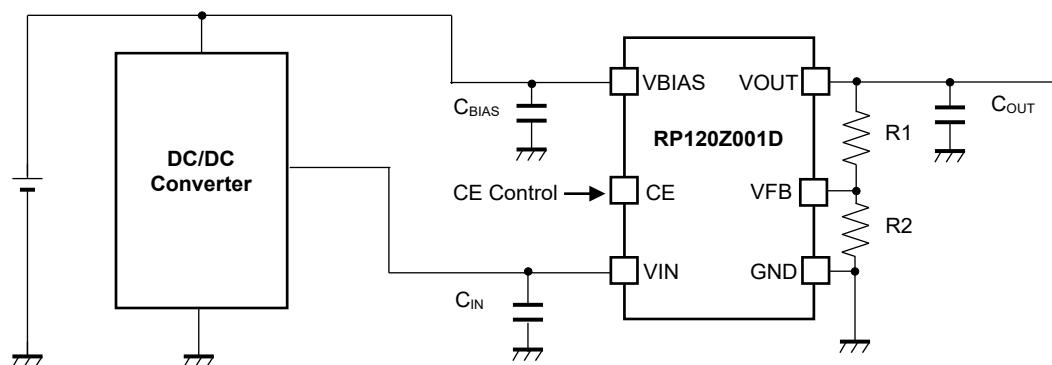
($T_a = 25^{\circ}C$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{FB}	Feedback pin Output Voltage	$T_a = 25^{\circ}C$	0.591	0.6	0.609	V
		$-40^{\circ}C \leq T_a \leq 85^{\circ}C$	0.582	0.6	0.618	
I_{BIAS}	VBIAS Pin Supply Current	$I_{OUT} = 0mA$		35	50	μA
I_{IN}	VIN Pin Supply Current	$I_{OUT} = 0mA$		1.5	2.8	μA
I_{STBB}	VBIAS pin Standby Current	$V_{BIAS} = 5.5V$, $V_{CE} = 0V$		0	0.2	μA
I_{STBI}	VIN pin Standby Current	$V_{BIAS} = 5.5V$, $V_{CE} = 0V$		0	0.2	μA
I_{CEH}	CE Pin Input Current "H"	$V_{BIAS} = V_{CE} = 5.5V$		0.25	0.6	μA
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	$1mA \leq I_{OUT} \leq 1.5A$	-1.7	0.1	1.7	%
$\Delta V_{OUT} / \Delta V_{IN}$	VIN Line Regulation	$V_{SET} + 0.1V \leq V_{IN} \leq 3.6V$	-0.25		0.25	%/V
$\Delta V_{OUT} / \Delta V_{BIAS}$	VBIAS Line Regulation	$V_{SET} + 1.5V \leq V_{BIAS} \leq 5.5V$	-0.25		0.25	%/V
R_{DISTR}	Auto-discharge NMOS On-resistance	$V_{CE} = 0V$		50		Ω
V_{CEH}	CE Pin Input Voltage "H"		0.9		5.5	V
V_{CEL}	CE Pin Input Voltage "L"		0		0.4	V
V_{DIF}	Dropout Voltage	$V_{SET} = 0.6V$, $V_{BIAS} = 3.3V$, $I_{OUT} = 1.0A$		0.067	0.115	V
		$I_{OUT} = 1.5A$		0.102	0.168	
t_{SS}	Soft Start Time ⁽¹⁾		100	185	320	μs
I_{SC}	Short-circuit Current	$V_{OUT} = 0V$		0.6		A
$I_{LIMRISE}$	Limit Current at Start-up	$V_{OUT} = 0V$		0.6		A
V_{UVLOF}	UVLO Detection Voltage	$V_{BIAS} = V_{CE} = 3.6V$, V_{IN} Falling	0.26	0.3	0.34	V
V_{UVLOR}	UVLO Release Voltage	$V_{BIAS} = V_{CE} = 3.6V$, V_{IN} Rising	0.36	0.4	0.44	V

All test items listed under Electrical Characteristics are done with short-circuiting VOUT pin and VFB pin, and under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$).

⁽¹⁾ It is specified based on the measurement result of the time when the VOUT pin voltage rises from 10% to 90%, and converted it to 100% time by calculation.

TYPICAL APPLICATION CIRCUIT



RP120Z001D (Adjustable Output Type) Typical Application Circuit

The output voltage is set by the ratio of two external resistors as shown above.

Output Voltage Setting Range : 0.6V to 3.6V
 $V_{FB} = 0.6V$ (Typ.)

The set output voltage (V_{SET}) is as follows.

$$V_{SET} = V_{FB} \times ((R1 + R2) / R2)$$

More precisely, the current in R1 is the current in R2 plus the internal current through the resistance (R_{IC}) between VFB pin and GND. The value of the R_{IC} is Typ.2.7M Ω , therefore, $V_{FB} \times R1/R_{IC}$ makes an error.

If $R1 \ll R_{IC}$, the error can be reduced.

Use a resistance value, R2 of 20k Ω or less for $V_{SET} < 1.3V$ and 10k Ω or less for $V_{SET} \geq 1.3V$.

External Components

V_{IN} , V_{BIAS} pins should be locally bypassed to GND to make their impedance low. If their impedance is high, making unexpected noise or unstable operation may result. A capacitor (C_{BIAS}) between VBIAS pin and GND and another capacitor (C_{IN}) between VIN pin and GND should be 1 μF or more each.

It is desirable to choose X7R and X5R ceramic capacitors (voltage rating should be more than twice as much as input), which have good temperature characteristics of ESR, ESL, and capacitance.

Phase Compensation

The RP120Z is designed to be stable with an output capacitor for phase compensation with whole range of the output load current. An output capacitor of minimum 4.7 μF ($V_{SET} \leq 2.0V$), or minimum 10 μF ($V_{SET} > 2.0V$) or greater value of C_{OUT} is recommended to ensure stability. Note that bypass capacitors used to decouple individual components powered by the more stable characteristics and are more suitable for use as the output capacitor.

The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Set Output Voltage (V_{SET})	Effective Capacity
$0.6V \leq V_{SET} < 1.2V$	Min. 2.7 μF
$1.2V \leq V_{SET} \leq 2.0V$	Min. 2.4 μF
$2.0V < V_{SET} \leq 3.6V$	Min. 6.0 μF

OPERATION

Chip Enable Function

Input "High" to CE pin, the RP120Z is active. Input "Low" to CE pin, the RP120Z is into shutdown.

Regardless of the state of V_{IN} and V_{BIAS} voltage, a voltage can be forced to CE pin.

The CE pin is pulled down inside the IC with a constant current of Typ.0.25 μ A, therefore, when the CE pin is left floating, the RP120Z goes into shutdown state. CE pin must be tied to a valid logic level (such as V_{BIAS}) if not used.

UVLO (Undervoltage Lock Out) Function

An undervoltage lockout comparator (UVLO) is activated while CE pin is "High".

The UVLO comparator senses V_{IN} pin voltage to ensure that the V_{IN} supply for the LDO is greater than UVLO released voltage ($V_{UVLO,R}$, Typ. 0.4V) before enabling the LDO. If V_{IN} is below the UVLO threshold ($V_{UVLO,F}$, Typ. 0.3V), the UVLO shuts down the LDO, and V_{OUT} is pulled to GND through the external divider and internal auto discharge transistor for Off state. After UVLO is released, the LDO starts up with soft-start.

Thermal Shutdown Function

The RP120Z has internal thermal limiting designed to protect the device during momentary overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. At higher temperatures, or in cases where internal power dissipation cause excessive self heating on-chip, the thermal shutdown circuitry will shut down LDO when the junction temperature exceeds Typ. 165°C, the RP120Z will reenale once the junction temperature drops back to thermal shutdown released threshold (Typ. 125°C), the IC will restart with the soft start operation.

Auto Discharge

When turning off, the V_{OUT} voltage quickly pulled down to near 0V by discharging electric charge stored in output capacitor through the MOSFET connected between the VOUT pin and GND.

The auto discharge function is enabled when CE pin = "Low", thermal shutdown detection, or UVLO detection. This function is effective when V_{BIAS} is the minimum operating voltage or higher. The on-resistance of the MOSFET is Typ.50 Ω .

Soft Start / Inrush Current Limit

The RP120Z includes a soft-start feature to prevent excessive inrush current flow at V_{IN} during start-up. When the LDO is enabled, the soft-start circuitry gradually increases the internal reference voltage of LDO over a period of approximately 185 μ s.

In addition, the RP120Z limits the inrush current up to Typ. 600mA during startup.

The inrush current depends on the capacitance value of C_{OUT} . Connecting a large load and the inrush current value may exceed the threshold of Typ. 600mA during startup, the slew rate is further limited and extended start-up time. If an effective capacitance value of the C_{OUT} is larger than about 110 μ F / V_{SET} is used, the output voltage ramp up time is determined by the inrush current limit value and C_{OUT} value.

The output turning on time (t_{ON}) can be calculated from the following equation:

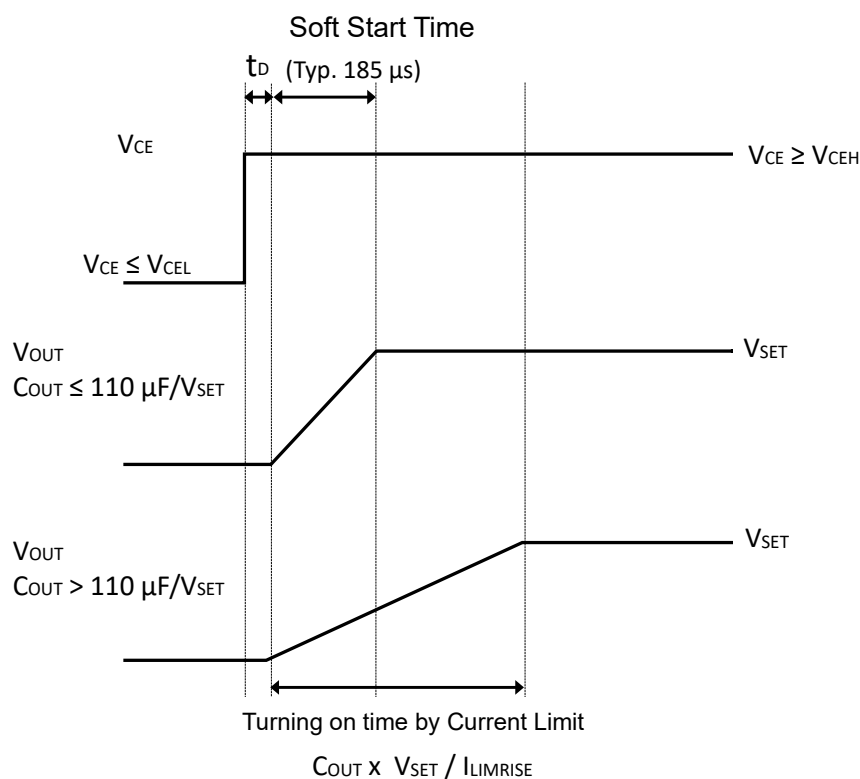
$$t_{ON} = t_D + C_{OUT} \times V_{SET} / I_{LIMRISE}$$

t_D : Delay Time at Start-up 60 μ s

V_{SET} : Set Output Voltage

$I_{LIMRISE}$: Current Limit at Start-up Typ. 600mA

If the load current (I_{LOAD}) exists other than the charge current to C_{OUT} during start-up, the start-up time is extended. The load current over $I_{LIMRISE}$ may interfere charging of C_{OUT} and the output does not rise up.



TECHNICAL NOTES

Constraints of the voltage value and the sequence of V_{BIAS} and V_{IN}

V_{IN} voltage must be applied below V_{BIAS} voltage since a forward current flows through the parasitic diode in the IC. $V_{BIAS} \geq V_{IN}$ should be true even when they turn on and off. At startup, supply V_{IN} and V_{BIAS} at the same time, or supply V_{IN} after V_{BIAS} . When turning off the supply voltage of V_{IN} and V_{BIAS} , turn them off at the same time, or turn off V_{IN} before V_{BIAS} .

Thermal Shutdown

The thermal shutdown function prevents the IC from fuming and firing but does not ensure the IC's reliability or keep the IC below the absolute maximum ratings. The thermal shutdown function does not operate against the heat generated by abnormal IC operation such as latch-up and overvoltage.

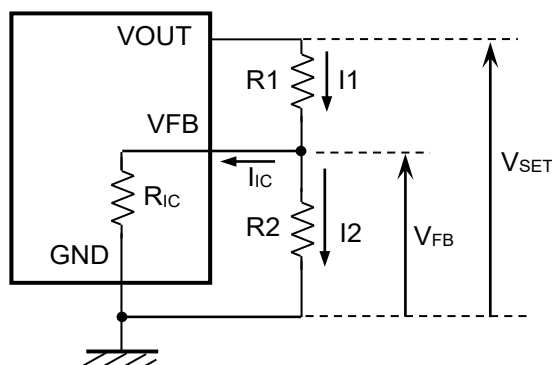
The thermal shutdown function operates in a state over the absolute maximum ratings, and should not be used for a system design.

APPLICATION INFORMATION

Adjustable Output Voltage

The output voltage is set by the ratio of two external resistors (R1, R2).

The device serves the output to maintain the VFB pin voltage at 0.6V(referenced to ground). The output voltage (V_{SET}) can be calculated using the formula below.



$$I1 = I_{IC} + I2 \dots\dots\dots (1)$$

$$I2 = V_{FB} / R2 \dots\dots\dots (2)$$

(1)、(2)

$$I1 = I_{IC} + V_{FB} / R2 \dots\dots\dots (3)$$

$$V_{SET} = V_{FB} + R1 \times I1 \dots\dots\dots (4)$$

I1 can be substituted by formula (3)

$$\begin{aligned} V_{SET} &= V_{FB} + R1 \times (I_{IC} + V_{FB} / R2) \\ &= V_{FB} \times (1 + R1 / R2) + R1 \times I_{IC} \dots\dots\dots (5) \end{aligned}$$

R1 × I_{IC} in the above formula (5) is the error.

$$I_{IC} = V_{FB} / R_{IC} \dots\dots\dots (6)$$

Thus,

$$\begin{aligned} R1 \times I_{IC} &= R1 \times V_{FB} / R_{IC} \\ &= V_{FB} \times R1 / R_{IC} \dots\dots\dots (7) \end{aligned}$$

If R1 << R_{IC}, the error can be minimized.

If the error is ignored, the output voltage is calculated by the next formula.

$$V_{SET} = V_{FB} \times ((R1 + R2) / R2) \dots\dots\dots (8)$$

R_{IC} of RP120Z is Typ.2.7MΩ (Ta=25°C, guaranteed by design value).

The accuracy of the output voltage is determined by the V_{FB} accuracy and resistance accuracy.

The current calculated by V_{SET} / (R1 + R2) flows between the VOUT pin and GND.

V_{FB} of RP120Z001D is typically 0.6V.

Recommended output voltage setting range: $0.6V \leq V_{SET} \leq 3.6V$

V_{FB} accuracy: $0.6V \pm 18mV$ (guaranteed by design in all temperature range).

Use a resistance value, R2 of 20k Ω or less for $V_{SET} < 1.3V$ and 10k Ω or less for $V_{SET} \geq 1.3V$.

Reference Resistance Value Table

Set Output Voltage [V]	R1 [k Ω]	R2 [k Ω]
0.6	Short	Open
0.7	3.3	20
0.8	6.6	20
0.9	9.9	20
1.05	14.9	20
1.1	16.5	20
1.2	19.9	20
1.3	11.6	10
1.5	14.9	10
1.8	19.9	10
2.5	31.6	10
2.8	36.5	10
3.0	39.9	10
3.3	44.8	10
3.6	49.8	10

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51

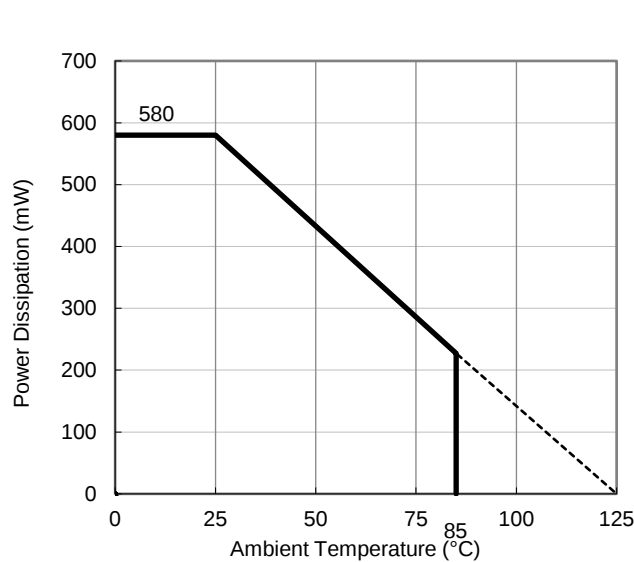
Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm x 114.3 mm x 1.6 mm
Copper Ratio	Outer Layer (First Layer): Less than 10% Inner Layers (Second and Third Layers): 74.2 x 74.2mm 100% Outer Layer (Fourth Layer): Less than 10%

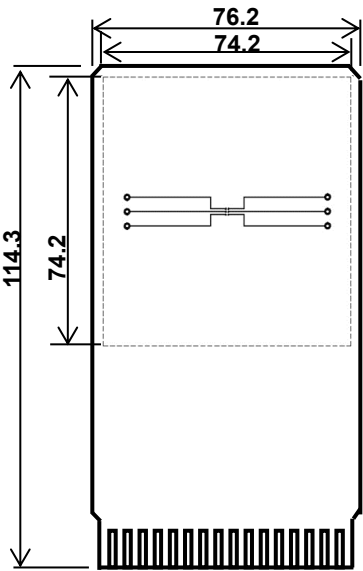
Measurement Result (Ta = 25°C, Tjmax = 125°C)

Item	Measurement Result
Power Dissipation	580 mW
Thermal Resistance (θja)	θja = 170°C/W

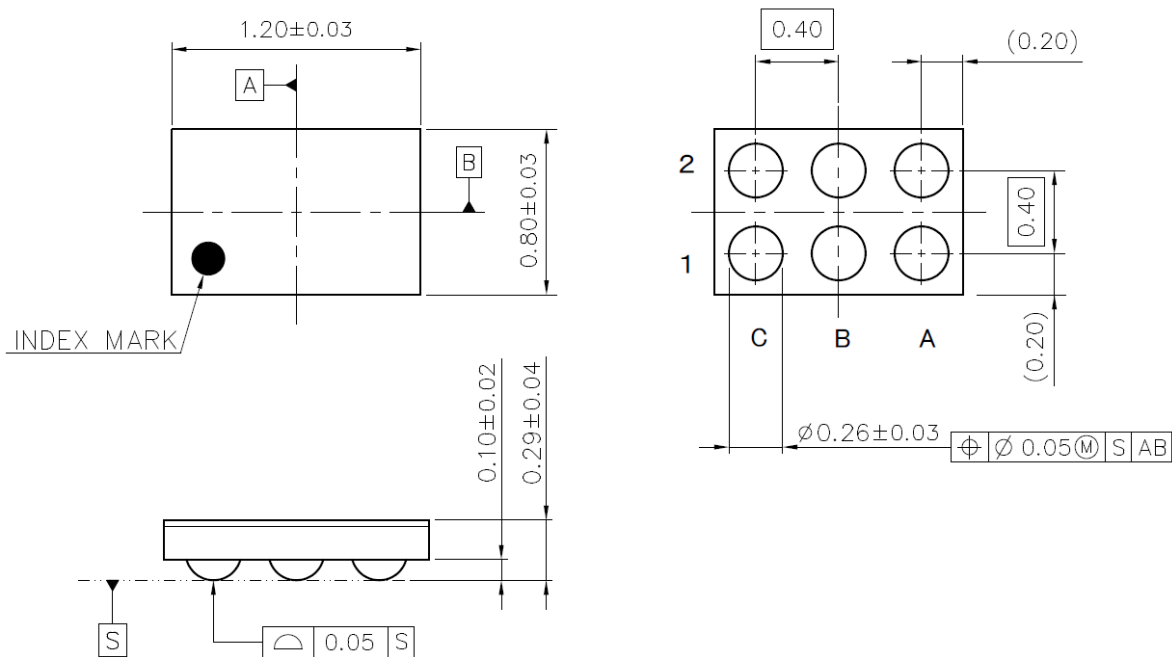
θja: Junction-to-Ambient Thermal Resistance



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



UNIT: mm

WLCSP-6-P11 Package Dimensions

No.	Inspection Items	Inspection Criteria	Figure
1	Package chipping	$A \geq 0.2\text{mm}$ is rejected $B \geq 0.2\text{mm}$ is rejected $C \geq 0.2\text{mm}$ is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	$A \geq 0.2\text{mm}$ is rejected $B \geq 0.2\text{mm}$ is rejected $C \geq 0.2\text{mm}$ is rejected But, even if $A \geq 0.2\text{mm}$, $B \leq 0.1\text{mm}$ is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	



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