AND9623/D

Paralleling eFuses

ON Semiconductor®

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APPLICATION NOTE

Brief introduction

The standard 12 V, 5 V and 3.3 V electronic fuses from ON Semiconductor provide overcurrent and overvoltage protection and come in different current limit configurations. As an example, the 5 V NIS5452 eFuse has a recommended operational 5 A current limit. Sometimes the operating current for the user system might be much higher than the maximum allowed current limit provided by the eFuse. This application note is intended to show the proper use of a parallel eFuse configuration to achieve a higher current limit.

Schematics consideration

The typical parallel eFuse connection is shown below in Figure 1. The example shows parallel connection of 5 V and 5 A NIS5452 eFuses, however; similar methods apply to almost all of the eFuses from the 5 V, 3.3 V or 12 V family.

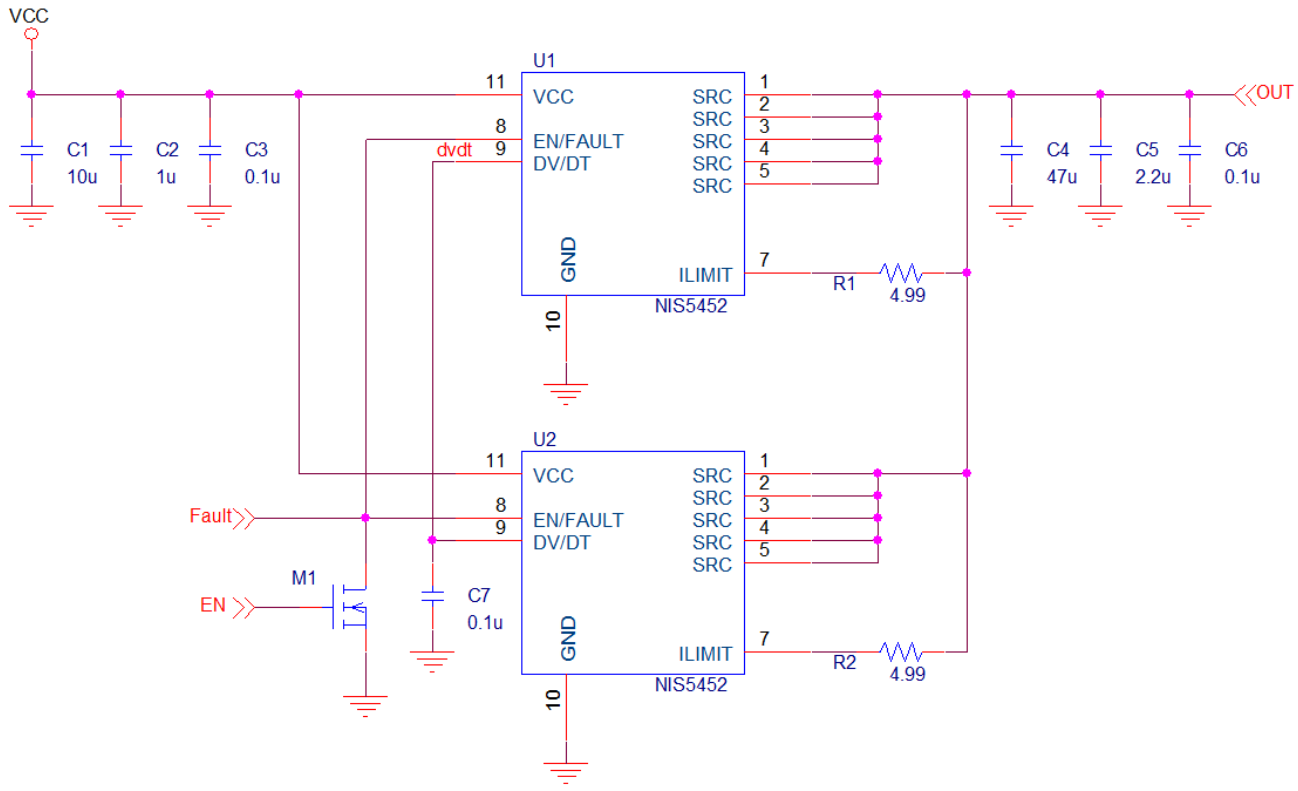

Figure 1. Parallel Connection Schematic of NIS5452 5 V, 5 A eFuse

The input pins and output pins of each eFuse are connected in common. The output capacitors can be shared by both eFuses, but it is recommended to use twice the higher value of capacitance than in a single eFuse case as recommended per datasheet if two eFuses are used in parallel and add more capacitance if more eFuses are added. The type of capacitor to be used should be the same as recommended in the individual datasheet of every eFuse as well.

The limiting resistors R1 and R2 for each eFuse cannot be shared, but both must be identical with 1% or better tolerance and same temperature coefficient. The Enable pin connection for each eFuse can be shared and connected to a common transistor switch. The dv/dt pin for each eFuse can also be left floating, shorted together, individually connected to the slew rate capacitor or connected to a single common slew rate capacitor.

If the dvdt pins are left floating the setup is configured for the fastest start−up, which in the case of the NIS5452 is around 1.4 ms. If the dv/dt lines are not connected together, it is possible to turn on only one of the eFuses at any point in time if the application requires so. If the dv/dt lines are shared, both eFuses must be enabled or disabled at the same time with a switch connected to common Enable line.

Layout and thermal consideration

Since the goal is to parallel the eFuses for higher current throughput, a special care should be taken when it comes to effective layout. One of the main aspects of layout is equal current sharing and thermal considerations. The equal current sharing is achieved by having a symmetric layout on the input “VCC” and output “OUT” nets, there should be no trace or plane dimension imbalance on those connections. The placement of the eFuses should not be very close to each other, so a distance of about 400 mils or more is recommended. The thermal pads of the package connected to “VCC” net should have dense via arrays on both the top and bottom sides of the pad. The vias of 13 mil drill diameter in an array of 4x5 are recommended on each side of the thermal pad. The resistors R1 and R2 should be placed near each eFuse symmetrically, so that they experience the same thermal gradient. The example layout is shown in Figure 2. Both eFuses are placed facing each other with the set of “SRC” output pins, this makes it possible to connect all output pins with a common big top plane metal connected with multiple vias to the inner layer for even more effective heatsinking. The VCC plane can extend further into the PCB but its connection to the eFuses should be made symmetrical as shown. Capacitors should be placed as close to the eFuses and planes connection as possible. The traces running from capacitor pads to the vias should be wide enough too; do not use thin traces for decoupling and filtering capacitors.

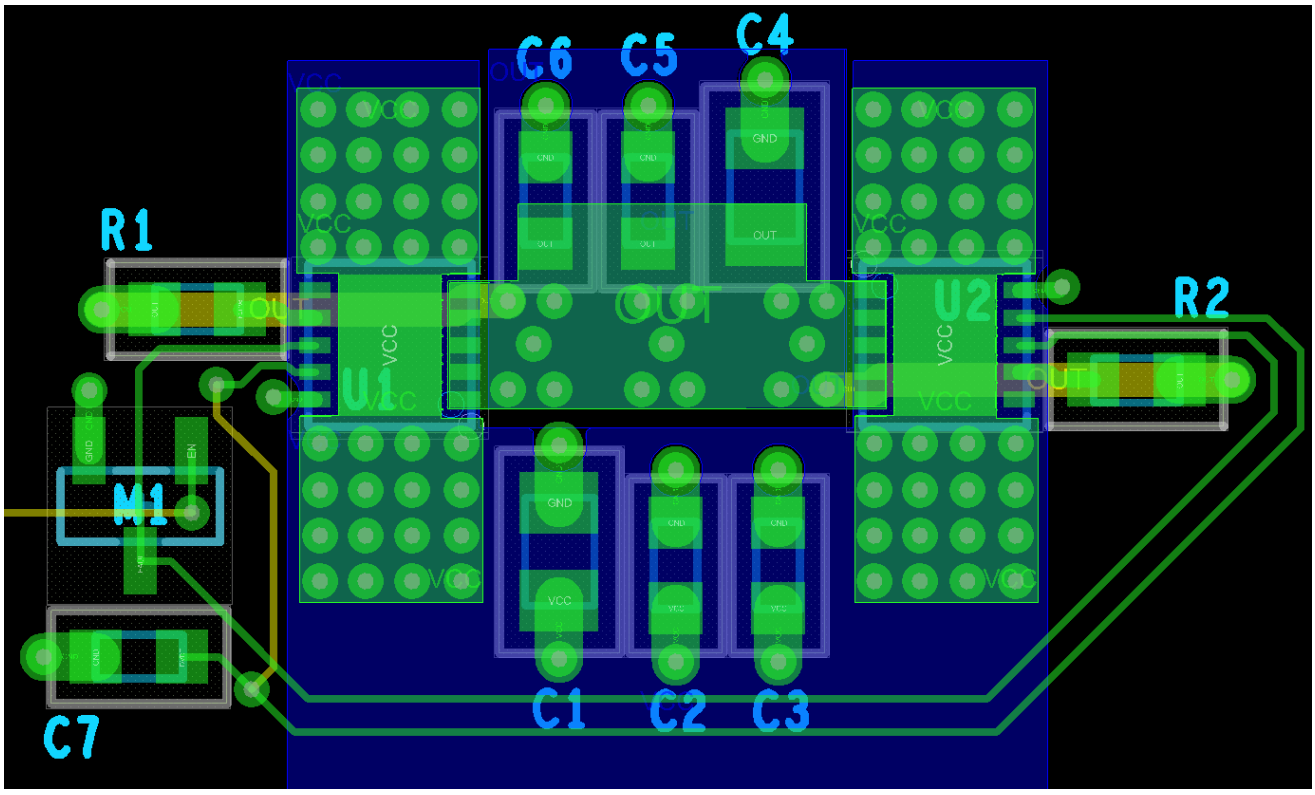

Figure 2. Example layout of 2 NIS5452 eFuses connected in parallel

As an example, below is a thermal picture snapshot of another PCB which had 4 NIS5452 devices on it connected in parallel and running a 5 A load current each. Total current load connected to the common output of all 4 eFuses was 20 A.

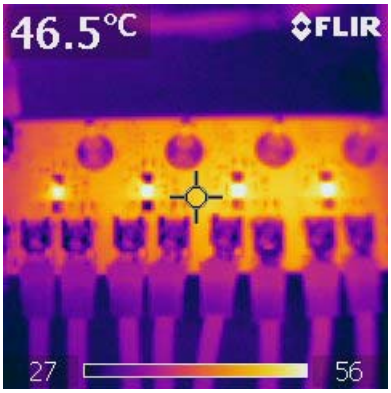

Figure 3. Thermal image of PCB running 4 eFuses in parallel each conducting 5A current

The thermal via design in the above PCB with 4 NIS5452 devices employed techniques with multiple via arrays described above and shown in Figure 2. The distance between the eFuses was around 1 inch. Even though each eFuse is running at maximum rated current of 5 A and output load is pulling 20 A of current, because of the effective thermal layout each eFuse operates at a temperature of around 60 ºC or below.

Parallel operation and current balancing

Once the eFuse common output is connected to the load, the currents through each eFuse will be equally shared after the startup event. The Figure 4 shows the measured current through each eFuse when both of the eFuses are enabled at the same time into the load of about 5 A.

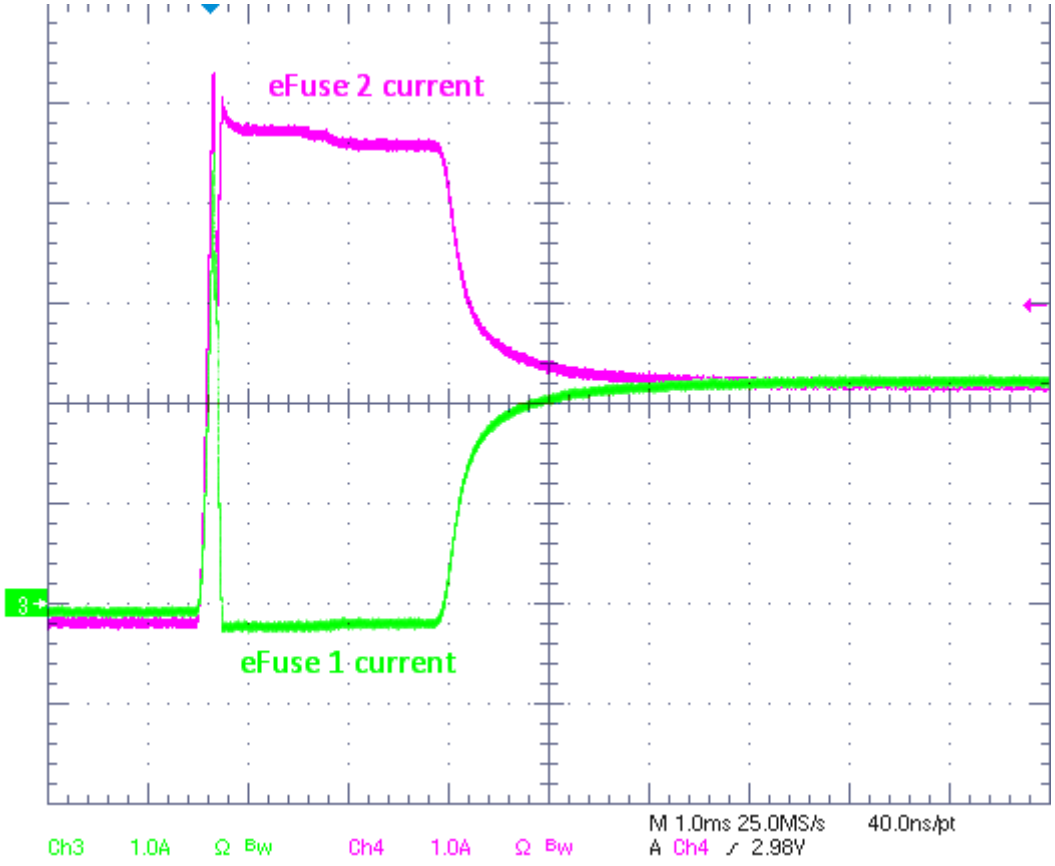

Figure 4. Current through each of the NIS5452 eFuse during enable startup event

The current through eFuse 1 is limited during a startup while the current through eFuse 2 is increased for around 2 ms. After the startup event currents through both eFuses are shared equally. The increased current throughput through one of the eFuses during a short startup event does not damage the eFuse or affect its lifetime or operation.

The picture in Figure 5 shows the same startup event simulated in the NIS5452 design environment. The simulated plot was one of the sets from the family of Monte Carlo variation curves. This type of startup event is common when eFuses are starting into the load and it is safe to use in the application.

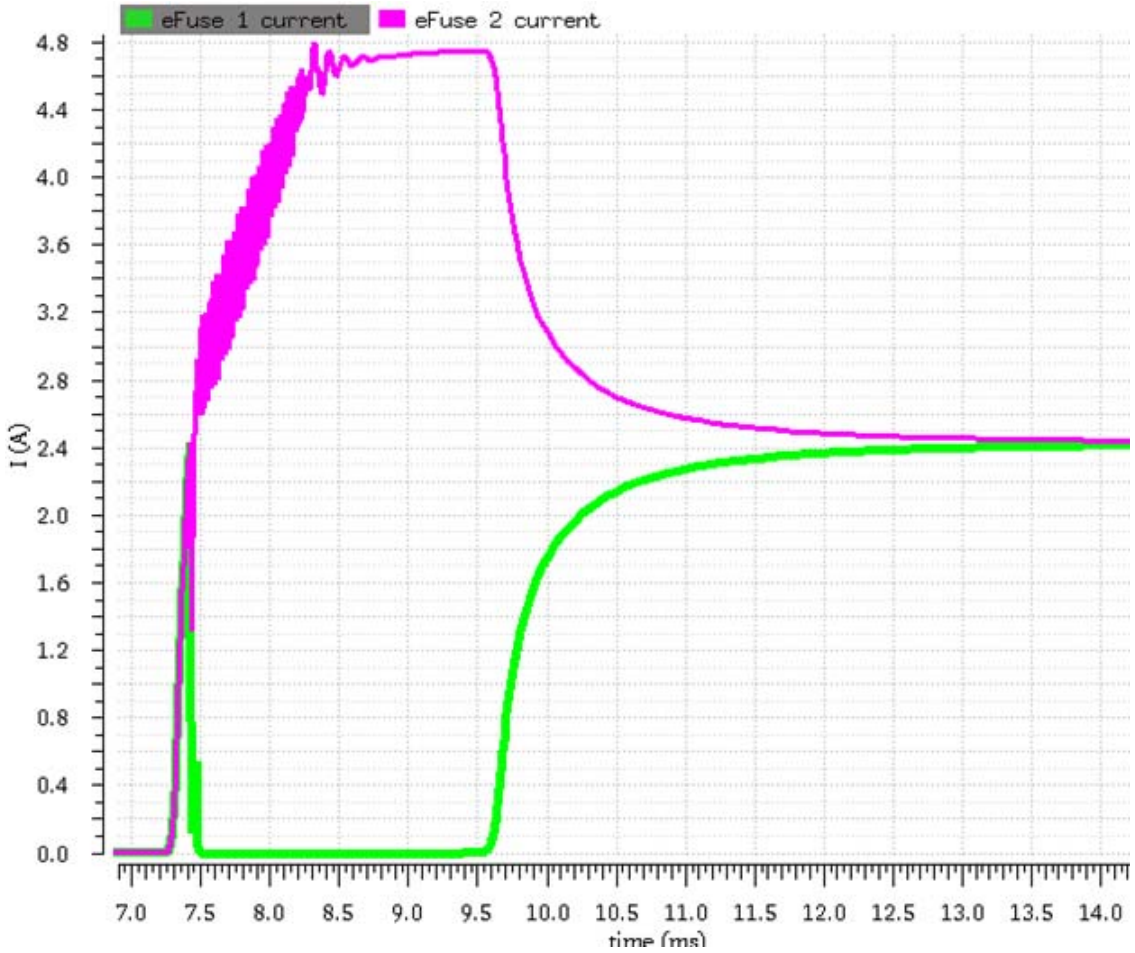

Figure 5. Simultaneous startup simulation from NIS5452 design environment

Another possible scenario is when the load is suddenly hot plugged to the output of the enabled eFuse. Such a measurement is shown in Figure 6.

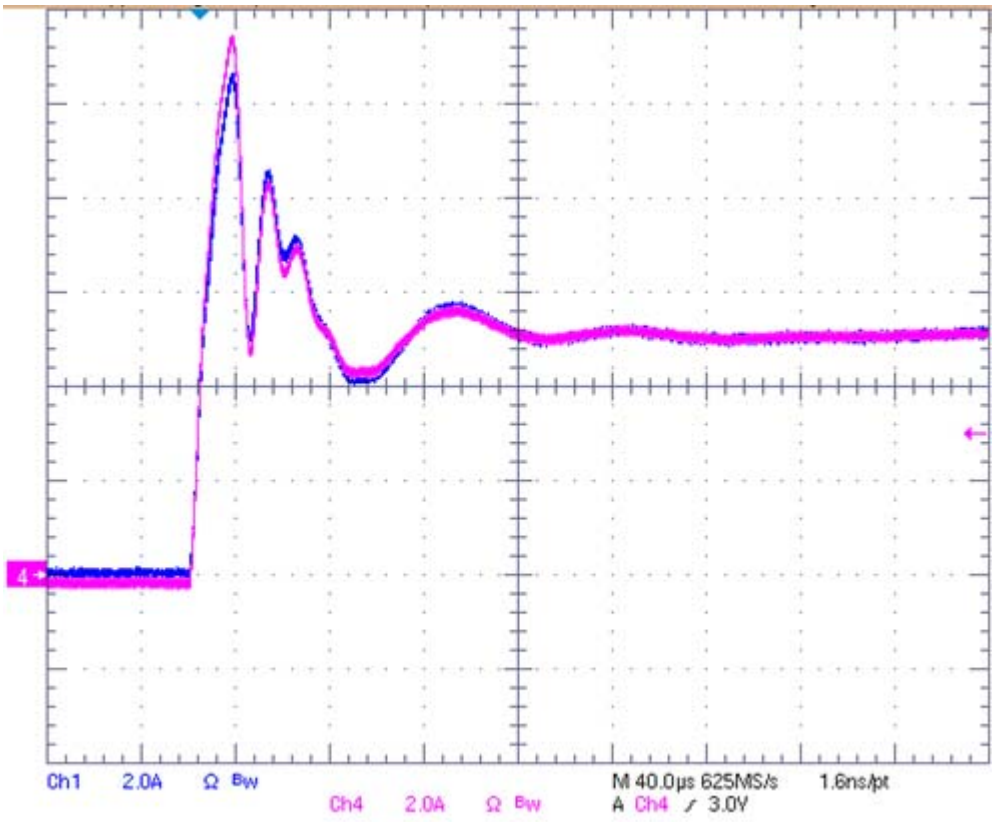

Figure 6. Hot plug event of both eFuses into the load

In this case, currents are shared equally again, but they are also shared during the hotplug event since the voltage on the eFuse output is already settled. 4ft cables were used for to connect the load in a hotplug mode, so as a result of additional inductance slight oscillation during startup is observed.

This same scenario has been simulated in the NIS5452 design environment as well with the results shown in Figure 7.

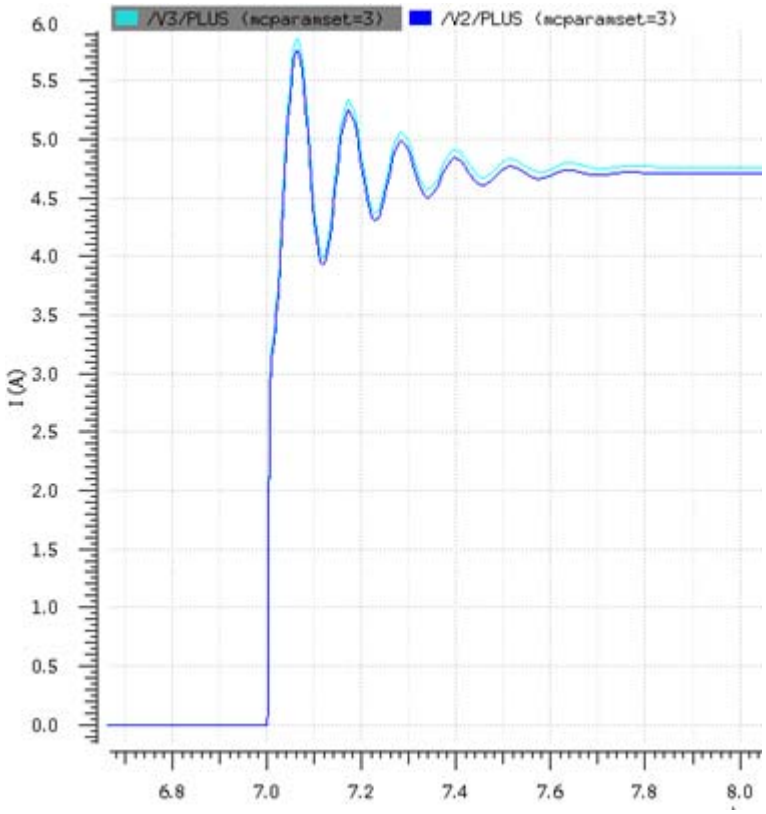

Figure 7. Hotplug event design simulation of 2 eFuses

Again the simulation and lab measurement results with similar conditions for the NIS5452 eFuse correlate.

Below in Figure 8 the measurement result of startup enabling of both eFuses to a 10 A load is shown.

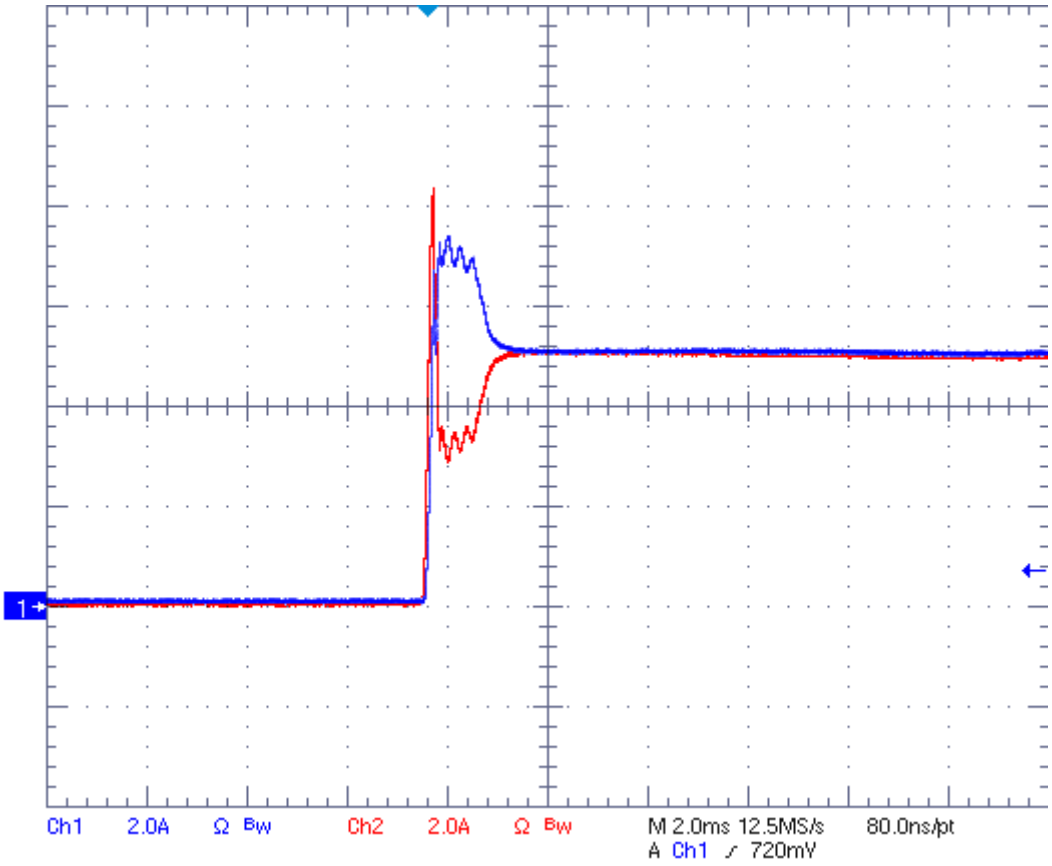

Figure 8. Startup of 2 eFuses into 10A load

Again the current through one of the eFuses during a startup is increased during a short amount of time and settles to the load current equally with another eFuse after the startup.

There are situations when user desires to control the output ramp up rate of the eFuse during the startup by connecting an appropriate capacitor to the “dvdt” pin of the eFuse. Care should be taken when dvdt capacitor is used. This is especially the case with parallel configuration where the high current loads are expected. Using the high value of the dvdt capacitor might create a big voltage difference between the input and output voltage of the eFuse. That voltage difference times the startup current might generate power enough to set one of the eFuses into a thermal shutdown during a startup. As a result, none of the eFuses would be able to startup to a high output load.

The Figure 9 shows the startup event of 2 eFuses into 4A load. In this case no dvdt capacitor is used.

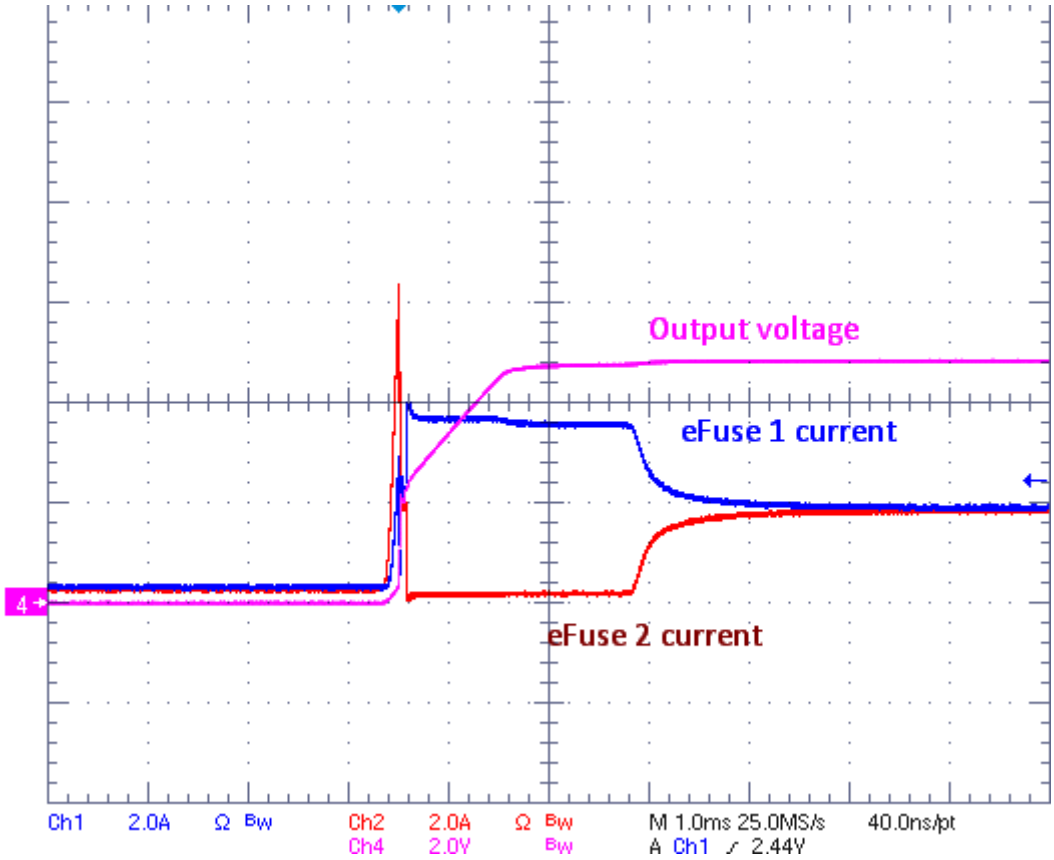

Figure 9. Startup of 2 eFuses with an output voltage rise shown, no dvdt capacitor used

For the small values of dvdt capacitor or when such capacitor is absent the output voltage ramps up quickly and there is no huge voltage difference between eFuse input and output during a long time generating a lot of heat. As a result, both loads startup and then balance nicely.

On the other hand, Figure 10 shows the case where 0.2 μF capacitor was used connected to a common dvdt pins of both eFuses. We can observe a very slow output voltage ramp up and current going through one of the eFuses during a startup. After about 16 ms from the enable event the eFuse carrying the startup current enters the thermal shutdown and none of the eFuses start up after that.

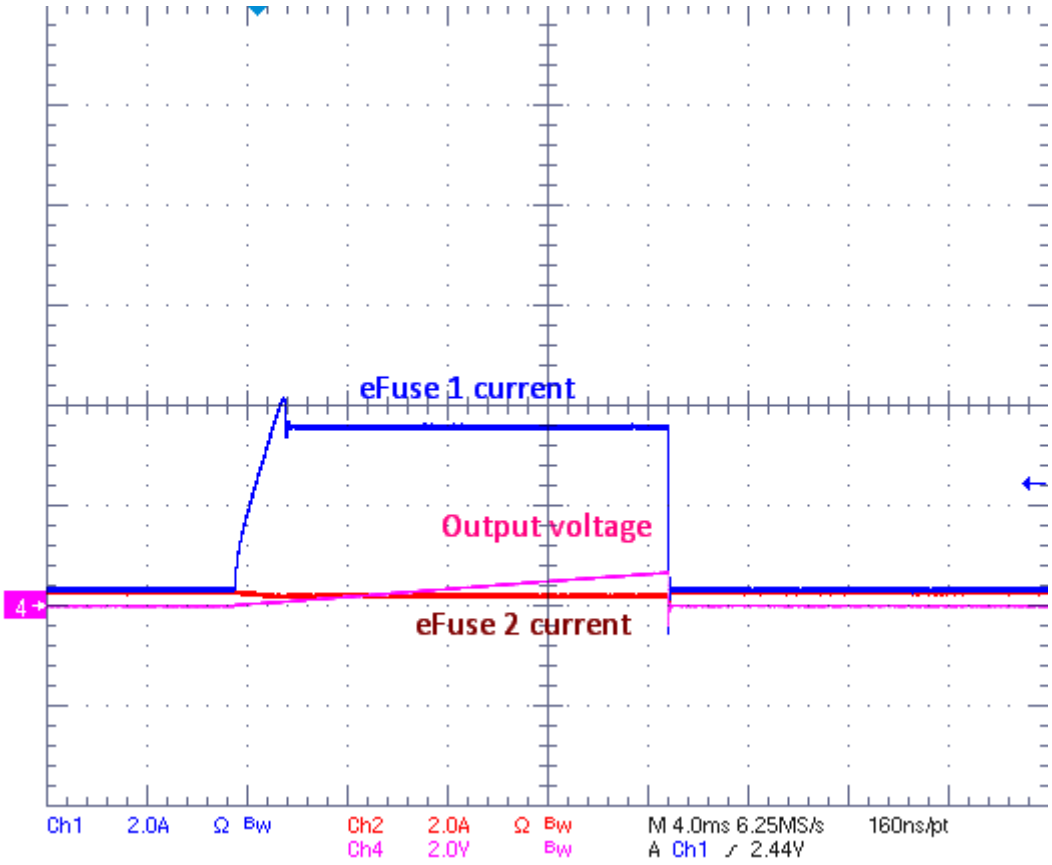

Figure 10. Startup of 2 eFuses with an output voltage rise shown, 0.2 μF dvdt capacitor used

As a result, user should be careful when selecting dvdt capacitor or using the delayed start feature when starting up to a high output load. Slow output ramp up times usually represent a potential of failure to start.

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