A Product Line of
Diodes Incorporated

PI2DPT821

DP-Alt Type-C 8.1Gbps Retimer with Adaptive Equalizer, Low-latency, Aux/SBU Switch with 1.8V Single Power Supply

Features

- Compliant for USB 5Gbps / DP1.4 8.1Gbps standard
- DP Alt standard mode support; DP 4-lane, USB 1 lane/DP 2 lane, USB 2 lane Retimer normal / flip insertion
- -18dB at 4.05GHz channel loss compensation
- Low Latency < 1ns.
- Adaptive Continuous Time Linear Equalizer (CTLE)
- No reference clock design.
- Rx termination detection for power saving control
- Selectable adjustment of 2-taps transmitter.
- Single power supply of 1.8±90mV.
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Application(s)

- Source Devices : Tablets, Smart Phones, Notebooks, Desktops, All-In-One PCs

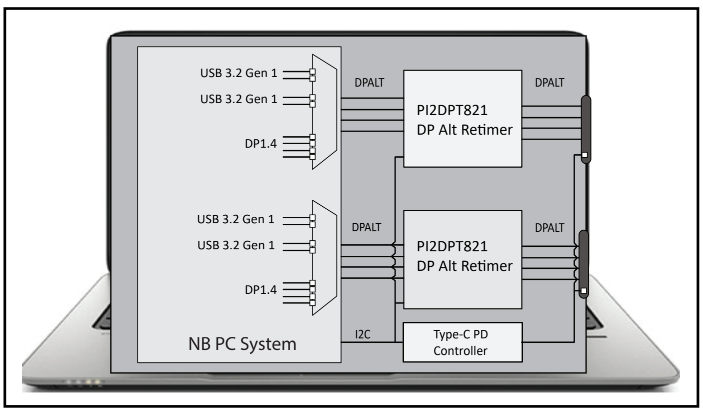


Figure 1-1 DP Alt Type-C Connectors inside PC

Description

The DIODES™ PI2DPT821 is a bit level Retimer with receiver adaptive CTLE and transmitter 2-tap equalization which can compensate channel loss up to -18dB for 4.05GHz signal transmission. It supports DP1.4 and USB 3.2 Gen 1 standards for USB Type-C® DP ALT mode operation. The operation configurations are programmable via I2C interface to select 4-lane DP, 2-lane DP/1 lane USB 3.2 Gen 1, 1 or 2 lane USB 3.2 Gen 1.

To achieve good power saving management, this device uses the common 1.8v Vdd power supply. It complies with USB link power management states for active mode (U0) and power saving mode (U1, U2, U3). USB Rx detection monitors the plug condition of the TX terminals continuously.

Under Displayport operation, the AUX Listener will monitor the AUX communication for data rate, lane count, swing & pre-emphasis setting and power saving D3 mode setting. The SINK side HPD connection signal is set via I2C register by the system PD controller. The integrated AUX/SBU switch switches the Displayport AUX+/- pins and the Type-C SBU1/SBU2 pins automatically.

With the merit of the bit level Retimer design, PI2DPT821 has very low latency from signal input to output (< 1ns) that serves good interoperability among various USB and DP devices.

Ordering Information

Ordering Number	Package Code	Package Description
PI2DPT821XEAEX	XEA	32-pin, X1-QFN2845-32 (2.85x4.5mm), 0.4mm pitch, 0.45mm height

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

USB Type-C® and USB-C® are registered trademarks of USB Implementers Forum.

2. General Information

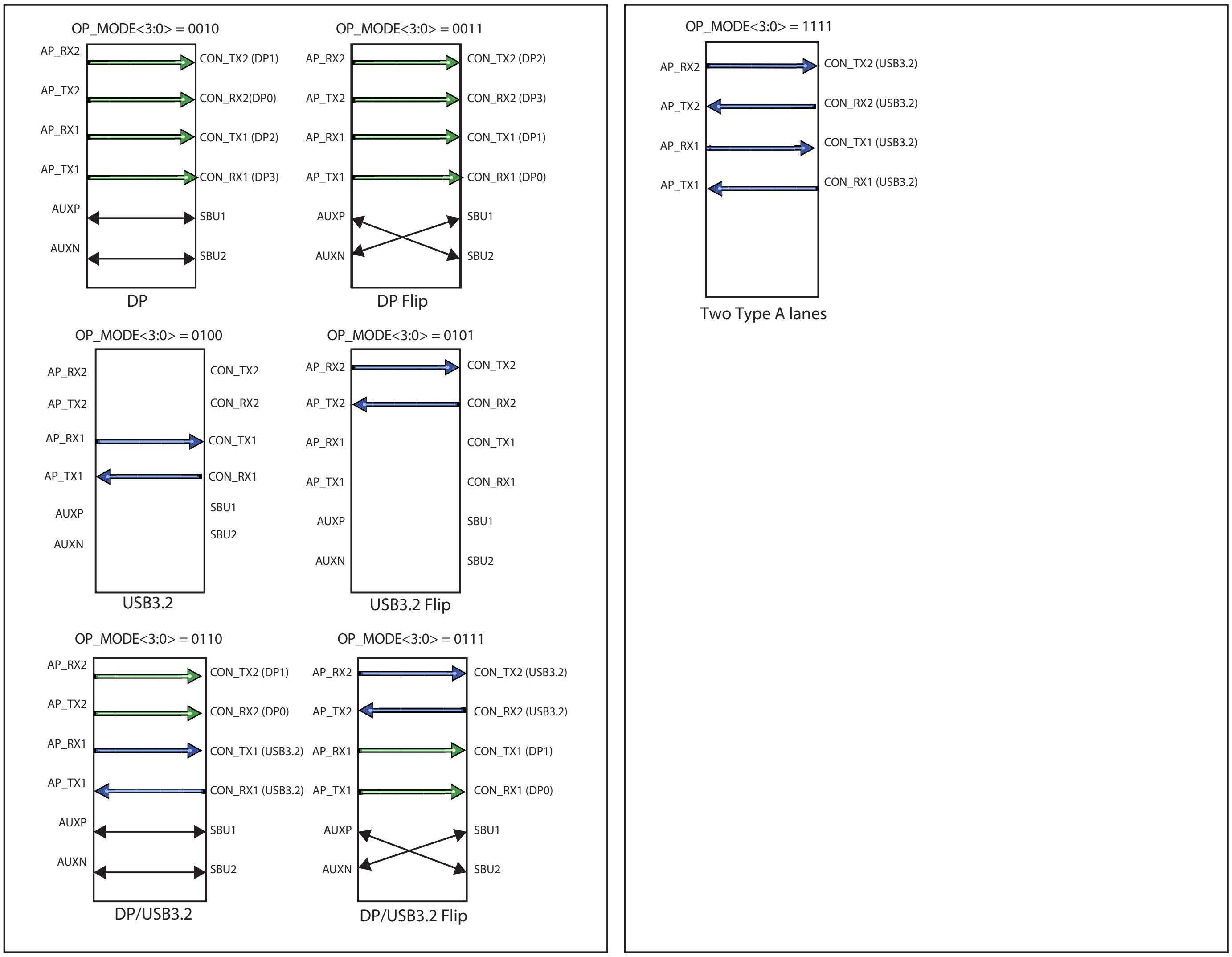


Figure 2-1 The Channel Configuration Against the OP_MODE<3:0>

Contents

3. Pin Configuration

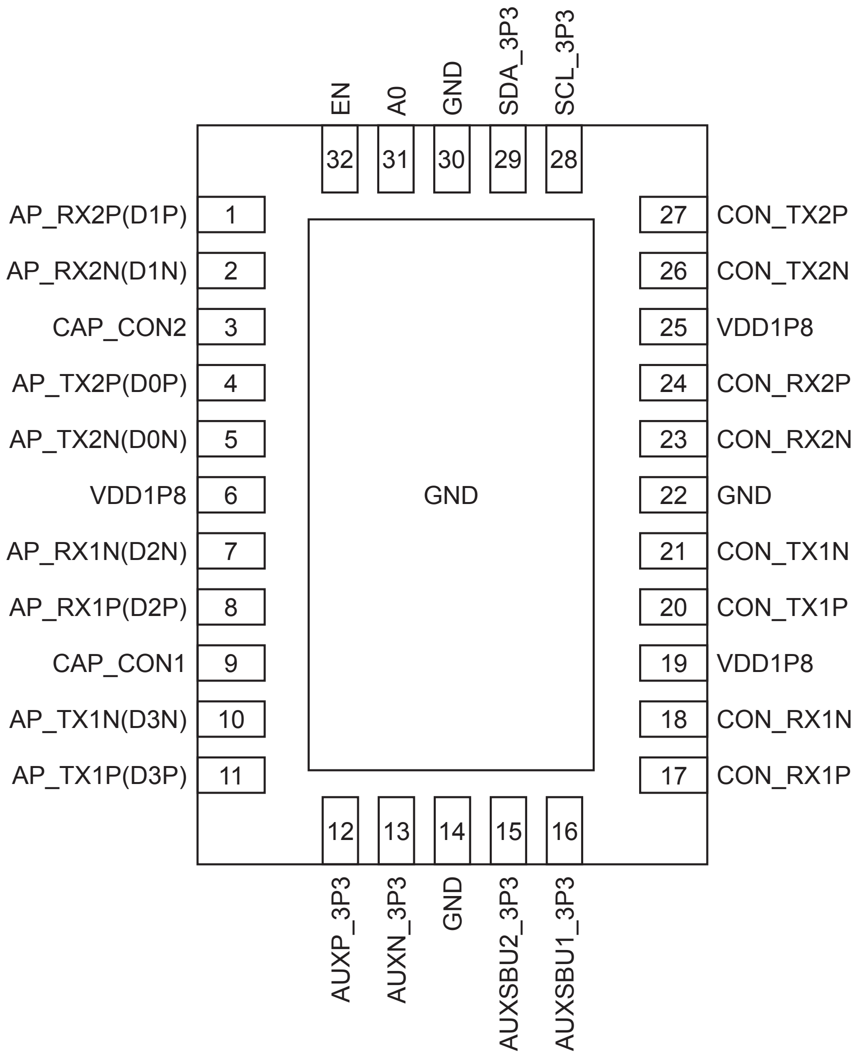


Figure 3-1 PI2DPT821 Pin Configuration

3.1 Pin Description

Pin #	Pin Name	Type	Description
Power and GND			
6, 19, 25	VDD1P8	Power	1.8V power supply, +/- 5%
14, 22, 30, Center Pad	GND	GND	Supply Ground
3	CAP_CON2	Power	The CON2 VDD1V external decoupling capacitor.
9	CAP_CON1	Power	The CON1 VDD1V external decoupling capacitor.
Control Pins			
32	EN	I	Chip Enable. With internal 340kΩ pull-up resistor. “Low”: Chip Power Down “High”: Normal Operation (Default)
28	SCL_3P3	I	SCL is I2C control bus clock. Open drain structure (3.3V tolerance)
29	SDA_3P3	I/O	SDA is I2C control bus data. Open drain structure. (3.3V tolerance)
31	A0	I	2-level I2C address selection pins. With internal 340kΩ pull-down resistor.
High Speed I/O Pins			
1, 2 4, 5 8, 7 11, 10	AP_RX2P/N, AP_TX2P/N AP_RX1P/N, AP_TX1P/N	I/O	Application Processor side Type-C receptacle RX/TX CML input/output terminals. Config as RX terminal: Input with termination 50Ω to GND or 75kΩ to GND. Config as TX terminal: Output termination 50/1.5kΩ to VbiasTx, 3kΩ to GND or 75kΩ to GND.
27, 26 24, 23 20, 21 17, 18	CON_TX2P/N, CON_RX2P/N CON_TX1P/N, CON_RX1P/N	I/O	Connector side Type-C receptacle RX/TX CML input/output terminals. Config as RX terminal: Input with termination 50Ω to GND or 75kΩ to GND. Config as TX terminal: Output termination 50/1.5kΩ to VbiasTX, 3kΩ to GND or 75kΩ to GND.
AUX I/O Pins			
12, 13	AUXP_3P3, AUXN_3P3	I/O	DP dual mode AUX CH differential signals, connected to Source. (3.3V tolerance)
16, 15	AUXSBU1_3P3, AUXSBU2_3P3	I/O	DP dual mode AUX CH differential signals, connected to Sink. (3.3V tolerance)

4. Functional Description

4.1 Detail Features

- Maximum channel loss compensation up to -18dB at 4.05GHz
- Bit-level USB and DP Retimer for low latency
- Adaptive receiver Continuous Time Linear Equalizer (CTLE)
- No reference clock design
- I2C slave to configure the channel setting and operation mode
- DP Alt standard mode support: DP 4-lane, DP 2-lane/USB 1-lane, USB 1-lane only and USB 2-lane for type A normal/flip modes
- Support USB3.2 Gen1 Retiming mode
- Supports DP RBR, HBR, HBR2 and HBR3 Retiming mode
- DP AUX channel listening (snooping) support for auto channel adjustment and D3 power down mode

Tx/Rx IO channels

- Rx termination detection for power saving control
- RX terminations: 50Ω to GND or 75kΩ to GND
- TX driver output termination: 50/1.5kΩ to VbiasTx, 3k/75kΩ to GND.
- Selectable adjustment of 2-taps transmitter.

Power

- Single power supply of 1.8±90mV
- 650mW active power consumption for 2-lane DP and 2-channel USB 5Gbps operating mode
- <500uW target in power down mode

4.2 Functional Block Diagram

Below is shown the simple re-timer. The termination resistors are shared between the TX and RX, and terminated to internal LDO supply (1.08V nominal). The TX driver is a 2-taps Feed Forward Equalization (FFE) driver with programmable tuning coefficient to meet multiple standards. The Continuous-Time-Linear Equalizer (CTLE) is adaptive and controlled by the digital state machine after the training.

The signal detector is used to control the power status.

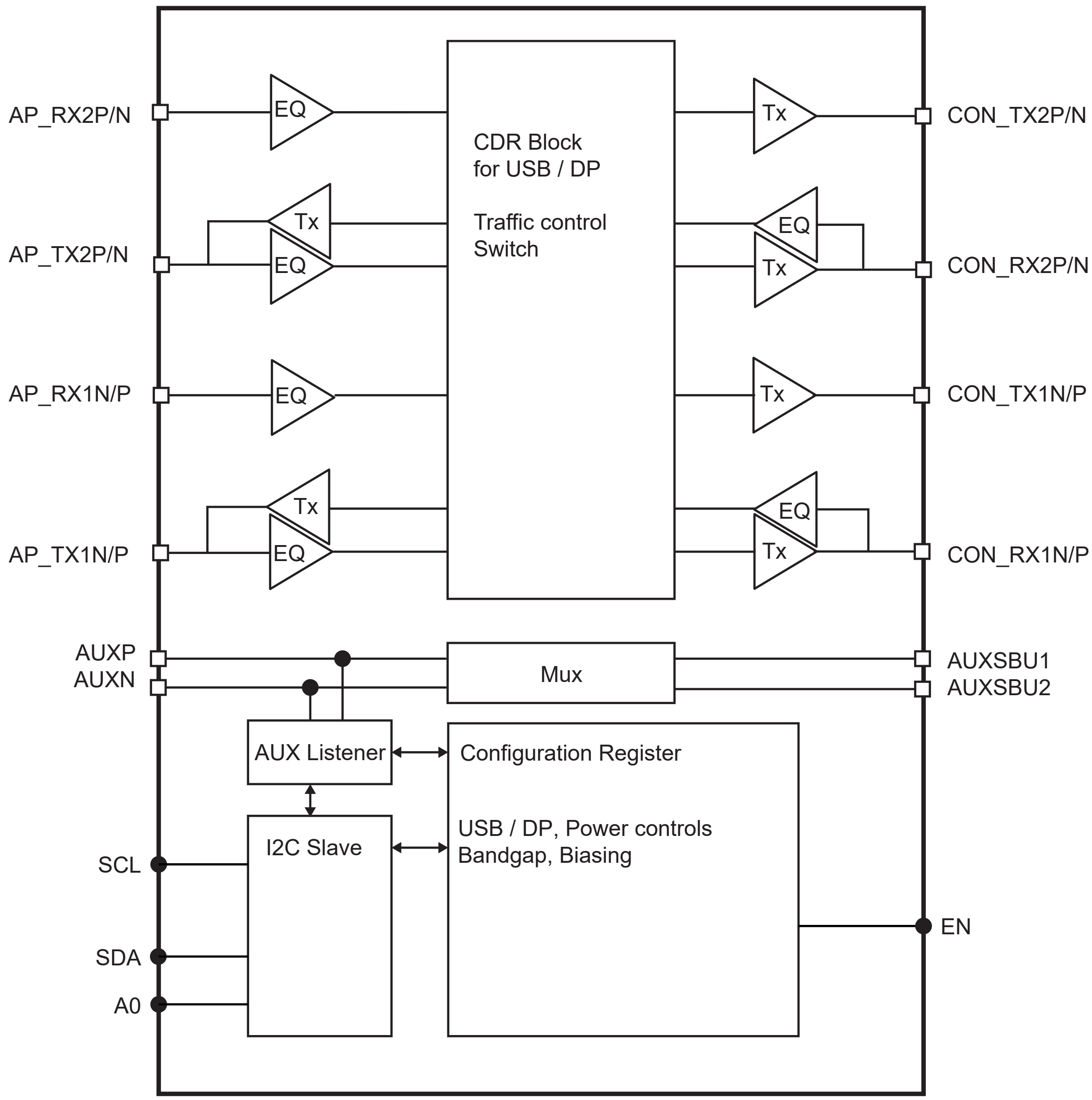


Figure 4-1 PI2DPT821 Retimer Block Diagram

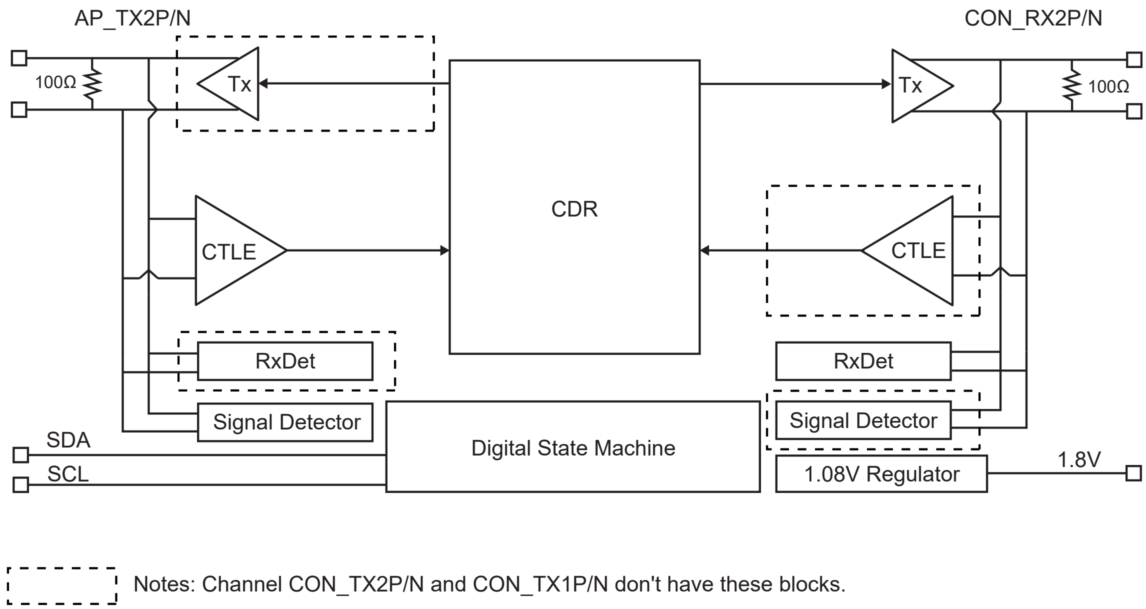


Figure 4-2 PI2DPT821 Functional Retimer Block Diagram

4.3 USB Mode

To be able to enhanced the re-timer's power efficiency, the supported power state in USB SSP is following: U0 and non-U0s (RXDET/U1/U2/U3).

The I/O termination resistance under different conditions

Symbol	Parameter	Resistance	Units
RX terminal			
Rin-pd	Input resistance at power down mode	75k to GND	Ω
Rin-U0	Input resistance at U0 condition	50 to GND	Ω
Rin-U1	Input resistance inU1 (1)	50 to GND	Ω
Rin-U2/U3	Input resistance in U2/U3 (1)	50 to GND	Ω
Rin-RXDet	Input resistance in RXDET (1)	75k to GND	Ω
TX terminal			
Rout-pd	Output resistance at power down mode	75k to GND	Ω
Rout-U0	Output resistance at U0 condition	50 to VbiasTx	Ω
Rout-U1	Output resistance in U1 mode (1)	1.5k to VbiasTx	Ω
Rout-U2/U3	Output resistance in U2/U3 mode (1)	3k to GND	Ω
Rout-RXDet	Output resistance in RXDET mode (1)	3k to GND	Ω

Notes: (1) The value of Rin-RxDet will be updated only after the receiver evaluation has been done. Thus, the value can be 50Ω or 75kΩ to GND.

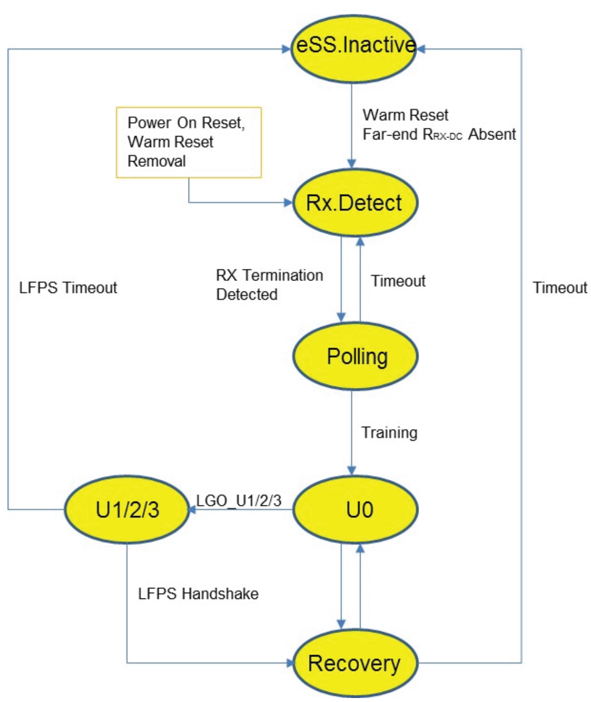


Figure 4-3 Re-timer Supported USB Power State Diagram

4.4 DisplayPort mode

By default, all channels will go to active modes if IN_HPD = 1. The ON/OFF of each DP channel is controlled by the Aux lane count and D3 command.

4.4.1 DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DPTX drives doubly terminated, AC-coupled differential pairs, as shown in Figure 4-4 in a manner compliant with the Main-Link Transmitter electrical specification.

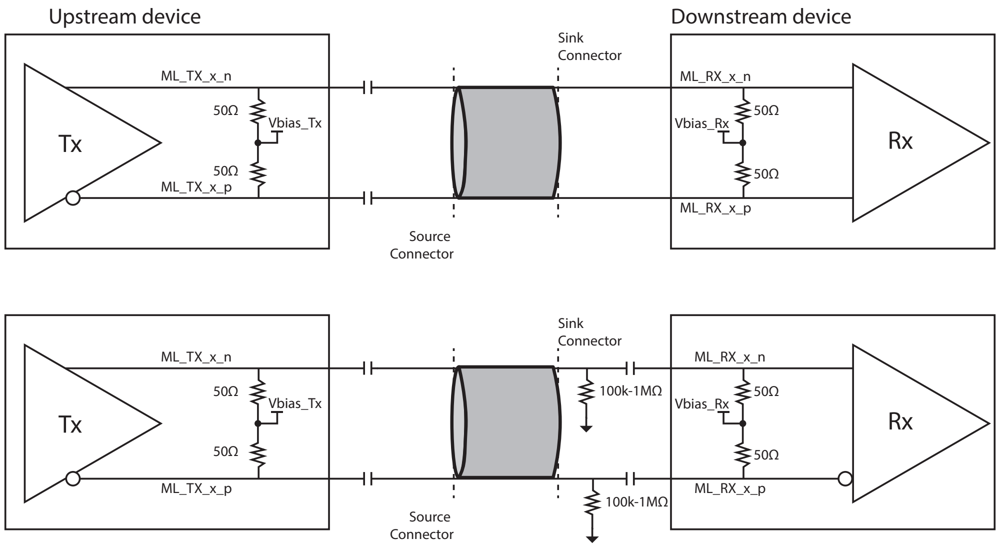


Figure 4-4 DisplayPort Main Link Connection Diagram

4.4.2 DP Low Power Mode Description

PM_State	Mode	Description
1	Active mode	Data transfer (normal operation); The AUX monitor is actively monitoring for Link Training unless it is disabled through I2C interface. At power-up all Main Link outputs are Enabled by default. AUX Link Training is necessary to overwrite the DPCD registers to Enable/Disable Main Link outputs.
2	Standby mode	Low power consumption (I2C interface is active; AUX monitor is inactive); Main Link outputs are disabled; the Sink device has de-asserted HPD
3	D3 power saving mode (Sleep)	Low power consumption(I2C interface is active; AUX monitor active); Main Link outputs are disabled; The Sink device has asserted HPD, and sufficiently enabled the AUX CH to at least monitor incoming AUX CH differential signals. The Main-Link RX disabled.
4	Power down mode(OFF)	Lowest power consumption (EN = 0); all outputs are high-impedance; I2C interface is turned off, all inputs are ignored, I2C register is reset and AUX DPCD is reset:

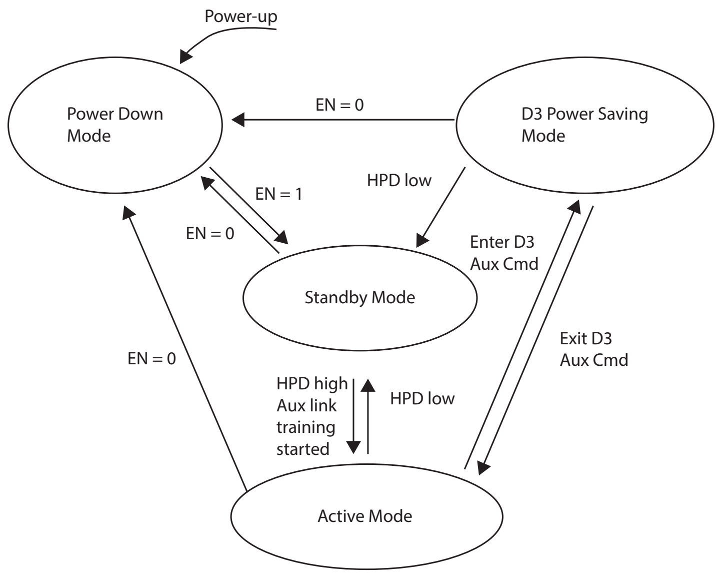


Figure 4-5 DisplayPort Operation Mode

4.4.3 DisplayPort Aux Channel

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction.

The system design of a DFP_D on a USB Type-C connector connected to a UFP_D on a USB Type-C connector using a USB Type-C to USB Type-C Cable. The 2MΩ pull-down resistors on SBU1 and SBU2 are representative of the leakage of ESD and EMI/RFI components including termination to ensure no floating nodes, and are intended to show compliance with zSBUTermination in USB Type-C r1.1. The plug orientation switch may be replaced by AUX polarity inversion logic in the DisplayPort transmitter or receiver, controlled by the plug orientation detection mechanism associated with the USB Type-C Receptacle.

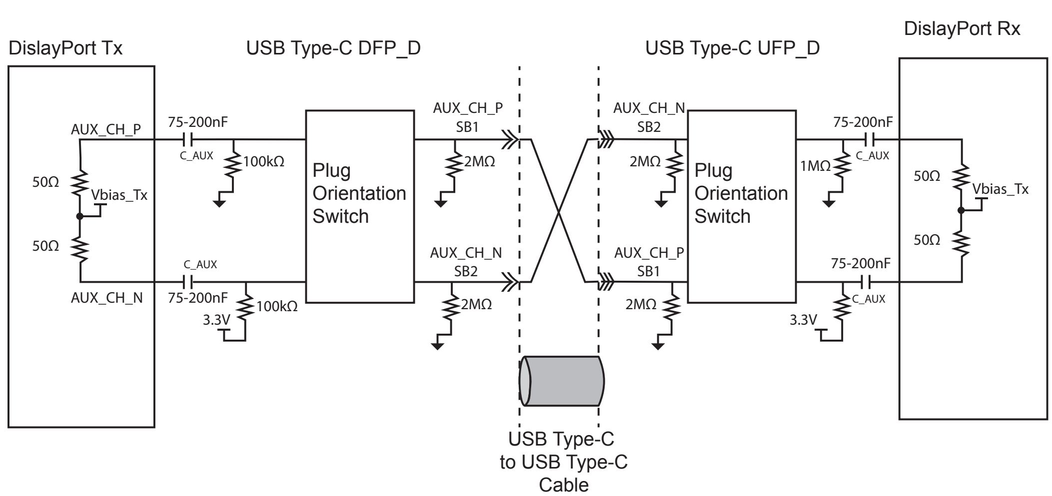


Figure 4-6 AUX Signaling Using USB Type-C to USB Type-C Cables

4.4.4 Aux Listener

The listener will reset the state machine if there is abnormal stop happen before the stop pattern is received.

- AUX listener monitors AUX channel from Source and Sink for transactions.
- AUX listener recovered the clock from Aux data input by cycle counting the synchronization pulse at the beginning of the AUX cycle.
- AUX listener stores the AUX command for Native AUX write request

4.4.5 DP Sleep Mode

AUX listener keep snooping the AUX communication between Source and Sink. Upon successful interception of DP entering D3 state, DP Retimer will enter sleep mode and its output to HiZ to save power.

4.4.6 Supported DisplayPort Swing and Deemphasis Setting

DE(dB)	Voltage Swing			
0	0.40	0.60	0.80	1.20
3.5	0.60	0.90	1.20	
6	0.80	1.20		
9.5	1.2			

4.4.7 AUX Read/Write

In AUX read/write request cycle, the AUX address compare the addresses with the following registers' address, data is extracted and stored into the respective registers when the addresses matches. These registers are set during link training sequence following hot plug detection.

00100h Data Rate register
00101h LANE_COUNT_SET
00103h TRAINING_LANE0_SET
00104h TRAINING_LANE1_SET
00105h TRAINING_LANE2_SET
00106h TRAINING_LANE3_SET
00600h Power Down

00206h ADJUST_REQUEST_LANE0_1
00207h ADJUST_REQUEST_LANE2_3
00218h TEST_REQUEST
00219h Test link rate
00220h Test Lane count
00260h Sink Test request response

4.4.8 Sink Request Test Mode

Registers used in the normal/ Sink Requested Test mode

DPCD Registers	Action	Buffer configuration outputs
0x00218<0> = 1b & 0x00260<1:0> = 01b	Sink Test mode	Use DPCD 0x00219h and 0x00220h for the LINK_BW_SET and LANE_COUNT_SET respectively.
0x00218<0> = 0b or 0x00260<1:0> = Not 01b	Normal mode	Use DPCD 0x00100h and 0x00101h for the LINK_BW_SET and LANE_COUNT_SET respectively.

4.5 I2C Programming

4.5.1 I2C Address

	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address	1	0	1	0	0	0	A0	0/1 (W/R)

4.5.2 I2C Operation

- I2C interface operates as a slave device.
- The device supports Indexed read/write
- Support operating speed up to 1MHz
- Supported 7-bit addressing
- The data byte format is 8-bit bytes with the most significant bit (MSB) first.
- Will never hold the clock line SCL LOW to force the master into a wait state.
- No response when the data on common bus is matched to the device address.
- If I2C master want read/write invalid register, i.e. the I2C slave just write/read from a dummy RO register with FF by default.

4.5.3 Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

4.5.4 Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first. It will never hold the clock line SCL LOW to force the master into a wait state.

4.5.5 Start & Stop Condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.

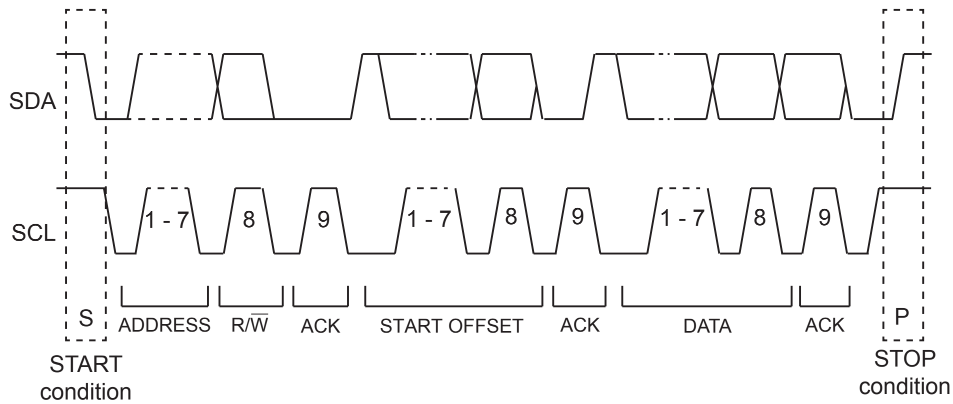


Figure 4-7 I2C Start and STOP Condition

S	SLAVE ADDRESS	RW	A	START OFFSET	A	Sr	SLAVE ADDRESS	RW	A	DATA	A	DATA	A	P
		"0" (write)						"1" (read)		data transferred (n bytes + acknowledge)				

From master to slave (shaded)
From slave to master (unshaded)

A= Acknowledge (SDA LOW)
$\overline{A}$= Not acknowledge (SDA HIGH)
S= Start condition

Sr= Repeated START condition
P= Stop condition

Figure 4-8 Indexed Read Protocol

S	SLAVE ADDRESS	R$\overline{W}$	A	START OFFSET	A	DATA	A	DATA	A/$\overline{A}$	P
		"0" (write)				data transferred (n bytes + acknowledge)				

From master to slave (shaded)
From slave to master (unshaded)

A= Acknowledge (SDA LOW)
$\overline{A}$= Not acknowledge (SDA HIGH)
S= Start condition

Sr= Repeated START condition
P= Stop condition

Figure 4-9 Indexed Write Protocol

4.6 Register Assignment

Byte 0 (Vendor ID Register)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Revision ID	Revision ID = 0010
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0	Vendor ID	Pericom ID = 0011
2	RO	0		
1	RO	1		
0	RO	1		

Byte 1 (Device Type/Device ID Register)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Device Type	Device Type 0010 = Retimer
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0	Device ID	Device ID =0001
2	RO	0		
1	RO	0		
0	RO	1		

Byte 2 (Byte Count Register)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	1	Register Byte count	I2C byte count = 128 bytes
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		

Byte 3 (Channel Assignment)

Bit	Type	Power up condition	Purpose	Comment
7	R/W	0	OP_MODE<3>	Selects the Application Mode
6	R/W	0	OP_MODE<2>	
5	R/W	0	OP_MODE<1>	
4	R/W	0	OP_MODE<0>	
3	R/W	0	Reserved	
2	R/W	0	Reserved	
1	R/W	0	Reserved	
0	R/W	0	Reserved	

Byte 4 (Override the Power Down Control and IN_HPD Control)

Bit	Type	Power up condition	Purpose	Comment
7	R/W	0	PD_CON_TX2	CONx power down override 0 – Do not force the CONx to power down state 1 – Force the CONx to power down state
6	R/W	0	PD_CON_RX2	
5	R/W	0	PD_CON_TX1	
4	R/W	0	PD_CON_RX1	
3	R/W	1	Reserved	
2	R/W	0	IN_HPD	0 – HPD is de-asserted 1 – HPD is asserted
1	R/W	0	Reserved	
0	R/W	0	Reserved	

Byte 5 (Enable/Disable the Auto SW&PE Control by the AUX in DP Mode)

Bit	Type	Power up condition	Purpose	Comment
7	R/W	1	Reserved	Reserved
6	R/W	1	Reserved	
5	R/W	1	Reserved	
4	R/W	1	Reserved	
3	R/W	0	CONX_DP_AUX_SW_PE_VAL_OR_EN	Override the AUX SW and PE control values for DP mode only Low: The DP TX SW and PE are controlled by the AUX CMD High: The DP TX SW and PE are controlled by the Manual setting
2	R/W	0	AUX _DISABLE_OR	Force to disable both AUX SW and AUX listener 0 – Normal (Default) 1 – Force to disable both AUX SW and AUX listener
1	R/W	0	AUX_LISTENER_DISABLE_OR	Force the AUX Listener only 0 – Normal (Default) 1 – Force to disable the AUX listener only
0	R/W	0	Reserved	

Byte 6 (CON2 USB Mode De-emphasis Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	Reserved	
6	R/W	0	Reserved	
5	R/W	0	Reserved	
4	R/W	0	Reserved	
3	R/W	0	CON_TX2_USB_SW_DE<1>	USB mode CON2: USB Gen1 De-emphasis setting USB_GEN1_SW_DE<1:0> 00 DE=0dB 01 DE = -3.5dB 1x Reserved
2	R/W	0	CON_TX2_USB_SW_DE<0>	
1	R/W	0	CON_RX2_USB_SW_DE<1>	
0	R/W	0	CON_RX2_USB_SW_DE<0>	

Byte 7 (CON1 USB Mode De-emphasis Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	Reserved	
6	R/W	0	Reserved	
5	R/W	0	Reserved	
4	R/W	0	Reserved	
3	R/W	0	CON_TX1_USB_SW_DE<1>	USB mode CON1: USB Gen1 De-emphasis setting USB_GEN1_SW_DE<1:0> 00 DE=0dB 01 DE = -3.5dB 1x Reserved
2	R/W	0	CON_TX1_USB_SW_DE<0>	
1	R/W	0	CON_RX1_USB_SW_DE<1>	
0	R/W	0	CON_RX1_USB_SW_DE<0>	

Byte 8 (Manual Override the DP SW and DE Settings of CON_TX2 and CON_RX2)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	CON_TX2_DP_SW<1>	SW&DE setting when CONX_DP_AUX_SW_PE_OR_EN=1 DP_SW<1:0> DP_DE<1:0> SW DE 00 00 0.4Vppd 0 00 01 0.4Vppd 3.0dB 00 10 0.4Vppd 5.6dB 00 11 0.4Vppd 7.9dB 01 00 0.6Vppd 0dB 01 10 0.6Vppd 2.6dB 01 1x 0.6Vppd 4.9dB 10 x0 0.8Vppd 0dB 10 x1 0.8Vppd 2.3dB 11 xx 1.05Vppd 0dB
6	R/W	0	CON_TX2_DP_SW<0>	
5	R/W	0	CON_TX2_DP_DE<1>	
4	R/W	0	CON_TX2_DP_DE<0>	
3	R/W	0	CON_RX2_DP_SW<1>	
2	R/W	0	CON_RX2_DP_SW<0>	
1	R/W	0	CON_RX2_DP_DE<1>	
0	R/W	0	CON_RX2_DP_DE<0>	

Byte 9 (Manual Override the DP SW and DE settings of CON_TX1 and CON_RX1)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	CON_TX1_DP_SW<1>	SW&DE setting when CONX_DP_AUX_SW_PE_OR_EN=1 DP_SW<1:0> DP_DE<1:0> SW DE 00 00 0.4Vppd 0 00 01 0.4Vppd 3.0dB 00 10 0.4Vppd 5.6dB 00 11 0.4Vppd 7.9dB 01 00 0.6Vppd 0dB 01 10 0.6Vppd 2.6dB 01 1x 0.6Vppd 4.9dB 10 x0 0.8Vppd 0dB 10 x1 0.8Vppd 2.3dB 11 xx 1.05Vppd 0dB
6	R/W	0	CON_TX1_DP_SW<0>	
5	R/W	0	CON_TX1_DP_DE<1>	
4	R/W	0	CON_TX1_DP_DE<0>	
3	R/W	0	CON_RX1_DP_SW<1>	
2	R/W	0	CON_RX1_DP_SW<0>	
1	R/W	0	CON_RX1_DP_DE<1>	
0	R/W	0	CON_RX1_DP_DE<0>	
Byte 10 (Reserved RW0x00h)				
Byte 11 (DP Datarate and Lane Count Detting when the AUX feature is Disabled)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	R/W	0	DP_DATARATE_FOR_AUX_IS_DISABLED<1>	Set the DP datarate when AUX feature is disabled 00 1.62Gbps 01 2.7Gbps 10 5.4Gbps 11 8.1Gbps
6	R/W	0	DP_DATARATE_FOR_AUX_IS_DISABLED<0>	
5	R/W	0	DP_LANE_COUNT_FOR_AUX_IS_DISABLED<1>	Set the DP Lane count when the AUX feature is disabled 00 Invalid 01 1 lane 10 2 lanes 11 4 lanes
4	R/W	1	DP_LANE_COUNT_FOR_AUX_IS_DISABLED<0>	
3	R/W	0	Reserved	
2	R/W	0	Reserved	
1	R/W	0	Reserved	
0	R/W	0	Reserved	
Byte 12-15 (Reserved RW: 0x00h)				
Byte 16-17 Reserved RO: 0x02h				

Byte 18 (Monitor the Channel feature Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	1	CON_TX2_AP2CON_SEL	Signal flow of channel 0: Signal is from CON side to AP side 1: Signal is from AP side to CON side
6	RO	1	CON_RX2_AP2CON_SEL	
5	RO	1	CON_TX1_AP2CON_SEL	
4	RO	1	CON_RX1_AP2CON_SEL	
3	RO	0	AUX_FLIP	AUX SW flip control for AUXSBU1/2 and AUXP/N 0 – Flip is disabled. AXSBU1 is connected to AUXP 1 – Flip is enabled
2	RO	0	DP FLIP	The logical definition of Lane0 of DP mode 0 – CON_RX2 is Lane0 1 – CON_RX1 is Lane0
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 19-23 Reserved R/W: 0x00h				
Byte 24 Reserved R/W: 0x20h				
Byte 25-27 Reserved R/W: 0x00h				
Read Only Register Section				
Byte 28 (Common Monitor for all CON Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	AUX_EN	Monitor the AUX_EN to the Core “0” – Disabled “1” – Enabled
6	RO	0	AUX_LISTENER_EN	Monitor the AUX_LISTENER_EN to the Core “0” – Disabled “1” – Enabled
5	RO	0	AUX_SIG	Detect the AUX activities “0” – Idle “1” – has activities
4	RO	0	AUX_BUSY_OUT	The status of the AUX Listener “0” – Idle “1” – Active
3	RO	0	DP_HPD_ASSERT_STATUS	The condition of IN_HPD 0 – De-asserted 1 – Asserted
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	
Byte 29 Reserved RO: 0x00h				

Byte 30 (Common Monitor for all CON Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	DP_DATARATE_TO_CORE<1>	DP Data Rate 00 1.62Gbps 01 2.7Gbps 10 5.4Gbps 11 8.1Gbps
5	RO	0	DP_DATARATE_TO_CORE<0>	
4	RO	0	PD_OSC50M_MON	Monitor the PD status of the internal 50MHz oscillator
3	RO	0	Reserved	
2	RO	0	PD_ALL#	The Silicon is in the I2C PD mode 0 – The silicon is in the I2C PD mode 1 – The silicon is not in the I2C PD mode
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 31-32 Reserved RO: 0xAAh and 0x08h

Byte 33 (Common Monitor for CON2 Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	Reserved	
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	CON2_WARMRESET_MON	Monitor the CON2 USB LBPM warmreset decoded value 0 – WarmReset pattern is not detected 1 – WarmReset pattern is detected
0	RO	0	CON2_DSM_TIMEOUT_MON	Monitor the CON2 USB 328ms electrical IDLE Timeout 0 – The electrical idle is shorter than 328ms typ 1 – The electrical idle is longer than 328ms typ

Byte 34 Reserved RO: 0x08h

Byte 35 (Common Monitor for CON1 Setting)

Bit	Type	Power up condition	Purpose	Comment
7	R/W	0	Reserved	
6	R/W	0	Reserved	
5	R/W	0	Reserved	
4	R/W	0	Reserved	
3	R/W	0	Reserved	
2	R/W	0	Reserved	
1	R/W	0	CON1_WARMRESET_MON	Monitor the CON2 USB LBPM warmreset decoded value 0 – WarmReset pattern is not detected 1 – WarmReset pattern is detected
0	R/W	0	CON1_DSM_TO_MON	Monitor the CON2 USB 328ms electrical IDLE Timeout 0 – The electrical idle is shorter than 328ms typ. 1 – The electrical idle is longer than 328ms typ.

Byte 36 Reserved RO: 0x00h

Byte 37 (Monitor for CON_TX2 CDR Lock Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX2_CDR_LOCKED	CON_TX2 CDR_LOCKED Monitor
4	RO	0	CON_TX2_PLL_LOCKED	CON_TX2 PLL LOCKED Monitor
3	RO	0	Reserved	Reserved
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 38 (Monitor for CON_TX2 RX Auto CTLE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX2_CTLE_CAL_DONE	CON_TX2 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_TX2_CTLE_CODE<3>	CON_TX2 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_TX2_CTLE_CODE<2>	
1	RO	0	CON_TX2_CTLE_CODE<1>	
0	RO	0	CON_TX2_CTLE_CODE<0>	

Byte 39 Reserved RO: 0x00h

Byte 40 (Monitor Channel PD Status and CON_TX2 LFPS_Decoder Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	1	CON_TX2_PD#	CON_TX2 PD# status monitor
5	RO	0	Reserved	
4	RO	0	Reserved	
3	RO	0	Reserved	
2	RO	0	CON_TX2_USB_WARMRESET	CON_TX2 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 41 Reserved RO: 0x00h

Byte 42 (Monitor for CON_TX2 Operating Mode Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	CON_TX2_HS_IDLE	CON_TX2 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_TX2_LFPS_IDLE	CON_TX2 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_TX2 DET_5Gbps	CON_TX2 input signal type 0 – LFPS signal 1 – 5Gbps high speed signal
4	RO	0	CON_TX2_HS_OP_MODE<4>	CON_TX2 channel operating mode
3	RO	0	CON_TX2_HS_OP_MODE<3>	
2	RO	0	CON_TX2_HS_OP_MODE<2>	
1	RO	0	CON_TX2_HS_OP_MODE<1>	
0	RO	0	CON_TX2_HS_OP_MODE<0>	

Byte 43 (Monitor for CON_TX2 RX Signal Status and USB Compliance Test Mode Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	CON_TX2_RX50	CON_TX2 50Ω load status 0 – No 50Ω load is detected 1 – 50Ω load is detected
6	RO	0	Reserved	
5	RO	0	CON_TX2_COMP_MODE_EN	CON_TX2 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_TX2_COMP_MODE<4>	CON_TX2 compliance test mode state monitor • CON_TX2_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping .LFPS pulse of the adjacent channels.
3	RO	0	CON_TX2_COMP_MODE<3>	
2	RO	0	CON_TX2_COMP_MODE<2>	
1	RO	0	CON_TX2_COMP_MODE<1>	
0	RO	0	CON_TX2_COMP_MODE<0>	

Byte 44 (Monitor for CON_TX2 TX SW & DE & PE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<4>	CON_TX2 SW&DE&PE setting Monitor
3	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<3>	
2	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<2>	
1	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<1>	
0	RO	0	CON_TX2_TX_SW_DE_PE_ CTRL<0>	

Byte 45 Reserved RO: 0x00h

Byte 46 (Monitor for CON_RX2 CDR Lock Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX2_CDR_LOCKED	CON_RX2 CDR_LOCKED Monitor
4	RO	0	CON_RX2_PLL_LOCKED	CON_RX2 PLL LOCKED Monitor
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 47 (Monitor for CON_RX2 RX Auto CTLE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX2_CTLE_CAL_DONE	CON_RX2 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_RX2_CTLE_CODE<3>	CON_RX2 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_RX2_CTLE_CODE<2>	
1	RO	0	CON_RX2_CTLE_CODE<1>	
0	RO	0	CON_RX2_CTLE_CODE<0>	

Byte 48 Reserved RO: 0x00h

Byte 49 (Monitor Channel PD Status and CON_RX2 LFPS_Decoder Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	1	CON_RX2_PD#	CON_RX2 PD# status monitor
5	RO	0	Reserved	
4	RO	0	Reserved	
3	RO	0	Reserved	
2	RO	0	CON_RX2_USB_WARMRESET	CON_RX2 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 50 Reserved RO: 0x00h

Byte 51 (Monitor for CON_RX2 Operating Mode Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_RX2_HS_IDLE	CON_RX2 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_RX2_LFPS_IDLE	CON_RX2 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_RX2 DET_5Gbps	CON_RX2 input signal type 0 – LFPS signal 1 – 5Gbps high speed signal
4	RO	0	CON_RX2_HS_OP_MODE<4>	CON_RX2 channel operating mode
3	RO	0	CON_RX2_HS_OP_MODE<3>	
2	RO	0	CON_RX2_HS_OP_MODE<2>	
1	RO	0	CON_RX2_HS_OP_MODE<1>	
0	RO	0	CON_RX2_HS_OP_MODE<0>	

Byte 52 (Monitor for CON_RX2 RX Signal Status and USB Compliance Test Mode Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	CON_RX2_RX50	CON_RX2 50Ω load status 0 – No 50Ω load is detected 1 – 50Ω load is detected
6	RO	0	CON_RX2_LOW_VCM_SEL	CON_RX2 channel status 0 – The channel is in DSM/UPM mode 1 – The Channel is in SM/AM mode
5	RO	0	CON_RX2_COMP_MODE_EN	CON_RX2 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_RX2_COMP_MODE<4>	CON_RX2 compliance test mode state monitor • CON_RX2_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping. LFPS pluse of the adjacent channels.
3	RO	0	CON_RX2_COMP_MODE<3>	
2	RO	0	CON_RX2_COMP_MODE<2>	
1	RO	0	CON_RX2_COMP_MODE<1>	
0	RO	0	CON_RX2_COMP_MODE<0>	

Byte 53 (Monitor for CON_RX2 TX SW & DE & PE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_RX2_TX_SW_DE_PE_ CTRL<4>	CON_RX2 SW&DE&PE setting monitor
3	RO	0	CON_RX2_TX_SW_DE_PE_ CTRL<3>	
2	RO	0	CON_RX2_TX_SW_DE_PE_ CTRL<2>	
1	RO	0	CON_RX2_TX_SW_DE_PE_ CTRL<1>	
0	RO	0	CON_RX2_TX_SW_DE_PE_ CTRL<0>	

Byte 54 Reserved RO: 0x00h

Byte 55 (Monitor for CON_TX1 CDR Lock Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX1_CDR_LOCKED	CON_TX1 CDR_LOCKED Monitor
4	RO	0	CON_TX1_PLL_LOCKED	CON_TX1 PLL LOCKED Monitor
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 56 (Monitor for CON_TX1 RX Auto CTLE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_TX1_CTLE_CAL_DONE	CON_TX1 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_TX1_CTLE_CODE<3>	CON_TX1 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_TX1_CTLE_CODE<2>	
1	RO	0	CON_TX1_CTLE_CODE<1>	
0	RO	0	CON_TX1_CTLE_CODE<0>	

Byte 57 Reserved RO: 0x00h

Byte 58 (Monitor Channel PD Status and CON_TX1 LFPS_Decoder Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	1	CON_TX1_PD#	CON_TX1 PD# status monitor
5	RO	0	Reserved	
4	RO	0	Reserved	
3	RO	0	Reserved	
2	RO	0	CON_TX1_USB_WARMRESET	CON_TX1 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 59 Reserved RO: 0x00h

Byte 60 (Monitor for CON_TX1 Operating Mode Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	CON_TX1_HS_IDLE	CON_TX1 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_TX1_LFPS_IDLE	CON_TX1 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_TX1 DET_5Gbps	CON_TX1 input signal type 0 – LFPS signal 1 – 5Gbps high speed signal
4	RO	0	CON_TX1_HS_OP_MODE<4>	CON_TX1 channel operating mode
3	RO	0	CON_TX1_HS_OP_MODE<3>	
2	RO	0	CON_TX1_HS_OP_MODE<2>	
1	RO	0	CON_TX1_HS_OP_MODE<1>	
0	RO	0	CON_TX1_HS_OP_MODE<0>	

Byte 61 (Monitor for CON_TX1 RX Signal Status and USB Compliance Test Mode Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	CON_TX1_RX50	CON_TX1 50Ohm load status 0 – No 50Ohm load is detected. 1 – 50Ohm load is detected
6	RO	0	CON_TX1_LOW_VCM_SEL	CON_TX1 channel status 0 – The channel is in DSM/UPM mode 1 – The Channel is in SM/AM mode
5	RO	0	CON_TX1_COMP_MODE_EN	CON_TX1 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_TX1_COMP_MODE<4>	CON_TX1 compliance test mode state monitor • CON_TX1_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping. LFPS pulse of the adjacent channels.
3	RO	0	CON_TX1_COMP_MODE<3>	
2	RO	0	CON_TX1_COMP_MODE<2>	
1	RO	0	CON_TX1_COMP_MODE<1>	
0	RO	0	CON_TX1_COMP_MODE<0>	

Byte 62 (Monitor for CON_TX1 TX SW & DE & PE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_TX1_TX_SW_DE_PE_ CTRL<4>	CON_TX1 SW&DE&PE setting monitor
3	RO	0	CON_TX1_TX_SW_DE_PE_ CTRL<3>	
2	RO	0	CON_TX1_TX_SW_DE_PE_ CTRL<2>	
1	RO	0	CON_TX1_TX_SW_DE_PE_ CTRL<1>	
0	RO	0	CON_TX1_TX_SW_DE_PE_ CTRL<0>	

Byte 63 Reserved RO: 0x00h

Byte 64 (Monitor for CON_RX1 CDR Lock Status)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX1_CDR_LOCKED	CON_RX1 CDR_LOCKED Monitor
4	RO	0	CON_RX1_PLL_LOCKED	CON_RX1 PLL LOCKED Monitor
3	RO	0	Reserved	
2	RO	0	Reserved	
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 65 (Monitor for CON_RX1 RX Auto CTLE Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	CON_RX1_CTLE_CAL_DONE	CON_RX1 CTLE AUTO_CAL CAL_DONE monitor
4	RO	0	Reserved	
3	RO	0	CON_RX1_CTLE_CODE<3>	CON_RX1 CTLE_CODE<3:0> monitor CTLE_CODE<3:0> 0000 Min CTLE setting 1111 Max CTLE setting
2	RO	0	CON_RX1_CTLE_CODE<2>	
1	RO	0	CON_RX1_CTLE_CODE<1>	
0	RO	0	CON_RX1_CTLE_CODE<0>	

Byte 66 Reserved RO: 0x00h

Byte 67 (Monitor Channel PD Status and CON_RX1 LFPS_Decoder Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	Reserved	Reserved
6	RO	1	CON_RX1_PD#	CON_RX1 PD# status monitor
5	RO	0	Reserved	
4	RO	0	Reserved	
3	RO	0	Reserved	
2	RO	0	CON_RX1_USB_WARMRESET	CON_RX1 LBPM USB WarmReset decoded value
1	RO	0	Reserved	
0	RO	0	Reserved	

Byte 68 Reserved RO: 0x00h

Byte 69 (Monitor for CON_RX1 Operating Mode Setting)

Bit	Type	Power up condition	Purpose	Comment
7	RO	0	CON_RX1_HS_IDLE	CON_RX1 idle status of the HS_IDET 0 – Signal is detected 1 – No input signal is detected
6	RO	0	CON_RX1_LFPS_IDLE	CON_RX1 idle status of the LFPS_IDET 0 – LFPS Signal is detected 1 – No input signal is detected
5	RO	0	CON_RX1 DET_5Gbps	CON_RX1 input signal type 0 – LFPS signal 1 – 5Gbps high speed signal
4	RO	0	CON_RX1_HS_OP_MODE<4>	CON_RX1 channel operating mode
3	RO	0	CON_RX1_HS_OP_MODE<3>	
2	RO	0	CON_RX1_HS_OP_MODE<2>	
1	RO	0	CON_RX1_HS_OP_MODE<1>	
0	RO	0	CON_RX1_HS_OP_MODE<0>	

Byte 70 (Monitor for CON_RX1 RX Signal Status and USB Compliance Test Mode Status)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	CON_RX1_RX50	CON_RX1 50Ohm load status 0 – No 50Ohm load is detected 1 – 50Ohm load is detected
6	RO	0	CON_RX1_LOW_VCM_SEL	CON_RX1 channel status 0 – The channel is in DSM/UPM mode 1 – The Channel is in SM/AM mode
5	RO	0	CON_RX1_COMP_MODE_EN	CON_RX1 USB compliance test mode status. 0 - The lane is in the normal USB mode. 1 - The lane is in the Compliance test mode.
4	RO	0	CON_RX1_COMP_MODE<4>	CON_RX1 compliance test mode state monitor • CON_RX1_COMP_MODE<4:0> register is cycling between 0x0d and 0x16d. • The register value is advanced by the Ping. LFPS pulse of the adjacent channels.
3	RO	0	CON_RX1_COMP_MODE<3>	
2	RO	0	CON_RX1_COMP_MODE<2>	
1	RO	0	CON_RX1_COMP_MODE<1>	
0	RO	0	CON_RX1_COMP_MODE<0>	
Byte 71 (Monitor for CON_RX1 TX SW & DE & PE Setting)				
Bit	**Type**	**Power up condition**	**Purpose**	**Comment**
7	RO	0	Reserved	
6	RO	0	Reserved	
5	RO	0	Reserved	
4	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<4>	CON_RX1 SW&DE&PE setting monitor
3	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<3>	
2	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<2>	
1	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<1>	
0	RO	0	CON_RX1_TX_SW_DE_PE_CTRL<0>	
Byte 72 (DPCD Address 00100h: LINK BW SET)				
Byte 73 (DPCD Address 00101h: LANE COUNT SET)				
Byte 74 (DPCD Address 00102h: TRAINING PATTERN SET)				
Byte 75 (DPCD Address 00103h: TRAINING LANE0 SET)				
Byte 76 (DPCD Address 00104h: TRAINING LANE1 SET)				
Byte 77 (DPCD Address 00105h: TRAINING LANE2 SET)				
Byte 78 (DPCD Address 00106h: TRAINING LANE3 SET)				
Byte 79 (DPCD Address 00107h: DOWNSPREAD CTRL)				
Byte 80 (DPCD Address 0010Bh: LINK_QUAL_LANE0_SET)				
Byte 81 (DPCD Address 0010Ch: LINK_QUAL_LANE1_SET)				

Byte 82 (DPCD Address 0010Dh: LINK_QUAL_LANE2_SET)
Byte 83 (DPCD Address 0010Dh: LINK_QUAL_LANE3_SET)
Byte 84 (DPCD Address 00201h: Device Service IRQ Vector)
Byte 85 (DPCD Address 00202h: Lane0/1 Status)
Byte 86 (DPCD Address 00203h: Lane2/3 Status)
Byte 87 (DPCD Address 00204h:Lane Align Status Updated)
Byte 88 (DPCD Address 00205h: SINK_STATUS)
Byte 89 (DPCD Address 00206h:Adjust Request Lane 0/1)
Byte 90 (DPCD Address 00207h:Adjust Request Lane 2/3)
Byte 91 (DPCD Address 00218h:Test Request)
Byte 92 (DPCD Address 00219h: Test Link Rate)
Byte 93 (DPCD Address 00220h: Test Lane Count)
Byte 94 (DPCD Address 00260h: Test Response)
Byte 95 (DPCD Address 00600h: Set Power and Set DP Power Voltage)
Byte 96-Byte 127 Reserved RW register

4.6.1 Each Lane Configuration Setting

Below is showing the configuration of each lane after decoded from the I2C OP_MODE<3:0>

Table 4-1. The channel configuration against the OP_MODE<3:0>

OP_ MODE<3:0>	CON_TX2	CON_ RX2	CON_TX1	CON_ RX1	AUXP	AUXN	IN_HPD/ AUX CMD	Mode
0000	X	X	X	X	X	X	X	Safe Sate
0001	X	X	X	X	X	X	X	Safe Sate
0010	AP_RX2/ DP1	AP_TX2/ DP0	AP_RX1/ DP2	AP_TX1/ DP3	SBU1	SBU2	All CON response	4 lane DP1.4 (AP to CON) + AUX
0011	AP_RX2/ DP2	AP_TX2/ DP3	AP_RX1/ DP1	AP_TX1/ DP0	SBU2	SBU1	All CON response	4 lane DP1.4 (AP to CON) + AUX (flipped)
0100	X	X	AP_RX1	AP_TX1	X	X	X	1 lane USB3.x (AP1 Active)
0101	AP_RX2	AP_TX2	X	X	X	X	X	1 lane USB3.x (AP2 Active) flipped
0110	AP_RX2/ DP1	AP_TX2/ DP0	AP_RX1 (USB3)	AP_TX1 (USB3)	SBU1	SBU2	CON2 response only	USB3 (AP1) + 2 lane DP1.4 (AP2, AP to CON) + AUX
0111	AP_RX2 (USB3)	AP_TX2 (USB3)	AP_RX1/ DP1	AP_TX1/ DP0	SBU2	SBU1	CON1 response only	USB3 (AP2) + 2 lane DP1.4 (AP1, AP to CON) + (AUX flipped)
1000	Reserved							Reserved
1001								
1010								
1011								
1100								
1101								
1110								
1111	AP_RX2	AP_TX2	AP_RX1	AP_TX1	X	X	X	2 lane USB3.x (Supports two Type-A USB lane)

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage....................................-0.3V to 2.0V
I/O Voltage (AP_RX, AP_TX, CON_RX, CON_TX, CAP_CON1, CAP_CON2)....................................-0.3V to 1.15V
I/O Voltage (AUXP/N, AUXSBU1/2, SDA, SCL)....................................-0.3V to 3.8V
I/O Voltage (EN, A0)....................................-0.3V to 2.0V
Storage Temperature....................................–65°C to +150°C
Max junction temperature....................................125°C
ESD HBM....................................±2kV
ESD CDM....................................±500V

Note:
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect inoperability and degradation of device reliability and performance.

5.2 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max	Units
V_{DD}	VDD Supply Voltage		1.71	1.8	1.89	V
V_{DD_I2C}	VDD I2C Supply Voltage				3.6	V
V_{NOISE}	Supply Noise up to 50 MHz(1)			100		mVpp
T_A	Ambient Temperature	Commercial range	0		70	ºC
		Industrial range	-40		85	
CAP_CON1	External VDD1V_CON1/2 decoupling capacitors with max ±20% tolerance				15	nF
CAP_CON2						

Notes:
(1) Allowed supply noise (mVpp sign wave) under typical condition
(2) Industrial temperature -40 to +85 ºC can be guaranteed by design. Commercial temperature 0 to +70 ºC is supported by the production-tested.

5.3 Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{D0_DP}	Active mode current in DP mode	1-lane DP, EN=1, IN_HPD=1, VDD=1.8V		90	105	mA
		2-lane DP, EN=1, IN_HPD=1, VDD=1.8V		180	210	mA
		4-lane DP, EN=1, IN_HPD=1, VDD=1.8V		360	420	mA
I_{SB_DP}	DP Standby current	IN_HPD=0, EN=1, VDD=1.8V		650	1500	µA
I_{D3_DP}	DP D3 mode current	IN_HPD=1, EN=1, D3 mode, VDD=1.8V		650	1500	µA
I_{PD}	Typical Pin Power Down current	EN = 0, VDD=1.8V		25	150	µA
I_{SS}	Safe Sate Current	EN=1 OP_MODE<3:0>=0x0000b/0x0001b		400	800	µA
I_{U0}	Current in USB U0 mode, VDD=1.8V	EN=1, USB U0 mode		130	150	mA
I_{U1}	Current in USB U1 mode, VDD=1.8V	EN=1, USB U1 mode		16	20	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$I_{U2/U3}$	Current in USB U2/U3 modes. VDD=1.8V	EN=1, USB U2/U3 mode		700	1800	µA
I_{RXDET}	Current in USB RXDET mode, VDD=1.8V	EN=1, USB RXDET mode		650	1700	µA

5.4 AC/DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
LVCMOS I/O DC Specifications						
V_{IH}	DC input logic High		V_{DD}*0.65			V
V_{IL}	DC input logic Low				V_{DD}*0.35	V
I_{IH}	Input High current				25	uA
I_{IL}	Input Low current		-25			uA

5.5 DisplayPort Electrical Specification

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
DisplayPort Main-Link Transmitter System Parameters						
fHBR3	Frequency for high bit rate 3	Frequency high limit = +300ppm Frequency low limit = -5300ppm	8.05707	8.1	8.10243	Gbps
fHBR2	Frequency for high bit rate 2		5.37138	5.4	5.40162	Gbps
fHBR	Frequency for high bit rate		2.68569	2.7	2.70081	Gbps
fRBR	Frequency for reduced bit rate		1.611414	1.62	1.620486	Gbps
Down_Spread _Amplitude	Link clock down-spreading	Range: 0 to 0.5% when down-spread enabled	0		0.5	%
Down_Spread _Frequency	Link clock down-spreading frequency	Range: 30 to 33kHz when down-spread enabled	30		33	kHz
CTX	AC-coupling Capacitor	All DP Main-Link lanes as well as AUX CH must be AC-coupled. AC-coupling capacitors must be placed on the transmitter side. Placement of AC-coupling capacitors on the receiver side is optional.	75		265	nF
DisplayPort Main-Link Transmitter TP2 Parameters						
VTX-OUTPUT-RATIO_RBR_HBR	Ratio of Output Voltage Level 1/ Level 0	Measured on non-transition bits at Pre-emphasis level 0 setting.	0.8		6.0	dB
	Ratio of Output Voltage Level 2/ Level 1		0.1		5.1	dB
	Ratio of Output Voltage Level 3/ Level 2		0.8		6.0	dB
VTX-PREEM-POFF	Maximum Pre-emphasis when disabled	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.			0.25	dB

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
VTX-PREEMP -DELTA	Delta of Pre-emphasis Level 1 vs. Level 0	Applies to all valid voltage settings. Support for Pre-emphasis Level 3 is optional.	2			dB
	Delta of Pre-emphasis Level 2 vs. Level 1		1.6			dB
	Delta of Pre-emphasis Level 3 vs. Level 2		1.6			dB
VTX-DIFF_ RE-DUCTION	Non-transition reduction Output Voltage Level 2	VTX_DIFF at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than VTX_DIFF at the zero nominal pre-emphasis level.			3	dB
	Non-transition reduction Output Voltage Level 1				3	dB
	Non-transition reduction Output Voltage Level 0				1.4	dB
VTX-DIFFp-p-MAX	Maximum Output Voltage Level	For all Output Level and Pre-emphasis combinations.			1.38	Vppd
tTX-SKEW-IN-TER_PAIR	Lane-to-Lane Output Skew	Applies to transmitters capable of 2- and 4-lane operation. Applies to all pairwise combinations of supported lanes for all data rates.			1250	ps
tTX-SKEW-IN-TRA_PAIR	Lane Intra-pair Output Skew	Applies to all supported lanes.			30	ps
TX TP3_EQ (Compliance Cable Model with HBR2 Reference Receiver Equalization)						
tTX-TJ_TPS4_ HBR3	Maximum TX Total Jitter	For HBR3. Measured at 1E-9 BER.			0.65	UI
tTX¬NonI-SI_ TPS4_HBR3	Maximum TX Non-ISI Jitter				0.56	UI
tTX-TJ_ CP2520_HBR2	Maximum TX Total Jitter	For HBR2. Measured at 1E-9 BER using the CP2520 PHY Layer Compliance EYE pattern.			0.62	UI
tTX-DJ_ CP2520_HBR2	Maximum TX Deterministic Jitter				0.49	UI
tTX-TJ_D10.2_ HBR2	Maximum TX Total Jitter	For HBR2. Measured at 1E-9 BER using the D10.2 Compliance pattern.			0.40	UI
tTX-DJ_D10.2_ HBR2	Maximum TX Deterministic Jitter				0.27	UI
tTX-RJ_D10.2_ HBR2	Maximum TX Random Jitter				0.13	UI
VTX-DIFFp-p_ HBR3	TX Differential Peak-to-Peak EYE Voltage	For HBR3. Measured at 1E-9 BER using TPS4.	75			mVppd
VTX-DIFFp-p_ HBR2	TX Differential Peak-to-Peak EYE Voltage	For HBR2. Measured at 1E-9 BER using the CP2520 PHY Layer Compliance EYE pattern.	90			mVppd

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
tTX-DIFFp-p_ RANGE_ HBR2_HBR	TX Differential Peak-to-Peak EYE Voltage Measurement Range	For HBR2 and HBR3. Uses 0.5 Cumulative Distribution Function (CDF) of the jitter distribution as the 0UI reference point. TX Differential Peakto-Peak EYE Voltage requirement can be met anywhere within this UI range.	0.375		0.625	UI
DisplayPort Main-Link Receiver System Parameters						
fHBR3	Frequency for high bit rate 3	Frequency high limit = +300ppm Frequency low limit = -5300ppm DP link RX does not require local crystal for link clock generation.	8.05707	8.1	8.10243	Gbps
fHBR2	Frequency for high bit rate 2		5.37138	5.4	5.40162	Gbps
fHBR	Frequency for high bit rate		2.68569	2.7	2.70081	Gbps
fRBR	Frequency for reduced bit rate		1.611414	1.62	1.620486	Gbps
Down_Spread _Am-plitude	Link clock down-spreading	Up to 0.5% down-spread support is required. Modulation frequency range of 30 to 33kHz must be supported.	0		0.5	%
TP3 (RX External Connector)						
tRX-EYE_ CONN	Minimum Receiver EYE Width at RX-side connector pins		0.25			UI
tRX-SKEW-INTRA_PAIR HBR3	Lane Intra-pair Skew Tolerance				50	ps
tRX-SKEW-INTRA_PAIR HBR2	Lane Intra-pair Skew Tolerance				50	ps
tRX-SKEW-INTRA_PAIR HBR	Lane Intra-pair Skew Tolerance				60	ps
tRX-SKEW-INTRA_PAIR RBR					260	ps
fRX-TRACK-INGBW_HBR3	Jitter Closed-Loop Tracking Bandwidth	Minimum CDR closed-loop tracking bandwidth at the receiver when the input is an 8b/10b pattern, such as a TPS4.	15			MHz
fRX-TRACK-INGBW_HBR2			10			MHz
fRX-TRACK-INGBW_HBR			10			MHz
fRX-TRACK-INGBW_RBR			5.4			MHz

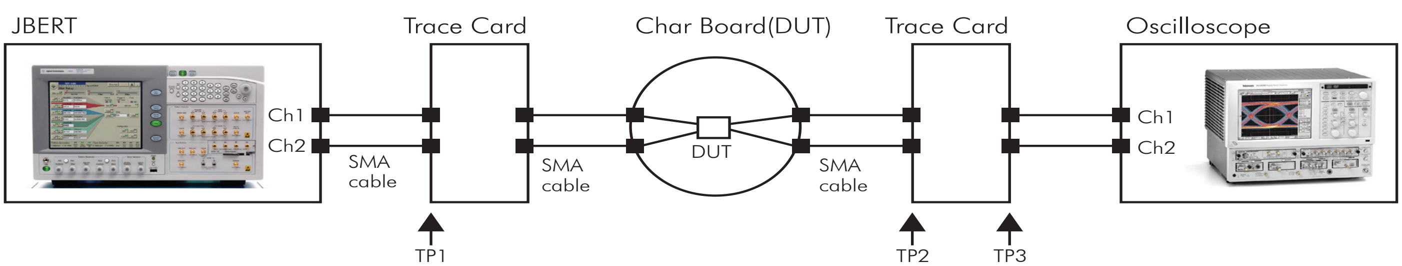
Symbol	Parameter	Condition	Min.	Typ.	Max	Units
RX TP3_EQ (RX External Connector after Reference Receiver Equalizer)						
tRX-TJ_TPS4_HBR3	Minimum Receiver EYE Width		0.35			UI
VRX-DIFFp-p_HBR3	RX Differential Peak-to-Peak EYE Voltage		75			mVppd
tRX-NonISI_TPS4_HBR3	Minimum Receiver Non-ISI Jitter		0.56			UI
tTX-RJ_TPS4_HBR3	Random Jitter Contribution from TX		0.16			UI
tRX-TJ_CP2520_HBR2	Minimum Receiver EYE Width		0.38			UI
VRX-DIFFp-p_HBR2	RX Differential Peak-to-Peak EYE Voltage		70			mVppd
tRX-DIF-Fp-p_RANGE_HBR2_HBR3	RX Differential Peak-to-Peak EYE Voltage Measurement Range		0.375		0.625	UI
DisplayPort AUX Channel DC and AC Specification						
Ron	The AUX MUX ON resistance	When the AUXSBU1/2 is biased to VDD3P3 or GND			10	Ω
Roff	The AUX MUX OFF resistance		280			kΩ
	Threshold of the AUX listener		100		220	mVppd
F3db	MUX 3dB bandwidth				100	MHz
DisplayPort AUX Channel Electrical Specifications						
UIMAN	Manchester transaction unit interval	Results in the bit rate of 1Mbps including the overhead of Manchester-II coding.	0.4		0.6	us
Pre-charge Pulses	Number of pre-charge pulses	Each pulse is a 0 in Manchester-II code.	10		16	
VAUX-DIF-Fp-p_TX	AUX peak-to-peak voltage at AUXP/N pins	VAUX-DIFFp-p = 2 * |VAUXP - VAUXN|	0.27		1.38	Vppd
VAUX-DC-CM	AUX DC common mode voltage	Common mode voltage is equal to Vbias_TX (or Vbias_RX) voltage.	0		2.0	V
IAUX_SHORT	AUX short circuit current limit	Total drive current of the transmitter when it is shorted to its ground.			90	mA
CAUX	AUX AC-coupling capacitor	The AUX CH AC-coupling capacitor placed on both the DP upstream and downstream devices.	75		200	nF

5.6 USB Electrical Specification

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
USB Differential Input						
UI	Unit Interval	Gen 1 5Gbps	199.94 200.34		200.06 200.46	ps
CRXPARA-SITIC	The parasitic capacitor for RX				1.0	pF
RRX-DIFF-DC	DC Differential Input Impedance		72		120	Ω
RRX-SINGLE_DC	DC single ended input impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max	18		30	Ω
ZRX-HIZ-DC-PD	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
CAC_COU-PLING	AC coupling capacitance		75		265	nF
VRX-CM-DC_CONN	Instantaneous DC common mode voltage coupled from the far-end Tx	Apply to all link states and during power-on, and power-off. (min1, max) is observed at receiver side of the connector when Rx termination is equivalent of 200KΩ, and (min2, max) when Rx termination is 50Ω.	-0.5 (min1) -0.3 (min2)		1.0	V
VRX-CM-AC-P	Common mode peak voltage	AC up to 5GHz			150	mVpeak
VRX-CM-DC-Active-Idle-Delta-P	Common mode peak voltage[1]	Between U0 and U1. AC up to 5GHz			200	mVpeak
USB Differential Output						
UI	Unit Interval	Gen 1 5Gbps	199.94 200.34		200.06 200.46	ps
VTX-DIFF-PP	Output differential p-p voltage swing	2*|VTX-D+-VTX-D-|	0.8		1.2	Vppd
RTX-DIFF-DC	DC Differential TX Impedance		72		120	Ω
VTX-RCV-DET	The amount of voltage change allowed during RxDet				600	mV
Cac_coupling	AC coupling capacitance		75		265	nF
TTJ_TP3_5Gbps	Total Jitter with pattern CP0, 5Gbps	Measure over 1E6 consecutive UI and extrapolated to BER=1E-12, Measure at TP3 with Compliance RX EQ function.			0.66	UI

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
TRJ_ TP3_5Gbps	Random Jitter with pattern CP1, 2.5GHz	Measure over 1E6 consecutive UI and extrapolated to BER=1E-12. The RJ is calculated as 14.069 x RMS random jitter for BER=1E-12. Measure at TP3.			0.43	UI
Veyeh_ TP3_5Gbps	Eye height for the CP9, 5Gbps	Measure over 1E6 consecutive UI and extrapolated to BER=1E-12. Measure at TP3 with Compliance RX EQ. Eye height measures the min opening over the range from the center of the eye +/- 0.05UI.	100		1200	mVppd
CTXPARASITIC	The parasitic capacitor for TX				1.1	pF
RTX-DC-CM	Common mode DC output Impedance		18		30	Ω
VTX-DC-CM	The instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors. min1 is measured with a 200KΩ receiver load, and min2 is measured with a 50Ω receiver load.	-0.5V (min1) -0.3V (min2)		1.0	V
VTx-CM-IDLE-DELTA	Transmitter idle common-mode voltage change	The maximum allowed instantaneous common-mode voltage at TP2 while the transmitter is in U2 or U3 and not actively transmitting LFPS. Note that this is an absolute voltage spec referenced to the receive-side termination ground but serves the purpose of limiting the magnitude and/or slew rate of Tx common mode changes.	-300		600	mV
VTX-C	Common-Mode Voltage	|VTX-D++VTX-D-|/2	0		1.15	V
VTX-CM-AC-PP-Active	Active mode TX AC common mode voltage	VTX-D++VTX-D- for both time and amplitude			100	mVpp
VTX-CM-DC-Ac-tive_ Idle-Delta	Common mode delta voltage |Avguo(|VTEX-D+ + VTX-D-|)/2-Avgu1(|VTX-D+ + VTX-D-|)/2|	Between U0 to U1			200	mVpeak

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
VTX-Idle-Diff-AC-pp	Idle mode AC common mode delta voltage|VTX-D+-VTX-D-|	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals .			10	mVppd
VTX-Idle-Diff-DC	Idle mode DC common mode delta voltage|VTX-D+-VTX-D-|	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.			10	mV
Signal and Frequency Detectors						
VTH_UPM	Unplug mode detector threshold	Threshold of LFPS when the input impedance of the retimer is 75kΩ to GND only. Used in the unplug mode.	200		600	mVppd
VTH_DSM	Deep slumber mode detector threshold	LFPS signal threshold in Deep slumber mode	200		600	mVppd
VTH_AM	Active mode detector threshold	Signal threshold in Active and slumber mode	50		100	mVppd
FTH	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz
TON_UPM	Turn on of unplug mode	TX pin to RX pin latency when input signal is LFPS			3	ms
TON-DSM	Turn on of deep slumber mode				5	us
TON_SM	Turn on of slumber mode				20	ns



1) Trace card before the DUT is designed to emulate the FR4 trace.
2) All jitter is measured at at BER=1E-9/BER=1E-12 for the DP/USB applications respectively.
3) Trace card after the DUT is designed to emulate the Compliance Cable Model.
4) VDD = 1.8V, RT = 50Ω

Figure 5-1 AC Electrical Parameter Test Setup

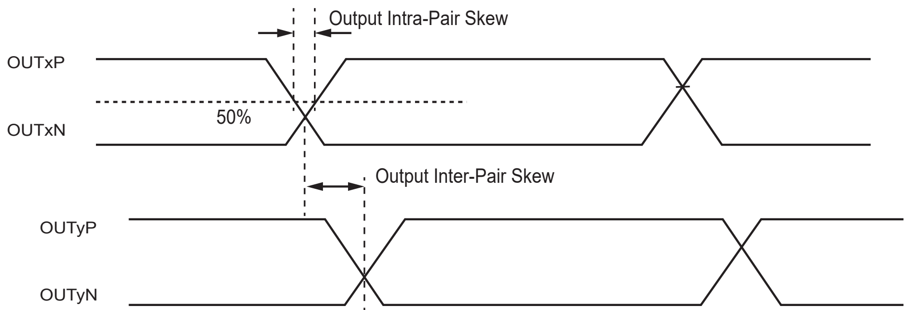


Figure 5-2 Intra and Inter-pair Differential Skew Definition

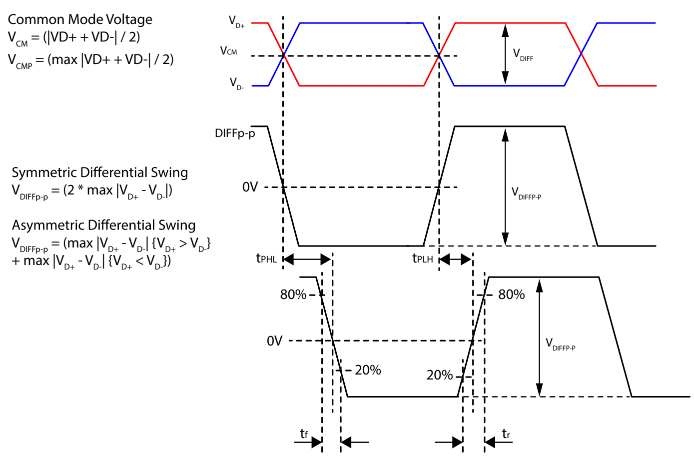


Figure 5-3 Definition of Differential voltage (VDIFF) and Differential Voltage Peak to peak (VDIFFPP)

5.7 I2C Interface Electrical Specification

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IL}	DC input logic LOW		-0.5		0.4	V
V_{IH}	DC input logic HIGH		1.2		V_{DD}	V
V_{OL1}	DC output logic LOW voltage	(open-drain or open-collector) at 3 mA sink current;	0		0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	20			mA
		V_{OL} = 0.6V	6			mA
I_i	Input current each I/O pin		-10		10	uA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	Bus Operation Frequency				1000	KHz
t_{BUF}	Bus Free Time Between Stop and Start condition		1.3			us
$t_{HD:STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$t_{SU:STA}$	Repeated start condition setup time		0.26			us
$t_{SU:STO}$	Stop condition setup time		0.26			us
$t_{HD:DAT}$	Data hold time		0			ns
$t_{SU:DAT}$	Data setup time		50			ns
t_{LOW}	Clock Low period		0.5			us
t_{HIGH}	Clock High period		0.26		50	us
t_F	Clock/Data fall time				120	ns
t_R	Clock/Data rise time				120	ns

Notes:
(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) VIL = 0.4V and VIH = 1.2V because the silicon needs to support both SCL/SDA with 1.8V/3.3V signaling level.

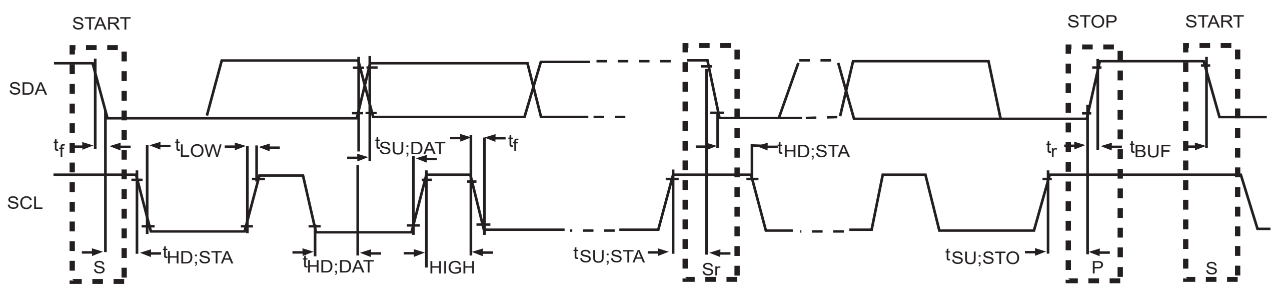


Figure 5-4 Definition of Timing on the I2C-Bus

6. Application

Note: Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 PI2DPT821 Reference Schematics

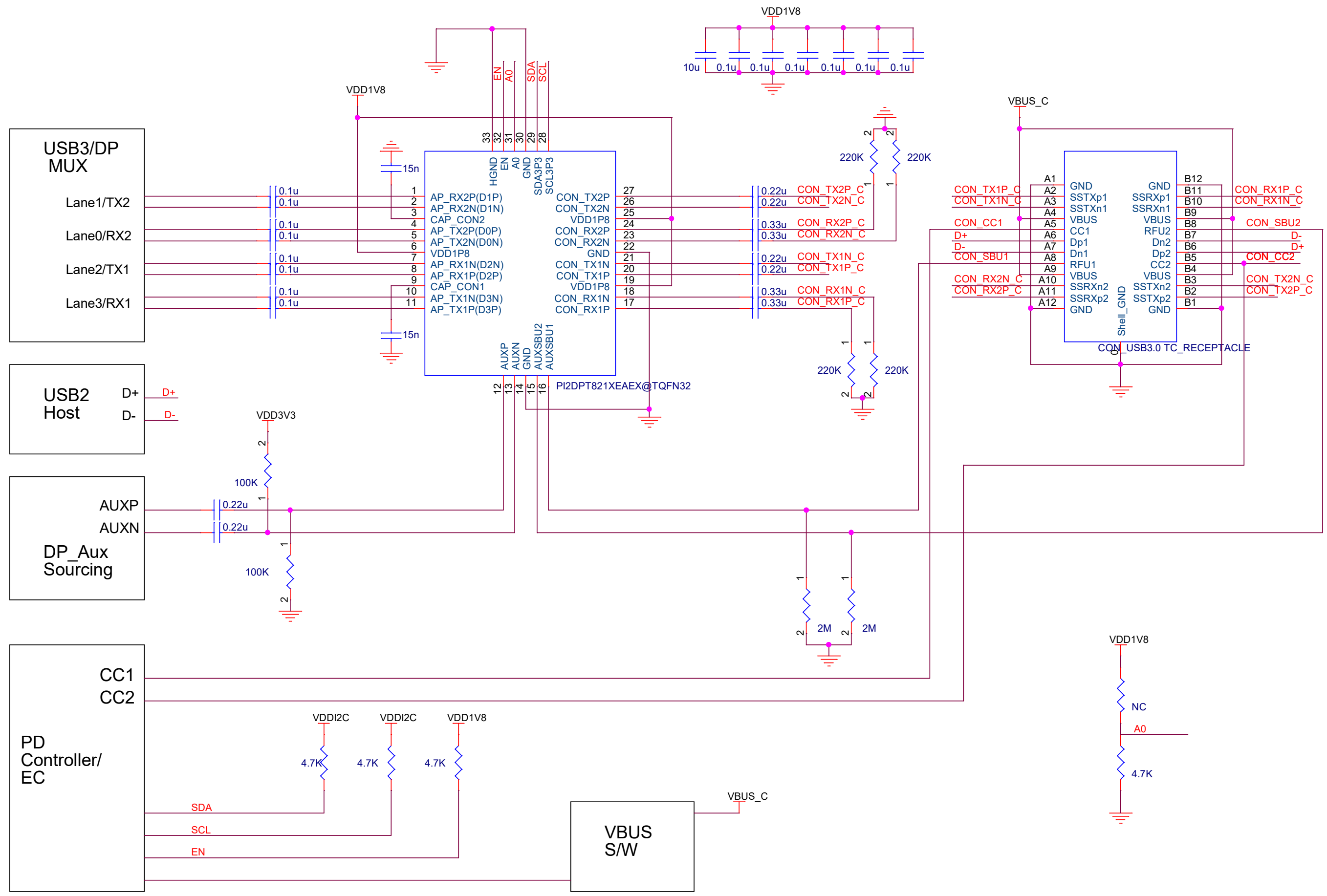


Figure 6-1 PI2DPT821 Reference Schematic

6.2 PCB Layout Guideline

6.2.1 General Power and Ground Guideline

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

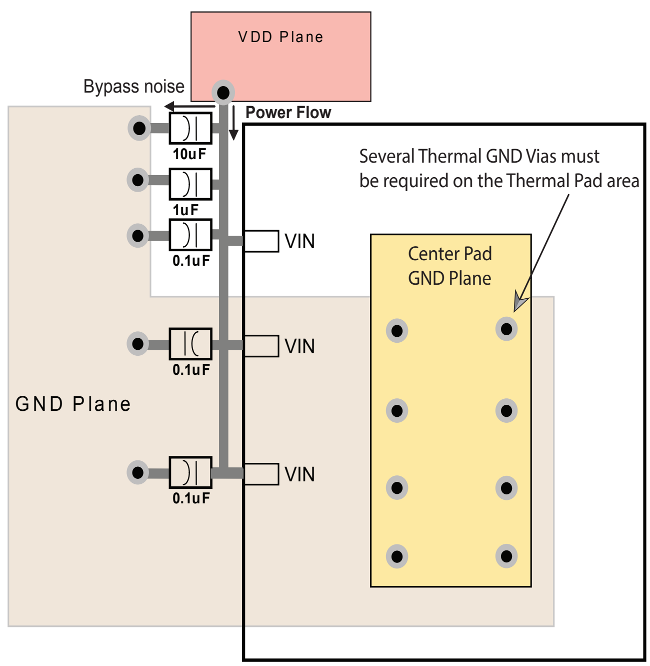


Figure 6-2 Decoupling Capacitor Placement Diagram

6.2.2 High-speed Signal Routing Guideline

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

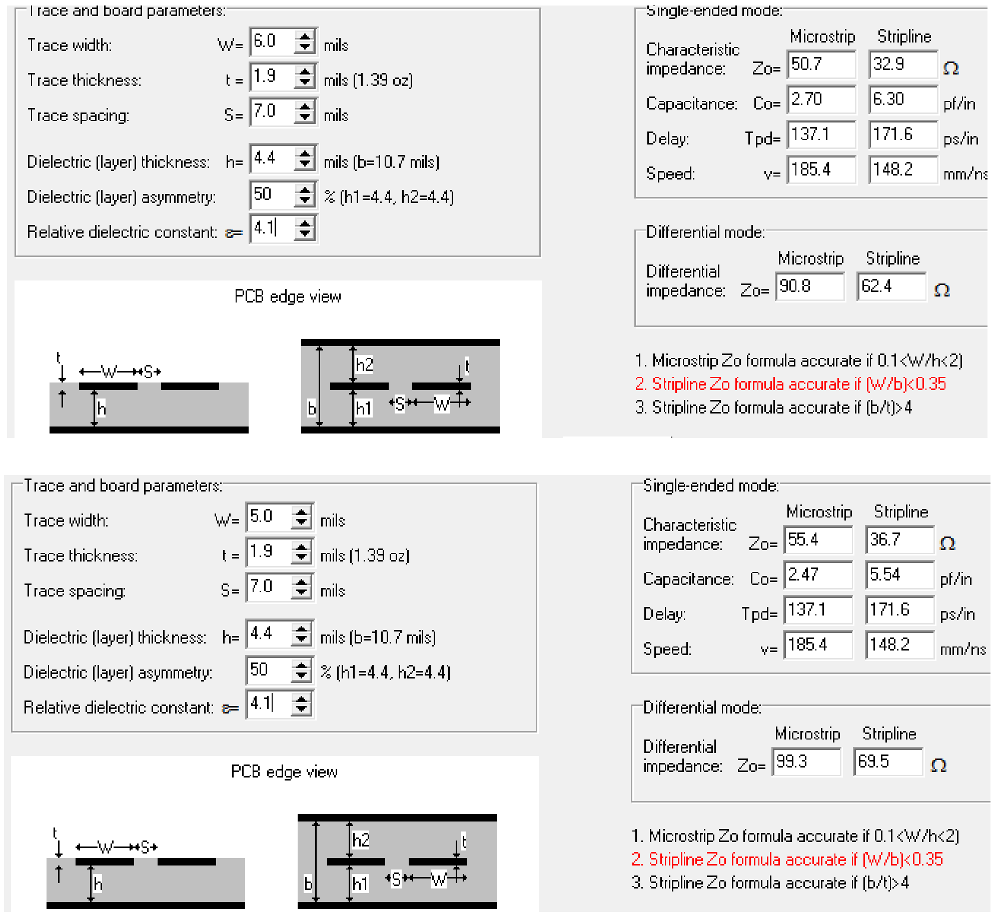


Figure 6-3 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

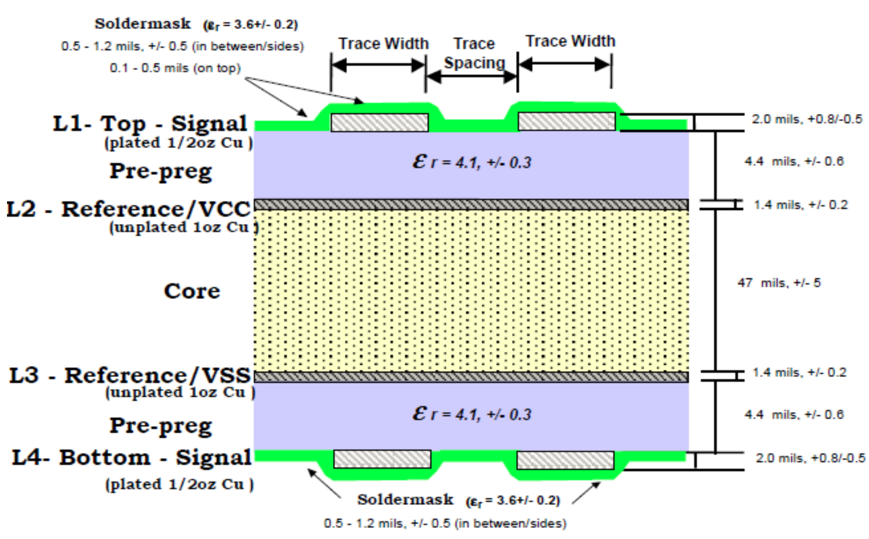


Figure 6-4 4-Layer PCB Stack-up Example

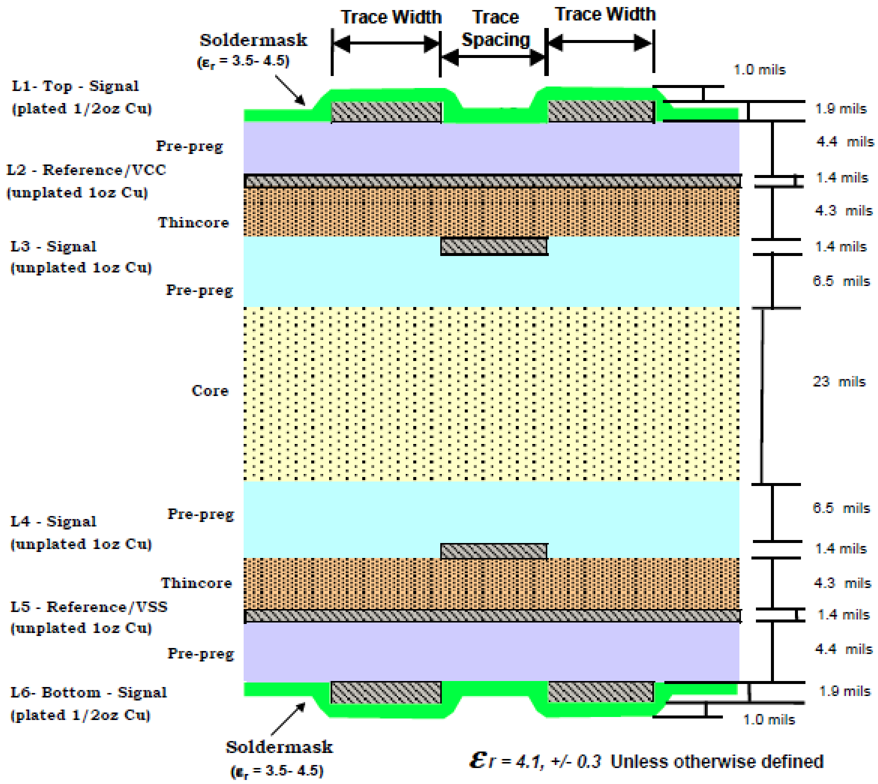


Figure 6-5 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

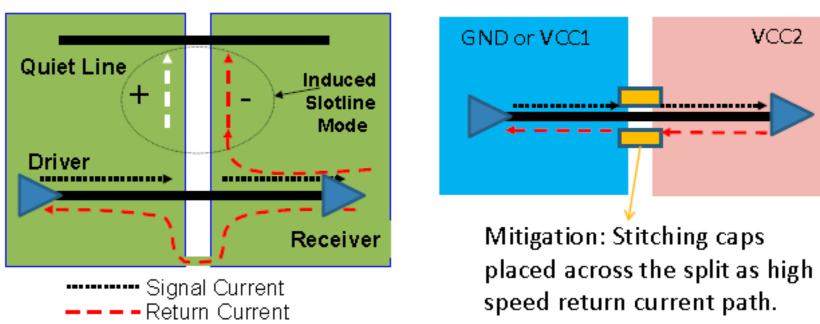


Figure 6-6 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

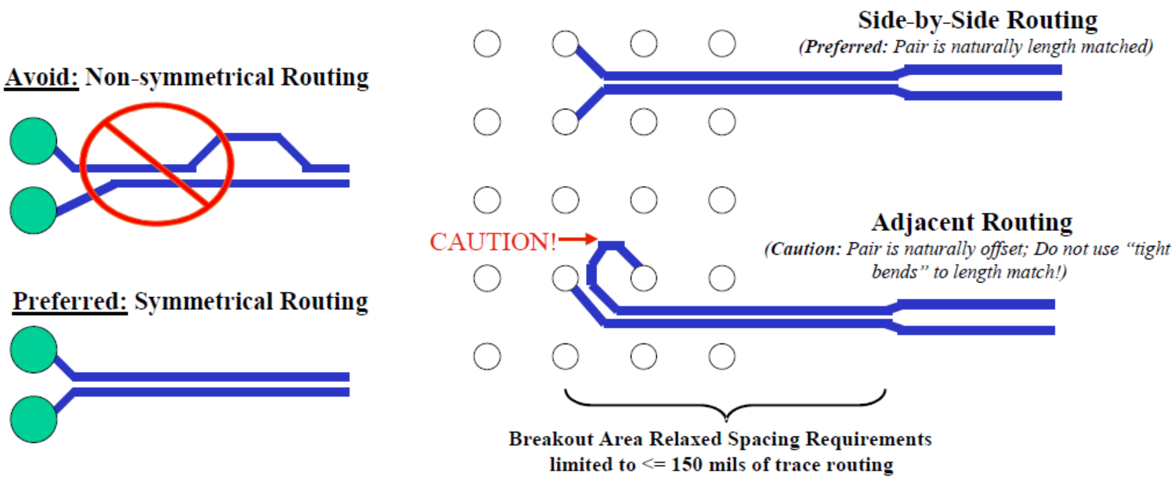


Figure 6-7 Layout Guidance of Matched Differential Pair

- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the spacing between the Trace and Reference plane.

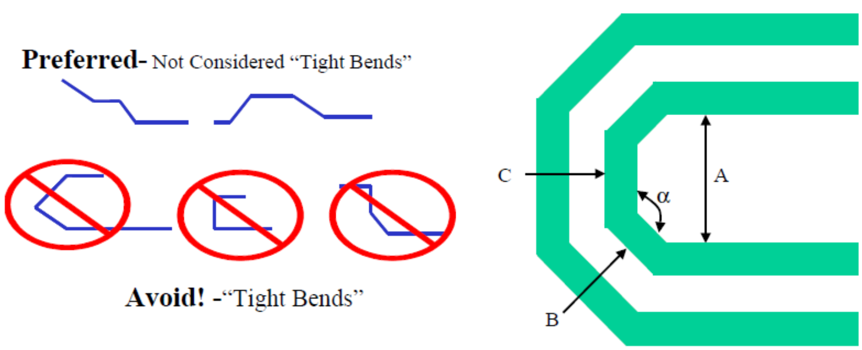


Figure 6-8 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

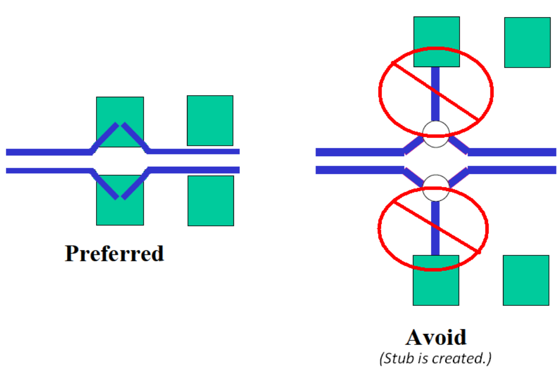


Figure 6-9 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

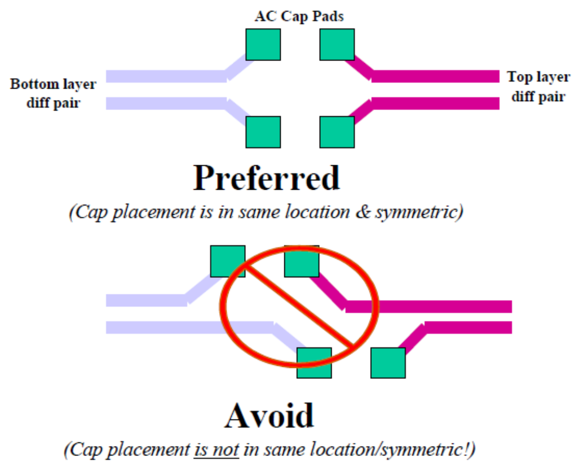


Figure 6-10 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

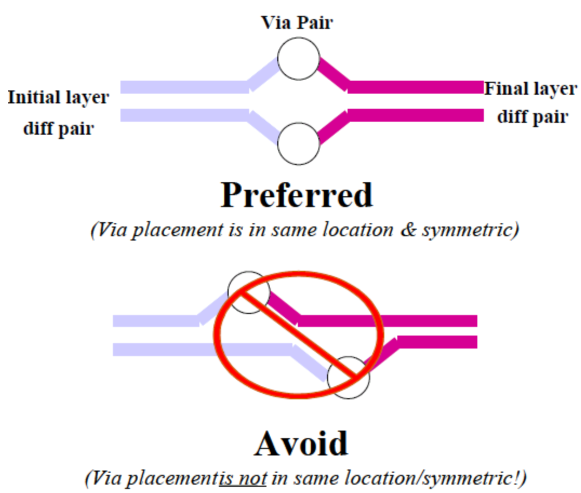


Figure 6-11 Layout Guidance of Stitching Via

6.2.3 PCB Crosstalk Minimization Recommendation

- Breakout Tx and Rx I/O on different PCB layers.
- Non-interleaved routing. Eliminates a key source of near end crosstalk.
- Inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the spacing between the Trace and Reference plane.
- Places requirements on Tx & Rx I/O placement as shown below.

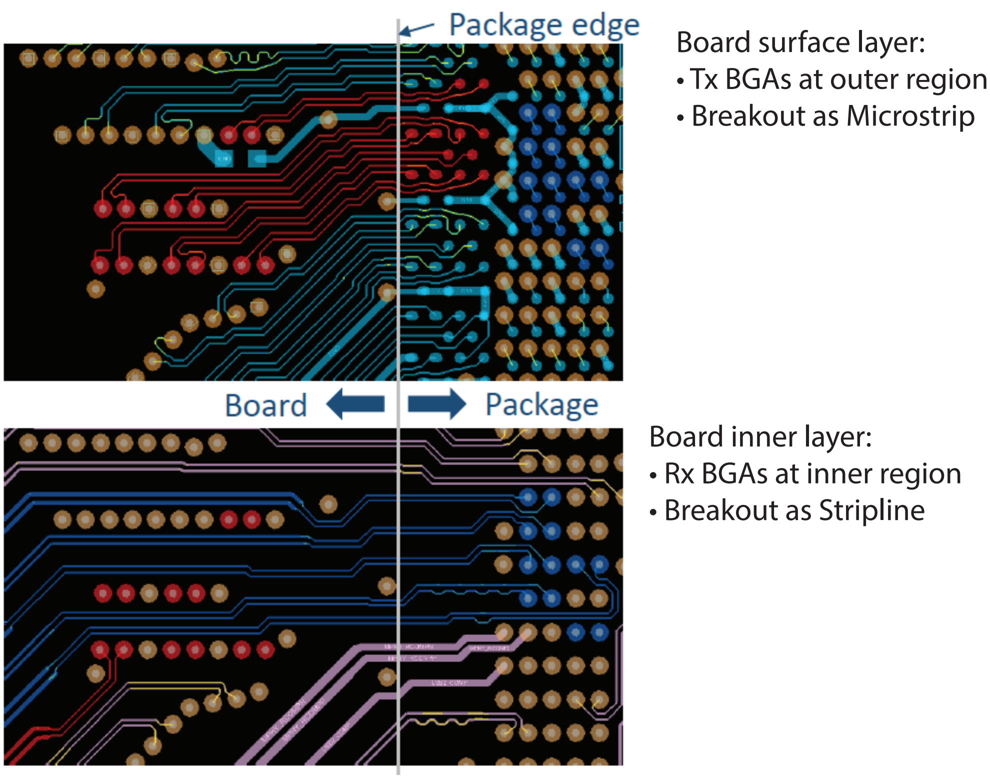
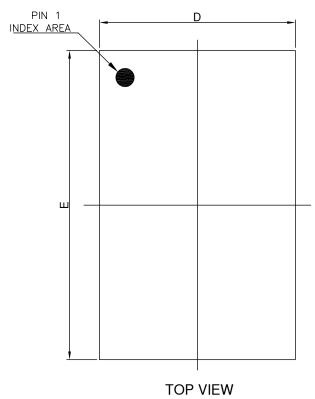
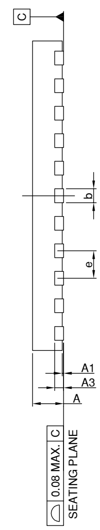


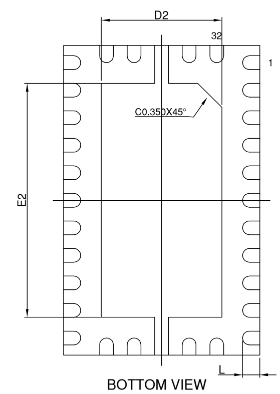
Figure 6-12 Breakout Tx and Rx I/O on Different PCB Layers

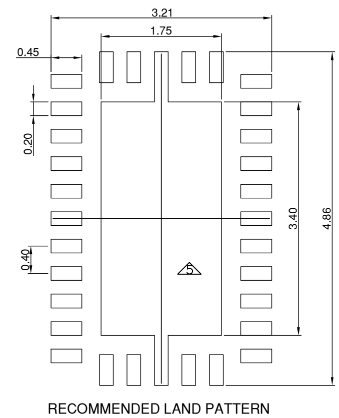
7. Mechanical/Packaging Information

7.1 Mechanical Outline









SYMBOLS	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3	0.127 REF.		
b	0.15	0.20	0.25
D	2.75	2.85	2.95
E	4.40	4.50	4.60
e	0.40 BSC		
L	0.20	0.25	0.30
D2	1.70	1.75	1.80
E2	3.35	3.40	3.45

NOTE :
1. **ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES**
2. **COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS**
3. **REFER JEDEC MO-288**
4. **RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY**
5. **THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)**

DIODES INCORPORATED PERICOM A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY

DATE: 01/14/22

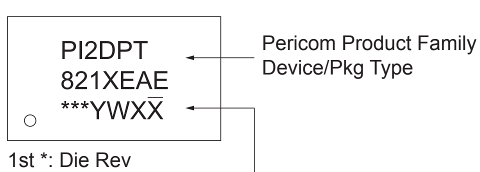
DESCRIPTION: 32-contact, X1-QFN2845-32

PACKAGE CODE: XEA (XEA32)

DOCUMENT CONTROL #: PD-2259 **REVISION:** B

22-1546

Figure 7-1 Package Mechanical Dimension



1st *: Die Rev
**: Option Code
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Bar above 2nd “X” means Cu wire
Note: Date Code per MA-1251

Figure 7-2 Part Marking

7.2 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

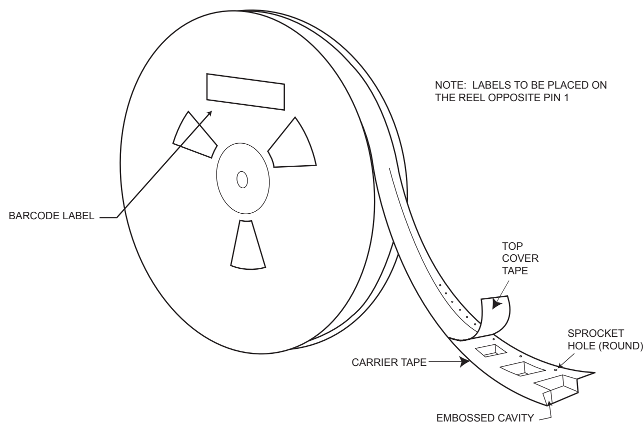


Figure 7-3 Tape & Reel Label Information

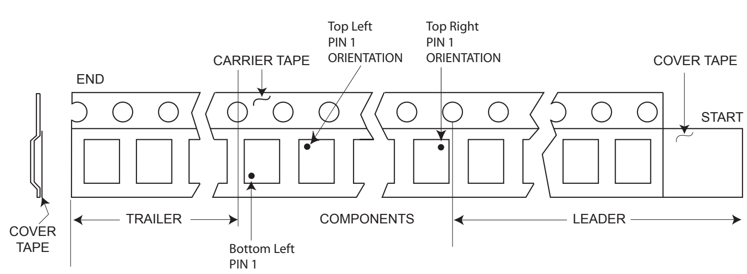


Figure 7-4 Tape Leader and Trailer Pin 1 Orientations

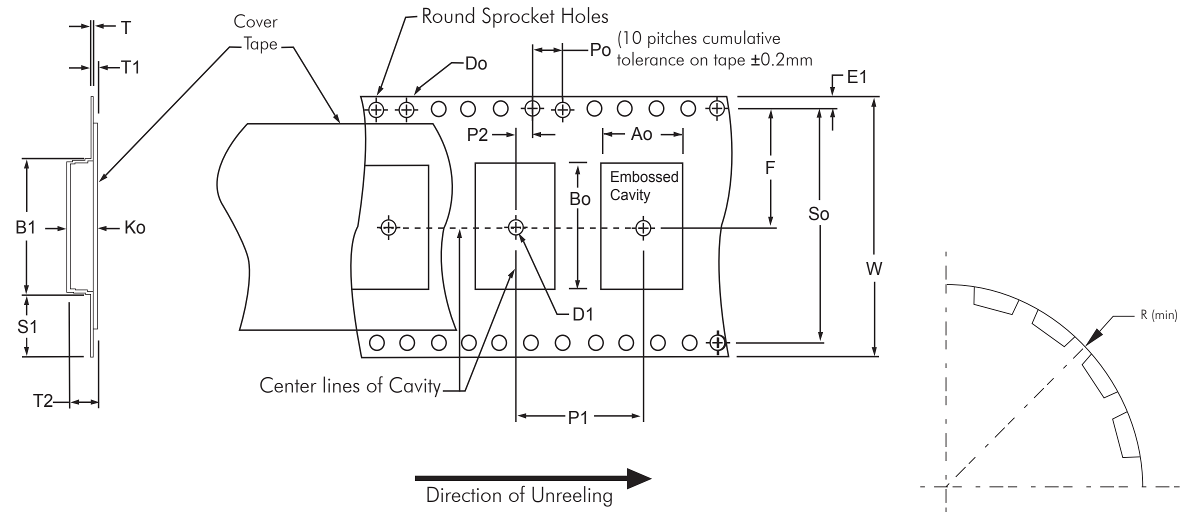


Figure 7-5 Standard Embossed Carrier Tape Dimensions

Table 7-1. Constant Dimensions

Tape Size	D_0	D_1 (Min)	E_1	P_0	P_2	R (See Note 2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

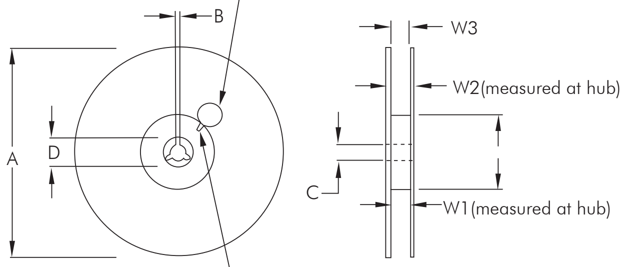


Table 7-3. Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W_1	W_2(Max)	W_3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

8. Important Notice

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

www.diodes.com