12-Bit Low Power SAR ADC

NCD98010, NCD98011

The NCD98010 (unsigned output) and the NCD98011 (signed output) ADC products provide an extremely low power solution for analog to digital conversion applications using a capacitor-based successive-approximation architecture. Optimized for low power and speed, the NCD98010/1 can achieve a sample rate of 2 MSPS while consuming less than 1 mW of power. The device also features a large input voltage range of 1.65 V to 3.3 V for various applications for both analog and digital supplies. The SPI-compatible interface provides a straight-forward data-acquisition method.

Features
- Nanowatt Power Consumption
- Fully Differential Input
- 2–MSPS Throughput
- Small Package Size
- Pre-Calibrated
- SPI Interface
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Low–Power Data Acquisition
- Battery–powered Equipment
- Level Sensors
- Ultrasonic Flow Meters
- Motor Controls
- Wearable Fitness
- Portable Medical Equipment
- Glucose Meters

![Figure 1. Block Diagram](image-url)
PIN DESCRIPTION

<table>
<thead>
<tr>
<th>X2QFN Pin No.</th>
<th>SSOP Pin No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>CSN</td>
<td>Chip select (active low)</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>OUT</td>
<td>Data Output (serialized)</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>CLK</td>
<td>Clock</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>VDD</td>
<td>Digital I/O supply voltage</td>
</tr>
<tr>
<td>5</td>
<td>8</td>
<td>GND</td>
<td>Common ground for all pins</td>
</tr>
<tr>
<td>6</td>
<td>7</td>
<td>VCC</td>
<td>Analog supply and ADC reference voltage</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>V_{INP}</td>
<td>Analog input, positive signal</td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td>V_{INN}</td>
<td>Analog input, negative signal</td>
</tr>
</tbody>
</table>

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage Range</td>
<td>V_{CC}</td>
<td>−0.3 to 3.63</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage Range</td>
<td>V_{DD}</td>
<td>−0.3 to 3.63</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>V_{INP}</td>
<td>−0.3 to 3.63</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>V_{INN}</td>
<td>−0.3 to 3.63</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>V_{OUT}</td>
<td>−0.3 to 3.63</td>
<td>V</td>
</tr>
<tr>
<td>CSN Input Voltage Range</td>
<td>V_{EN}</td>
<td>−0.3 to 3.63</td>
<td>V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_{STG}</td>
<td>−40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature, Soldering (10 sec.)</td>
<td>T_{SLD}</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Human Body Model (Note 1)</td>
<td>ESD_{HBM}</td>
<td>2.0</td>
<td>kV</td>
</tr>
<tr>
<td>ESD Capability, Charged Device Model (Note 1)</td>
<td>ESD_{CDM}</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>Latch–up Current Immunity (Note 1)</td>
<td>LU</td>
<td>100</td>
<td>mA</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested by the following methods @ T_{A} = 25°C:
   - ESD Human Body Model tested per JESD22–A114
   - ESD Charged Device Model per ESD STM5.3.1
   - Latch–up Current tested per JESD78.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Supply Voltage</td>
<td>V_{CC}</td>
<td>1.65</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Digital I/O Supply Voltage</td>
<td>V_{DD}</td>
<td>1.65</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Ground</td>
<td>GND</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>T_{A}</td>
<td>−40</td>
<td>120</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>T_{J}</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
## ELECTRICAL CHARACTERISTICS

(TJ = 25°C, VCC = 3 V, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLY REQUIREMENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Supply and ADC reference</td>
<td>VCC</td>
<td>1.65</td>
<td>3</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Digital I/O Supply</td>
<td>VDD</td>
<td>1.65</td>
<td>3</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Analog Supply Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2 MSPS for VCC = 3.6 V | IVCC | 100 | 150 | µA |
| 1 MSPS for VCC = 3 V | | 50 | 100 kSPS for VCC = 3.6 V | 7.6 | 20 | µA |
| 1 MSPS for VCC = 1.8 V | | 30 | | | | |
| Analog Power Dissipation | 
2 MSPS for VCC = 3.6 V | PVCC | 300 | 540 | µW |
| 1 MSPS for VCC = 3 V | | 150 | 100 kSPS for VCC = 3.6 V | 15 | 72 | µW |
| 1 MSPS for VCC = 1.8 V | | 7.6 | 20 | | | |
| Digital Supply Current | 
Dependent on SDO loading (tested with ~7 pF) | 
2 MSPS for VDD = 3.6 V | IVDD | 852 | | µA |
| 1 MSPS for VDD = 3 V | | 425 | 100 kSPS for VDD = 3.6 V | 45 | | µA |
| 1 MSPS for VDD = 1.8 V | | 136 | | | | |
| Standby current (CSN high) (Note 2) | VCC = 3.6 V | ISTNDBY | 3.9 | 6 | µA |
| **ANALOG INPUT** | | | | | | |
| Full−Scale Voltage Span | Common Mode Voltage=VCC/2 | Vfs | −VCC | VCC | Vppd |
| Absolute Voltage Range | VIN to GND | −0.2 | VCC + 0.1 | V |
| | VIN to GND | −0.2 | VCC + 0.1 | V |
| Sampling Capacitance | Measured with 1kHz, 1V Stimuli | CS | 2 | pF |
| **SYSTEM PERFORMANCE** | | | | | | |
| Resolution | | | 12 | Bits |
| Integral Nonlinearity (Note 3) | VCC = 1.8 V | INL | −2 | 0 | 2 | LSB |
| VCC = 3.3 V | | | −2 | 0 | 2 | LSB |
| Differential Nonlinearity (Note 3) | VCC = 1.8 V | DNL | −1.5 | 0 | 1.5 | LSB |
| VCC = 3.3 V | | | −1.5 | 0 | 1.5 | LSB |
| Offset Error | VCC = 1.8 V | EO | 0 | | | LSB |
| VCC = 3.3 V | | | −10 | 0 | 10 | LSB |
| Effective Number of bits | VCC = 1.8 V | ENOB | 10 | | | |
| VCC = 3.3 V | | | | 11.2 | | |
| Offset error drift with temperature | dVOS/dT | 0.02 | ppm/°C |
| Gain Error | VCC = 1.8 V | EG | −0.6 | 0.3 | 0.6 | %FS |
| VCC = 3.3 V | | | | 0.3 | | |
| Gain error drift with temperature | | | 0.0006 | %FS/°C |
| **SAMPLING DYNAMICS** | | | | | | |
| Acquisition Time | | | 62.5 | ns |
| Maximum throughput rate | | | 2 | MSPS |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Signal−to−Noise Ratio | fIN = 1 kHz VCC = 3.3 V | SNR | 70 | dB |
| fIN = 1 kHz VCC = 1.8 V | | 65 | |
| Total−Harmonic Distortion | fIN = 1 kHz VCC = 3.3 V | THD | −80 | dB |
| fIN = 1 kHz VCC = 1.8 V | | −80 | |
**ELECTRICAL CHARACTERISTICS** *(T_J = 25°C, V_CC = 3 V, unless otherwise noted)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal–to–Noise and Distortion (Note 4)</td>
<td>f_IN = 1 kHz V_CC = 3.3 V</td>
<td>SINAD</td>
<td>68</td>
<td>69</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>f_IN = 1 kHz V_CC = 1.8 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spurious–Free Dynamic Range (Note 4)</td>
<td>f_IN = 1 kHz V_CC = 3.3 V</td>
<td>SFDR</td>
<td>69</td>
<td>80</td>
<td>74</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>f_IN = 1 kHz V_CC = 1.8 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DIGITAL INPUT/OUTPUT</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>High–Level Input Voltage</td>
<td>V_INH</td>
<td>V_DD*0.7</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low–Level Input Voltage</td>
<td>V_IL</td>
<td>V_DD*0.3</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High–Level Output Voltage</td>
<td>2 mA drive</td>
<td>V_OUT</td>
<td>V_DD − 0.5 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low–Level Output Voltage</td>
<td>2 mA drive</td>
<td>V_OUT</td>
<td>GND+0.5 V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Standby current includes both digital and analog currents.
3. INL and DNL parameters were verified via bench testing and are not used for production screening.
4. SINAD and SFDR are tested at production and guaranteed by correlation to bench test results.

**TIMING CHARACTERISTICS** *(T_J = 25°C unless otherwise specified)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TIMING SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Throughput</td>
<td>f_THROUGH</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>Cycle Time</td>
<td>f_CYC</td>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Conversion Time</td>
<td>f_CONV</td>
<td>437.5</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data Delay</td>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>cycle</td>
</tr>
</tbody>
</table>

**TIMING REQUIREMENTS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Time (CSN high)</td>
<td></td>
<td>t_AQ</td>
<td>62.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK Frequency</td>
<td>f_CLK</td>
<td></td>
<td>32</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>CLK Period</td>
<td>t_CLK</td>
<td></td>
<td>31.25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CSN Falling to 1st SCLK falling edge</td>
<td>t_CSNSCLK</td>
<td>15.75</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Last SCLK falling edge to CSN rising</td>
<td>t_SCLCKCSN</td>
<td>15.75</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Falling SCLK to SDO valid (Note 5)</td>
<td>Assumed 10 pF Load</td>
<td>t_SDO_VALID</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

5. When SCLK is running at higher frequencies, the t_SDO_VALID of 30 ns requires SDO to be sampled on the falling edge of SCLK at the end of the bit width just before SDO changes to the next output. This will ensure acquisition of the correct data. For example, location A shown below would be the best place to sample SDO for the acquisition of bit 9.

---

**Figure 2. Serial Interface Timing**
TYPICAL CHARACTERISTICS

Figure 3. SNR vs. SCLK Frequency

Figure 4. SNR vs. Temperature

Figure 5. SNDR vs. SCLK Frequency

Figure 6. ENOB vs. SCLK Frequency

Figure 7. THD vs. SCLK Frequency

Figure 8. DVDD Current vs. Temperature

(SCLK = 2 kHz)
Figure 9. Current vs. SCLK Frequency

Figure 10. AVDD Current vs. Frequency

Figure 11. SDO Delay from Falling Edge of SCLK

AVDD = 3.3 V
AVDD = 1.8 V
AVDD = 3.3 V
TERMINOLOGY

Understanding how ADC metrics affect application performance is key to obtaining desired performance. Key terminology are defined below and should be used when determining overall system performance when using the NDC98010/1.

Offset and Gain Error

Offset and gain, if characterized, can be calibrated out post digitization. An ideal ADC has a linear transfer function following the equation \( y = m \cdot x + b \), where \( m \) is the gain and \( b \) is the offset. Ideally the offset would be 0, and the gain would be

\[
m = \frac{(2^{n-1})}{\text{InputRange}} \quad \text{(eq. 1)}
\]

Any deviation from an offset of 0 and the ideal gain is considered error. Although these errors can be calibrated out, any initial gain error reduces the ADCs dynamic range. The plots below shows examples of these errors. Calibrating these errors out would be achieved by adding / subtracting codes to get the digitized output to 0 when the inputs are shorted together at \( V_{\text{CM}} \). After the offset (for signed output format) has been calibrated, samples can be taken at both polarities to determine the gain error. The output can be multiplied by a scale factor (after the offset has been adjusted) to compensate for the gain error.

SFDR

SFDR is the Spurious Free Dynamic Range. SFDR is the ratio of the RMS value of the signal to the RMS value of the highest magnitude spurious signal regardless of where it falls in the frequency spectrum. The highest spur might not be a harmonic, though it typically is.

THD

THD is the total harmonic distortion, defined as ratio of the RMS of the primary signal and the mean of the root sum squared of all the harmonics. Generally only the first 5 harmonics are considered. The figure below shows an example of these AC metrics in the frequency domain.

\[
\text{THD} = 20 \log \left( \frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + H_5^2}}{H_1} \right) \quad \text{(eq. 2)}
\]
Figure 14. Spurious Free Dynamic Range in the Frequency Domain

ENOB

The effective number of bits describes the dynamic range of the ADC. It quantifies the actual resolution of the ADC taking into account noise and distortion. ENOB typically changes over ADC input frequency, and is an important metric for non-DC applications. It is defined as:

$$ENOB = \frac{\text{SINAD} - 1.76}{6.02} \quad \text{(eq. 3)}$$

THEORY OF OPERATION

The NCD98010/1 uses a successive approximation architecture. Conversion from an analog signal to a digital signal occurs in 2 different stages over 16 clock cycles. The first stage is a differential sample and hold operation, where the input V_{INN} and V_{INP} voltages are sampled onto a differential charge re-distribution capacitive array. The second stage implements a binary decision tree, bit cycling through $1/2^N$ divisions of the reference. The internal digital control block steps through each of 12 bits to determine whether that bit in the digital output code is higher or lower than the sampled signal. V_{CC} acts as the analog supply and the ADC reference. This allows for a maximum input range of 0 V to V_{CC}.

Figure 15. SAR ADC Internal Operation

ADC TRANSFER FUNCTION

The NCD98010/1 offers a full input range of 0 V to V_{CC}. The format of the digital output is offered in an unsigned format (NCD98010) and a signed format (NCD98011). The output code resulting from $V_{INN}$ and $V_{INP}$ tied together and held at VCC/2 is therefore 0h000 for the NCD98011 and 0h100 for the NCD98010. This distinction is shown below in Figures 16 and 17.

Figure 16. NCD98010 Unsigned Output Definition

Figure 17. NCD98011 Signed Output Definition
The NCD98010/1 supports many applications due to its small size and low power. The typical connection diagram for the NCD98010/1 maximizing performance is shown below in Figure 18.

### Buffering

Many applications of the NCD98010/1 benefit by a differential input buffer. A unity gain buffer provides current drive to support the anti-aliasing filter and the 2 pF of ADC input capacitance for applications where very high input impedance is required. Input buffers also allow for control of the common mode voltage to maximize the full scale range of the ADC by setting $V_{CM}$ to VCC/2. Input buffers are recommended for applications where the source of the differential analog inputs require extremely high input impedance. Noise introduced by the input buffers should be less than the quantization noise of the ADC (74 dB SNR) to avoid becoming the dominant noise source. Use buffers with sufficient bandwidth (> Nyquist: $F_{SAMPLE}/2$) and an offset less than 1/2 LSB to avoid introducing additional noise and offset errors.

### Anti-Alias Filter

The use of 2 common mode filters in addition to a differential filter is recommended to maintain high common mode rejection. These anti-aliasing filter are built using $R_{CM}$, $C_{CM}$, and $C_{DIFF}$ as shown above in Figure 12 in the Anti-Aliasing Filter box. The equations for determining the cutoff frequencies of each filter are as follows:

$$f_{cutoff\_CM}(\text{HZ}) = \frac{1}{2\pi \cdot R_{CM} \cdot C_{CM}} \quad (eq. 4)$$

1. Cutoff frequency for the common mode filters.

$$f_{cutoff\_DIFF}(\text{HZ}) = \frac{1}{2\pi \cdot 2R_{CM} \cdot C_{DIFF}} \quad (eq. 5)$$

2. Cutoff frequency for the differential filter.

The common mode filter cutoff frequency should be no greater than the Nyquist frequency ($F_{SAMPLE}/2$). Set the differential cutoff frequency to be one decade less than the common-mode cutoff frequency by increasing the differential capacitor ($C_{DIFF}$) by a factor of 10 over $C_{CM}$. This will help to reduce errors caused by common mode filter component mismatch. Selecting the appropriate values for the anti-aliasing filter is important to maintain peak performance. Adding resistors to the signal path will introduce noise. Keeping $R_{CM}$ as small as possible will mitigate additional noise and error. The thermal noise introduced by the filter resistors can be calculated by:

$$V_n = \sqrt{4 \cdot k \cdot T \cdot R_{CM}} \quad (eq. 6)$$

(3) Noise introduced by series anti-aliasing filter.

Where $k = 1.38E-23$ J/K (Boltzmann’s constant) and $T$ is the temperature in degree Kelvin.

Using smaller resistors and larger capacitors to achieve the desired cutoff frequency will help mitigate noise and charge injection. When choosing anti-aliasing filter components, ensure that the settling time is short enough for the input to be within 1/2 LSB of the desired value before the CSN goes low to begin the conversion.

### Power Supply Decoupling

Local ADC supply decoupling is essential for maintaining high power supply rejection ratio. For the NCD98010/1, the analog supply (VCC) is also the reference for the ADC. Any noise or drift greater than 1/2 LSB will affect the DNL and INL of the converter. Use local decoupling capacitors of
1 μF. All decoupling capacitors must connect directly to a low impedance ground plane in order to be effective. Short traces or vias are required to minimize additional series inductance. Ceramic capacitors are recommended based on their low ESR and ESL. X7R ceramic capacitors are recommended for applications involving a wide temperature range.

**Minimal Component Realization**

For applications where minimizing board space trumps ADC performance, the NCD98010/1 connection diagram can be reduced as shown in Figure 19 below. The removal of the input buffering may be an option depending on the nature of the differential analog input source. Removing the anti–aliasing filter would come at the expense of reduced ENOB due to the digitization of aliased signals.

**Output Timing / Definition**

Figure 20 below shows the NCD98010/1 output format. There is a 1 sample latency associated with the output data. The digital data for analog input sampled are clocked out of the ADC by SCLK one conversion later, as shown in the diagram below.

**Layout Guidelines**

Ideal PCB layouts have a ground plane placed underneath the device and the PCB is partitioned into digital and analog sections supporting the analog inputs to the ADC on one side, and the digital interface on the other side. To avoid the coupling of digital noise into the analog partition, care must be taken not to cross digital signals with the analog input signals. Keep the analog input signals and the VCC supply / reference signal away from noise digital signals. Recommended bypass capacitances should be places as close as possible to the VCC and VDD pins, and the path to ground needs to be a low inductance low resistance local connection.
PACKAGE DIMENSIONS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 ").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 ").

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
PACKAGE DIMENSIONS

X2QFN8, 1.5x1.5, 0.5P
CASE 722AM
ISSUE O

NOTES:
2. CONTROLLING DIMENSIONS MILLIMETERS
3. DIMENSION "b" APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

<table>
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<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
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<td>A3</td>
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RECOMMENDED MOUNTING FOOTPRINT

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