

Migrating from the ATECC608A to the ATECC608B

Introduction

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Over time, security capabilities and expectations evolve within the security world along with the capabilities of attacks that seek to compromise secure systems. Recognizing these changes, Microchip has developed a security-enhanced version of the ATECC608A, known as the ATECC608B. The security changes implemented in the device are largely behind the scenes and are not directly observable during normal operation. The ATECC608B has been designed to allow an easy migration from the ATECC608A, while improving the overall security.

For new designs, it is recommended that users start directly with the ATECC608B. For designs that are going through an upgrade or a revision, it is recommended that part of the upgrade include the ATECC608B. For other designs, users must do an overall security assessment and determine if they need to migrate to the ATECC608B.

The ATECC608B continues the line of security products developed as part of the Microchip CryptoAuthentication[™] family of high-security cryptographic devices. These devices combine world-class hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols. All applications and use cases previously supported by the ATECC608A are also supported by the ATECC608B.

Applications Summary

- Network/Internet of Things (IoT) Node Endpoint Security Manages node identity authentication and session key creation and management. Support is provided for the ephemeral session key generation flow for multiple protocols including TLS 1.2 and TLS 1.3.
- Firmware Validation (Secure Boot) Supports the microcontroller (MCU) host by validating code digests and
 optionally enabling communication keys upon a successful secure boot. For an enhanced performance, various
 configurations are available.
- Small Message Encryption Hardware Advanced Encryption Standard (AES) engine to encrypt and/or decrypt small messages or data such as Personally Identifiable Information (PII). The device supports the AES-ECB mode directly. Other AES modes are supported with help from the host. Additional Galois Field Multiply (GFM) calculation functions support the AES Galois Counter Mode (AES-GCM).
- Secure Over-the-Air (OTA) Updates Supports local protected key generation for downloaded images. Both
 broadcasts of one image to many systems, each with the same decryption key, and point-to-point download of
 unique images per system are supported.
- Accessory/Disposable Authentication Validates the authenticity of a system or component. This capability is often sought where disposable components are part of a system.

Table of Contents

Intro	oduction1				
1.	Device Differences				
2.	ATECC608B Migration				
3.	Conclusion				
The Microchip Website					
Product Change Notification Service7					
Customer Support7					
Microchip Devices Code Protection Feature					
Legal Notice7					
Trademarks					
Qua	Quality Management System				
Wor	Worldwide Sales and Service				

1. Device Differences

The overall structure of the ATECC608B is identical to that of the ATECC608A. The ATECC608B does not introduce any new configuration bits and has the same number of data slots as that of the ATECC608A. All commands and command modes are still supported. The device supports both the I²C and SWI interface I/O protocols. The pinouts for the 8-pin SOIC and UDFN packages remain unchanged.

The following sections describe the differences between the ATECC608A and the ATECC608B devices.

Low-Frequency I²C Issue

The ATECC608A has an error in the I²C circuitry, where the device may respond incorrectly under the following conditions:

- Multiple I²C devices are on the same bus as the ATECC608A.
- The ATECC608A device was in Idle mode.
- The I²C operation frequency is \leq 300 kHz.
- A data pattern from other devices on the I²C bus could be interpreted by the ATECC608A as a wake pulse.

Under the above conditions, the ATECC608A wakes up and may corrupt data being sent to other devices on the bus. Whether or not data are corrupted depends on the frequency of operation and the actual data being sent.

This issue has been corrected for the ATECC608B device by modifying the I²C circuitry to eliminate this issue. Note that the ATECC608B may still wake up at low frequency but it does not respond or cause data corruption.

Device Revision (DevRev) Differences

The package marking on Microchip security devices does not identify the device type. Therefore, the package marking cannot be used to identify the ATECC608B. The only way to identify the device is through use of the device revision. The hardware device revision of the device can be read by using the Revision mode (0x00) of the Info command. The output response of the Info command for each device is as follows:

Table 1-1. Revision Response

Device	Revision Response
ATECC608A	0x00 0x00 0x60 0x02
ATECC608B	0x00 0x00 0x60 0x03 (Note)

Note: The value of the fourth byte may change over time but it is 0x03 at the time of the initial product release.



Important: The value of the Revision mode response is not the same as the 4-byte RevNum (Bytes[4:7]) in the device configuration zone. Only the Revision mode response can be used for device identification.

Execution Time Differences

The implementation of security enhancements has resulted in changes to the execution times of a few commands. The variation depends on the actual Clock Divider mode as well as the specific mode of operation. The following table shows a list of commands and expected differences in execution times.



Notice: For a more detailed understanding of the execution times, refer to the complete data sheet.

Command	Description of Changes
Verify	 The execution times of the Verify command will increase by no more than 10%. Actual variation may depend on the specific mode of the command. The execution time increase will occur for all three Clock Divider modes.
SecureBoot	 The SecureBoot command includes a verify operation. The increase in execution time is due to the Verify portion of this command. The execution times of the SecureBoot command will increase by no more than 10%. Actual variation may depend on the specific mode of the command. The execution time increase will occur for all three Clock Divider modes.
Read	 The increase in read times is dependent on what is being read. Reads of the configuration zone have increased by roughly 50% (0.8 ms to 1.2 ms) for a 32-byte read. Reads of the data zone have approximately doubled. (0.9 ms to 1.8 ms) for a 32-byte read. This does not apply to reading back a command response. This time will remain the same. The execution time increase does not vary with the Clock Divider modes.
Lock	 The maximum lock time for either the configuration zone or the data zone increases by approximately 30%. Since production units are shipped in a locked state, this does not impact normal device operation and is just observed by the user during the prototyping or development phase. The execution time increase does not vary with the Clock Divider modes.

Table 1-2. ATECC608A vs. ATECC608B Execution Time Differences

Enhanced Temperature Range

The ATECC608A is specified over the industrial temperature range of -40°C to +85°C.

The ATECC608B is specified over the standard industrial range of -40° C to $+85^{\circ}$ C and an extended range of -40° C to $+100^{\circ}$ C, for those users that need an upper ambient temperature value > $+85^{\circ}$ C. The enhanced temperature range devices have a unique ordering code that is found in the device's data sheet.

New Packages

The ATECC608B is now available in a 3-pin RBH contact package. This is in addition to the already existing 8-pin SOIC and UDFN packages. This package has been used previously for the ATSHA204A and the ATECC508A CryptoAuthentication devices. The RBH package is only available for devices in SWI interface mode.

The RBH package is a contact package that is typically mounted by gluing the package to an enclosure with the signal pads exposed. Contacts to the pads are usually made through pogo pins when the disposable unit is connected to the host system.

2. ATECC608B Migration

The ATECC608B has the same form, fit and function as the ATECC608A. The packages and pinouts are the same, the device structure is the same and so are the commands and command structure. This makes the ATECC608B a functional drop-in replacement of the ATECC608A. If the users implement their design utilizing the Microchip's software library (CryptoAuthLib), this further simplifies the migration process.

An additional factor that has to be considered is the timing differences between the ATECC608A and the ATECC608B for a specific design. This really depends on how the software was implemented. There are two cases that require consideration:

Fixed Timing Implementation

If the code is written assuming hardwired timing parameters, careful analysis must be undertaken to evaluate the impact of changing from the ATECC608A to the ATECC608B. Under this method, after a command is issued, the microcontroller will wait a fixed period of time before reading the response data back. If the delay required for the ATECC608B is significantly longer than the ATECC608A, this command may fail. Using an older version of CryptoAuthLib meant for the ATECC608A or a customer-generated library with the ATECC608B could cause some timing errors. Implementing the latest version of CryptoAuthLib correctly updates the timing information and, through just recompiling the code and reflashing the micro, the timing issues may be corrected. In general, the parameters used for fixed timing are broad enough that they will be conservative to actual worst-case timing values and may still not be an issue. As noted in **Section 1. Device Differences**, the timing changes of the ATECC608B and ATECC608A are relatively minor. Also, these are representative times for the specific command modes and there are other items (as noted in the data sheet) that could cause these values to step out further.

If timing is an issue, the following solutions can be considered:

- 1. Migrate the code to use the latest version of the CryptoAuthLib library.
- 2. Migrate the code to use polled timing. See **Section 2.** Polled Timing Implementation below.
- 3. If a custom library with fixed timing is used, update the library timing parameters needed for the ATECC608B.
- 4. Implement redundancy by trying to read back data a second time upon receiving a failure code that indicates the response was not yet ready.

Polled Timing Implementation

Polled timing is set as the default mode of operation when using the CryptoAuthLib library. If the code is written using polling, there will be no issues with migrating to the ATECC608B. In this scenario, the microcontroller would poll the ATECC608B to determine when data are available to be read. Minor timing differences would be absorbed by the polling command. These differences can be fully absorbed by the ATECC608B device because none of the execution times of the commands have stepped out significantly.

2.1 I²C Low-Frequency ATECC608B Migration

Migrating an ATECC608A design that has to deal with the low-frequency I²C issue requires no changes to either hardware or firmware. The changes implemented for a correct operation with the ATECC608A will not cause an issue with the fixed ATECC608B.

The user must consider if the operation of the system is better served by backing out the firmware changes implemented to correct the ATECC608A issues. Removing these changes would most likely result in reduced firmware size and improved system performance. Whether these are reasons valuable enough to modify the working code is up to the implementer.

3. Conclusion

Because the form, fit and function of the ATECC608B are nearly identical to those of the ATECC608A, the migration is typically a fairly minor task. The minor timing differences between the devices, in general, will not cause an issue and can be easily corrected if they do. The addition of the new RBH package and the enhanced temperature range also increase the market space for the ATECC608B secure element.

The changes implemented in the ATECC608B were primarily done to enhance device security and are largely transparent to the user. For new system designs and a refresh of the existing systems, it is strongly recommended to convert to the ATECC608B as a way to enhance overall system security.

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ISBN: 978-1-5224-6331-3

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