

LITIX™ Basic+ Family Board V1.1

November 2018



1 Board description

2 Quick start

3 Schematic and layout

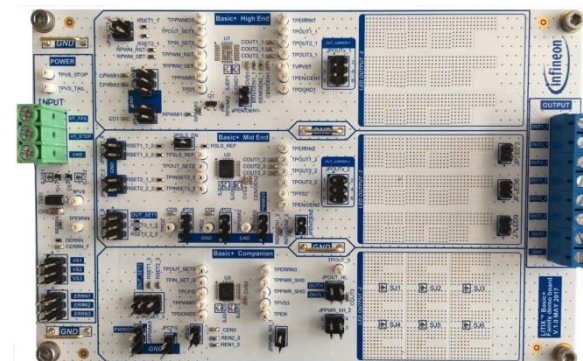
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Board description

- › Equipped with one TLD2141-3EP (High End), one TLD2331-3EP (Mid End) and one TLD1114-1EP (Companion) LITIX™ Basic+ devices
- › Compatible with all LITIX™ Basic+ High End and Mid End devices
- › Typical supply voltage range: 8V – 16V (5.5V – 40V), with possibility to power-ON and test each device separately
- › On-board LED load for each device, 3x3 LEDs per device
- › Possibility to connect to external load
- › 15cm x 10cm 2-layer PCB



Board connectors

- › POWER: Supply connector, VS and GND
 - VS_STOP: Board power supply and activation of the internal PWM engine for Basic+ High End device
 - VS_TAIL: Board power supply without activation of the internal PWM engine
 - GND

- › OUTPUT: External load
 - OUT1_1, OUT2_1, OUT3_1: For the Basic+ High End device (OUT1, OUT2, OUT3)
 - OUT1_2, OUT2_2, OUT3_1: For the Basic+ Mid End device (OUT1, OUT2, OUT3)
 - OUT3: For the Basic+ Companion
 - GND

Jumpers – Power Supply, Error Network

- › JPVS: Select which devices will be supplied (all devices share the same reverse polarity protection circuit)
 - VS1: Close to supply the Basic+ High End
 - VS2: Close to supply the Basic+ Mid End
 - VS3: Close to supply the Basic+ Companion

- › JPERRN: Select which devices will be connected to the error network (all devices share the same error network pull-up circuit)
 - ERRN1: Close to connect the Basic+ High End device to the error network
 - ERRN2: Close to connect the Basic+ Mid End device to the error network
 - ERRN3: Close to connect the Basic+ Companion device to the error network

Jumpers - Basic+ High End

- › JPIN_SET_1: Sets the output current of OUT
 - RSET1_1 (37.4 k Ω): sets output current to 10 mA (30 mA for TLD2142-1EP)
 - RSET2_1 (6.19 k Ω): sets output current to 59 mA (177 mA for TLD2142-1EP)

- › JPPWMI1: PWMI connection
 - CPWMI1 (120 nF): Set the PWM frequency to 220 Hz and duty cycle* 10%
 - CPWMI2 (68 nF): Set the PWM frequency to 400 Hz and duty cycle* 10%
 - GND: duty cycle is 100%

* Duty cycle set by the RPWM_SET and RPWM_RST resistors

Jumpers - Basic+ High End cont'd

- › JPD1: Diagnosis management
 - CD1: When a fault is detected, or ERRN is pulled-down externally, all the channels driven by the device are switched off after a delay time $t_{D(set)}$. Delay time is set by CD1 capacitor
 - GND: Only the channel under fault condition will be deactivated
- › JPEN/DEN1: Close to connect EN/DEN to resistor divider to activate device and diagnosis

Jumpers – Basic+ Mid End

- › JPINSETx_2: Sets the output current of OUTx (1 or 2)
 - RSETx_1_2 (37.4 k Ω): sets output current to 10 mA (30 mA for TLD2132-1EP)
 - RSETx_2_2 (6.19 k Ω): sets output current to 59 mA (177 mA for TLD2132-1EP)

- › JPINSET3_2: Sets the output current of OUT3
 - OUT_SET1: Output current is controlled by the OUT_SET of the Basic+ High End device
 - RSET3_1_2 (37.4 k Ω): sets output current to 10 mA (30 mA for TLD2132-1EP)
 - RSET3_2_2 (6.19 k Ω): sets output current to 59 mA (177 mA for TLD2132-1EP)

- › JSLS_EN: When closed, the SLS diagnosis is deactivated. When open the voltage reference is set by the resistor RSLS_REF

Jumpers – Basic+ Mid End cont'd

- › JPEN/DEN2: Close to connect EN/DEN to resistor divider to activate device and diagnosis
- › JPD: Diagnosis management
 - GND: Only the channel under fault condition will be deactivated
 - CD2: When a fault is detected, or ERRN is pulled-down externally, all the channels driven by the device are switched off after a delay time $t_{D(set)}$. Delay time is set by CD2 capacitor
- › JPDS: SLS diagnosis
 - GND: Latched SLS detection
 - CDS: Automatic retry after $t_{SL(wait)}$. $t_{SL(wait)}$ time defined by CDS capacitor
- › JPWMI2: PWMI connection
 - PWMO1: Use of PWMO signal of Basic+ High End
 - GND: Outputs activated

Jumpers - Companion

- › JPIN_SET3: Sets the output current
 - OUT_SET2: Output current is driven by the OUT_SET
 - RSET1_3 (13.7 k Ω): Sets the output current to 80 mA
 - RSET2_3 (2.94 k Ω): Sets the output current to 373 mA

- › JPPWMI3: PWM connection
 - PWMO1: Use of PWMO signal of Basic+ High End
 - GND: Output activated

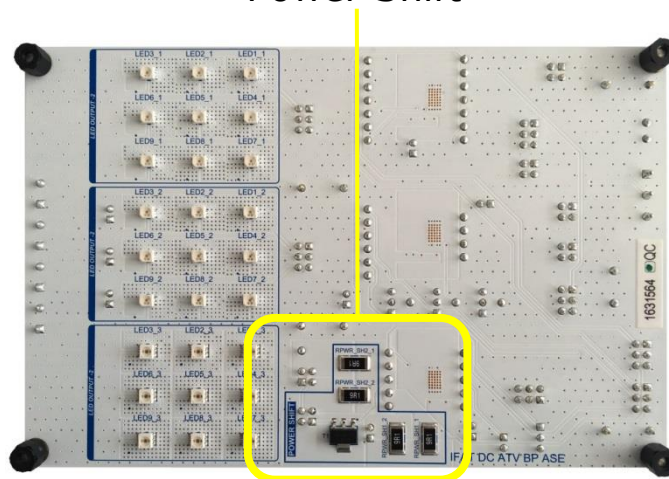
- › JPCFG: Close if higher current accuracy is needed to drive the target load (closed when OUTH is connected to the load)

- › JPEN3: Close to connect EN/DEN to resistor divider to activate device and diagnosis

Jumpers – Companion cont'd

- › JPPWR_SH_1: Close to allow Power Shift control
- › JPPWR_SH_2: Change of R2
 - 1 – 2 or 3 – 4 closed: $R2 = 9.1 \Omega$, $IPSH_{max} = 350 \text{ mA}$
 - 1 - 2 and 3 - 4 closed: $R2 = 4.55 \Omega$, $IPSH_{max} = 700 \text{ mA}$

Power Shift



Jumpers – Load selection

- › OUT_JUMPER-1, 2: Bypass to connect the on-board load, LED OUTPUT-1, 2 to the outputs of Basic+ High End, Basic+ Mid End. Leave open to connect external load
 - 1-2 closed: Connect OUT1 of Basic+ High End, Basic+ Mid End
 - 3-4 closed: Connect OUT2 of Basic+ High End, Basic+ Mid End
 - 5-6 closed: Connect OUT3 of Basic+ High End, Basic+ Mid End

- › JPOUT_HL: Bypass to connect the on-board load, LED OUTPUT-3 to the output of Basic+ Companion. Leave open to connect to external load
 - OUTH: Connect OUTH of Basic+ Companion (JPCFG must be closed)
 - OUTL: Connect OUTL of Basic+ Companion (JPCFG must be open)

On-board Load

- › LED OUTPUT-1: 1 rows of 3 red LEDs (LS E6SF) for each channel (3x3) of Basic+ High End
- › LED OUTPUT-2: 1 rows of 3 red LEDs (LS E6SF) for each channel (3x3) of Basic+ Mid End
 - JPLED3, JPLED6, JPLED9: Bypass to simulate a SLS fault on the LED3, LED6 and LED9 respectively
- › LED OUTPUT-3: 3 rows of 3 LEDs (LR G6SP) for the output of Basic+ Companion. The middle row is currently in use
 - SJ1 – SJ6: Close to create an LED matrix for high current applications

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Quick Start

- › Connect battery to VS_TAIL or VS_STOP and GND (e.g. 8V – 16V)
- › Supply the device(s) under test (JPVS)
- › Connect the device(s) to the Error network (JPERRN)
- › Select the output current (JPINSET_x)
- › Enable the device(s) and diagnosis (JPEN/DENx)
- › Select the desired fault management (JPDx, JPDS)
- › Select load, close OUT_JUMPER-x jumpers to use the on-board LEDs or leave open and connect external load to the connector OUTPUT
- › Activate outputs using PWM input (JPPWMIx)

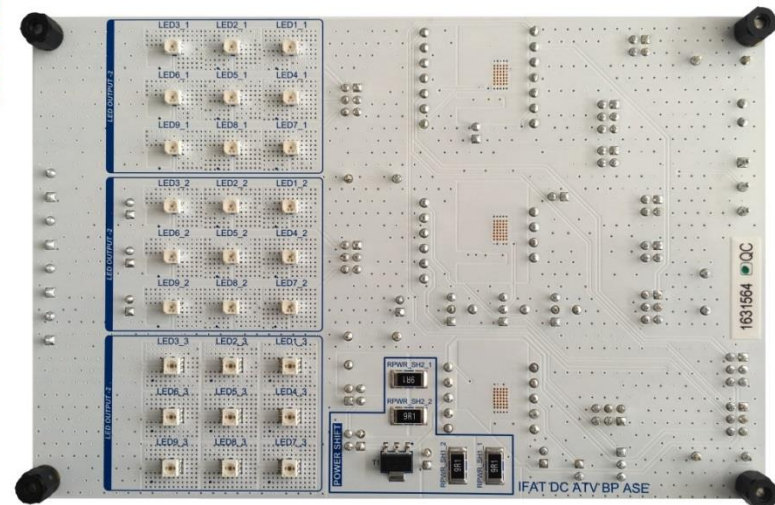
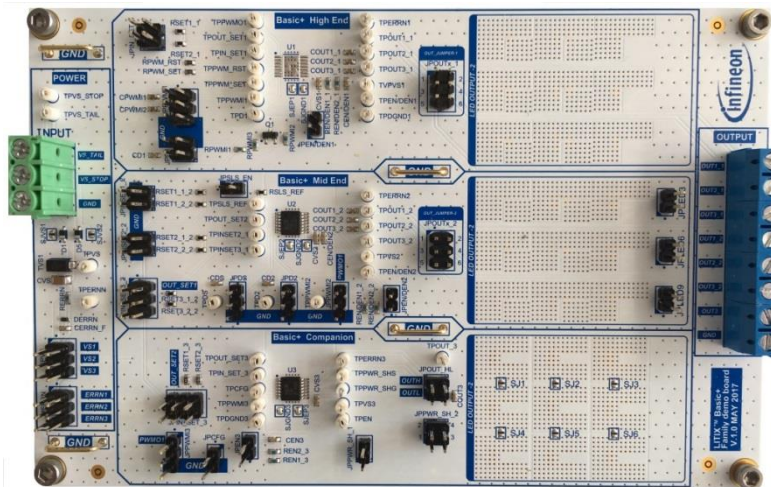
1 Board description

2 Quick start

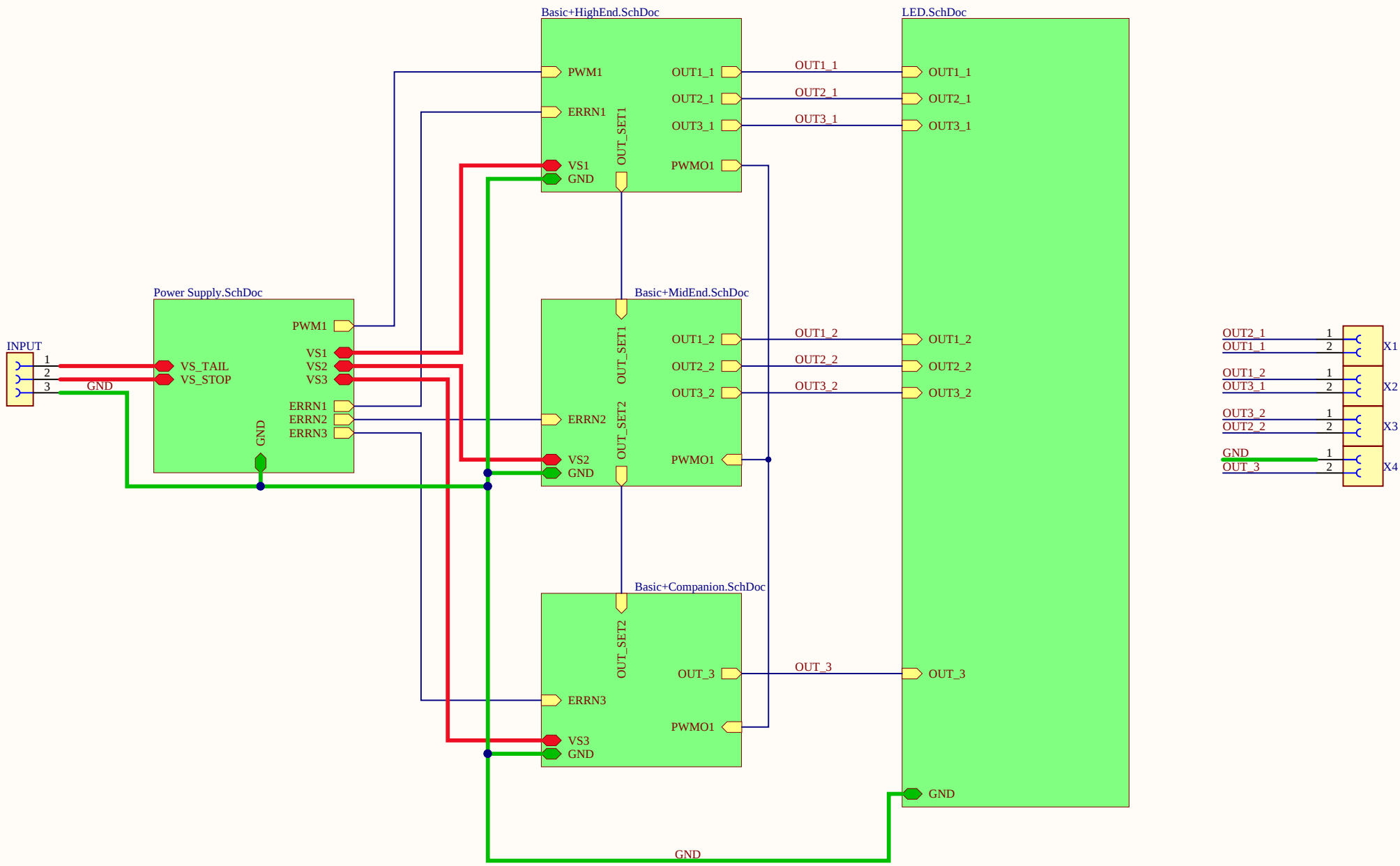
3 Schematic and layout

Schematic and board layout

- › The schematic and layout designs are shown on the following pages.
- › The visible content (names,...) can be activated or deactivated using the PDF reader layer settings.



02_Top_Level.SchDoc



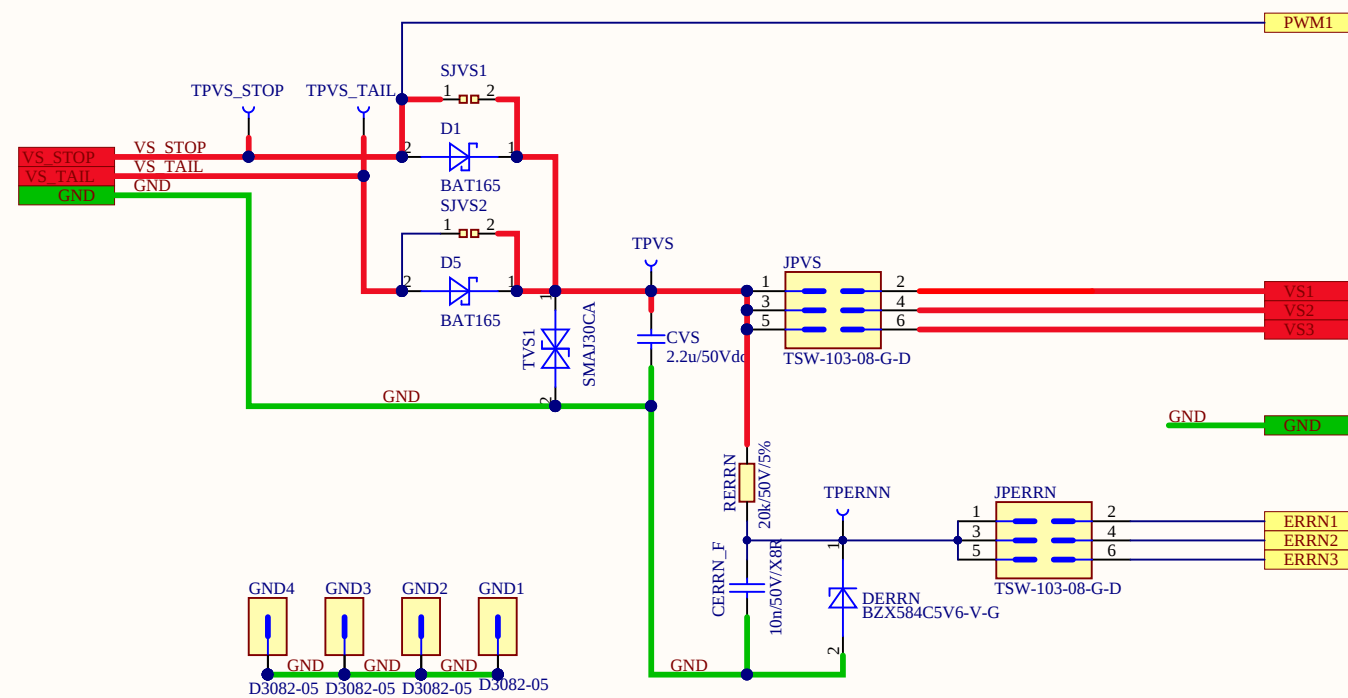
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Miscellaneous
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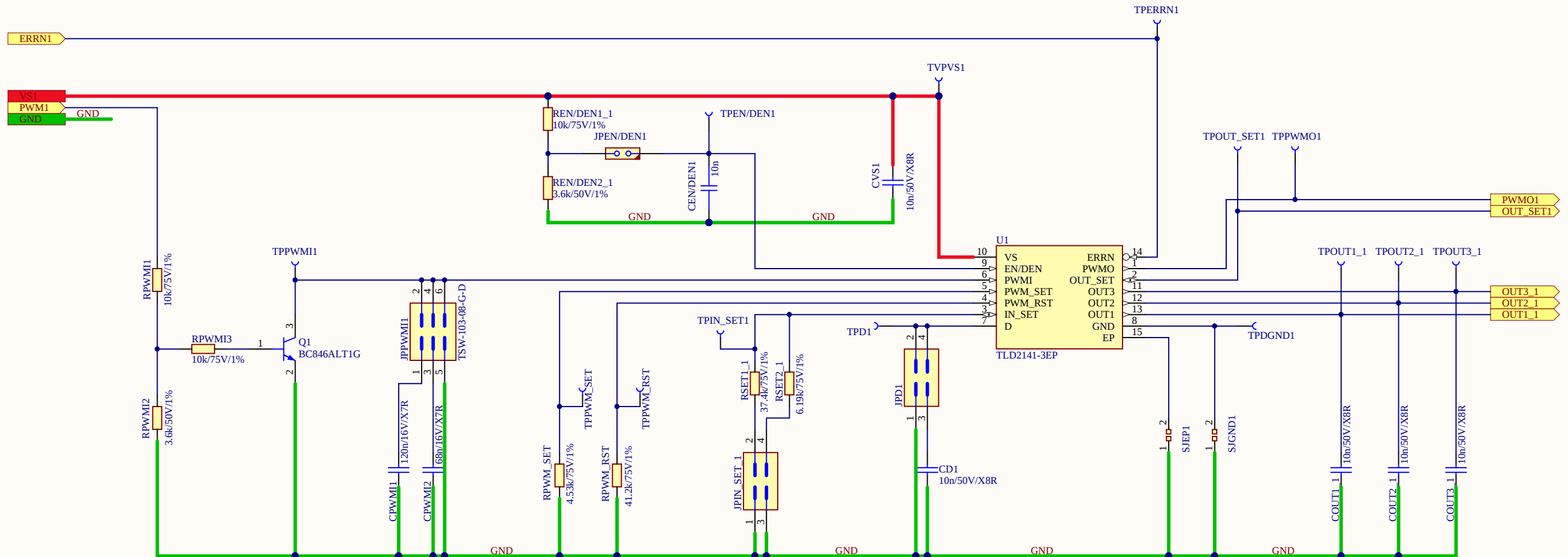


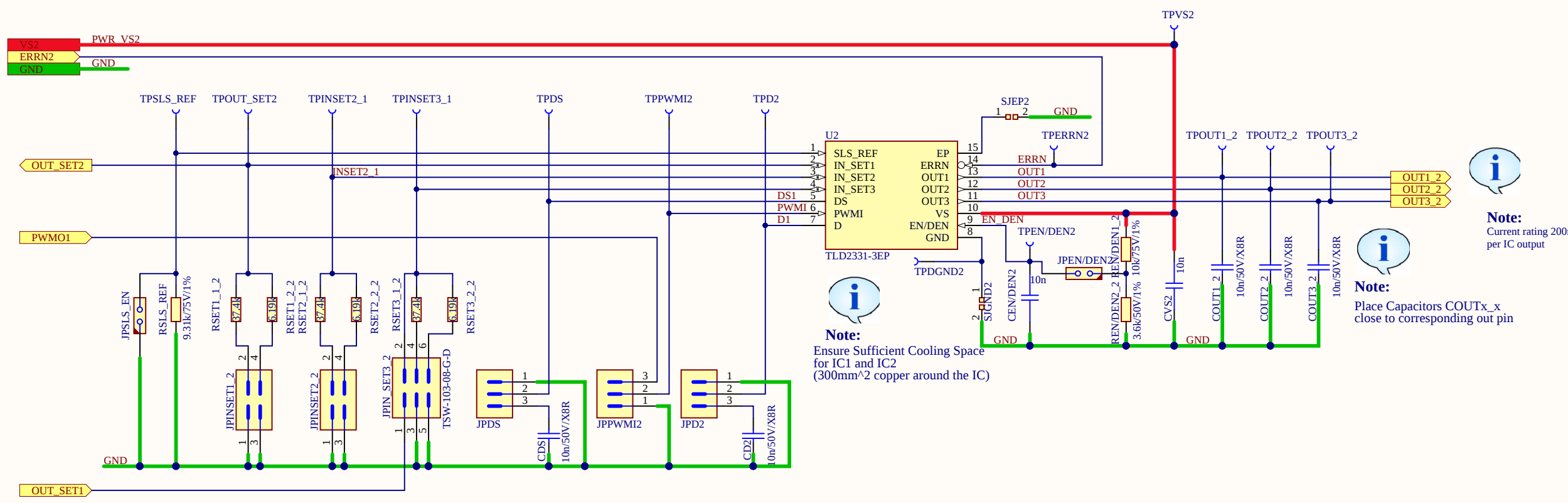
Infineon Technologies Austria AG

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LITIX™ Basic+ family board				
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Size:	Document Name		Rel.	Rev.
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Author:				
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Power Supply.SchDoc

Basic+HighEnd.SchDoc





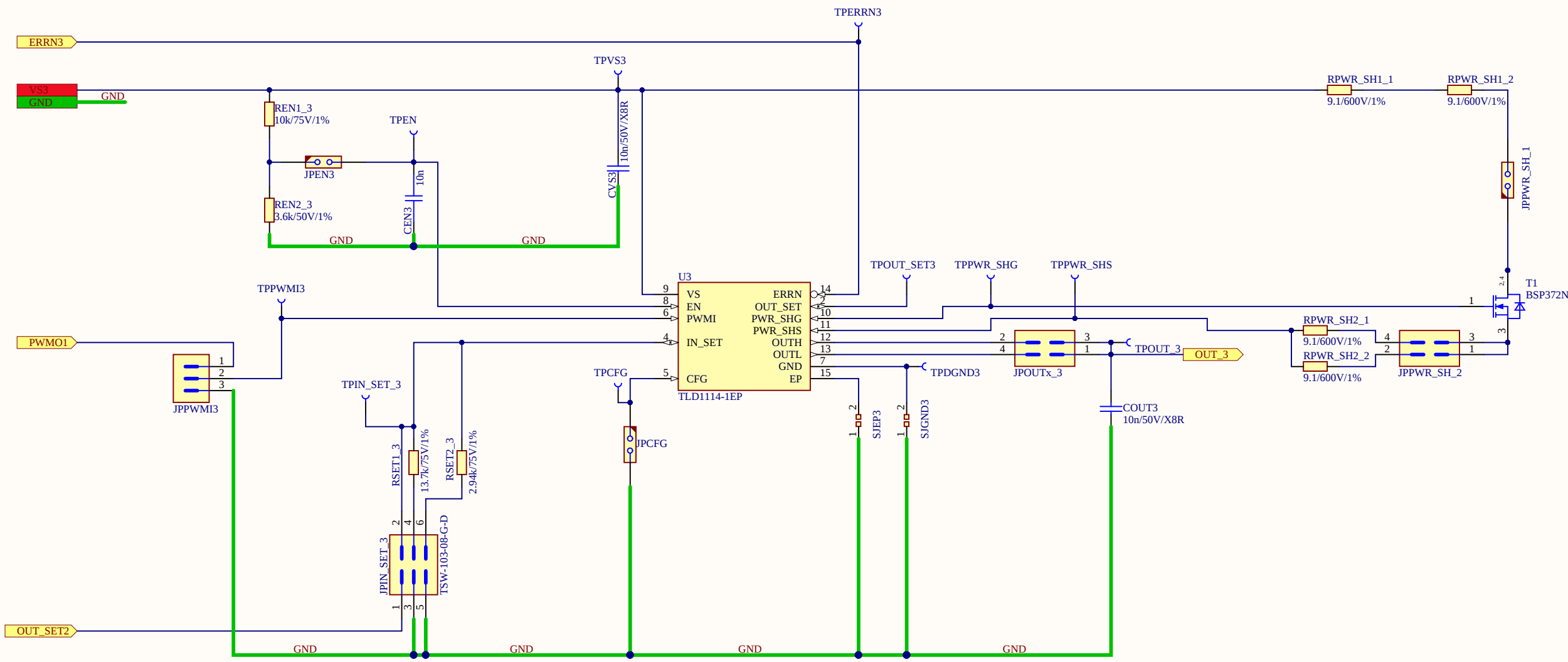
Note:
Ensure Sufficient Cooling Space
for IC1 and IC2
(300mm^2 copper around the IC)

Note:
Place Capacitors COUTx_x
close to corresponding out pin

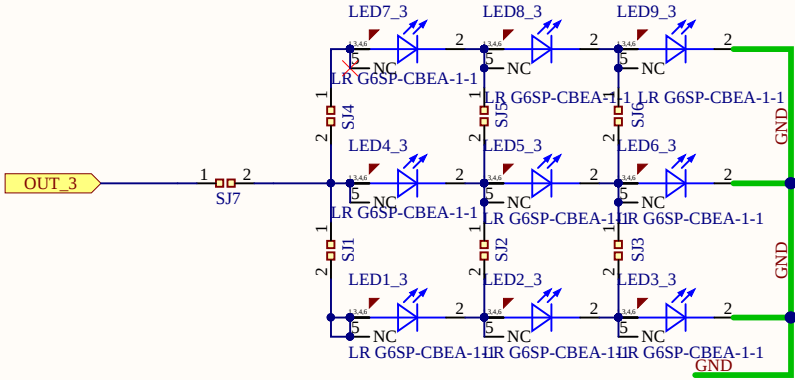
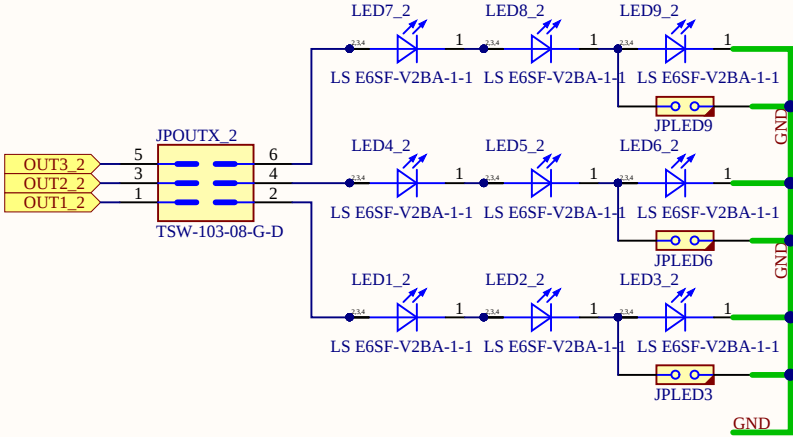
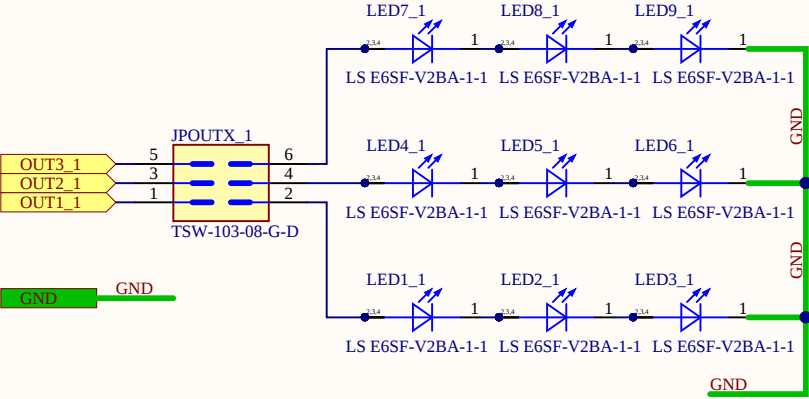
Note:
Current rating 200mA
per IC output

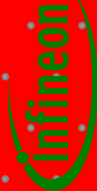
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Basic+Companion.SchDoc

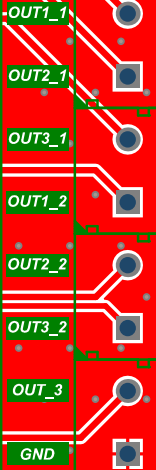


LED.SchDoc

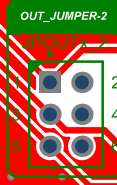
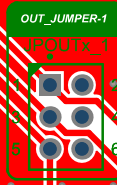
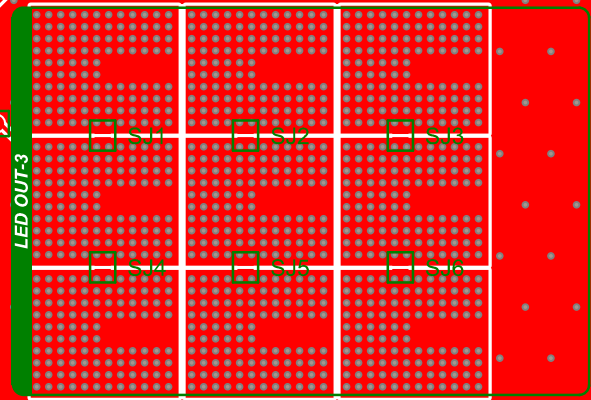
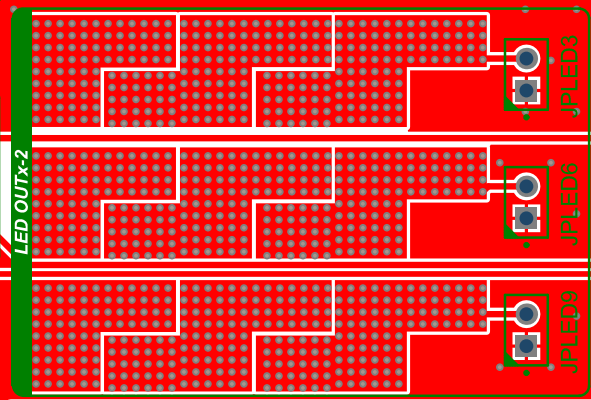
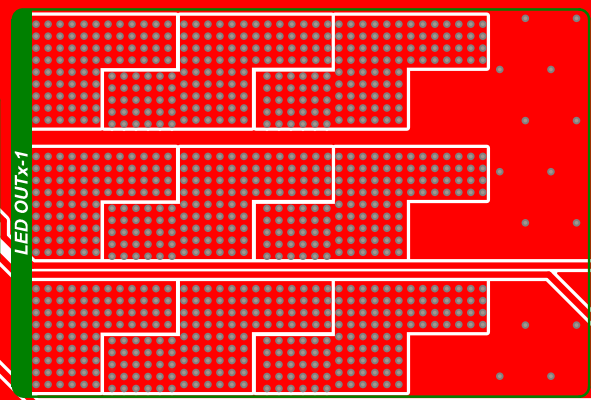




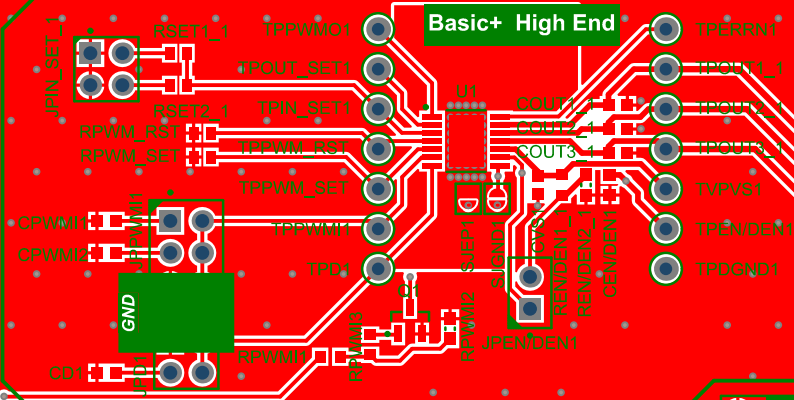
OUTPUT



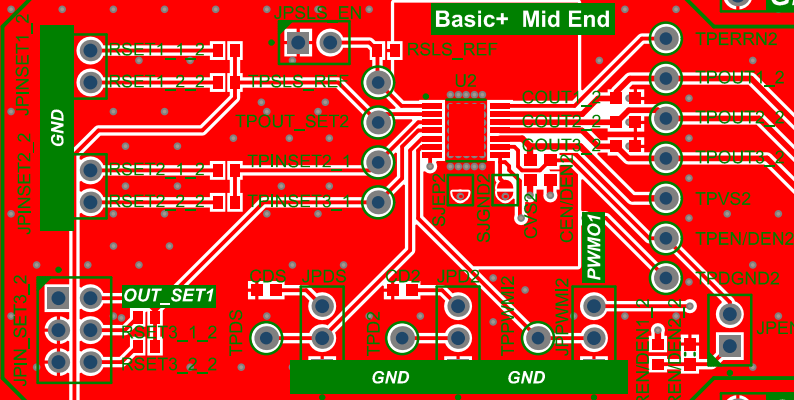
LITIX™ Basic+
Family demo board
V1.1 March 2018



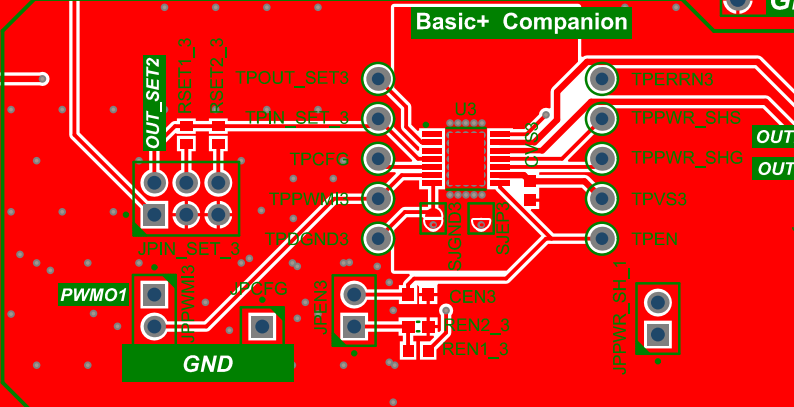
Basic+ High End



Basic+ Mid End



Basic+ Companion

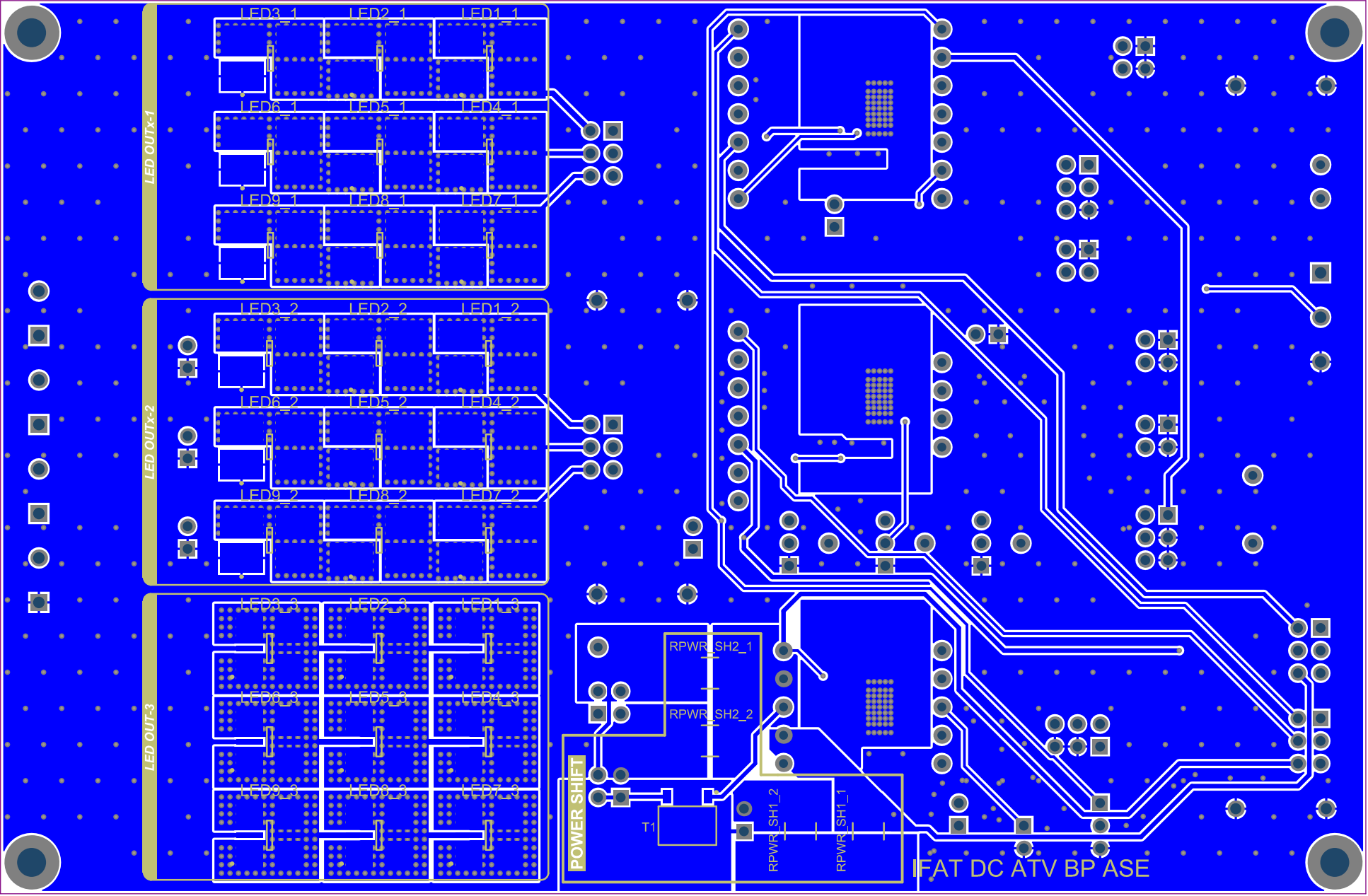


POWER



INPUT





LED OUTx-1

LED OUTx-2

LED OUTx-3

LED3_1 LED2_1 LED1_1
LED6_1 LED5_1 LED4_1
LED9_1 LED8_1 LED7_1

LED3_2 LED2_2 LED1_2
LED6_2 LED5_2 LED4_2
LED9_2 LED8_2 LED7_2

LED3_3 LED2_3 LED1_3
LED6_3 LED5_3 LED4_3
LED9_3 LED8_3 LED7_3

POWER SHIFT

T1

RPWR_SH2_1
RPWR_SH2_2

RPWR_SH1_2

RPWR_SH1_1

FAT DC ATV BP ASE

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