Frequently asked questions for TLE92108/4

About this document

Scope and purpose

This document compiles frequently asked questions for the TLE92108/4 and provides solutions to common problems which might occur during the development using these devices. This document must be used in conjunction with the device datasheets, which contain full technical details, specifications and description of operation.

Intended audience

Developers working with the TLE92108 / TLE92104.

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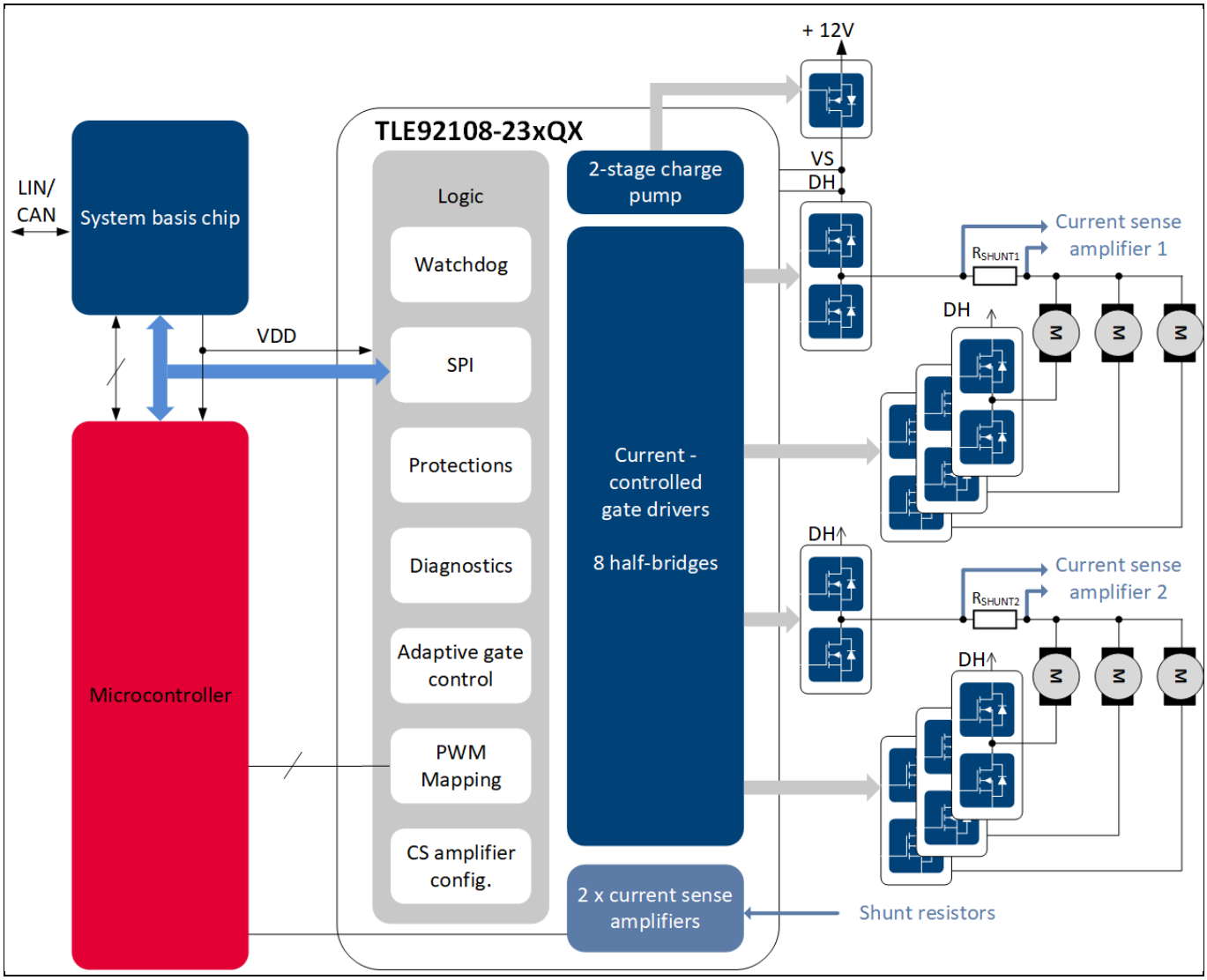
1 Introduction

The TLE92108/4 are Multiple MOSFET drivers, dedicated to control up to sixteen n-channel MOSFETs. They integrate eight half-bridge drivers (TLE92108), repectively four half-bridge drivers (TLE92104) for DC motor control applications such as automotive power seats, power lift gates, cargo cover, sunroof, door lock, window lifts, etc…

Figure 1 Block diagram of the TLE92108-231/232QX in one of the possible half-bridge configurations



2 Frequently asked questions

Table 1 List of frequently asked questions

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2.1 Does the TLE92108/4 support 32-bit SPI frames?

The register definition of the TLE92108/4 is optimized for 24-bit frames. However, it is possible to use 32-bit SPI frames as well.

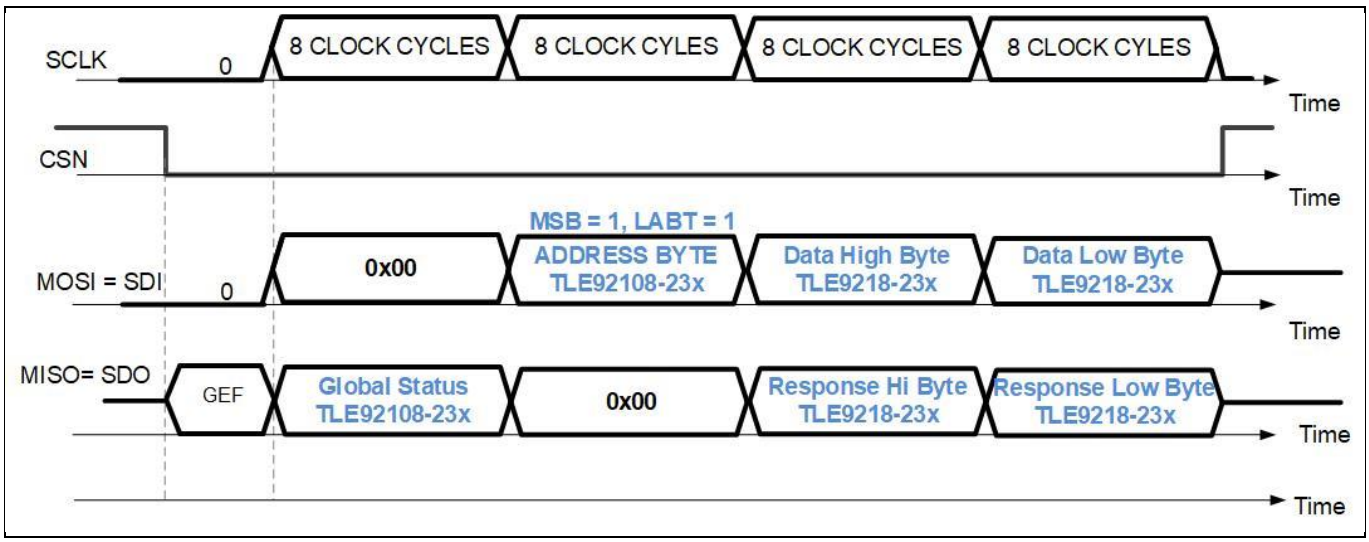
For 32-bit SPI frames, the four bytes must be sent in the following order (refer to Figure 2):

1. Byte 1: Dummy byte 0x00
2. Byte 2: Address byte
3. Byte 3 and byte 4: Data word

The microcontroller receives the following information from the TLE92108-23x SDO in the following order (refer to Figure 2):

1. Byte 1: Global status byte
2. Byte 2: Dummy byte 0x00
3. Byte 3 and byte 4: Response word

Figure 2 32-bit SPI frame with the TLE92108/4



It is recommended to use the dummy byte 0x00 to prevent the first byte from being wrongly interpretated as an address byte.

2.2 What are the benefits of the active free-wheeling control scheme?

The active free-wheeling reduces the power losses in the free-wheeling MOSFET during the PWM operation (pulse width modulation), therefore reducing costs at system level:

- allowing the usage of smaller MOSFETs and/or smaller MOSFET packages
- reducing the required PCB cooling surface of the free-wheeling MOSFET

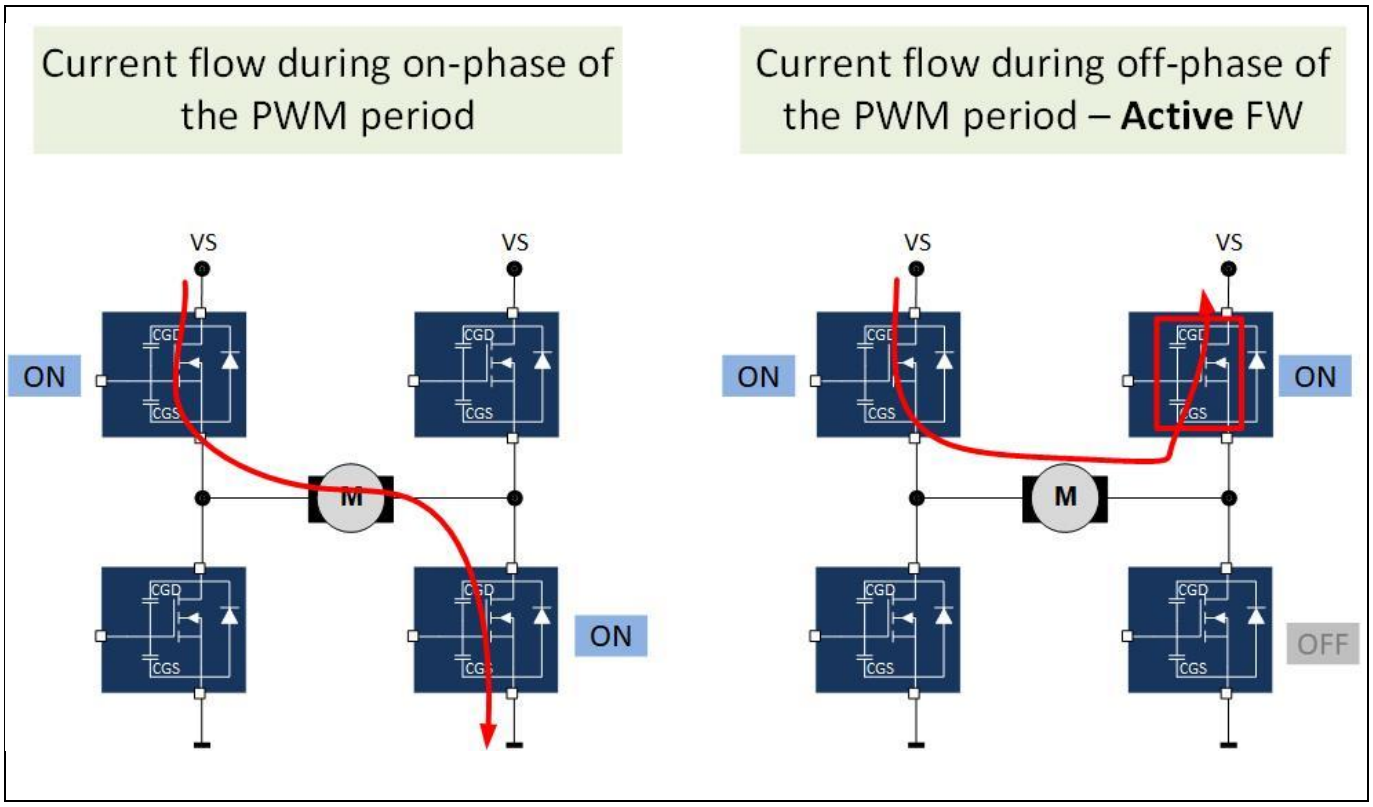
2.2.1 Active free-wheeling

During the off-phase of the PWM period, the free-wheeling (FW) MOSFET is turned on.

Therefore the current flows through FW MOSFET instead of flowing through the MOSFET body diode.

Note that the current of the FW MOSFET flows from the source to the drain, due to the load inductance.

Figure 3 Current flow during off-phase of the PWM period – Active free-wheeling (with low-side PWM)



The peak power dissipation in the FW MOSFET during the PWM off-phase is given by (1):

(1) $P_{DISS\_FW\_MOSFET\_INST} = R_{DSON} \times I_{LOAD}^2$

The peak power disspation in the FW MOSFET is present only during the PWM off-phase, therefore, the average power dissipation in the free-wheeling MOSFET over a PWM period is:

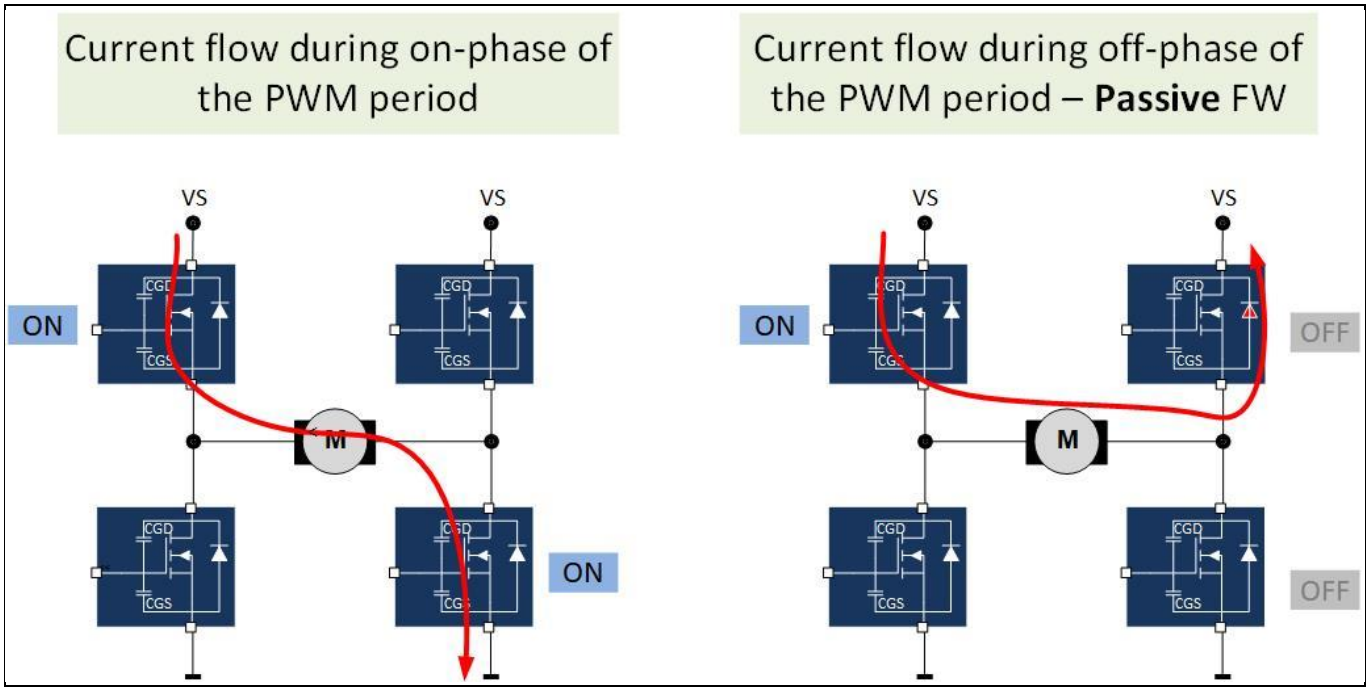
(2) $P_{DISS\_FW\_MOSFET\_AVR} = R_{DSON} \times I_{LOAD}^2 \times (1\text{-Duty})$ where Duty designates is the duty cycle (Ton / (Ton + Toff))

Note: The current ripple during the FW phase is neflected, in other words, it is assumed that the load current is constant over a PWM period

Note: For the sake of clarity, the passive FW during to avoid cross-currents is neglected, due to the short duration of this phase.

2.2.2 Passive free-wheeling

Figure 4 Current flow during the off-phase of the PWM period – Passive free-wheeling (with low- side PWM)



The peak power dissipation in the free-wheeling diode during the PWM off-phase and the average power dissipation over a PWM period are given respectively by (3) and (4).

(3) $P_{DISS\_FW\_PEAK} = V_F \times I_{LOAD}$

(4) $P_{DISS\_FW\_AVR} = V_F \times I_{LOAD} \times (1 - Duty)$

V_F designates the forward voltage of the MOSFET body diode

2.2.3 Example

Example: I_{LOAD} @70 % duty cycle = 15A, V_F = 1V, R_{DSON} = 7 mΩ

Power disspation	Active free-wheeling	Passive free-wheeling
Peak power dissipation[1] [W]	1.58 ☑	15 ☒
Average power dissipation [W]	0.47 ☑	4.5 ☒

[1] during the PWM off-phase

In this example, the active free-wheeling decreases the average power dissipation in the free-wheeling MOSFET by 4 W.

Assuming a junction-to-ambient thermal resistance ($R_{TH-JAMB}$) of 25 K/W, the active free-wheeling control scheme reduces the average FW MOSFET temperature by 100 K, compared to a passive free-wheeling scheme!

This is the reason why the active free-wheeling integrated in the TLE92108/4 reduces the system cost, compared to a solution with passive free-wheeling.

2.3 What is the utility of the watchdog?

The watchdog (WD) monitors the SPI communication between the TLE92108/4 and the microcontroller, avoiding uncontrolled motor activations.

Note that the WD can be activated or deactivated by SPI (Chapter 2.4, How to disable the watchdog?).
By default, the watchdog is enabled.

Case 1: The following sequence occurs:

1. one motor is turned on by the microcontroller
2. then a local failure on the SPI bus occurs, for example one of the SPI line is shorted

If the watchdog is deactivated prior to the failure: The SPI failure prevents any communication between the microcontroller and the TLE92108/4. The microcontroller cannot disable with an SPI command the gate drivers controlling the motor.
The remaining option consists in stopping the motor by pulling the EN pin to low, setting the device in sleep mode. This assumes however that the microcontroller is able to detect the SPI failure.

If the watchdog is activated prior to the failure: The WD cannot be served due to the faulty SPI bus. After the configured WD timeout (50 or 200 ms), a watchdog failure is detected by the TLE92108/4. The device goes in in fail safe mode and all all MOSFETs are turned off.

Case 2: The following sequence occurs:

1. one motor is turned on by the microcontroller
2. a failure leads to a microcontroller malfunction

If the watchdog is deactivated prior to the failure: The motor stays on, unless for example a safety logic detects a malfunction of the microcontroller and pulls the EN pin to low.

If the watchdog is activated prior to the failure: The WD cannot be served due to the microcontroller's malfunction. After the configured WD timeout (typ. 50 or 200 ms), a watchdog failure is detected, the TLE92108/4 go in fail safe mode and all MOSFETs are turned off. This results in a deactivation of all motors.

2.4 How to disable the watchdog?

The watchdog is one possible protection against unintentional motor activation or in case of system failure (e.g. SPI bus issues, microcontroller malfunction…), therefore it recommended to keep it enabled. However it may be convenient to disable the WD during the development phase.

The following sequence disables the watchdog:

1. SPI Frame 1: Set the UNLOCK bit (GENCTRL1)

Important: While setting the UNLOCK bit, the WDTRIG bit must be inverted to avoid a wrong watchdog failure. The default value WDTRIG right after a power-on reset is 0.

2. SPI Frame 2: Set WDDIS (in GENCTRL2)

If a SPI frame is added between SPI Frame 1 and SPI Frame 2, then the UNLOCK bit is cleared. Consequently the WD stays enabled despite the SPI Frame 2.

This sequence requiring **two consecutive SPI frames** and involving two different registers, prevents a deactivation of the watchog "by accident" with one single SPI command (e.g. due to a flipped bit).

2.5 What is the difference between the drain-source overvoltage and the overcurrent detection?

Two complementary protection strategies are implemented in the TLE92108/4 to detect short circuits while a MOSFET is on:

- the drain-source overvoltage monitoring
- the overcurrent detection with the shunt resistor and the current sense amplifier

Note: To avoid the MOSFETs activation in case of a short circuit in the first place, the TLE92108/4 also provide a **diagnostic in off-state** (refer to the dedicated application note and to the datasheet chapter 7.6). With this feature, short circuits can be detected prior to the MOSFET activation.

Table 2 Comparison between the V_{DS} overvoltage and the overcurrent detection

	VDS overvoltage	Overcurrent detection
Type of detected short circuits	Hard short circuits (very low impedance)	Soft short circuits / overloads
Precision of the short circuit current detection (i.e. current threshold)	Low	High
Reaction time	~ 0.5 µs to 3 µs	~ 6 µs to 100 µs

Drain-source overvoltage

The drain-source overvoltage detection is intended to detect hard short circuits, i.e. with a low impedance. As described in the datasheet, this protection monitors the drain-source voltage of the activated MOSFETs and turns off the impacted MOSFETs when the drain-source voltage (V_{DS}) exceeds the configured threshold for a duration longer than the configured filter time (t_{FVDS} is set by control bit TFVDS).

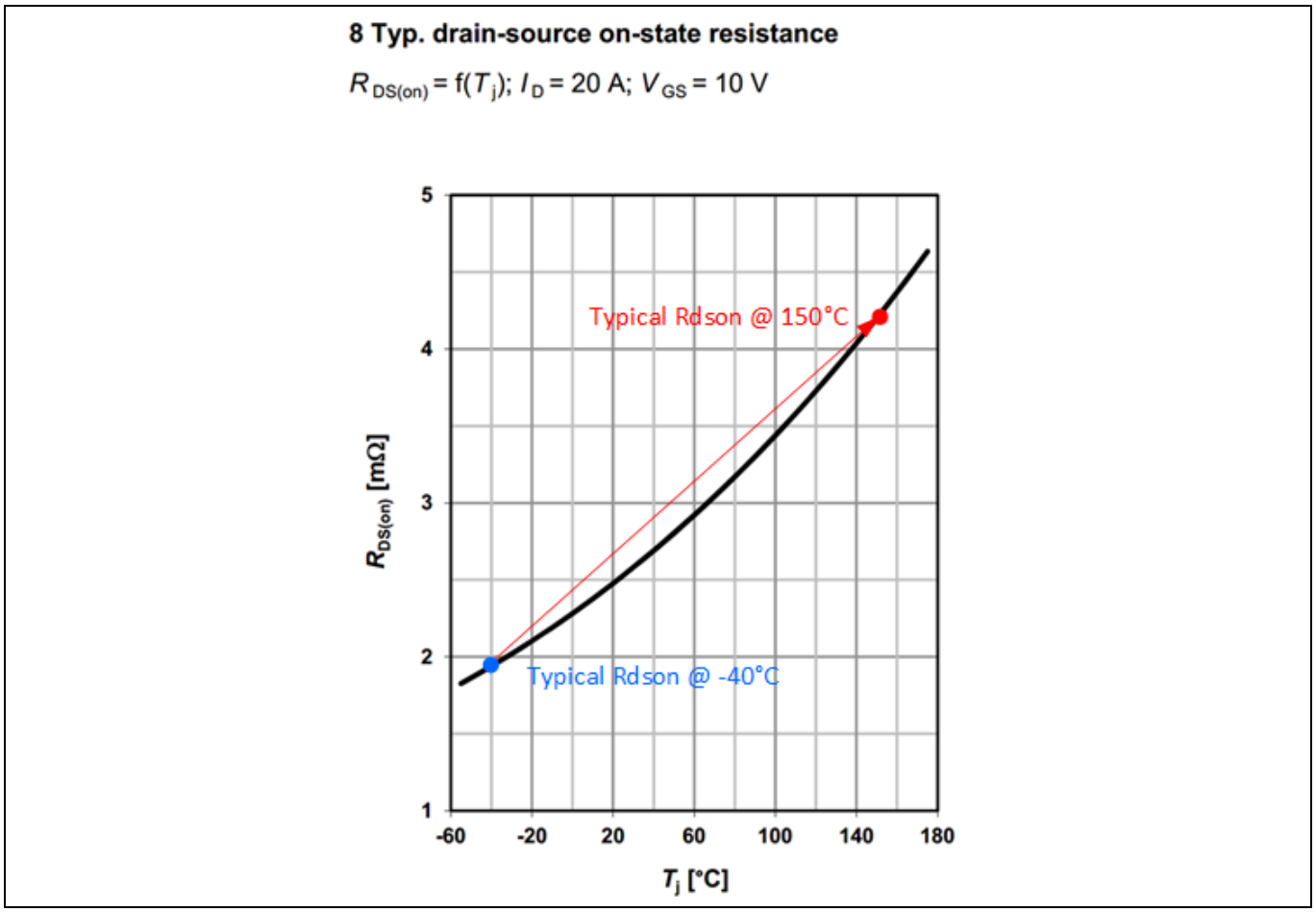
The drain-source overvoltage detection is fast but not precice:

V_{DS} = Rdson x I_{DS} where Rdson is the MOSFET drain-to-source resistance in on-state, I_{DS} is the MOSFET drain-to-source current.

However, the MOSFET Rdson:

- has a spread inherent to the production process
- varies with the junction temperature of the MOSFET. Depeding on the MOSFET technology, the Rdson of a given MOSFET can double from - 40 °C to 150 °C

Figure 5 Example of Rdson variation with the temperature. Source datasheet: IPZ40N04S3R1



The drain-source overvoltage detection of the TLE92108/4 is optimized for speed (at the expense of the precision). The thresholds are specified with a tolerance of +/- 25 %.

The resulting load current triggers a drain-source overvoltage can be high (e.g. at low Rdson, low MOSFET junction temperature, max. VDS overvoltage threshold …).

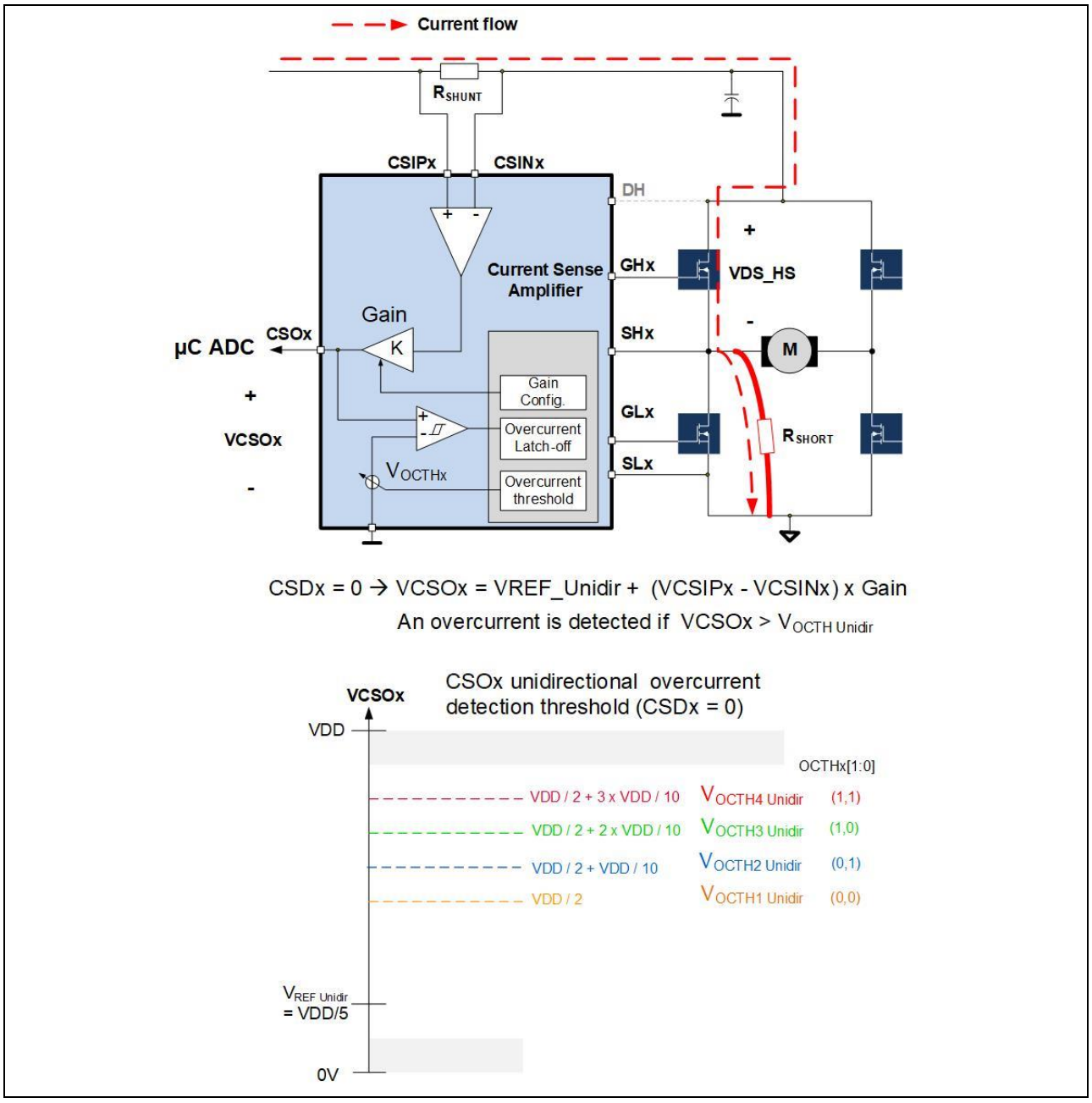
Therefore the reaction time must be very short to prevent MOSFET damages: t_{FVDS} is typically 0.5 µs / 1 µs / 2 µs or 3 µs, depending on the SPI configuration.

Due to the tolerance of the short circuit detection, some margin must be taken into account, in order to avoid a wrong short-circuit detection under normal load conditions.

Overcurrent detection

The overcurrent detection is based on the monitoring of the voltage drop across a shunt resistor (0), which has a much lower thermal coefficient than the R_{DSON} of a MOSFET and a lower tolerance.
This overcurrent thresholds have a tolerance of +/- 4 %.

Figure 6 Overcurrent detection with shunt resistor in high-side configuration, current sense amplifier in unidirectional configuration (CSDx = 0)



Due to the higher precision of the overcurrent detection the overcurrent threshold can be set to a lower level compared to the drain-source overvoltage.

The lower current threshold which triggers an overcurrent detection results in lower stress for the MOSFET, and allows the usage of longer filter times: t_{FOC} can be typically set between 6 µs to 100 µs.

2.6 How to configure the sensing of the drain voltage of the high-side MOSFETs?

The TLE92108/4 use the voltage at the DH pin or at the CSIN1 pin as the drain voltage for each high-side MOSFETs.

The following examples are applicable for the TLE92108. The same considerations can be extended to the **TLE92104 for half-bridges 1-4**.

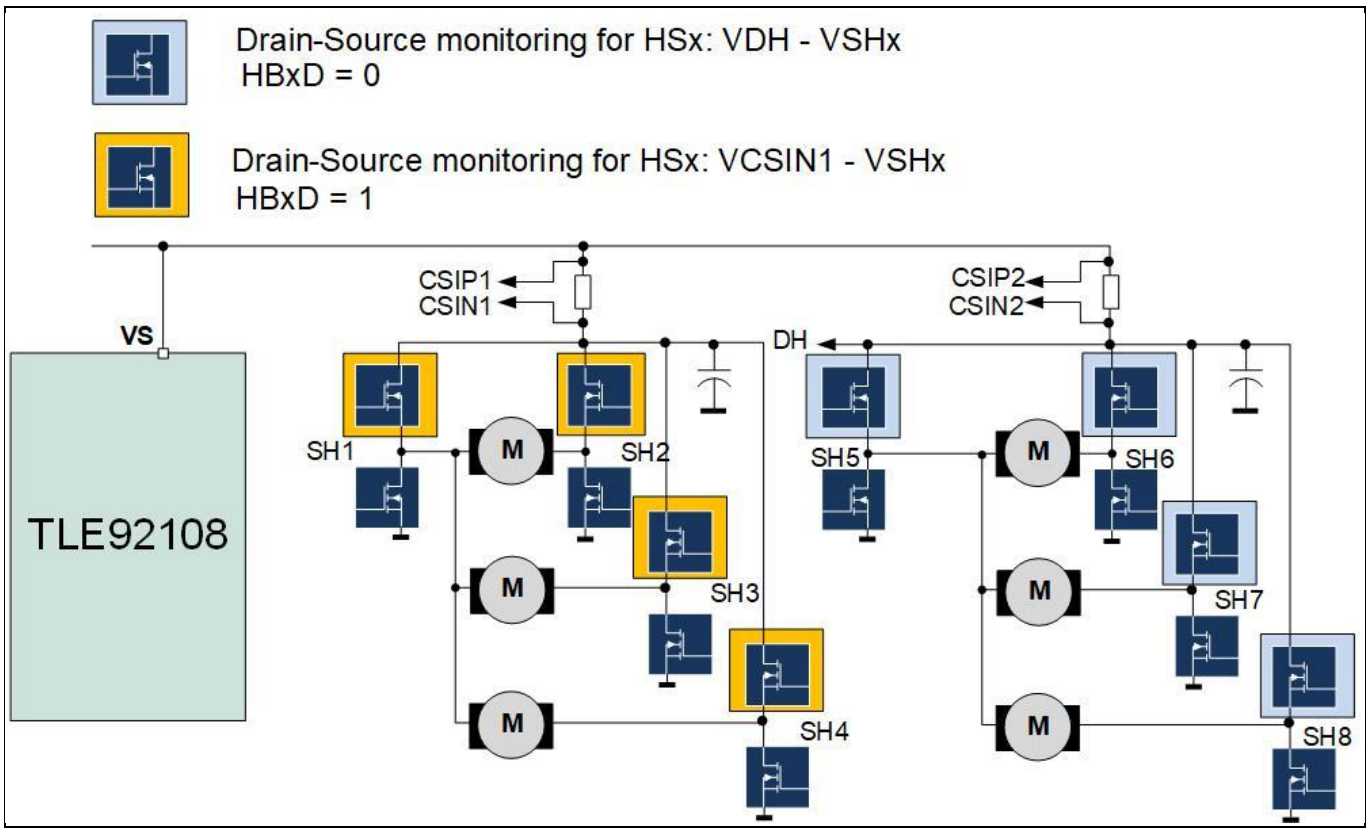
The correct content of the control bits HBxD, depends on the position of the shunt resistors.
A wrong configuration leads to a wrong drain-source overvoltage detection.
Three configurations are considered in this section for the TLE92108.

2.6.1 Both shunt resistors are in high-side configuration

If both shunt resistors are in high-side configuration (refer to Figure 7), the drains of the high-side MOSFETs have different voltages due to the voltage drop accorss the shunt resistors. Therefore the drain reference for the drain-source overvoltage detection can be set for each MOSFET group:

- the drains of HS1-HS4 **may not** be connected to DH
- the drains of HS5-HS8 **must be** connected to DH
- CSIN1 is used as drain voltage reference: HB1D = HB2D = HB3D =HB4D = 1
- DH is used as drain voltage reference: HB5D = HB6D = HB7D =HB8D = 0

Figure 7 Both shunt resistors are in high-side configuration

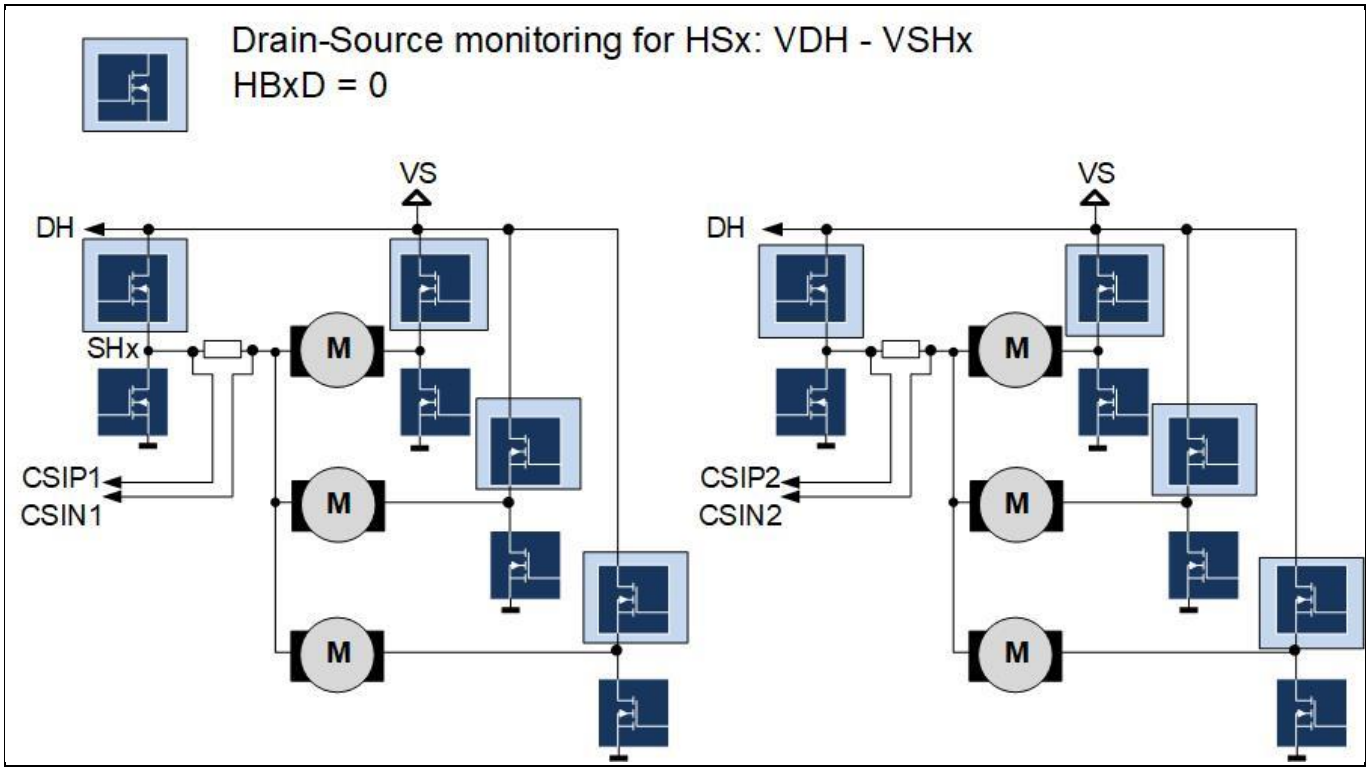


2.6.2 Both shunt resistors are in series to the motors

If both shunt resistors are in series to the motors (refer to Figure 8):

- All high-side drains **must be** connected to DH
- HB1D = HB2D = HB3D =HB4D =HB5D = HB6D = HB7D =HB8D = 0

Figure 8 Both shunt resistors are in series to the motor

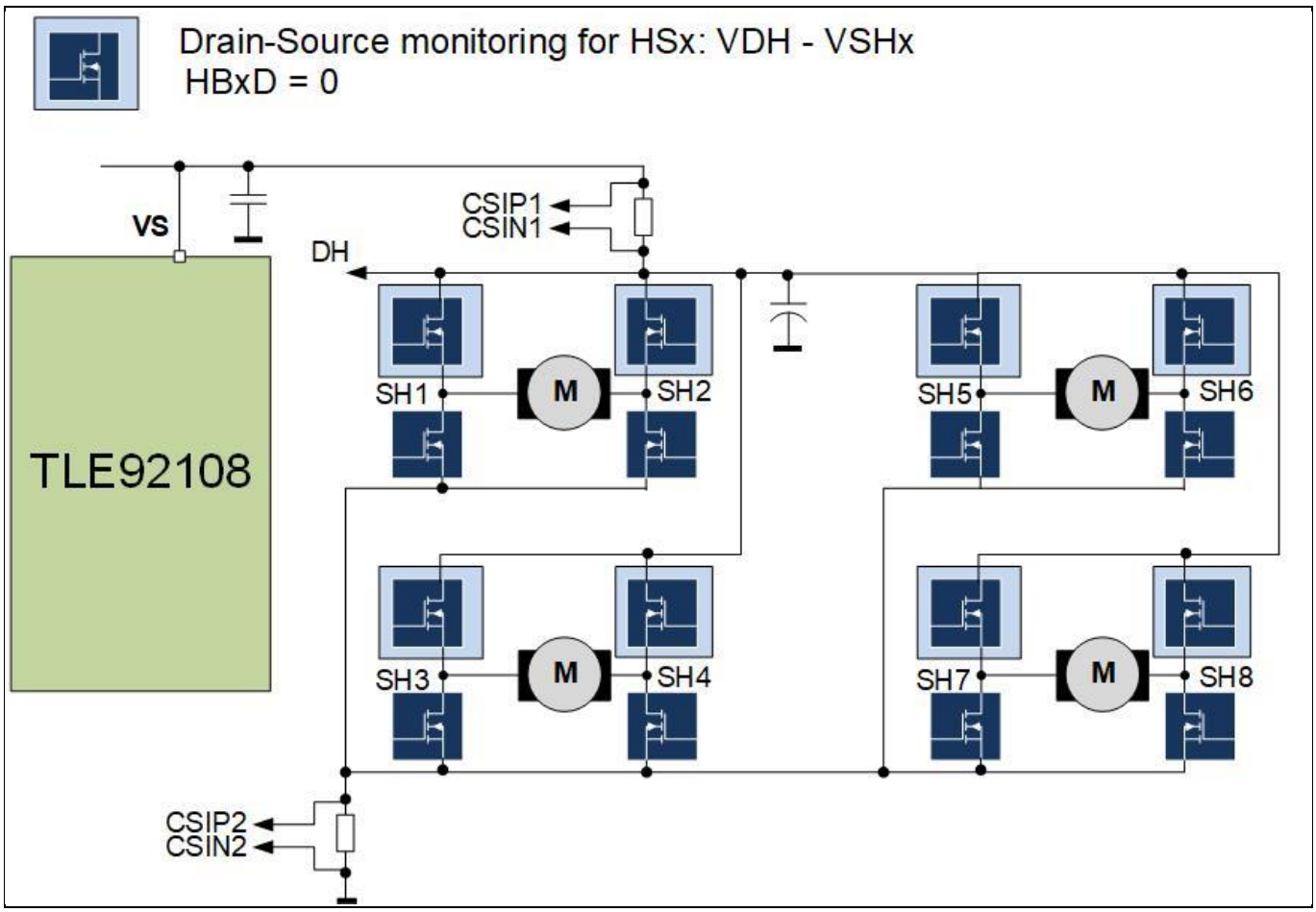


2.6.3 One shunt resistor is in high-side configuration, one shunt resistor is in low-side configuration

If one shunt resistor is in a high-side configuration, and the other shunt resistor is in a low-side configuration, several solutions are possible. (Figure 9) shows one possibility:

- All high-side drains **can be:**
  - Either connected to CSIN1 and HB1D = HB2D = HB3D =HB4D =HB5D = HB6D = HB7D =HB8D = 1
  - Or connected to DH and HB1D = HB2D = HB3D =HB4D =HB5D = HB6D = HB7D =HB8D = 0

Figure 9 One shunt resistor is in high-side configuration, the other shunt resistor is in low-side configuration



2.7 Why is the gate of the high-side MOSFETs at the VS potential while the MOSFETs are off?

When the bridge driver is **in active mode** (control bit BD_PASS = 0) and both MOSFETs of all half-bridges are off (HBxMODE = 00_B or 11_B), then the MOSFETs are indeed **actively turned off** by the current sinks of the **floating gate drivers** (Refer to Figure 10).

Indeed, the current sink between GHx (gate of high-side x) and SHx (source of high-side x) keeps the the gate of the high-side MOSFETs discharged, therefore $\mathbf{V_{GHx} = V_{SHx}}$.

If no short circuit is present at SHx and the pull-down diagnostic currents are deactivated, then SHx is pulled up to VS by the pull-up diagnostic current (which is also enabled if the bridge driver is in active mode):

$\mathbf{V_{GHx} = V_{SHx} = VS}$, theferore $V_{GHx} \neq 0$ V.

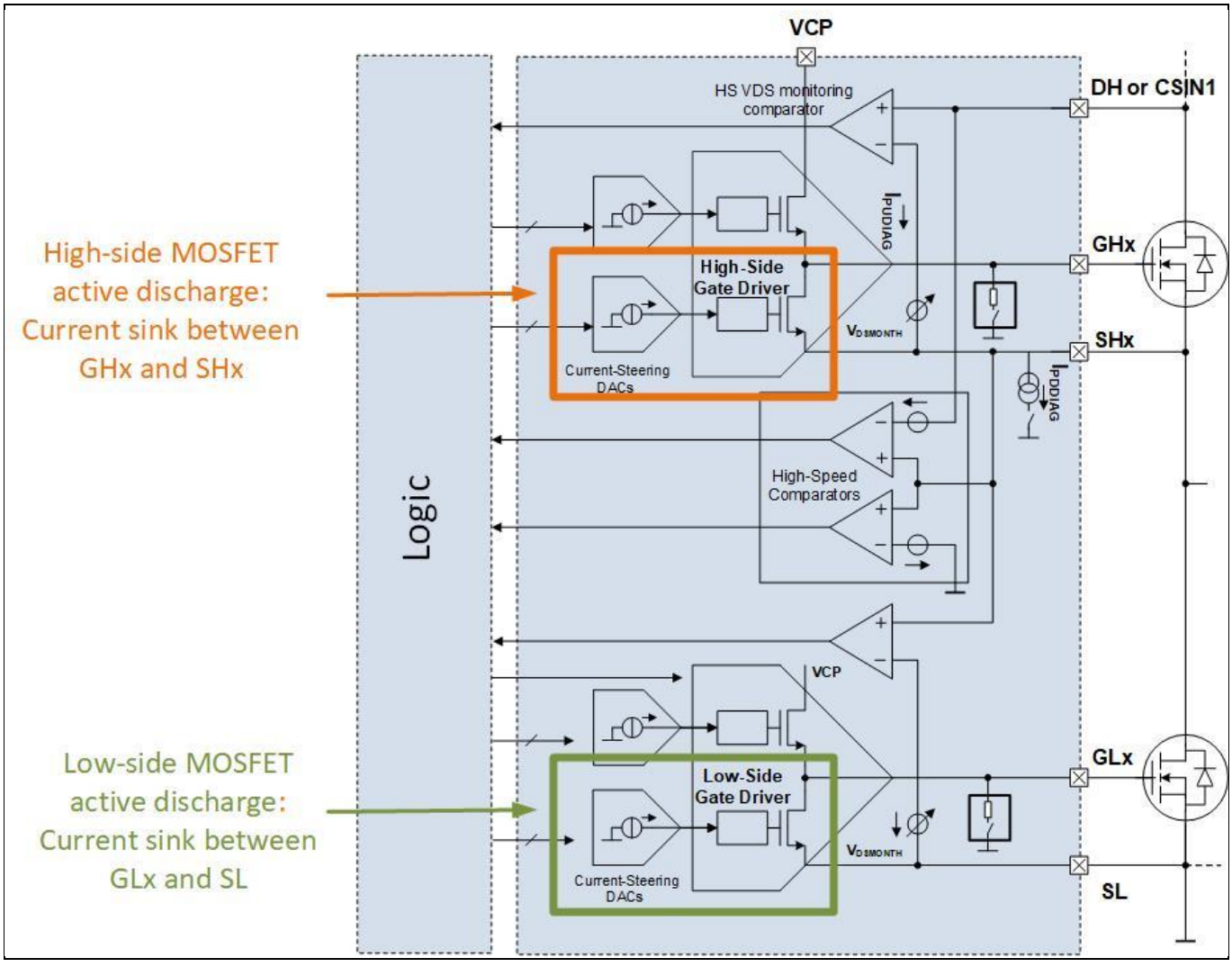


Figure 10 Gate driver active discharge for one half-bridge

Although $V_{GHx} \neq 0$ V, the high-side MOSFET is off because $\mathbf{V_{GHSx} = V_{GHx} - V_{SH} \sim 0\ V}$

Note: If SHx is pulled down e.g. by a pull-down diagnostic current, then $V_{GHx} = V_{SH} = GND$. Likewise, a current sink between the GLx and SL pins keeps the gate of the low-side MOSFETs discharged. As V_{SL} is connected to GND, then $V_{GLx} = GND$.

2.8 What is the difference between active and passive discharge?

The active discharge for the high-side and low-side MOSFETs is described in the chapter 2.7 and highlighted in Figure 10.

In normal mode, the half-bridges are in **passive discharge if BDPASS = 1** and **all HBxMODE = 00_B or 11_B**.

The passive discharge consists of a pull-down resistor:

- Between GHx and GND to keep the high-side MOSFETs off
- Between GLx and GND to keep the low-side MOSFETs off

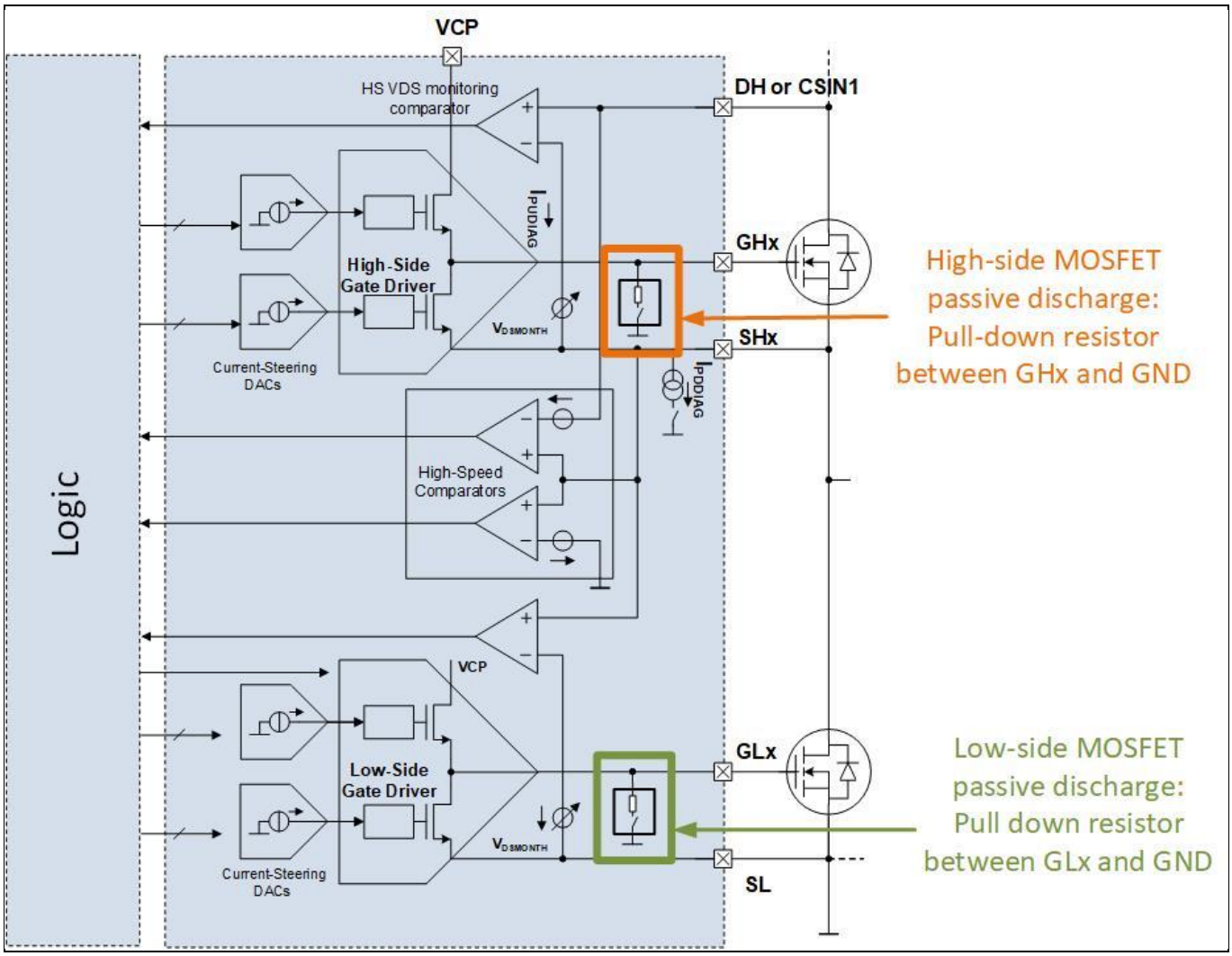


Figure 11 Gate driver passive discharge for one half-bridge

The passive discharge is enabled for example:

- in sleep mode, in order to reduce the current consumption of the device
- in active mode, while no MOSFET is activated, in order to reduce the current consumption
- to ensure the termination of GHx and GLx when an active discharge is not possible (e.g. when the charge pump is deactivated or in case of charge pump undervoltage):
    - Overtemperature event
    - VS undervoltage / overvoltage event
    - Charge pump undervoltage
    - Fail safe mode

2.9 Why is the power-on reset bit of the global status byte active low?

Unlike the other status bits of the global status byte, the (negated) power-on reset (NPOR) bit is active low:

- NPOR = 0 after a power-on reset of the device. NPOR stays 0 until GENSTAT is cleared
- NPOR = 1 if GENSTAT is cleared

The arbitrary polarity definition of this bit allows the microcontroller to detect a shorted SDO line to GND: After a clear command on GENSTAT, NPOR should be 1(the power on-reset is “cleared”), unless SDO is shorted to GND.

If the SDO line is shorted to GND or the device is in sleep mode, then the microcontroller reads NPOR = 0, despite the attempt to clear the GENSTAT register.

Note: The microcontroller can detect a short circuit to VDD if the most significant bit (MSB) of the Global Status Register is set. Indeed, according to the SPI protocol of the TLE92108/4, the MSB of the Global Status Register must be 0, unless the SDI line is shorted to VDD.

3 History

Document version	Date of release	Description of changes
1.0	2019-09-23	First release
1.1	2020-08-24	Document extended to TLE92104 Chapter 2.6: Updated cross-references to figures Chapter 2.6.1: corrected bit setting

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