HFC0512

Fixed-Frequency Flyback Controller with Ultra-Low No-Load Power Consumption

DESCRIPTION

The HFC0512 is a fixed-frequency, current-mode controller with internal slope compensation. It is specifically designed for medium-power, offline, flyback, switch-mode power supply applications. The HFC0512 is a highly efficient, green-mode controller. At light loads, the controller freezes the peak current (I_{PEAK}) and reduces its switching frequency (f_{SW}) to 27kHz for excellent light-load efficiency. At very light loads, the controller enters burst mode to achieve very low standby power consumption.

The HFC0512 offers frequency jittering to help dissipate energy generated by the conducted noise.

The HFC0512 features an over-power compensation (OPC) to reduce the difference between the low line and high line for the overload protection (OLP) point.

Full protection features include thermal shutdown, V_{CC} under-voltage lockout (UVLO), OLP, over-voltage protection (OVP), and brownout protection.

The HFC0512 is available in an SOIC8-7A package.

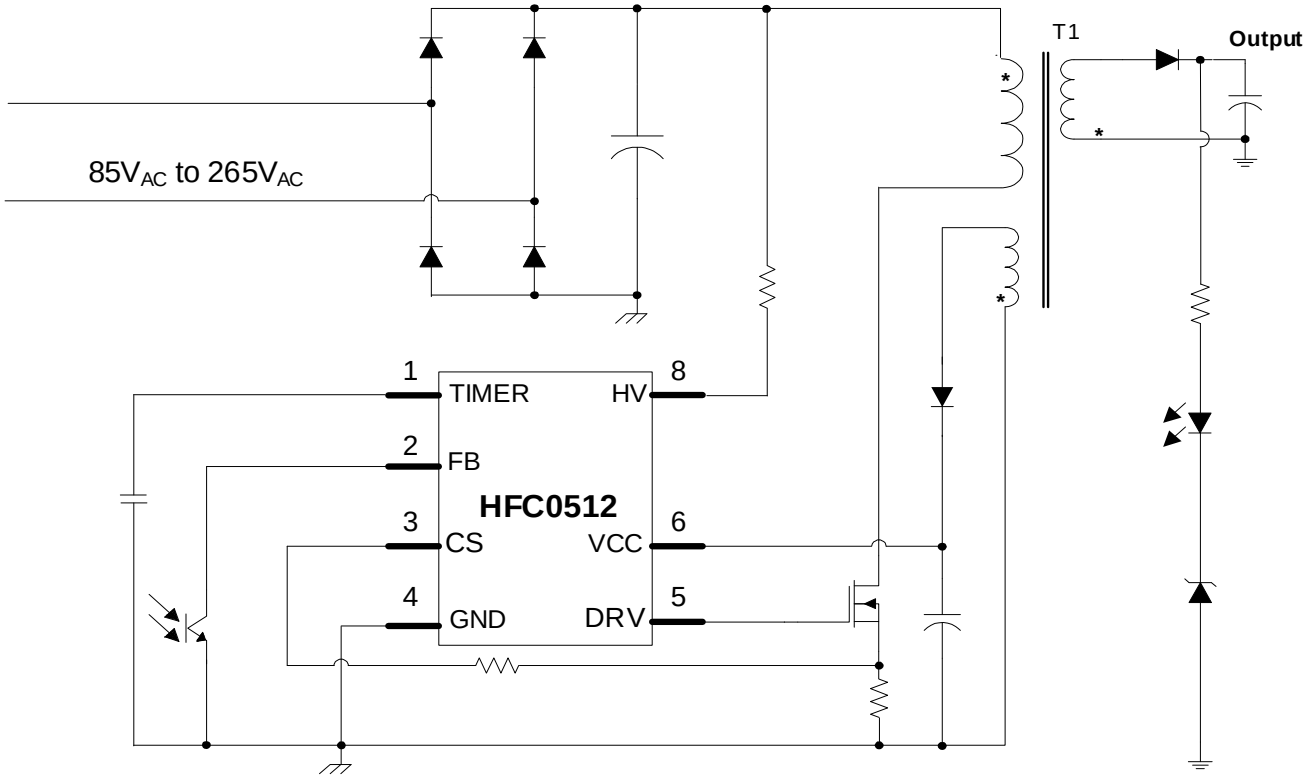
FEATURES

- Fixed-Frequency, Current Mode Control with Internal Slope Compensation
- Frequency Foldback Down to 27kHz at Light Loads
- Burst Mode for Low Standby Power Consumption, Meeting EuP Lot 6 Standard
- Frequency Jittering for Reduced Electromagnetic Interference (EMI)
- Adjustable Over-Power Compensation
- Internal High-Voltage Current Source
- V_{CC} Under-Voltage Lockout (UVLO) Protection with Hysteresis
- Brownout Protection via the HV Pin
- Overload Protection (OLP) with Configurable Delay
- Thermal Shutdown (Auto-Restart with Hysteresis)
- Latch-Off Protections:
  - External Over-Voltage Protection (OVP) and Over-Temperature Protection (OTP) via the TIMER Pin
  - V_{CC} OVP
- Short-Circuit Protection (SCP)
- Configurable Soft Start (SS)
- Available in an SOIC8-7A Package

APPLICATIONS

- AC/DC Power for Small and Large Appliances
- AC/DC Adapters for Notebook Computers, Tablets, and Smartphones
- Offline Battery Chargers
- LCD Televisions and Monitors

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HFC0512GS	SOIC8-7A	*See Below*	2

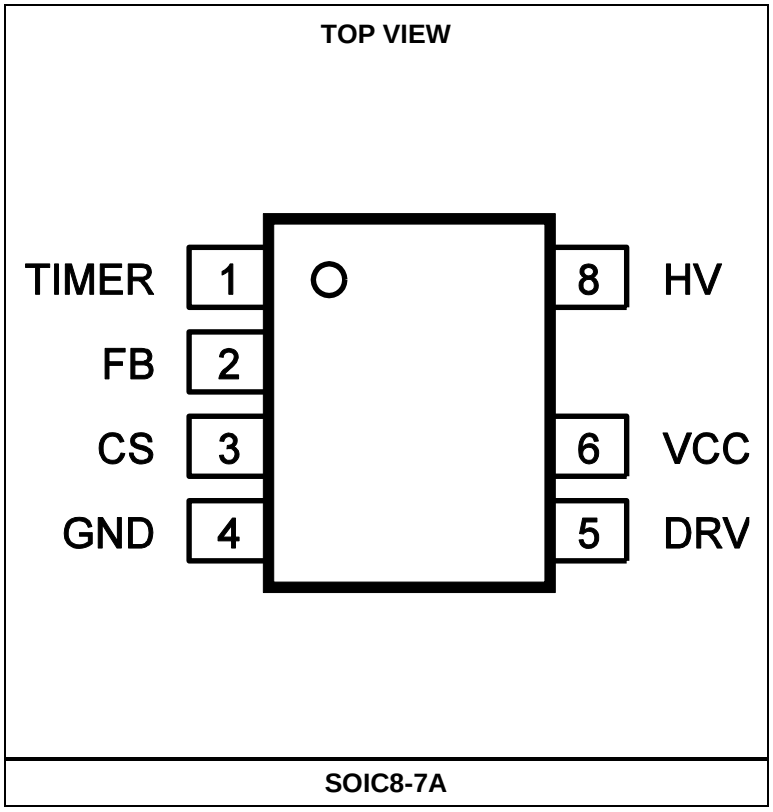
* For Tape & Reel, add suffix -Z (e.g. HFC0512GS-Z).

TOP MARKING

HFC0512
LLLLLLLL
MPSYWW

HFC0512: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	TIMER	**Timer.** The TIMER pin can set the time duration for overload protection (OLP) and brownout protection, as well as the soft start (SS) time and frequency jittering period. Pull TIMER low to latch off the device.
2	FB	**Feedback.** Use a pull-down optocoupler to control the output regulation.
3	CS	**Current sense.** The CS pin senses the primary-side current for current-mode operation and provides a mean for over-power compensation (OPC) adjustment.
4	GND	**IC ground.**
5	DRV	**Drive signal output.**
6	VCC	**Power supply.**
8	HV	**High-voltage current source.** The HV pin includes a brownout function.

ABSOLUTE MAXIMUM RATINGS (1)

HV ..... -0.7V to +700V
VCC, DRV to GND..... -0.3V to +30V
FB, TIMER, CS to GND ..... -0.3V to +7V
Continuous power dissipation (T_A = 25°C) (2)
.....1.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature.....-60°C to +150°C

ESD Ratings

Human body model (HBM)
HV 1.5kV
All other pins.....2kV
Charged-device model (CDM) 2kV

ESD Capability

ESD capability for machine mode 400V
ESD capability HBM
DRV.....3.5kV
HV 1kV
All other pins.....4kV

Recommended Operating Conditions (3)

Operating junction temp (T_J) .... -40°C to +125°C
Operating V_{CC} range ..... 9V to 24V

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8-7A.....	96.....	45 ...	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 18V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-Up Current Source (HV)						
Supply current from HV	I_{HV_400}	V_{CC} = 12V, V_{HV} = 400V	1.5	3.2	4	mA
	I_{HV_120}	V_{CC} = 12V, V_{HV} = 120V	1.5	3.1	3.9	
HV leakage current	I_{LK_400}	V_{HV} = 400V, V_{CC} increases to 18V, then decreases to 14V	1	16	28	µA
	I_{LK_200}	V_{HV} = 200V, V_{CC} increases to 18V, then decreases to 14V	1	13	25	µA
Breakdown voltage	V_{BR}	T_J = 25°C	700	790		V
Supply Voltage (V_{CC}) Management						
V_{CC} rising threshold at which current source turns off	V_{CC_OFF}		12.5	15.5	18	V
V_{CC} falling threshold above which SS is initiated	V_{CC_SS}	SS will be initiated if HV > HV_{ON} and V_{CC}>V_{CC_SS}	10.5	12	13	V
V_{CC} brown-in detection hysteresis	V_{CC_OFF} - V_{CC_SS}		1.35	3.5		V
V_{CC} falling threshold at which current source turns on	V_{CC_ON}		7.3	8.5	9.6	V
V_{CC} under-voltage lockout (UVLO) hysteresis	V_{CC_OFF} - V_{CC_ON}		5	7		V
V_{CC} recharge threshold (protection is initiated)	V_{CC_PRO}		4.9	5.5	6.2	V
V_{CC} falling threshold (latch-off phase ends)	V_{CC_LATCH}			2.5		V
Internal IC consumption	I_{CC}	V_{FB} = 2V, C_L = 1nF, V_{CC} = 12V	0.9	2.5	2.8	mA
		V_{FB} = 0.8V, C_L = 1nF, V_{CC} = 12V	1	1.35	1.7	
Internal IC consumption during latch-off phase	I_{CC_LATCH}	V_{CC} = V_{CC_OFF} - 1V, T_J = 25°C	520	700	880	µA
VCC over-voltage protection (OVP)	V_{CC_OVP}		24	26.5	28.5	V
OVP blanking time	t_{OVP}			60		µs
Brownout						
HV start-up threshold	HV_{ON}	V_{HV} increasing, T_J = 25°C	90	104	119	V
HV shutdown threshold	HV_{OFF}	V_{HV} decreasing, T_J = 25°C	82	95	110	V
Brownout hysteresis	ΔHV	T_J = 25°C	6.5	10	13.5	V
Timer duration for line cycle dropout	t_{HV}	C_{TIMER} = 47nF	40			ms
Oscillator						
Oscillator frequency	f_{OSC}	V_{FB} > 1.85V, T_J = 25°C	125	130	135	kHz
Frequency jittering amplitude	A_{JITTER}	V_{FB} > 1.85V, T_J = 25°C	±4.5	±5.7	±7.3	% of f_{OSC}
Frequency jittering entry	V_{FB_JITTER}				1.95	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 18V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency jittering modulation period	t_{JITTER}	C_{TIMER} = 47nF		3.7		ms
Current Sense (CS)						
Current-limit point	V_{ILIMIT}		0.93	1	1.07	V
Short-circuit protection (SCP) point	V_{SCP}		1.3	1.47	1.63	V
Current limit during frequency foldback	V_{FOLD}	V_{FB} = 1.85V	0.63	0.68	0.73	V
Current limit when burst mode entry	V_{IBURL}	V_{FB} = 0.7V		0.11		V
Current limit when burst mode exit	V_{IBURH}	V_{FB} = 0.8V		0.15		V
Leading-edge blanking time for V_{ILIMIT}	t_{LEB1}			350		ns
Leading-edge blanking time for V_{SCP}	t_{LEB2}			270		ns
Slope ramp compensation	S_{RAMP}		18	25	33	mV/μs
Feedback (FB)						
Internal pull-up resistor	R_{FB}		11.5	14	17	kΩ
Internal pull-up voltage	V_{DD}			4.3		V
V_{FB} to internal current setpoint division ratio	K_{FB1}	V_{FB} = 2V	2.55	2.8	3.05	-
	K_{FB2}	V_{FB} = 3V	2.8	3.1	3.4	-
V_{FB} falling threshold (burst mode entry)	V_{BURL}		0.63	0.7	0.77	V
V_{FB} rising threshold (burst mode exit)	V_{BURH}		0.72	0.8	0.88	V
Overload Protection (OLP)						
FB level at which the controller enters OLP after a dedicated time	V_{OLP}			4		V
Time duration before OLP when FB reaches the protection point	t_{OLP}	C_{TIMER} = 47nF	40			ms
Over-Power Compensation (OPC)						
V_{HV} to I_{OPC} ratio	K_{OPC}			0.52		μA/V
Current flowing out of the CS pin	I_{OPC}	V_{HV} = 120V, V_{FB} = 2.5V		0		μA
		V_{HV} = 155V, V_{FB} = 2.5V		13		μA
		V_{HV} = 310V, V_{FB} = 2.5V		93		μA
		V_{HV} = 380V, V_{FB} = 2.5V, T_J = 25°C	97	130	164	μA
V_{FB} below which compensation is removed	V_{OPC_OFF}		0.55			V
V_{FB} above which compensation is applied	V_{OPC_ON}				2.2	V
Frequency Foldback						
V_{FB} threshold during frequency foldback entry	V_{FB_FOLD}			1.8		V
Minimum switching frequency (f_{SW})	f_{SW_MIN}	T_J = 25°C	21	27	33	kHz
V_{FB} threshold during frequency foldback exit	$V_{FB\_FF\_EXIT}$			1		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 18V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Latch-Off Input (Integration in the TIMER Pin)						
Latch-off threshold	V_{TIMER_LATCH}		0.7	1	1.3	V
Blanking time during latch detection	t_{LATCH}			12		µs
Driver (DRV) Voltage						
DRV high voltage	V_{HIGH}	C_L = 1nF, V_{CC} = 12V		10.3		V
DRV clamped voltage	V_{CLAMP}	C_L = 1nF, V_{CC} = 24V		13.4		V
DRV low voltage	V_{LOW}	C_L = 1nF, V_{CC} = 24V		0		mV
DRV rise time	t_{RISE}	C_L = 1nF, V_{CC} = 16V		23		ns
DRV fall time	t_{FALL}	C_L = 1nF, V_{CC} = 16V		13		ns
Driver pull-up resistance	R_{DRV_PU}	C_L = 1nF, V_{CC} = 16V		10		Ω
Driver pull-down resistance	R_{DRV_PD}	C_L = 1nF, V_{CC} = 16V		8		Ω
Thermal Shutdown						
Thermal shutdown threshold (5)	T_{SD}			150		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			25		°C

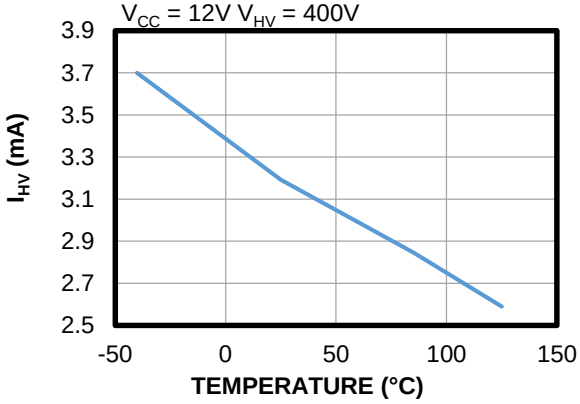
Note:

5) Guaranteed by design.

TYPICAL CHARACTERISTICS

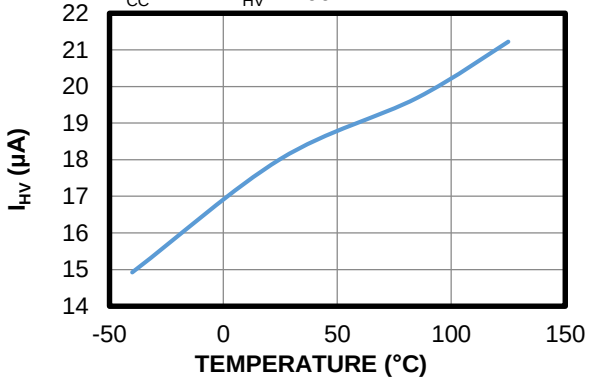
Supply Current from HV vs. Temperature

V_{CC} = 12V V_{HV} = 400V

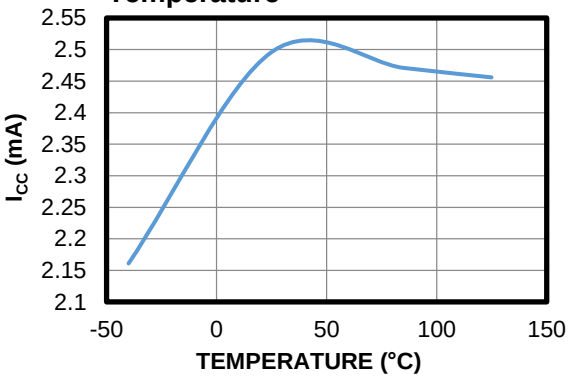


Leakage Current from HV vs. Temperature

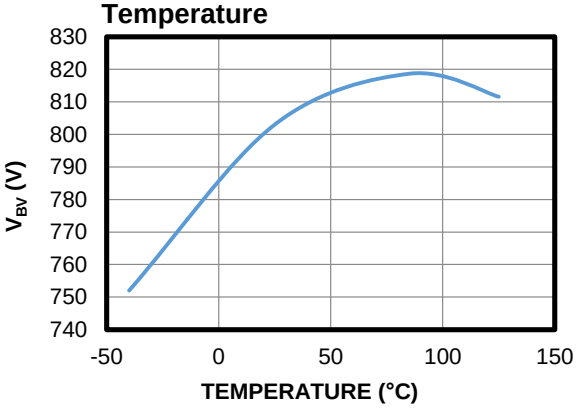
V_{CC} = 14V V_{HV} = 400V



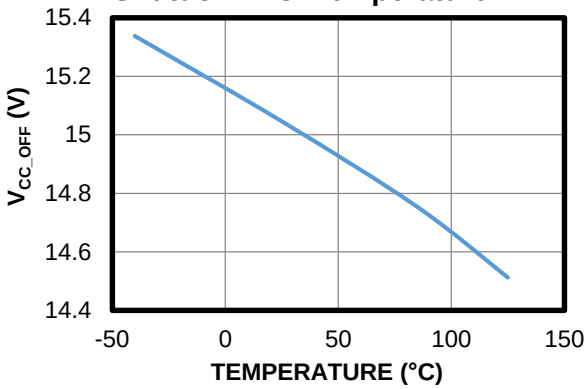
Internal IC Consumption vs. Temperature



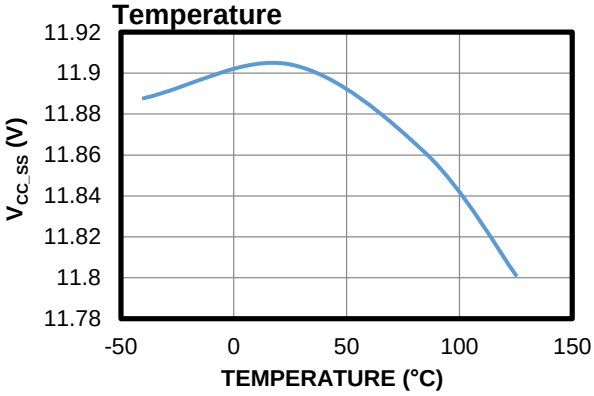
Break-Down Voltage vs. Temperature



V_{CC} Rising Threshold during Shutdown vs. Temperature

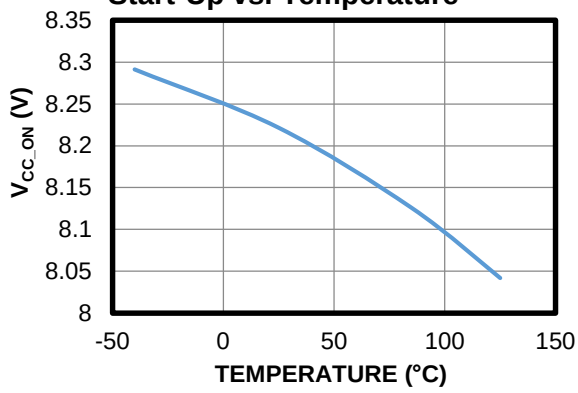


V_{CC} Falling Threshold for HV Turn-On Detection vs. Temperature

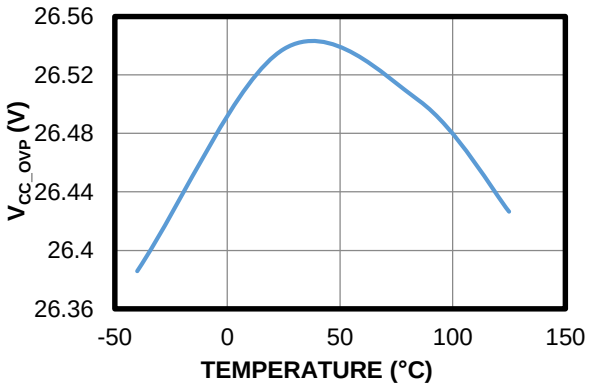


TYPICAL CHARACTERISTICS *(continued)*

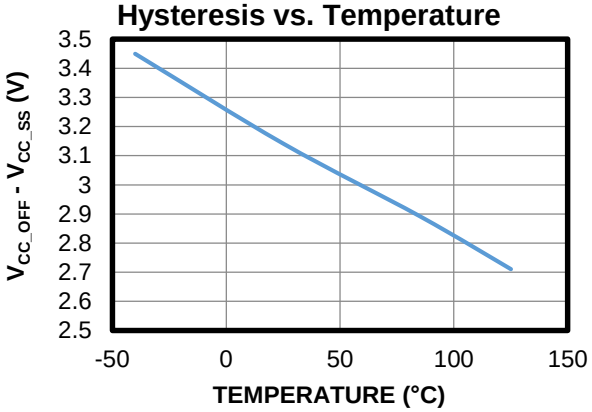
V_{CC} Falling Threshold during Start-Up vs. Temperature



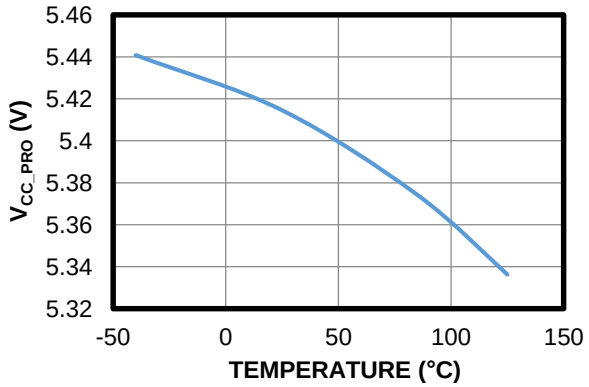
V_{CC} OVP vs. Temperature



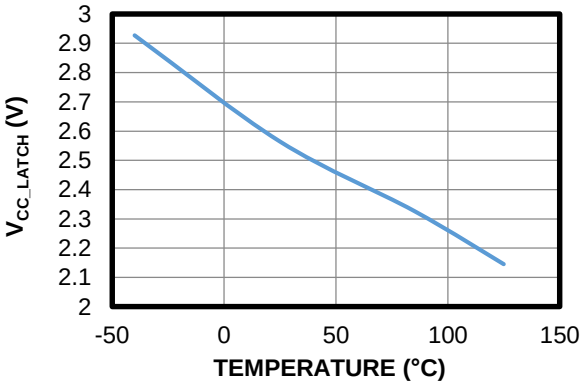
V_{CC} Brown-In Detection Hysteresis vs. Temperature



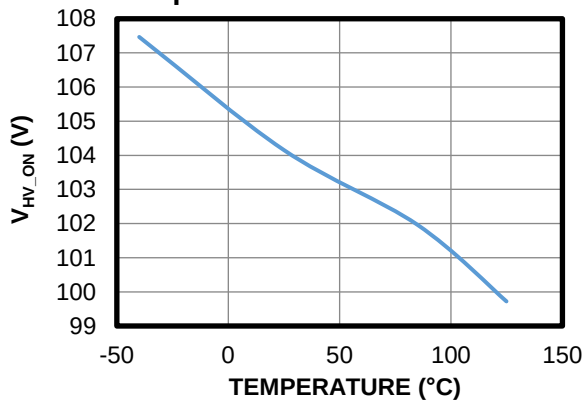
V_{CC} Recharge Threshold vs. Temperature



V_{CC} Falling after Latch-Off Phase vs. Temperature

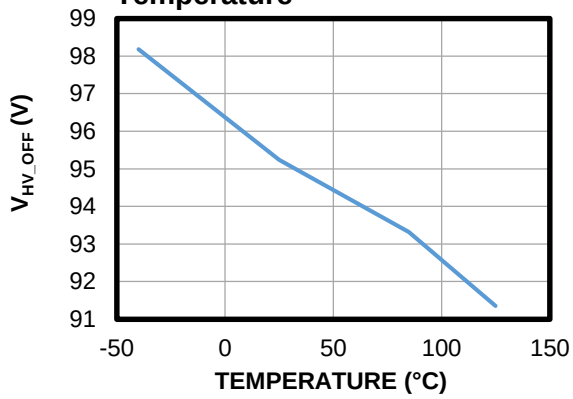


HV Turn-On Threshold vs. Temperature

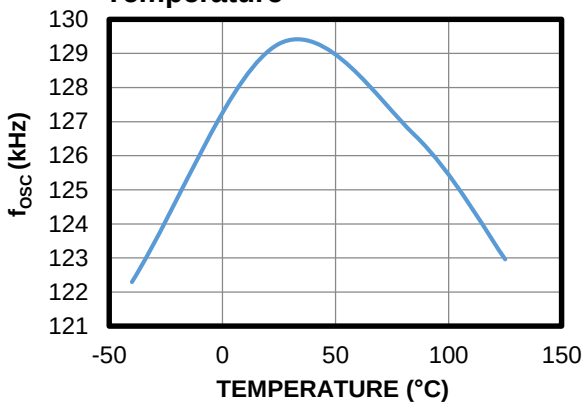


TYPICAL CHARACTERISTICS *(continued)*

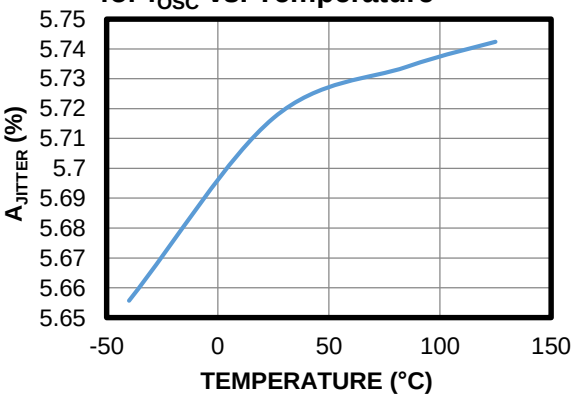
Supply Current from HV vs. Temperature



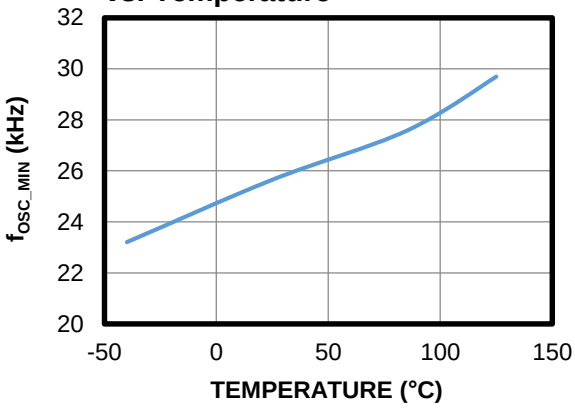
Oscillator Frequency vs. Temperature



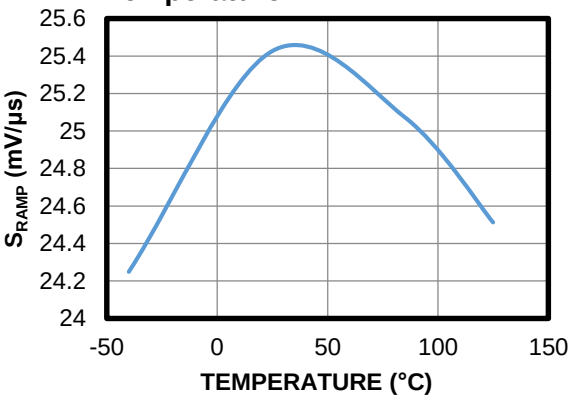
Frequency Jittering Amplitude for f_{OSC} vs. Temperature



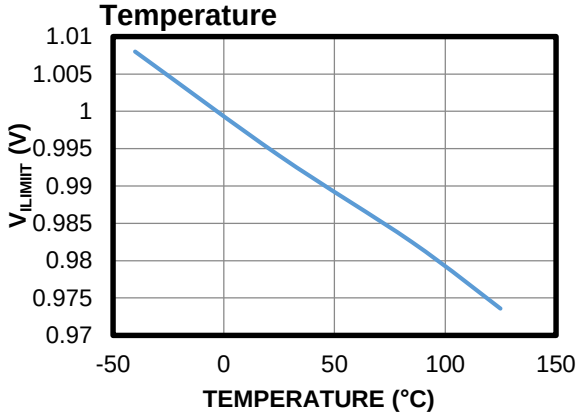
Minimum Switching Frequency vs. Temperature



Compensation Ramp Slope vs. Temperature

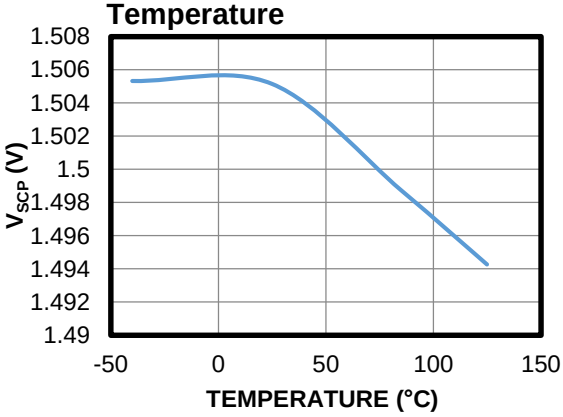


Current Limit Point vs. Temperature

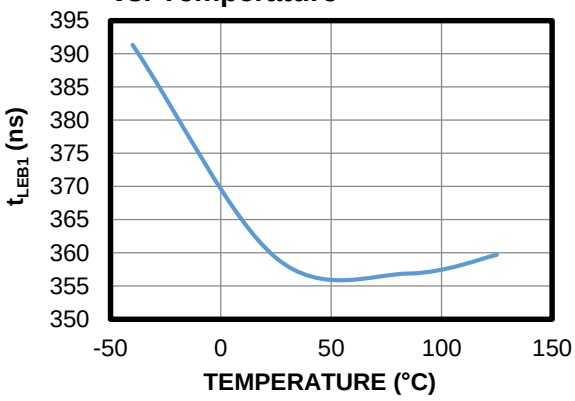


TYPICAL CHARACTERISTICS *(continued)*

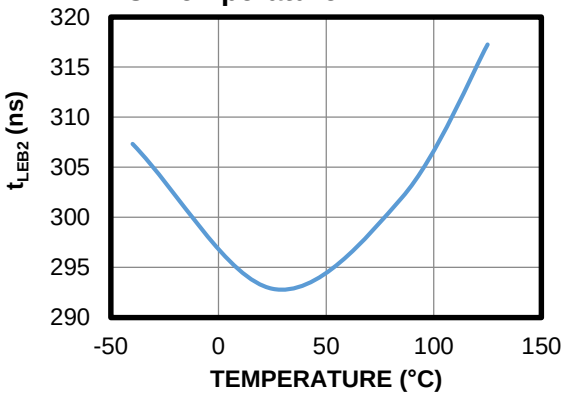
Short-Circuit Protection vs. Temperature



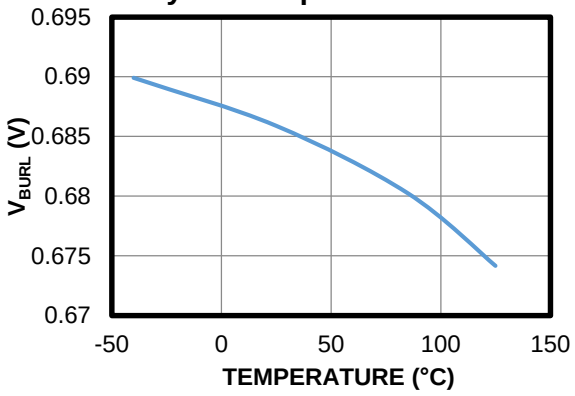
Leading Edge Blanking for V_{ILIMT} vs. Temperature



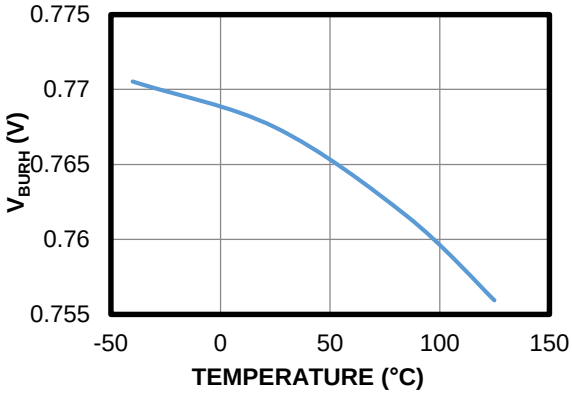
Leading Edge Blanking for V_{SCP} vs. Temperature



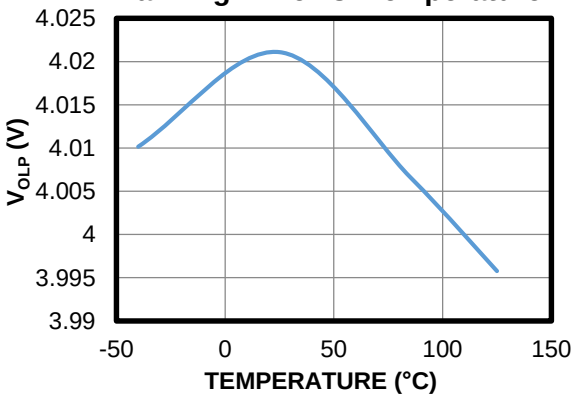
V_{FB} Falling during Burst Mode Entry vs. Temperature



V_{FB} Rising during Burst Mode Exit vs. Temperature



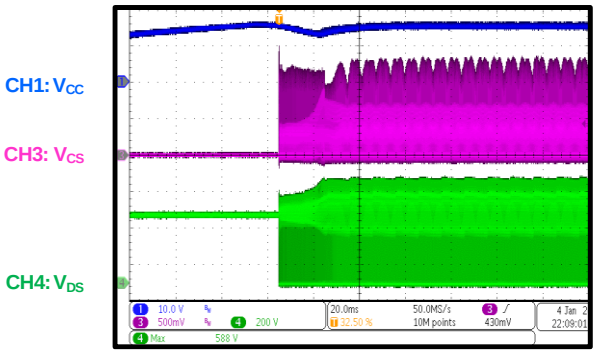
V_{FB} during OLP Entry after Blanking Time vs. Temperature



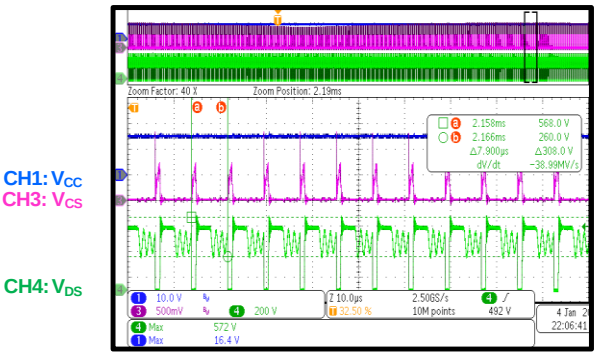
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 265V_{AC}, V_{OUT} = 12V, I_{OUT} = 1.67A, T_A = 25°C, unless otherwise noted.

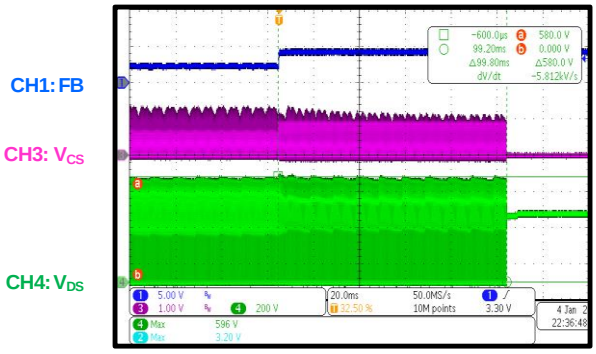
Start-Up



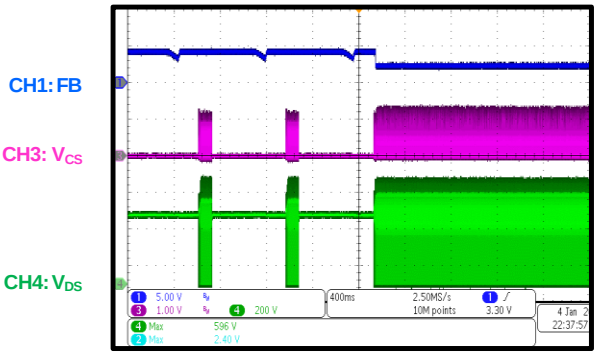
Steady State



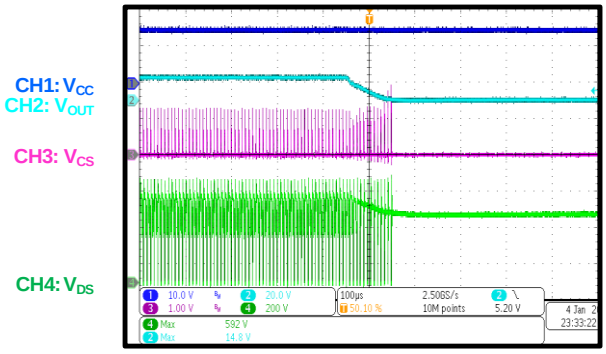
OLP Entry



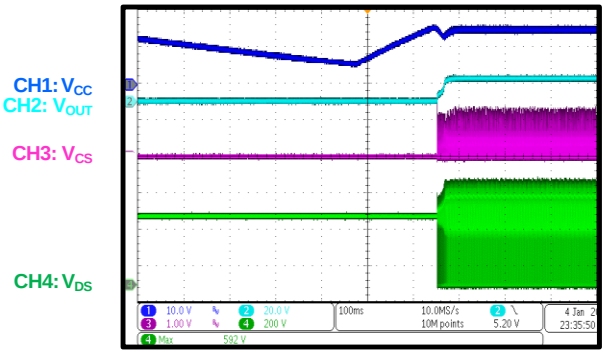
OLP Recovery



SCP Entry



SCP Recovery

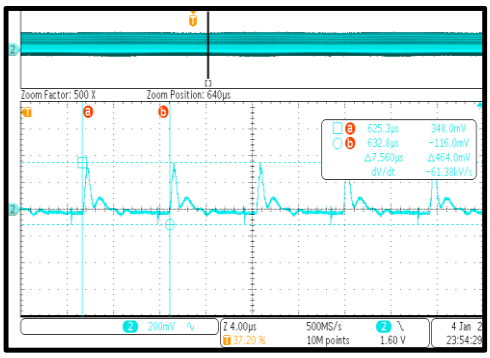


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

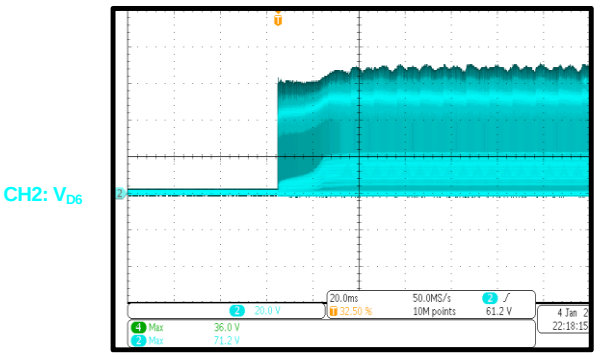
Performance waveforms are tested on the evaluation board. V_{IN} = 265V_{AC}, V_{OUT} = 12V, I_{OUT} = 1.67A, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple

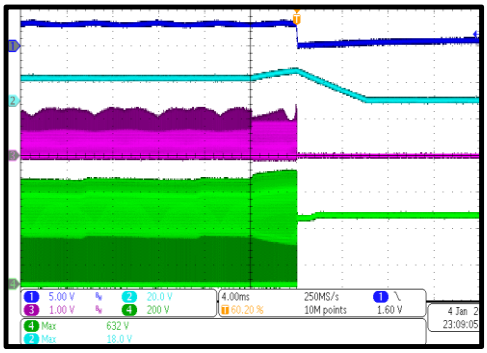
V_{IN} = 230V_{AC}



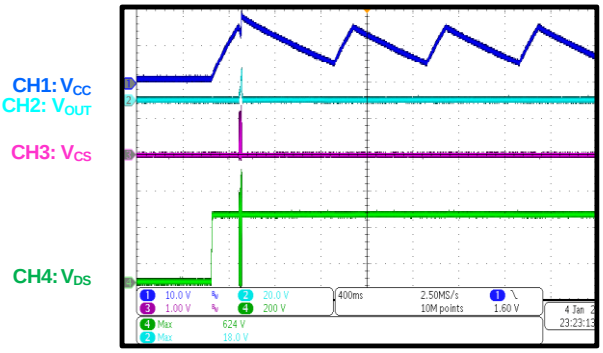
Secondary Diode Stress



TIMER Latch-Off Entry

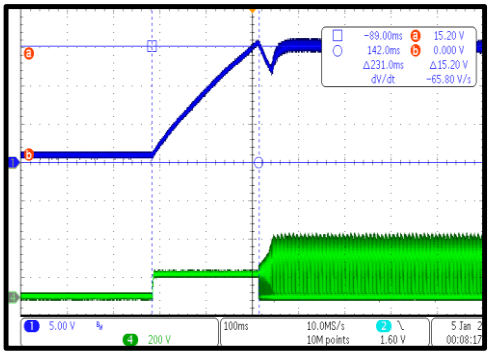


TIMER Latch-Off after Start-Up



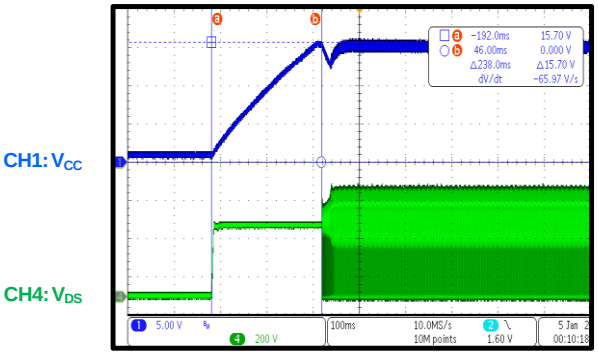
Turn-On Delay

V_{IN} = 85V_{AC}



Turn-On Delay

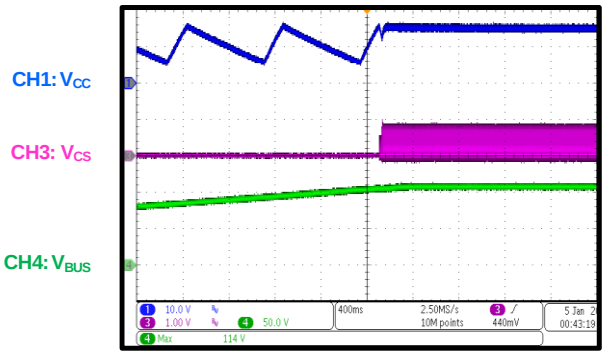
V_{IN} = 265V_{AC}



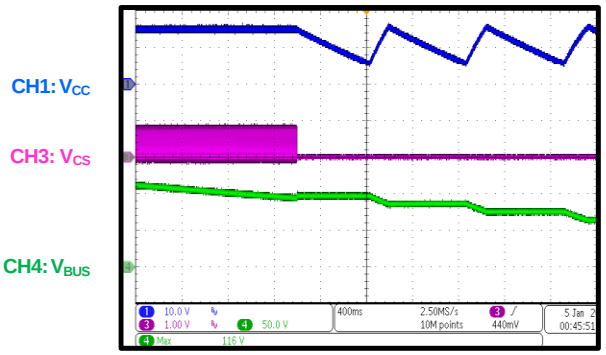
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 265V_{AC}, V_{OUT} = 12V, I_{OUT} = 1.67A, T_A = 25°C, unless otherwise noted.

Brown-In

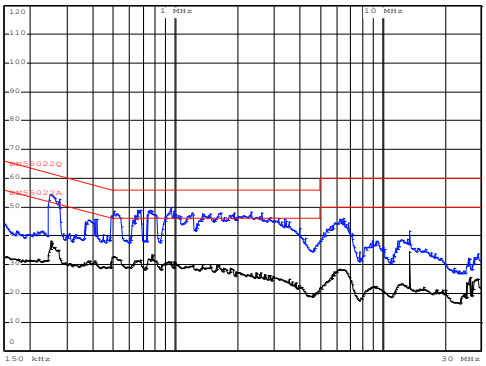


Brownout



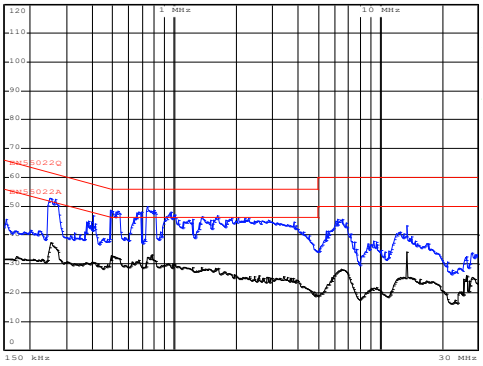
EMI

115V_{IN} live wire



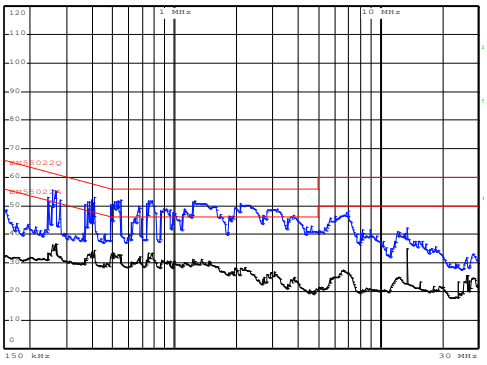
EMI

115V_{IN} neutral wire



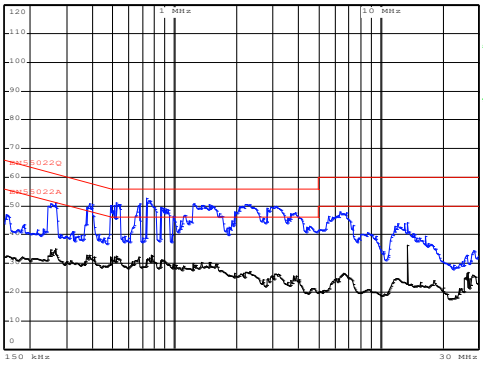
EMI

230V_{IN} live wire



EMI

230V_{IN} neutral wire



FUNCTIONAL BLOCK DIAGRAM

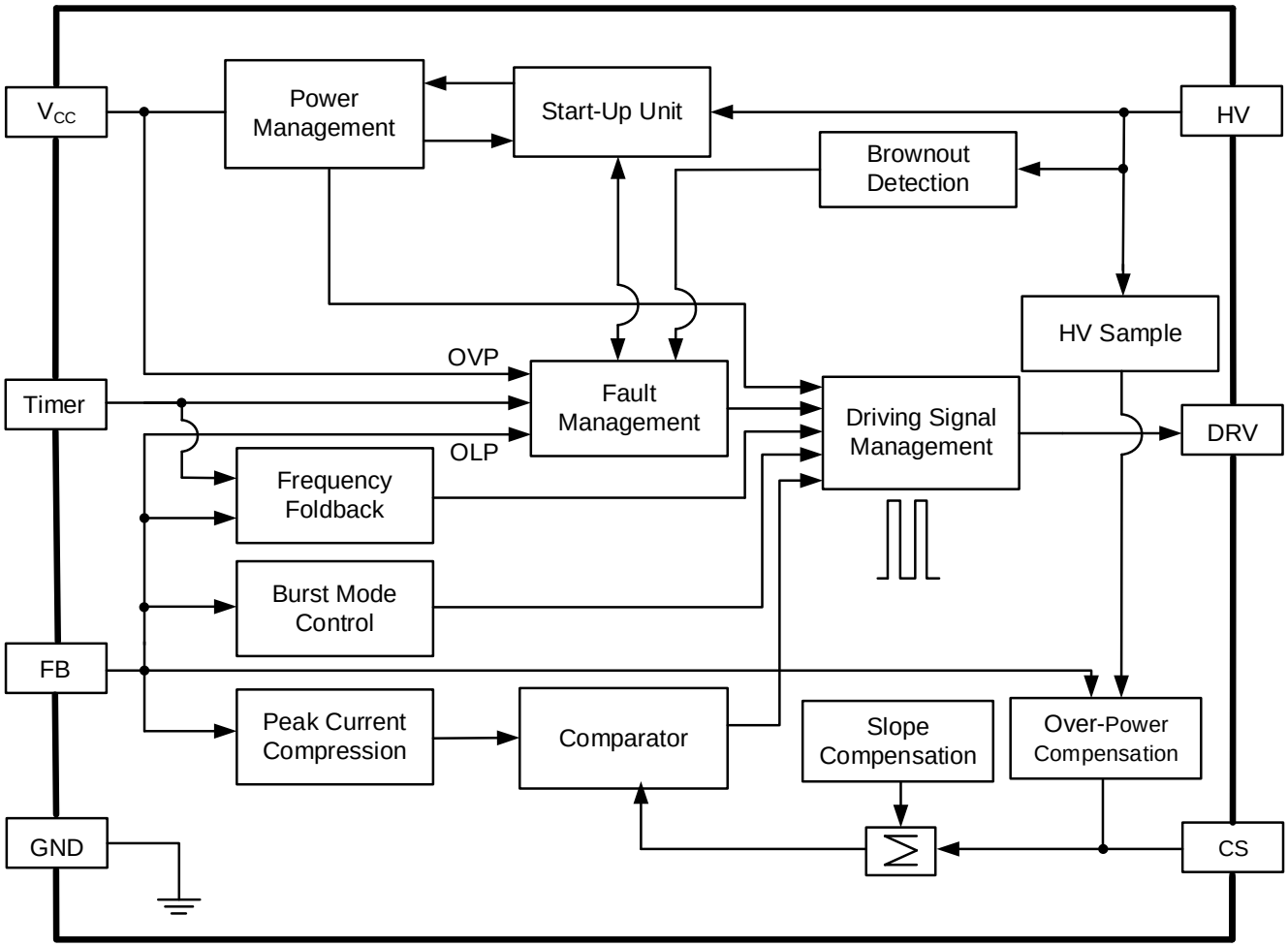


Figure 1: Functional Block Diagram

OPERATION

The HFC0512 is a fixed-frequency, current-mode controller with internal slope compensation. The HFC0512 incorporates all the necessary features to build a reliable switch-mode power supply. At light loads, the controller freezes the peak current (I_{PEAK}) and reduces its switching frequency (f_{SW}) down to 27kHz to minimize switching losses. When the output power (P_{OUT}) drops to a point where FB decreases to the V_{FB} falling threshold (V_{BURL}), the controller enters burst mode. Frequency jittering helps reduce electromagnetic interference (EMI). The HFC0512's high level of integration means that it requires a minimal number of external components.

Fixed Frequency with Frequency Jittering

Frequency jittering reduces EMI by spreading the energy over the frequency jittering range. Figure 2 shows a frequency jittering circuit.

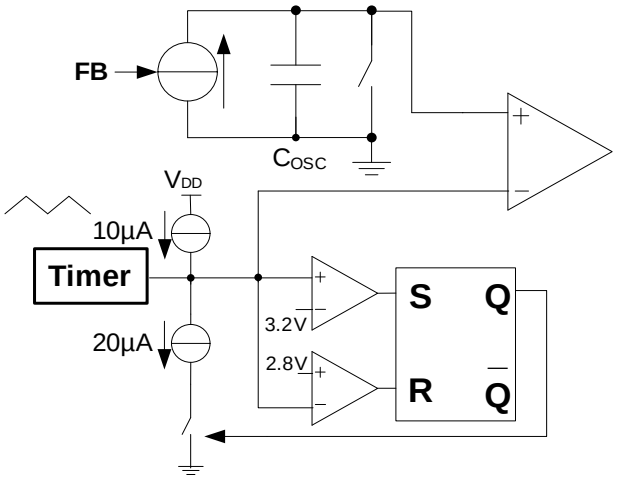


Figure 1: Frequency Jitter Circuit

A controlled current source (fixed at 5.4µA when V_{FB} = 2V) charges the internal oscillator capacitor (C_{OSC}). Comparing the capacitor voltage to the TIMER pin voltage determines f_{SW}. Frequency jittering is accomplished by varying V_{TIMER} between 3.2V and 2.8V (see Figure 3). The frequency jitter period (t_{JITTER}) can be determined with Equation (1):

$$T_{JITTER} = 2 \times \frac{C_{TIMER} \times (3.2V - 2.8V)}{10\mu A} \quad (1)$$

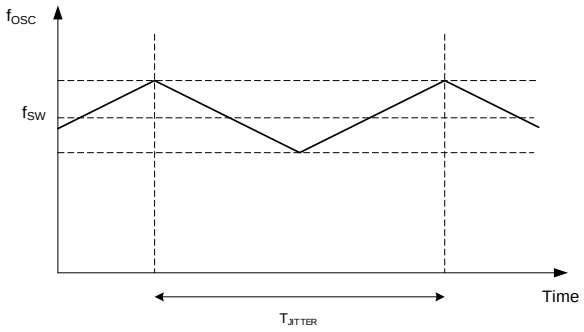


Figure 2: Frequency Jittering

Frequency Foldback

Frequency foldback improves efficiency under light-load conditions.

When the load decreases to a set level (1V < V_{FB} < 1.8V), the controller freezes I_{PEAK} (as measured on the CS pin, typically 0.7V) while reducing f_{SW} to 27kHz to reduce switching losses. If the load continues to decrease, I_{PEAK} decreases with the 27kHz fixed frequency to avoid audible noise. Figure 3 shows the relationship between f_{SW} and the feedback voltage (V_{FB}), as well as between I_{PEAK} (V_{CS}) and V_{FB}.

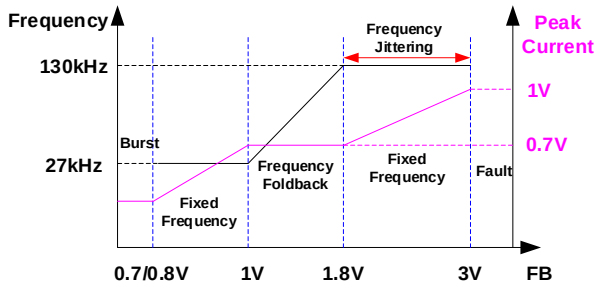


Figure 3: f_{SW} and I_{PEAK} (V_{CS}) vs. V_{FB}

Current-Mode Operation with Slope Compensation

V_{FB} controls the primary I_{PEAK}. When I_{PEAK} reaches the level determined by V_{FB}, DRV turns off. The internal slope compensation (typically 25mV/µs) allows the controller to operate in continuous conduction mode (CCM) with a wide input voltage (V_{IN}) range. The internal slope compensation avoids subharmonic oscillations above 50% duty cycle.

High-Voltage Start-Up Current Source with Brownout Detection

During start-up, the internal high-voltage (HV) current source supplies power to the controller. The controller turns off the current source once V_{CC} reaches V_{CC_OFF} (typically 15.5V) and detects the voltage on the HV pin. If the HV pin voltage (V_{HV}) exceeds HV_{ON} before V_{CC} drops down to V_{CC_SS} (typically 12V), the controller begins switching. If V_{HV} does not exceed HV_{ON}, the system treats this as a brownout and latches DRV low. When V_{CC} drops to V_{CC_PRO} (typically 5.5V), the high-voltage current source turns on to recharge V_{CC}. The auxiliary transformer winding supplies the IC after the controller starts switching. If V_{CC} falls below V_{CC_ON} (typically 8.5V), then the switching pulse stops and the current source turns on again. Figure 4 shows V_{CC} under-voltage lockout (UVLO).

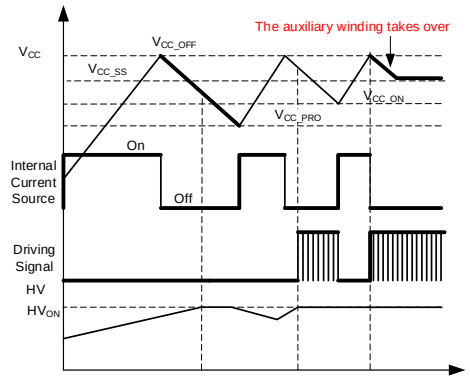


Figure 4: V_{CC} Under-Voltage Lockout

The lower V_{CC} UVLO threshold drops from V_{CC_ON} to V_{CC_PRO} when a fault protection is triggered, such as overload protection (OLP), short-circuit protection (SCP), over-temperature protection (OTP), or brownout.

Soft Start (SS)

The controller features a configurable external soft-start time (t_{SS}) via the TIMER capacitor (C_{TIMER}). As this capacitor charges from 1V to 1.75V using 25% of the normal charge current, the I_{PEAK} limit (V_{CS}) gradually increases from 0.25V to 1V, which also slowly increases f_{SW}. Figure 6 shows the SS function. Calculate t_{SS} with Equation (2):

$$t_{SS} = \frac{C_{TIMER} \times (1.75V - 1V)}{10/4\mu A} \quad (2)$$

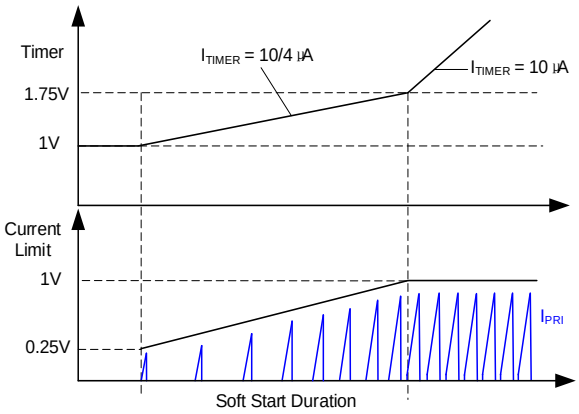


Figure 5: Soft Start

Burst Mode

The HFC0512 employs burst mode to minimize power dissipation under no-load and light-load conditions. As the load decreases, V_{FB} decreases. When V_{FB} drops below its falling threshold (V_{BURL}, typically 0.7V), the controller enters burst mode and the output stops switching. Then V_{OUT} drops, which causes V_{FB} to increase again. Once V_{FB} exceeds its rising threshold (V_{BURH}, typically 0.8V), the part resumes switching. Burst mode alternately enables and disables MOSFET switching, which reduces switching losses at no load or light loads.

Adjustable Over-Power Compensation

An offset current proportional to V_{IN} is added to the current-sense voltage (V_{CS}). The amount of compensation can be adjusted via the resistor placed in series with CS (R_{SERIES}). This allows for a more accurate output power (P_{OUT}) limit across the total V_{IN} range. Figure 7 shows the compensation current in relation to FB.

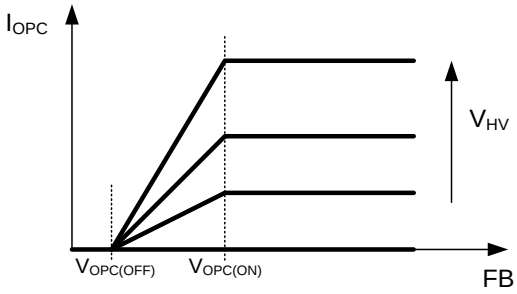


Figure 7: Compensation Current vs. FB and HV Voltage

Figure 8 shows the compensation current in relation to the peak voltage on HV.

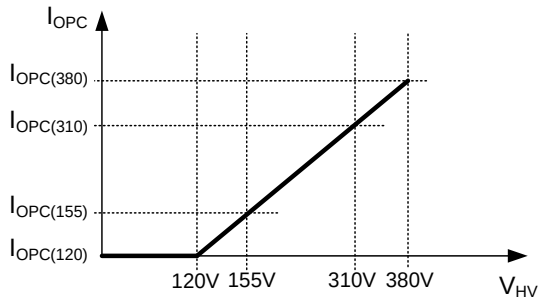


Figure 8: Compensation Current vs. Peak Rectified Input Line AC Voltage

Timer-Based Overload Protection (OLP)

In a flyback converter, if f_{SW} is fixed, the maximum P_{OUT} is limited by I_{PEAK}. V_{OUT} drops below the set value when the P_{OUT} exceeds its limit. This reduces the current through the optocoupler, pulling V_{FB} high.

If V_{FB} exceeds the OLP voltage (V_{OLP}) (typically 4V), it is considered an error flag and the timer begins counting. If the error flag is removed during the count, the timer resets. If the timer reaches 17 periods, OLP triggers. This timer duration prevents OLP from triggering during power supply start-up or short load transients. Figure 9 shows the OLP function.

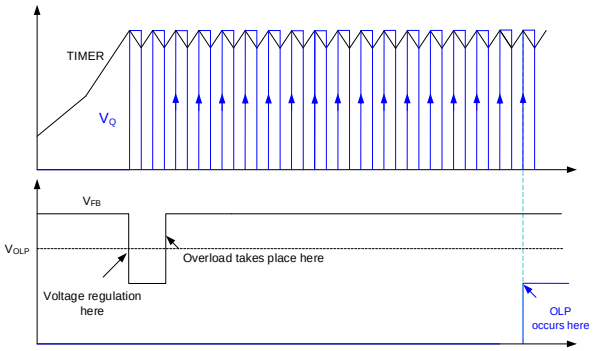


Figure 9: Overload Protection

Timer-Based Brownout Protection

The brownout protection block is similar to the OLP block. When V_{HV} drops below HV_{OFF} (typically 95V), it is considered an error flag and the timer begins counting. Once the V_{HV} exceeds HV_{OFF}, the timer resets. When the timer counts to 17 periods, brownout protection is triggered and the device stops switching.

Short-Circuit Protection (SCP)

The HFC0512 features short-circuit protection (SCP). If V_{CS} reaches V_{SCP} (typically 1.47V) after a reduced leading-edge blanking time (t_{LEB2}), SCP is triggered. Once the fault is removed, the power supply resumes operation.

Thermal Shutdown

If the temperature exceeds 150°C, the HFC0512 stops switching to prevent thermal damage. Once the temperature drops below 125°C, the power supply restarts and resumes normal operation. During thermal shutdown, the V_{CC} UVLO falling threshold drops from 8.5V to 5.5V.

V_{CC} Over-Voltage Protection (OVP)

The HFC0512 enters a latched fault condition if V_{CC} exceeds V_{CC_OVP} (typically 26.5V) for 60µs. The controller remains latched until V_{CC} drops below V_{CC_LATCH} (typically 2.5V), such as when the user unplugs the power supply from the main input and plugs it in again. This situation usually occurs if the optocoupler fails, which results in the loss of V_{OUT} regulation.

TIMER Latch-Off for OVP and OTP

Pull the TIMER pin below 1V for 12µs to latch off the controller. This function can be used for external OVP and OTP.

Clamped Driver

If V_{CC} exceeds 16V, V_{CLAMP} is typically 13.4V. This allows the use of any standard MOSFET.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit with two LEB times is connected between the CS pin and the current comparator to prevent premature switching pulse termination due to parasitic capacitances (see Figure 10). During the blanking time (t_{LEBx}), the current comparator is disabled and cannot turn off the external MOSFET.

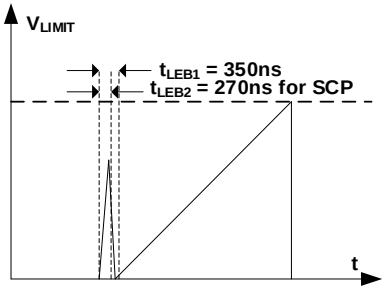


Figure 10: Leading-Edge Blanking Time

APPLICATION INFORMATION

Selecting the VCC Capacitor

The VCC capacitor (C_{VCC}) is charged via the HV pin once V_{IN} is applied. V_{CC} should exceed V_{CC_ON} until V_{OUT} is high enough for the auxiliary winding to supply the VCC pin. If V_{OUT} is not high enough, the controller stops switching and V_{OUT} cannot be set normally. For most applications, choose C_{VCC} to exceed 10μF. C_{VCC} can be estimated with Equation (3):

$$C_{VCC} > \frac{I_{CC} \times t_{RISE}}{V_{CC\_OFF} - V_{CC\_ON}} \quad (3)$$

Where I_{CC} is the internal IC consumption current and t_{RISE} is the V_{OUT} rise time.

Figure 11 shows the start-up circuit.

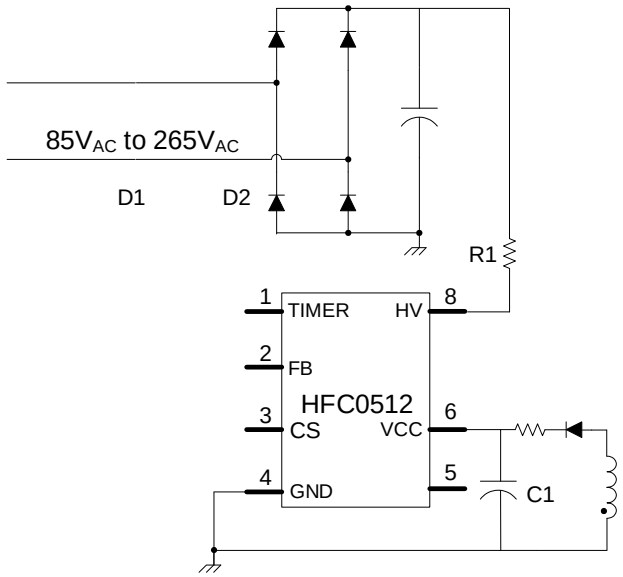


Figure 11: Start-Up Circuit

A higher R1 decreases the internal HV current source, especially under low V_{IN} conditions. Ensure that the practical supply current from HV is not less than the corresponding internal IC consumption current, which is the same as I_{CC_LATCH}. For the universal input range, R1 should be less than 80kΩ. 20kΩ is generally recommended.

Primary-Side Inductor Design (L_M)

With internal slope compensation, the HFC0512 can support CCM when the duty cycle exceeds 50%. Set the ratio (K_P) of the primary inductor's ripple current amplitude and I_{PEAK} to $0 < K_P \leq 1$, where $K_P = 1$ for discontinuous conduction mode (DCM). Figure 12 shows the relevant waveforms.

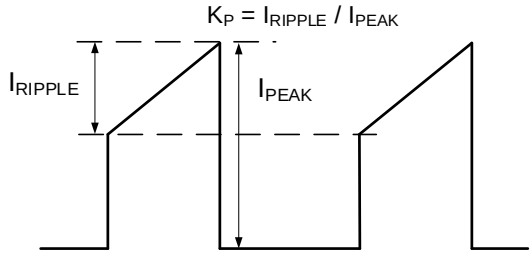


Figure 12: Typical Primary-Current Waveform

A larger-value inductor leads to a smaller K_P, which can reduce the RMS current, but increases transformer size. An optimal K_P value is between 0.6 and 0.8 for the universal input range, and between 0.8 and 1 for a 230V_{AC} input range.

The input power (P_{IN}) at the minimum V_{IN} can be estimated with Equation (4):

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (4)$$

Where V_{OUT} is the output voltage, I_{OUT} is the rated output current, and η is the estimated efficiency, which is generally between 0.75 and 0.85 depending on V_{IN} range and output application.

For CCM at minimum V_{IN}, the converter's duty cycle can be calculated with Equation (5):

$$D = \frac{(V_{OUT} + V_{FB}) \times N}{(V_{OUT} + V_{FB}) \times N + V_{IN\_MIN}} \quad (5)$$

Where V_F is the secondary diode's forward voltage, N is the transformer turns ratio, and V_{IN_MIN} is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time (t_{ON}) can be calculated with Equation (6):

$$T_{ON} = D \times T_S \quad (6)$$

Where t_S is the switching period.

The primary current's average current (I_{AV}) can be calculated with Equation (7):

$$I_{AV} = \frac{P_{IN}}{V_{IN\_MIN}} \quad (7)$$

The primary current's I_{PEAK} can be calculated with Equation (8):

$$I_{PEAK} = \frac{I_{AV}}{\left(1 - \frac{K_P}{2}\right) \times D} \quad (8)$$

The ripple current (I_{RIPPLE}) can be calculated with Equation (9):

$$I_{RIPPLE} = K_P \times I_{PEAK} \quad (9)$$

The valley current (I_{VALLEY}) can be calculated with Equation (10):

$$I_{VALLEY} = (1 - K_P) \times I_{PEAK} \quad (10)$$

The magnetic inductance (L_M) can be estimated with Equation (11):

$$L_M = \frac{V_{IN\_MIN} \times t_{ON}}{I_{RIPPLES}} \quad (11)$$

Current-Sense Resistor

Figure 13 and Figure 14 show the peak-current comparator logic and the subsequent waveform.

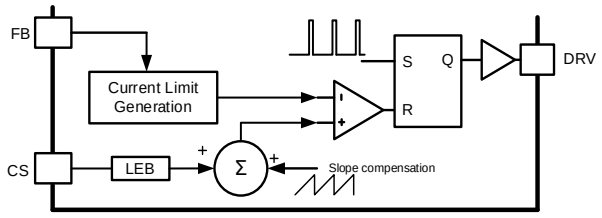


Figure 13: Peak-Current Comparator Circuit

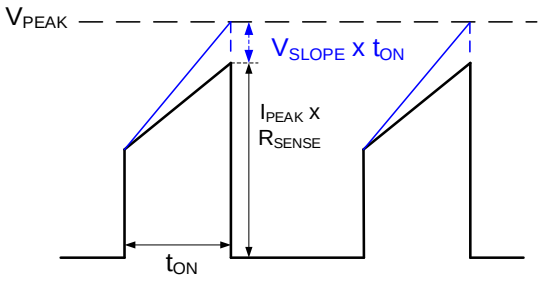


Figure 14: Typical Peak-Current Comparator

When the sense resistor (R_{SENSE}) voltage (V_{SENSE}) and the slope compensator (V_{SLOPE}) equal V_{PEAK}, the comparator goes high to reset the reset/set (RS) flip-flop. Pull DRV low to turn off the MOSFET. The maximum current limit (V_{LIMIT}, as measured by V_{CS}) is 0.95V. V_{SLOPE} is about 25mV/µs. At full loads, use 0.95 x V_{LIMIT} as V_{PEAK}. V_{SENSE} can be calculated with Equation (12):

$$V_{SENSE} = 95\% \times V_{LIMIT} - V_{SLOPE} \times t_{ON} \quad (12)$$

R_{SENSE} can be calculated with Equation (13):

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK}} \quad (13)$$

Select R_{SENSE} with an appropriate power rating. The sense resistor power loss (P_{SENSE}) can be calculated with Equation (14):

$$P_{SENSE} = \left[\left(\frac{I_{PEAK} + I_{VALLEY}}{2}\right)^2 + \frac{1}{12}\left(I_{PEAK} - I_{VALLEY}\right)^2\right] \times D \times R_{SENSE} \quad (14)$$

Low-Pass Filter on the CS Pin

A small capacitor (C_{CS}) connected to the CS pin via the series resistor (R_{SERIES}) forms a low-pass filter for noise filtering when the MOSFET turns on and off (see Figure 15).

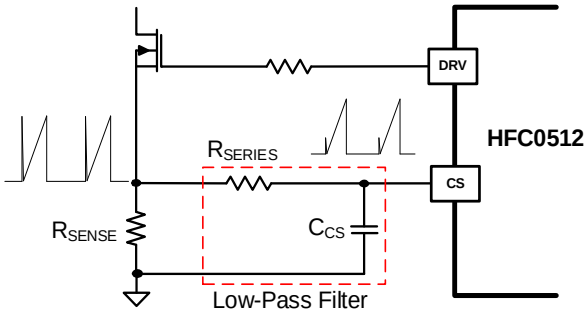


Figure 15: Low-Pass Filter on CS

The low-pass filter's R x C constant should not exceed 1/3 of the leading-edge blanking time for SCP (t_{LEB2}, typically 270ns). Otherwise, the filtered sensed voltage cannot reach the SCP point (1.45V) to trigger SCP if an output short circuit occurs.

Over-Power Compensation (OPC)

The HFC0512 employs over-power compensation (OPC) by drawing current from the CS pin. OPC minimizes the OLP difference caused by different input voltages. The offset current is proportional to the peak input voltage sensed by the HV pin.

If the resistor in the CS loop is R_{SERIES}, and the input voltage is $220V_{AC}$, calculate the compensation voltage (V_{COMP}) on CS with Equation (15):

$$V_{COMP} = R_{SERIES} \times I_{OPC\_310V} \quad (15)$$

The compensation criteria is to make V_{FB} under full-load conditions similar whether in high line or low line.

Frequency Jittering Period

Frequency jittering is an effective method to reduce EMI by dissipating energy. The nth-order harmonic noise bandwidth (B_{TN}) is calculated with Equation (16):

$$B_{Tn} = n \times (2 \times \Delta f + f_{JITTER}) \quad (16)$$

Where Δf is the frequency jitter amplitude. The jittering frequency (f_{JITTER}) is determined by Equation (1) on page 16.

If B_{TN} exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequencies below 150kHz, 9kHz for noise frequencies between 150kHz and 30MHz), the spectrum analyzer receives less noise energy.

The TIMER capacitor (C_{TIMER}) determines the frequency jitter period. A 10μA current source charges C_{TIMER}. When the TIMER voltage reaches 3.2V, another 10μA current source discharges C_{TIMER} to 2.8V. This charging and discharging cycle repeats.

Equation (1) on page 16 describes the theory of frequency jittering. Less f_{JITTER} reduces EMI. However, the measurement bandwidth requires more f_{JITTER} compared to the spectrum analyzer RBW to effectively reduce EMI. f_{JITTER} should also be less than the control-loop-gain crossover frequency to avoid disturbing V_{OUT}. Simultaneously, consider the practical application when selecting C_{TIMER}. A larger value capacitor may cause start-up failure at full loads because of a long t_{SS} (see Equation (2) on page 17). A smaller value C_{TIMER} causes a shorter TIMER period, and the TIMER count capability may overload, which can cause logic problems. For most applications, a frequency jitter between 200Hz and 400Hz is recommended.

Ramp Compensation

When adopting peak current control, subharmonic oscillation occurs when D > 0.5 in CCM. The HFC0512 is equipped with internal ramp compensation to solve this problem. The loop gain of the flyback transfer function (α) is calculated with Equation (17):

$$\alpha = \frac{\frac{D_{MAX} \times V_{IN\_MIN}}{(1-D_{MAX}) \times L_M} \times R_{SENSE} - m_A}{\frac{V_{IN\_MIN}}{L_M} \otimes R_{SENSE} + m_A} \quad (17)$$

Where m_A = 18mV/μs is the minimum internal slope value of the compensation ramp, $\frac{V_{IN\_MIN}}{L_M} \times R_{SENSE}$ is the slew rate of the primary-side sensed by the CS resistor, and $\frac{D_{MAX} \times V_{IN\_MIN}}{(1-D_{MAX}) \times L_M} R_{SENSE}$ is the slew rate of the equivalent secondary-side voltage sensed by the CS resistor. For stable operation, α must be less than 1.

Design Example

Table 1 shows a design example for power adapter applications using the HFC0512.

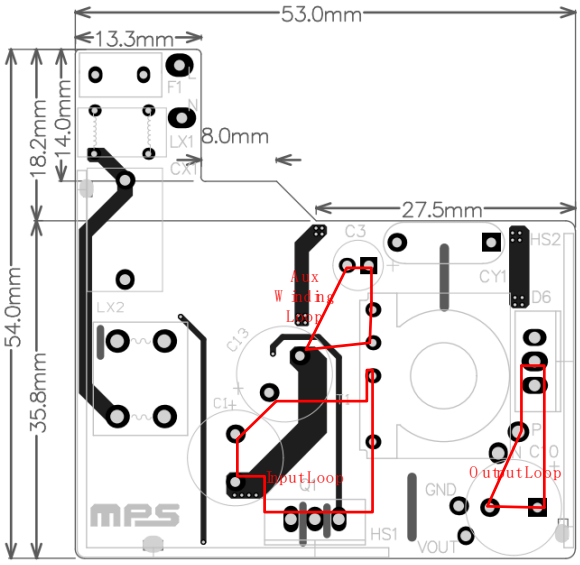
Table 1: Design Example

V_{IN}	$85V_{AC}$ to $265V_{AC}$
V_{OUT}	12V
I_{OUT}	1.67A

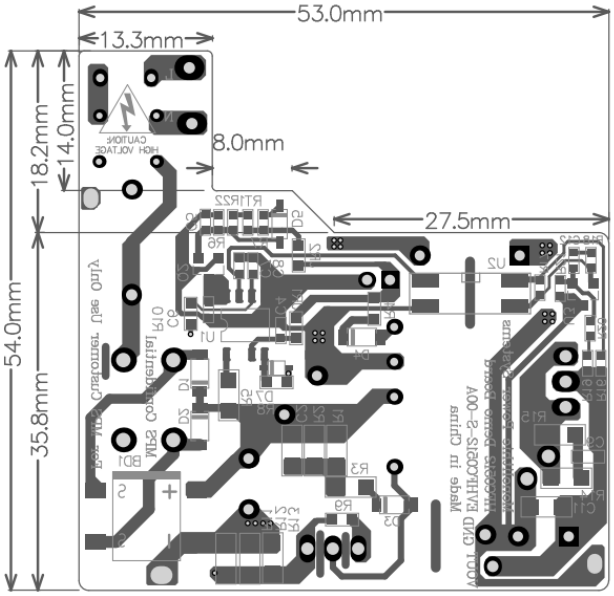
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 16 and follow the guidelines below:

1. Minimize the power stage loop area, including the input loop, the auxiliary winding loop, and the output loop.
2. Keep the input loop GND and control circuit separated.
3. Connect the heatsink to the primary GND plane to improve EMI.
4. Place the control circuit capacitors (such as those for FB, CS, and VCC) close to the IC to decouple noise.



Top Layer



Bottom Layer

Figure 16: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

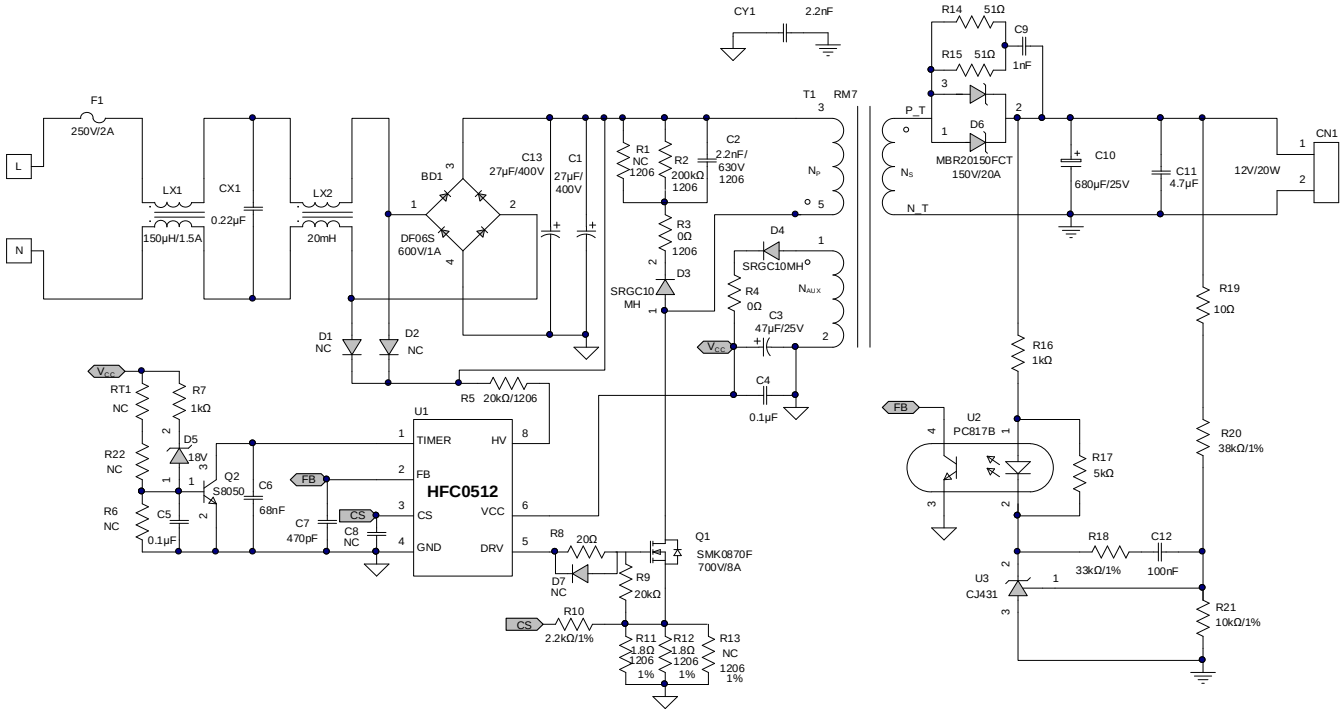
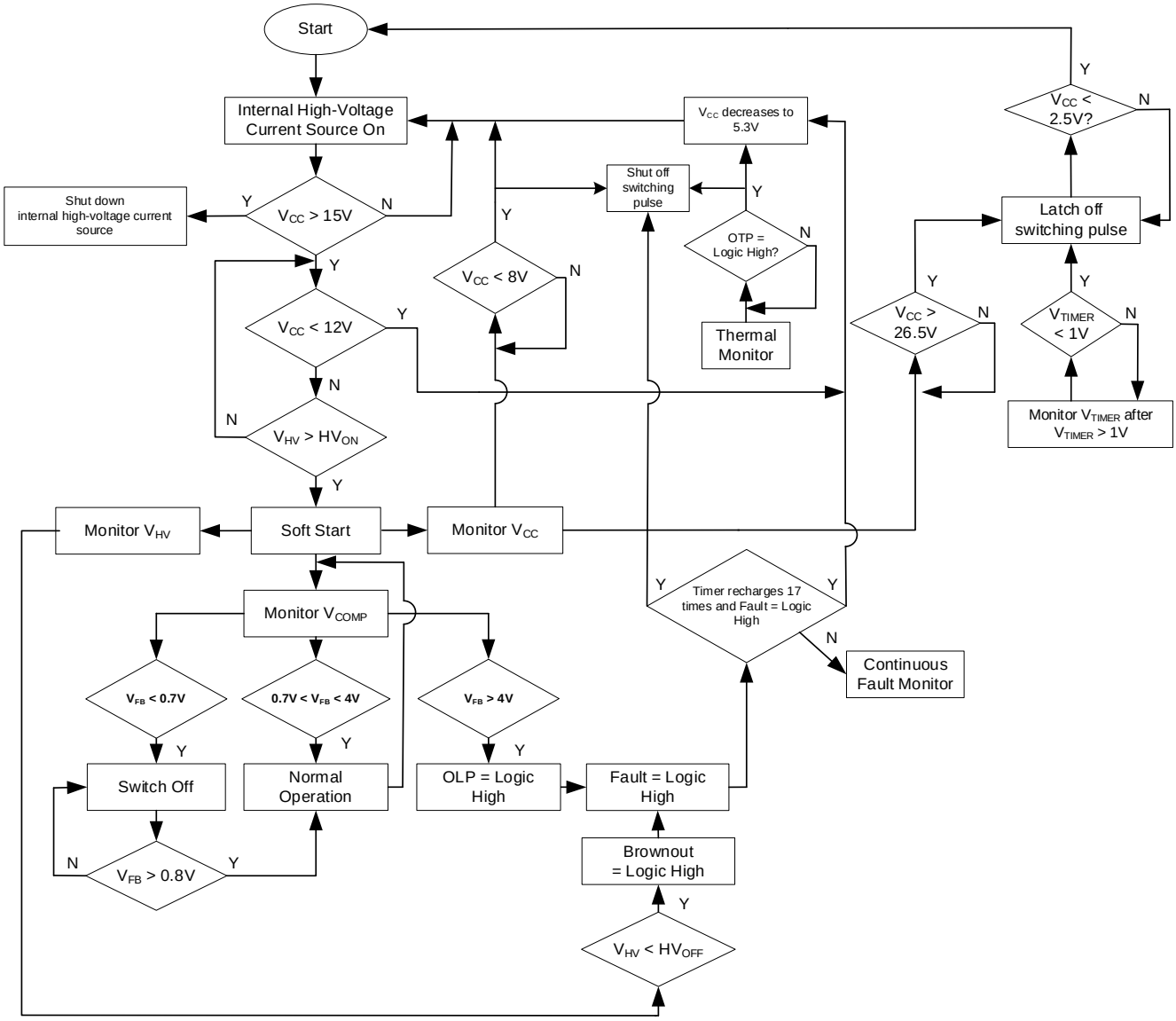


Figure 17: Typical Application Circuit

FLOWCHART



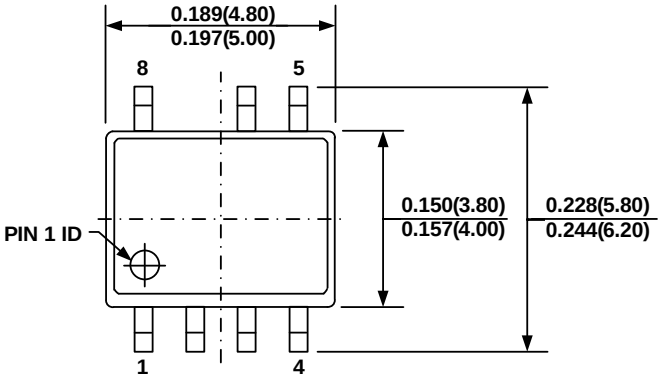
UVLO, brownout, OTP, and OLP are auto-restart. OVP on VCC and the latch-off on-timer are in latch mode.

To release from latch mode, it needs to be unplugged from the main input.

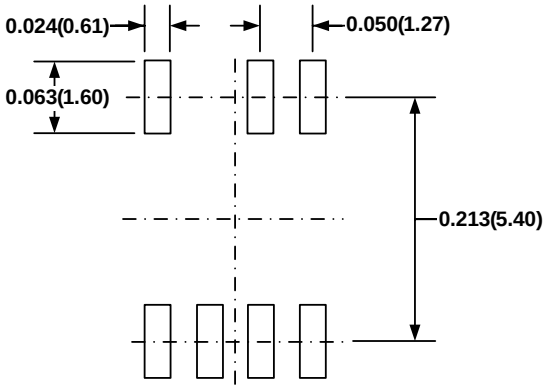
Figure 18: Control Flowchart

PACKAGE INFORMATION

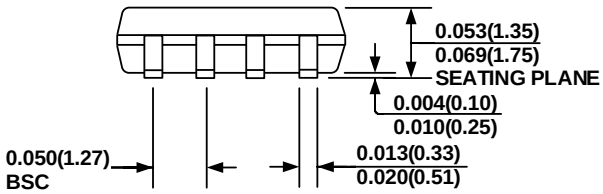
SOIC8-7A



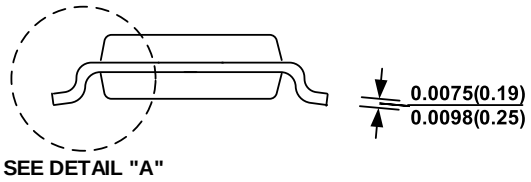
TOP VIEW



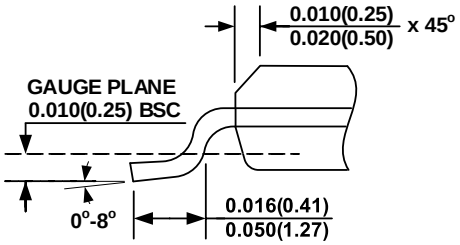
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

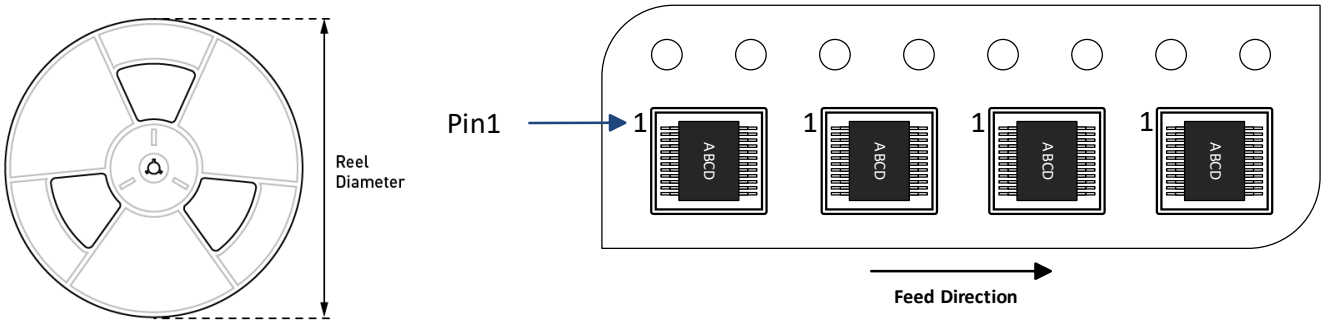


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HFC0512GS-Z	SOIC8-7A	2500	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/11/2024	Initial Release	-