Data Sheet

PRELIMINARY DATASHEET

GRF6403

31.75 dB RANGE / 0.25dB STEP DSA
0.05 to 6 GHz

FEATURES

- 31.75dB range
- 0.25dB steps via 7-bit Control
- Supports Multiple Control Interfaces – Serial, Direct Parallel and Latched Parallel
- Programmable *Rapid Fire*™ Attenuation Setting Which Circumvents Delays Associated with SPI Programming
- Defaults to Full Attenuation for Power-On Resets
- Glitchless Stepping (< 2 dB Over/Undershoot)
- 165 ns settling time for 0.25dB steps
- Bi-directional RF Use
- 3.3 V and 5 V Supply Voltages
- 50 Ω Single-ended Input and Output Impedances
- -40 to 115 °C Operating Temperature Range
- Compact 4 x 4 mm QFN-24 Package

Reference: 5 V / 2 GHz

- IL: 1.3 dB
- IP0.1dB: 30 dBm
- IIP3: 58 dBm
- INL Attenuation Error: ± (0.15 + 2%) dB
- DNL Attenuation Error: ± 0.1 dB

APPLICATIONS

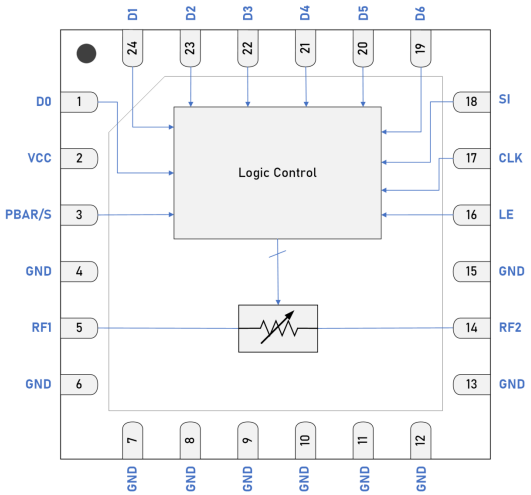
- 5G Wireless Infrastructure
- Cellular Repeaters/Boosters & DAS Systems
- Automotive Cellular and V2X Compensators
- Millimeter Wave IF Stages
- High Performance Gain Trim & AGC Loops
- TDD Applications where a Common DSA is Shared for Both TX and RX Modes of Operation

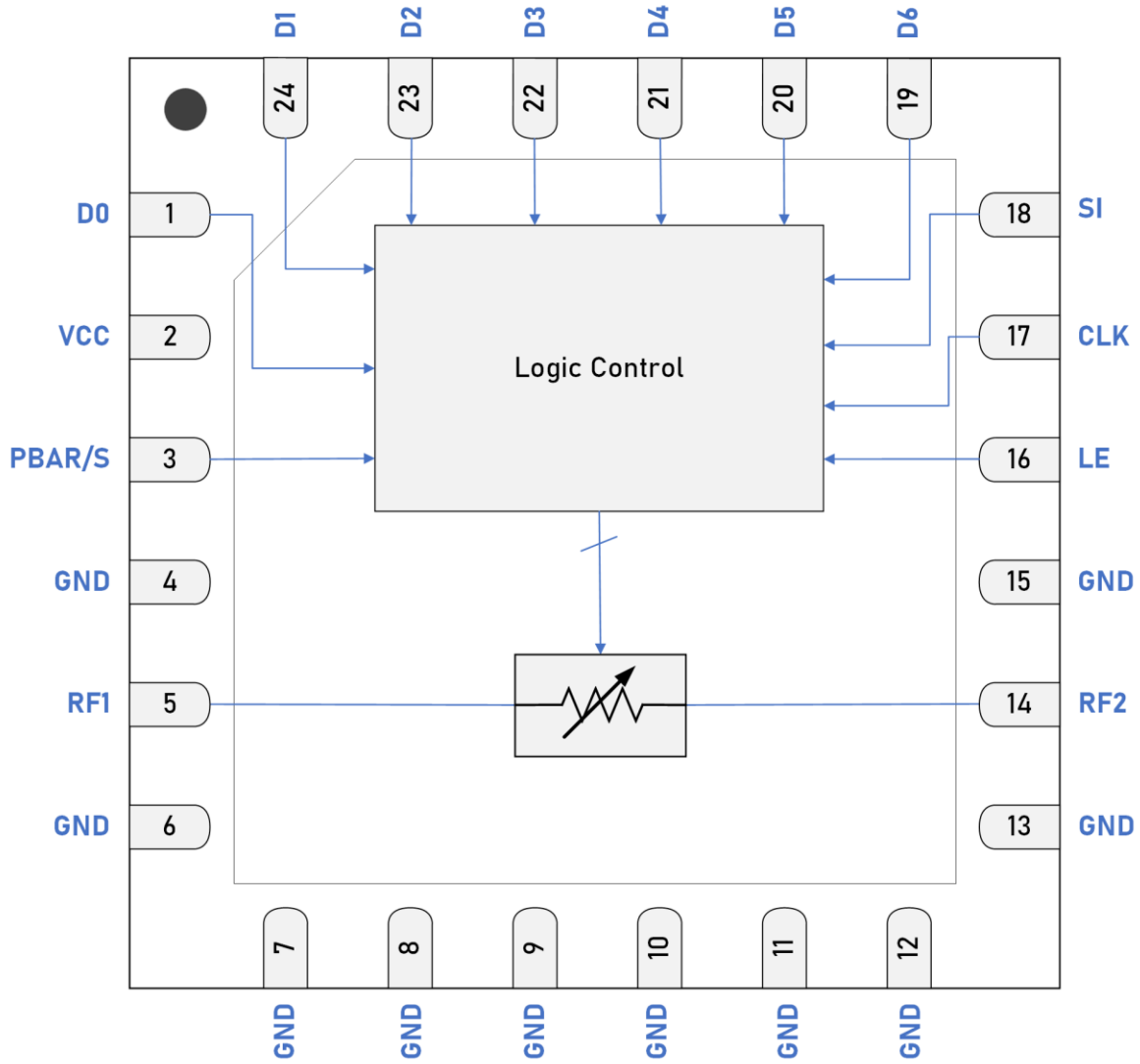
DESCRIPTION

The GRF6403 is a bi-directional, 31.75 dB range digital step attenuator which provides precise stepping in 0.25 dB increments. The device supports three unique programming modes, including serial, direct parallel, and latched parallel. In addition, the GRF6403 also includes a special *Rapid Fire*™ selection pin which allows the device to be immediately switched into a pre-defined attenuation state. This ability to quickly shift into a secondary state allows a single device to be used in TDD applications where different attenuation levels are needed for TX and RX modes of operation.

In terms of performance, the GRF6403 can cover the entire 50 MHz to 6 GHz range while still maintaining precise and monotonic gain stepping. Glitching has been minimized to < 2 dB for all steps. The device delivers up to 30 dBm of IP0.1dB, 58 dBm of IIP3 and a low IL of less than 1.3 dB at 2 GHz.

BLOCK DIAGRAM





Pin Out (Top View)

Pin Assignments

Pin	Name	Description	Note
1	D0	0.25 dB Parallel Control Bit	Pull high to select 0.25 dB attenuation.
2	VCC	V_{CC} Bias Voltage	Connect to V_{CC} . Use bypass capacitors as close to the pin as possible.
3	PBAR/S	Mode Select Pin	If left unconnected, logic will default to HIGH due to included pull-up on chip. **RFA Feature Disabled/Unused:** Logic Low = Parallel Control. Logic High = Serial Control **RFA Feature Enabled:** Logic Low = Switch in '*Rapid Fire*' attenuation. Logic High = Device reverts back to the previous attenuation state as defined during the last programming sequence. Refer to the programming section for details.
4, 6-13, 15	GND	Ground	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
5	RF1	RF Port 1	Internally matched 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the device supports bi-directional operation, the RF1 port can serve as an input or output.
14	RF2	RF Port 2	Internally matched 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the device supports bi-directional operation, the RF2 port can serve as an input or output.
16	LE	Latch Enable	**Serial Mode (PBAR/S = HIGH):** Logic LOW allows data to be shifted in. Logic HIGH updates the programming register. **Direct Parallel Mode (PBAR/S = LOW):** For direct parallel mode, keep the LE pin HIGH. Whenever the LE pin is set to logic HIGH, any attnuation value present at the parallel logic pins D[6:0] will be immediately written into the ATTEN[7:0] register. **Latched Parallel Mode (PBAR/S = LOW):** To realize the latched parallel mode, simply toggle the LE pin HIGH and then LOW to latch in the value present at the parallel logic pins D[6:0] into ATTEN[7:0]. Note that while the LE pin is LOW, the data values present on pins D[6:0] have no effect on the ATTEN[7:0] register.
17	CLK	Clock	Serial clock input.
18	SI	Serial Input	Serial data input.
19	D6	16 dB Parallel Control Bit	Pull high to select 16 dB attenuation.

Pin	Name	Description	Note
20	D5	8 dB Parallel Control Bit	Pull high to select 8 dB attenuation.
21	D4	4 dB Parallel Control Bit	Pull high to select 4 dB attenuation.
22	D3	2 dB Parallel Control Bit	Pull high to select 2 dB attenuation.
23	D2	1 dB Parallel Control Bit	Pull high to select 1 dB attenuation.
24	D1	0.5 dB Parallel Control Bit	Pull high to select 0.5 dB attenuation.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	0	6	V
SI, LE, CLK	V_{SPI}	0	6	V
D0, D1, D2, D3, D4, D5, D6	V_{LOGIC}	0	6	V
Externally Applied DC Voltage to RF1 Pin	V_{RFIN}	0	0	V
Externally Applied DC Voltage to RF2 Pin	V_{RFOUT}	0	0	V
RF Input Power to RF1 or RF2 (Load VSWR < 2:1)	$P_{IN\ MAX}$		27	dBm
Operating Temperature (Package Heat Sink)	$T_{PKG\ HEAT\ SINK}$	-40	115	°C
Maximum Junction Temperature (MTTF >10^6 Hours)	T_{J-MAX}		125	°C
Electrostatic Discharge				
Charged Device Model	CDM	1		kV
Human Body Model	HBM	1		kV
Storage				
Storage Temperature	T_{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	–

Caution! ESD Sensitive Device.
Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to *Manufacturing Note MN-001 — Package and Manufacturing Information.*

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the *Certificate of RoHS Compliance*.

Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	3	5	5.5	V	
Operating Temperature Range	$T_{PKG\ HEAT\ SINK}$	-40		+115	°C	Measured on Package Heat Sink
RF Frequency Range (Note 1)	F_{RF}	0.05		6	GHz	
RF1 Port Impedance	Z_{RFIN}		50		Ω	Single Ended
RF2 Port Impedance	Z_{RFOUT}		50		Ω	Single Ended

Note 1: Operation outside of these ranges is possible, but with degraded performance of some parameters.

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Nominal Operating Parameters - General

Parameter		Symbol	Specification			Unit	Condition
			Min.	Typ.	Max.		
Logic Input Low		V_{IL}	0		0.63	V	
Logic Input High		V_{IH}	1.17		V_{CC}	V	
Logic Current		I_{IL}, I_{IH}		200		µA	
Supply Current	5 V Supply	I_{CC-5V}		190		µA	Static operation
				230			During programming state.
	3.3 V Supply	$I_{CC-3.3V}$		225		µA	Static operation
				230			During programming state.
Serial Clock Speed		f_{CLK}			30	MHz	
LE to First Serial Clock Rising Edge		t_{LS}	10			ns	50% of LE falling edge to 50% of CLK rising edge.
Serial Data Hold Time		t_H	10			ns	50% of CLK rising edge to 50% of Data falling edge.
Final Serial Clock Rising Edge to LE		t_{CLS}	10			ns	50% of CLK rising edge to 50% of LE rising edge.
DSA Settling Time	Any Adjacent Step	$T_{SETTLE-ADJ}$		210		ns	50% of LE to within 0.1dB of the final value.
	Max to Min Attenuation	$T_{SETTLE-MAX-MIN}$		370		ns	
	Min to Max Attenuation	$T_{SETTLE-MIN-MAX}$		635		ns	

Thermal Data

Thermal Resistance (Infrared Scan)		Θ_{JC}		TBD		°C/W	On Standard Evaluation Board
Junction Temperature @ +115 °C Reference (Package Heat Sink)		T_J		TBD		°C	V_{CC}: 5.0 V, I_{CC}: TBD mA, P_{DISS}: TBD mW, No RF (Note 2).

Note 2: MTTF $>10^6$ hours for $T_J \leq 170$ °C.

Nominal Operating Parameters – RF

The following conditions apply unless noted otherwise: Typical Application Schematic, V_{CC} = 5 V, 50 Ω system impedance, F_{TEST} = 2.0 GHz, $T_{PKG\ HEAT\ SINK}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Attenuation Range	G_{RANGE}		31.75		dB	
Attenuation Resolution	G_{STEP}		0.25		dB	
Over/Undershoot During Step Transition	$G_{OVER/UNDERSHOOT}$			2	dB	Any step.
Step Error Between Any Two Adjacent States	DNL		± 0.03		dB	0.05 GHz ≤ F_{RF} ≤ 1 GHz
			± 0.05			1 GHz ≤ F_{RF} ≤ 2 GHz
			± 0.07			2 GHz ≤ F_{RF} ≤ 3 GHz
			± 0.10			3 GHz ≤ F_{RF} ≤ 4 GHz
			± 0.11			4 GHz ≤ F_{RF} ≤ 5 GHz
			± 0.14			5 GHz ≤ F_{RF} ≤ 6 GHz
Absolute Attenuation Error	INL		±(0.01+2.4%)		dB	0.05 GHz ≤ F_{RF} ≤ 1 GHz
			±(0.01+2.5%)			1 GHz ≤ F_{RF} ≤ 2 GHz
			±(0.01+3.3%)			2 GHz ≤ F_{RF} ≤ 3 GHz
			±(0.01+3.5%)			3 GHz ≤ F_{RF} ≤ 4 GHz
			±(0.02+6.1%)			4 GHz ≤ F_{RF} ≤ 5 GHz
			±(0.01+7%)			5 GHz ≤ F_{RF} ≤ 6 GHz
Relative Phase Between the MIN and MAX Attenuation States	Φ_{Δ}		6		°	F_{RF} = 0.5 GHz
			11			F_{RF} = 1 GHz
			21			F_{RF} = 2 GHz
			26			F_{RF} = 2.5 GHz
			36			F_{RF} = 3.55 GHz
			47			F_{RF} = 4.7 GHz
			55			F_{RF} = 6 GHz

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Phase Deviation Between Any Two Adjacent States	Φ_{ADJ}		2.3		°	
Insertion Loss	S21, S12		1.15	TBD	dB	F_{RF} = 0.5 GHz
			1.2	TBD		F_{RF} = 1 GHz
			1.3	TBD		F_{RF} = 2 GHz
			1.4	TBD		F_{RF} = 2.5 GHz
			1.7	TBD		F_{RF} = 3.55 GHz
			2.0	TBD		F_{RF} = 4.7 GHz
			2.5	TBD		F_{RF} = 6 GHz
Gain Flatness Over any 200 MHz Band	$S21_{FLAT}$		0.06		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			0.06			2 GHz ≤ F_{RF} ≤ 3 GHz
			0.06			3 GHz ≤ F_{RF} ≤ 4 GHz
			0.06			4 GHz ≤ F_{RF} ≤ 5 GHz
			0.06			5 GHz ≤ F_{RF} ≤ 6 GHz
Gain Variation Over Temp	$S21_{TEMP}$		+0.35 / -0.25		dB	$T_{PKG\ HEAT\ SINK}$ = -40 to 115 °C, Referenced to $T_{PKG\ HEAT\ SINK}$ = 25 °C
RF Port 1 Return Loss	S11		> 23		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 23			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 23			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 20			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz
RF Port 2 Return Loss	S22		> 23		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 23			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 23			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 20			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz

Parameter	Symbol	Specification			Unit	Condition	
		Min.	Typ.	Max.			
Input 3rd Order Intercept	IIP3		57		dBm	F_{RF} = 0.5 GHz	18 dBm P_{OUT} per Tone at 1 MHz Spacing ATTN = 0 dB
			60			F_{RF} = 1 GHz	
			60			F_{RF} = 2 GHz	
			60			F_{RF} = 2.5 GHz	
			60			F_{RF} = 3.55 GHz	
			62			F_{RF} = 4.7 GHz	
			64			F_{RF} = 6 GHz	
			60			ATTN = 0 dB	18 dBm P_{OUT} per Tone at 1 MHz Spacing F_{RF} = 2 GHz
			TBD			ATTN = 15.75 dB	
			TBD			ATTN = 31.75 dB	
Input 0.1dB Compression	$IP_{0.1dB}$		30		dBm	F_{RF} = 0.5 GHz	ATTN = 0 dB
			30			F_{RF} = 1 GHz	
			30			F_{RF} = 2 GHz	
			31			F_{RF} = 2.5 GHz	
			35			F_{RF} = 3.55 GHz	
			31			F_{RF} = 4.7 GHz	
			32			F_{RF} = 6 GHz	
			30			ATTN = 0 dB	F_{RF} = 2 GHz
			TBD			ATTN = 15.75 dB	
			TBD			ATTN = 31.75 dB	

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Functional Description

The GRF6403 employs a number of programming options to control the device's digital step attenuator. Parallel programming is supported via the device's 7 external control pins. Alternatively, the device can be programmed using an enhanced 3-wire SPI (serial-parallel interface). As a supplement to its traditional serial programming, the GRF6403 also includes a special *Rapid Fire*™ selection pin which allows the device to be immediately switched into a pre-defined attenuation state. The following sections provide specific details on each programming mode.

Direct Parallel Programming

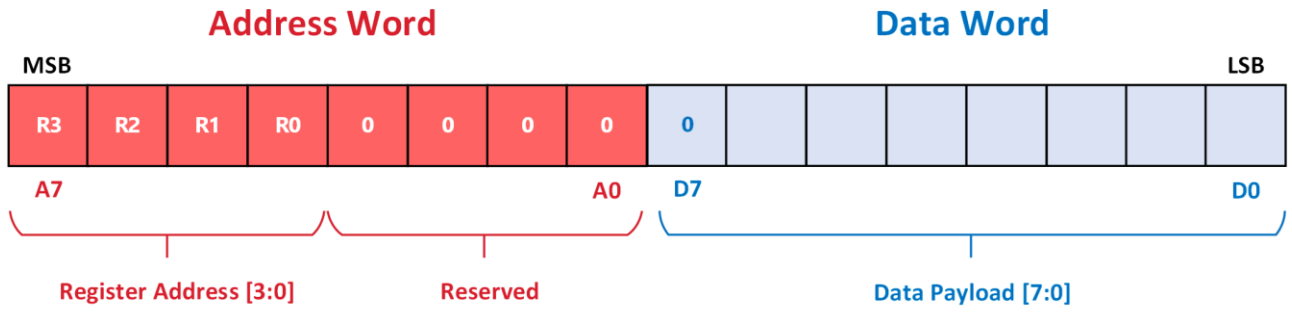
To use the direct parallel programming mode, simply apply a logic LOW to the PBAR/S pin while simultaneously keeping the LE pin HIGH. Whenever the LE pin is set to logic HIGH, any attenuation value present at the parallel logic pins D[6:0] will be immediately written into the ATTEN[7:0] register.

Latched Parallel Programming

To realize the latched parallel mode of programming, set PBAR/S to logic LOW; toggle the LE pin HIGH and then LOW to latch in the value present at the parallel logic pins D[6:0] into ATTEN[7:0]. Note that while the LE pin is LOW, the data values present on pins D[6:0] have no effect on the ATTEN[7:0] register.

Serial Programming

A 16-bit SPI transaction is required to program the GRF6403. Information is shifted in with the least significant bit (LSB) first. Refer to the figure below for an overview of the relevant bit assignments:



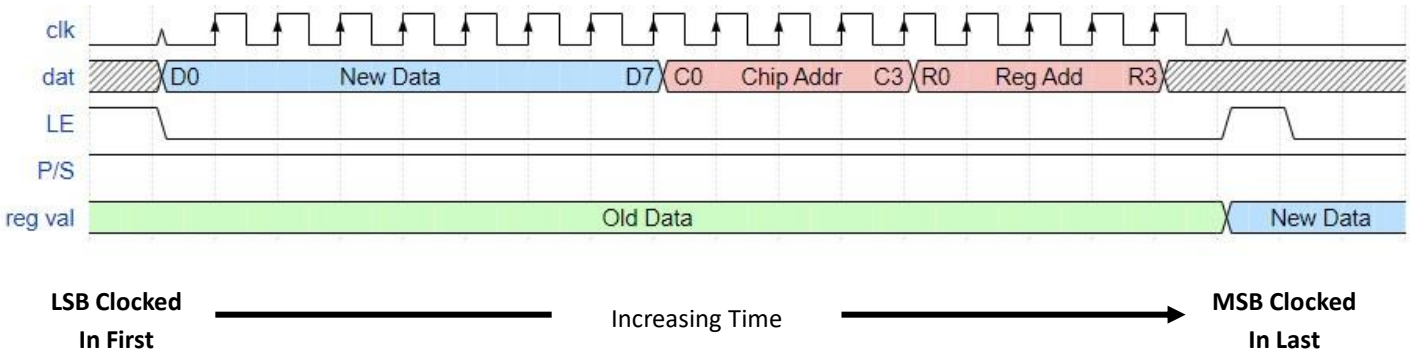
16-Bit SPI Transaction Payload Diagram

Per the diagram above, the payload consists of two separate 8-bit words. The data word is clocked in first with bits D7-D0 making up the 8-bit data payload. Note that the data payload will vary depending upon the register being targeted with the write command; *separate 16-bit SPI transactions are therefore required for programming each of the device's three*

registers.

The *address word* is clocked in next, and it includes two separate bit fields. Bits A7-A4 identify the desired register address. ***Bits A3-A0 are reserved and must be programmed with a '0000' during each 16-bit SPI transaction.***

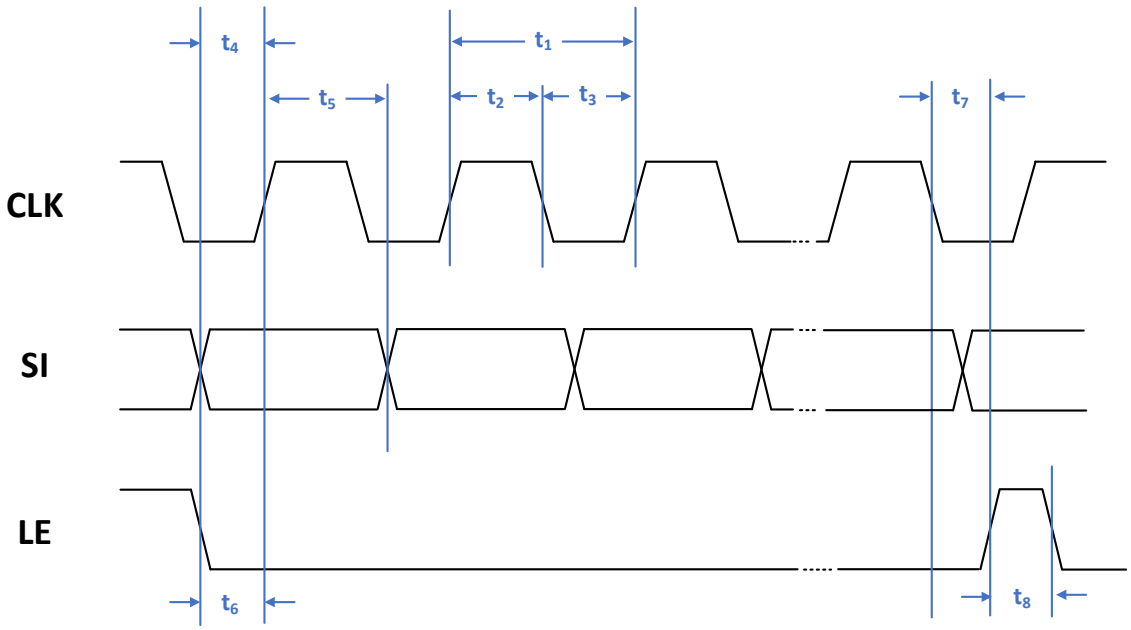
The figure below depicts the timing associated with each programming sequence.



16-Bit SPI Programming Sequence

As shown, the sequence begins when the latch enable (LE) line is pulled LOW. After clocking in all 16 bits of the SPI payload, an LE line transition to HIGH will latch bits D7-D0 into the addressed register. ***This latching process occurs as soon as LE transitions back to LOW.***

SPI Timing Intervals



SPI Timing Diagram

SPI Timing Specifications

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Serial Clock (CLK) Speed	f_{CLK}			12.5	MHz	
CLK Period	t_1	80			ns	
CLK High Duration Time	t_2	40			ns	
CLK Low Duration Time	t_3	40			ns	
SI to CLK Setup Time	t_4	10			ns	
SI Hold Time	t_5	10			ns	
LE Low Setup Time	t_6	10			ns	
LE High Setup Time	t_7	10			ns	
LE High Time	t_8	10			ns	

Register Mapping

The GRF6403 includes 3 separate 8-bit registers which help to facilitate the device's various programming functions. The first register, **ATTEN**, is used to set the device's attenuation state when operated in its normal serial mode. Upon all power-on resets (PORs), the register defaults to [01111111], meaning that the attenuator will be set to its maximum attenuation state.

The **CONFIG** register is used to activate the RFA feature. Upon PORs, all bits within the register will default to 0s, thus placing the RFA feature in a disabled state. If the user decides to employ the RFA option, then the [0] and [1] bit fields must be set to 1 with a separate SPI transaction.

The third register, **RFAREG**, is tied to the GRF6403's *Rapid Fire™ Attenuation* feature. As with the ATTEN register, the RFAREG will default to its maximum attenuation state for all POR conditions. Subsequent SPI programming transactions allow the user to set this register to any customized state between 0 and 31.75dB. The bit assignments within this particular register get passed along to the attenuator core whenever the RFA feature is enabled *AND* the external PBAR/S pin (pin 3) goes LOW.

The remaining registers are unused, and they should NOT be written to with any SPI transactions.

Detailed Register Map

Register Address	Name	Width	Description	Bit Fields	POR Value
0x0	ATTEN	8 bits	Attenuator state when in serial mode.	**[6:0]:** DSA Attenuation Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; can be set to **0** or **1***	[01111111]
0x1	CONFIG	8 bits	Stores configuration settings	**[0]:** *Rapid Fire™ Pointer Flag* **1** = RFA attenuation is set from RFAREG **[1]:** *Rapid Fire™ Feature On/Off Selection* **0** = RFA Disabled **1** = RFA Enabled **[7:2]:** *Unused; all bits can be set to **0** or **1***	[00000000]
0x2	RFAREG	8 bits	Stores value for Rapid-Fire mode attenuation	**[6:0]:** RFA (*Rapid Fire™* Attenuation) Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; can be set to **0** or **1***	[01111111]
0x3-0xF	Unused	8 bits	Do not write to these registers		[00000000]

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Register Truth Tables

The following truth tables pertain to the attenuator words as used within the ATTEN and RFAREG registers.

7-Bit SPI Word Bit Assignments

Data Bit	Attenuation Control
D7	Not Used
D6	16 dB Attenuator Control
D5	8 dB Attenuator Control
D4	4 dB Attenuator Control
D3	2 dB Attenuator Control
D2	1 dB Attenuator Control
D1	0.5 dB Attenuator Control
D0	0.25 dB Attenuator Control

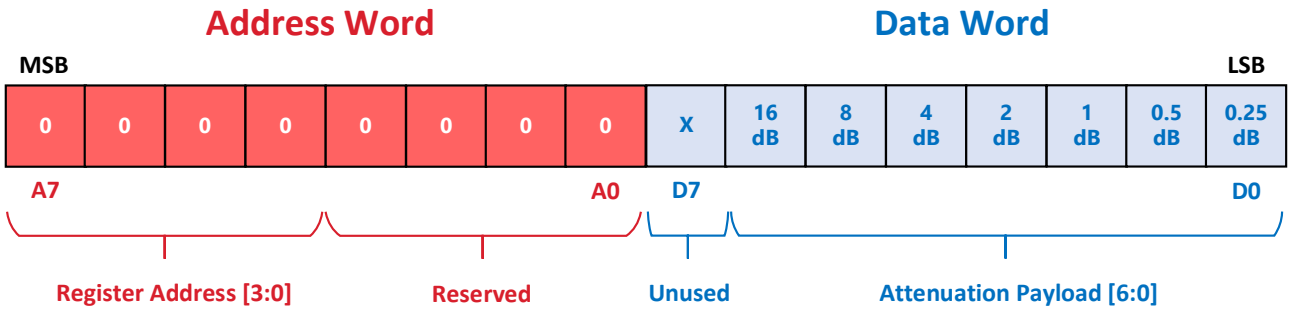
Serial Control Word Abbreviated Truth Table

Attenuation	D7	D6	D5	D4	D3	D2	D1	D0
0 dB	0	0	0	0	0	0	0	0
0.25 dB	0	0	0	0	0	0	0	1
0.5 dB	0	0	0	0	0	0	1	0
1 dB	0	0	0	0	0	1	0	0
2 dB	0	0	0	0	1	0	0	0
4 dB	0	0	0	1	0	0	0	0
8 dB	0	0	1	0	0	0	0	0
16 dB	0	1	0	0	0	0	0	0
31.75 dB	0	1	1	1	1	1	1	1

Note: D7 must be set to 0 with every SPI transaction.

Basic DSA Serial Programming

Upon power-on / reset (POR), the GRF6403 will default to an attenuation setting of 31.75 dB. A simple SPI command can then be executed to change this attenuation setting by writing directly to the device's ATTEN register (0x0). Be sure to include the relevant '0s' noted in the diagram below for bits A3-A0. Bit D7 is unused, and it can be assigned a '0' or '1' logic. Apply the relevant attenuation bits within the data word per the truth tables provided above.

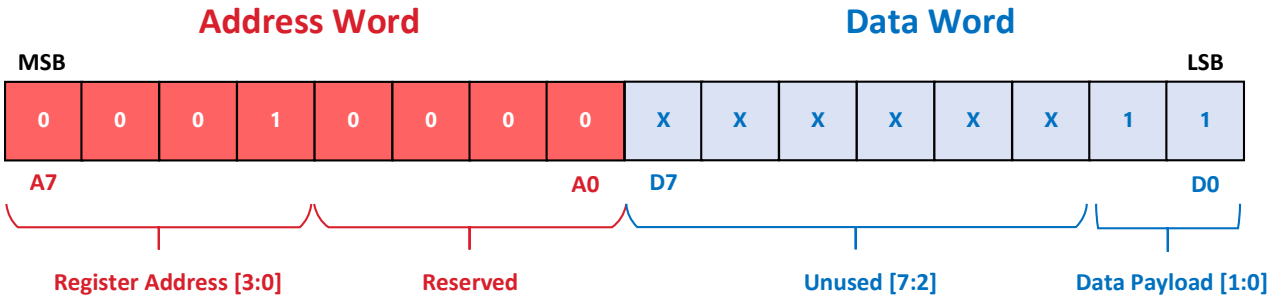


16-Bit SPI Payload for Basic DSA Programming

Rapid Fire™ Attenuation (RFA) Feature

The RFA feature enables the user to quickly switch the attenuator into a pre-defined state, thus circumventing the delays commonly associated with serial programming. A single control line allows the user to rapidly toggle between two attenuation states. In essence, the RFA feature provides a hybrid control mechanism which combines the speed of parallel programming with the convenience of a single control line. This form of control is useful for a multitude of applications where this fast switching is crucial for protecting downstream stages from overexposure to excessively large RF signals. This ability to quickly shift into a secondary state also allows a single device to be used in TDD applications where different attenuation levels are needed for RX and TX applications.

To use the GRF6403's RFA feature, a one-time SPI command must first be sent to the device to activate the feature set. (Note that any subsequent PORs will also require the user to re-activate the RFA feature; PORs force the CONFIG register to revert to its default setting, and the RFA is de-activated as part of this default).



16-Bit SPI Payload for Activating the RFA Feature

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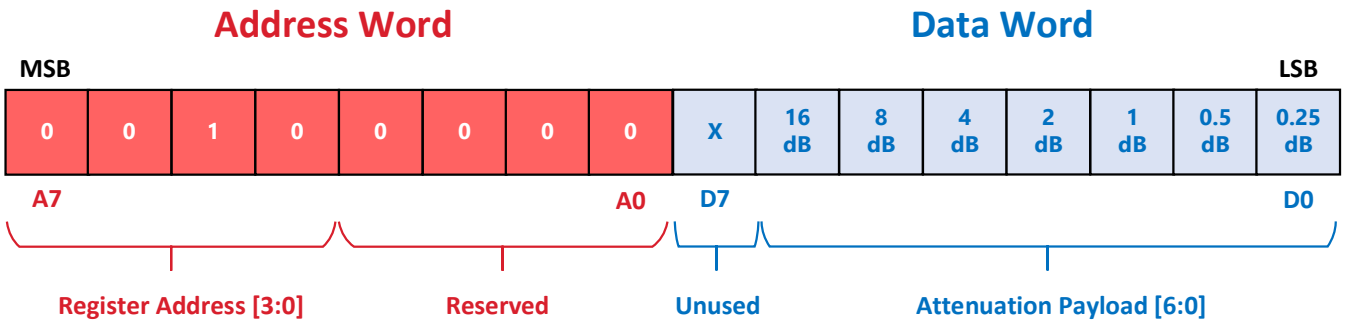
Be sure to include the relevant '0s' noted in the diagram for bits A3-A0. Bits D7-D2 are unused and can be assigned a '0' or '1' logic. D1 is set to '1' to activate the RFA feature. ***Note that D0 must also be set to '1' as part of this activation process.*** Setting D0 to '1' instructs the device to pull the attenuation setting directly from the RFAREG whenever the RFA is activated.

To deactivate the RFA feature, simply perform an identical SPI transaction, but set D1 to '0' instead.

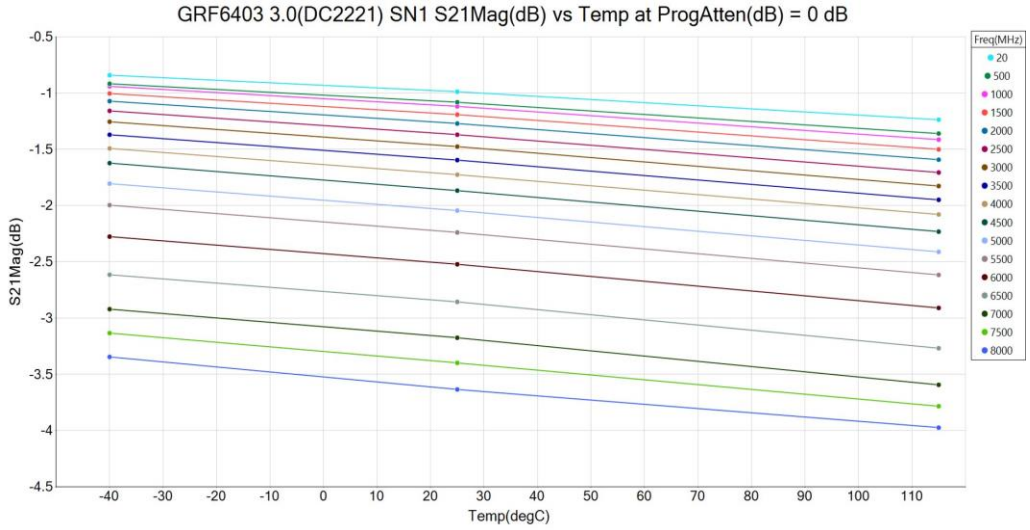
Once the feature is enabled, simply toggle the logic on the PBAR/S pin (pin 3) to switch between the attenuation settings stored in registers *ATTEN* (0x0) and *RFAREG* (0x2). A logic 'LOW' switches in the attenuation settings from RFAREG, and a logic 'HIGH' reverts back to the previous attenuation state in the ATTEN register as defined during the last programming sequence.

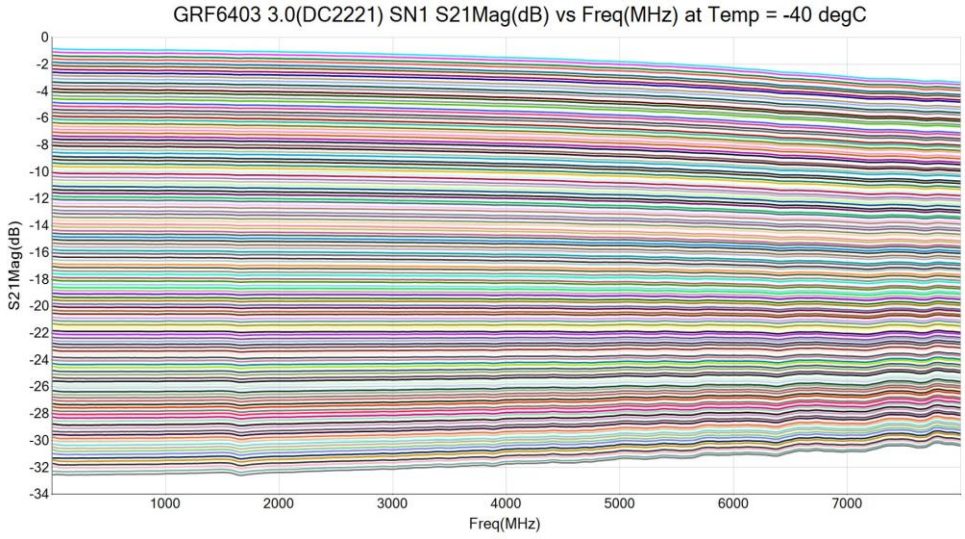
To customize the amount of attenuation being 'fired in', an additional SPI command must also be sent to change the RFA level from its default of 31.75dB. Simply perform a separate SPI transaction to write to the RFAREG:

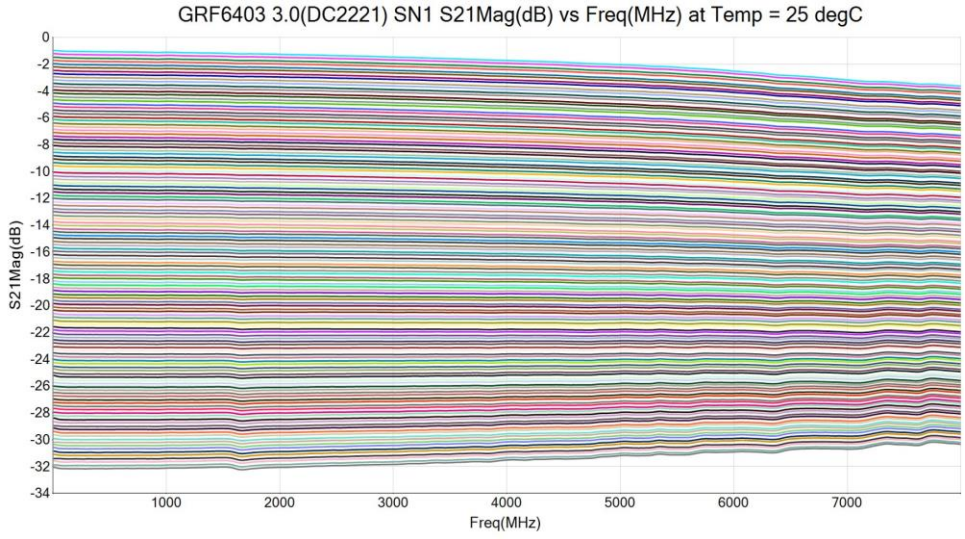


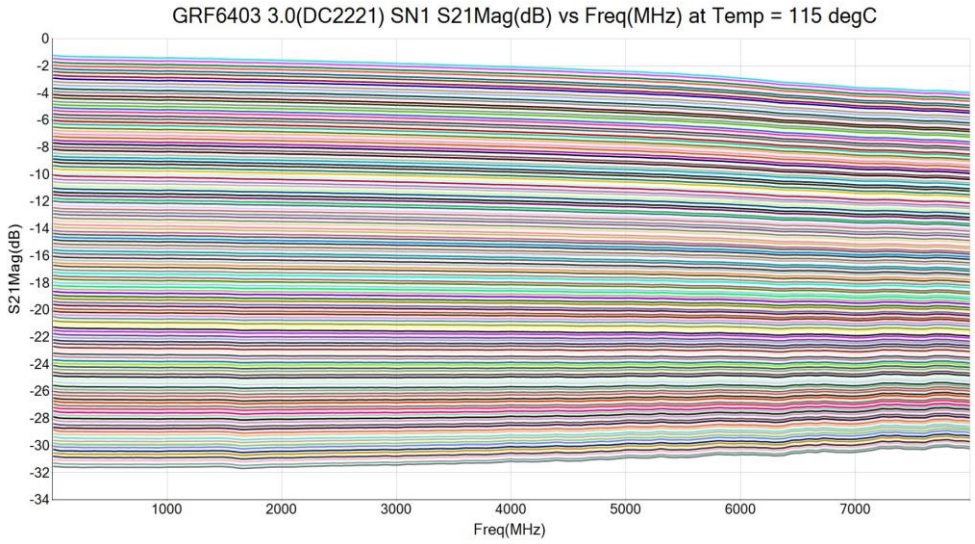
16-Bit SPI Payload for Customizing the RFA's Attenuation Setting

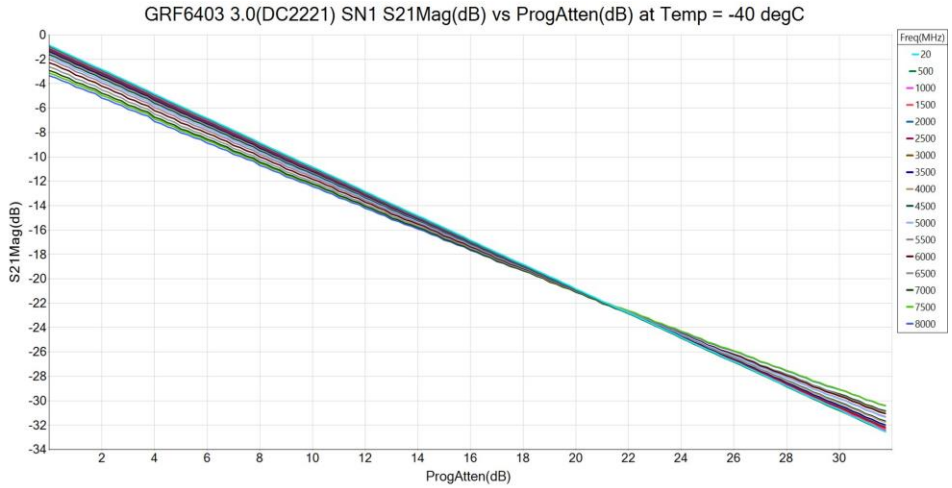
As mentioned earlier, be sure to include the '0s' noted in the diagram for bits A3-A0. Apply the relevant attenuation bits within the data word per the truth tables provided above.

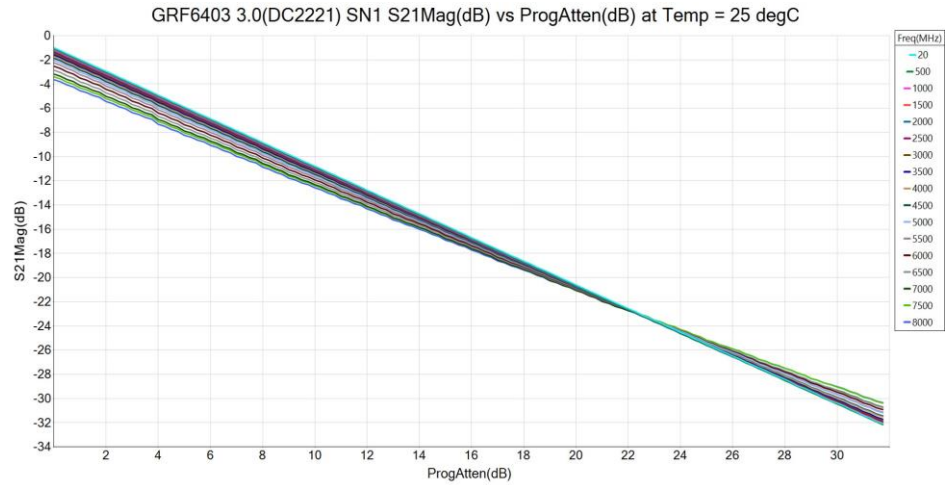


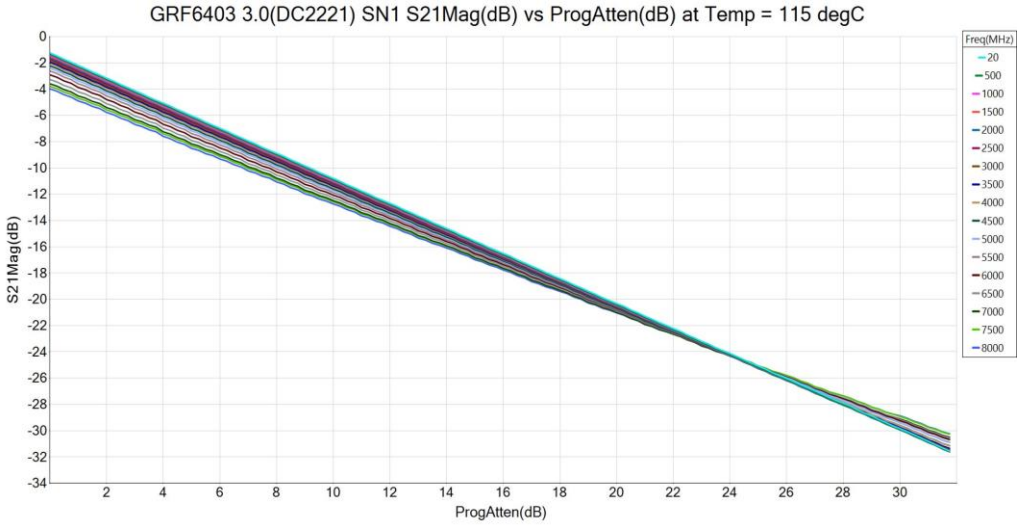


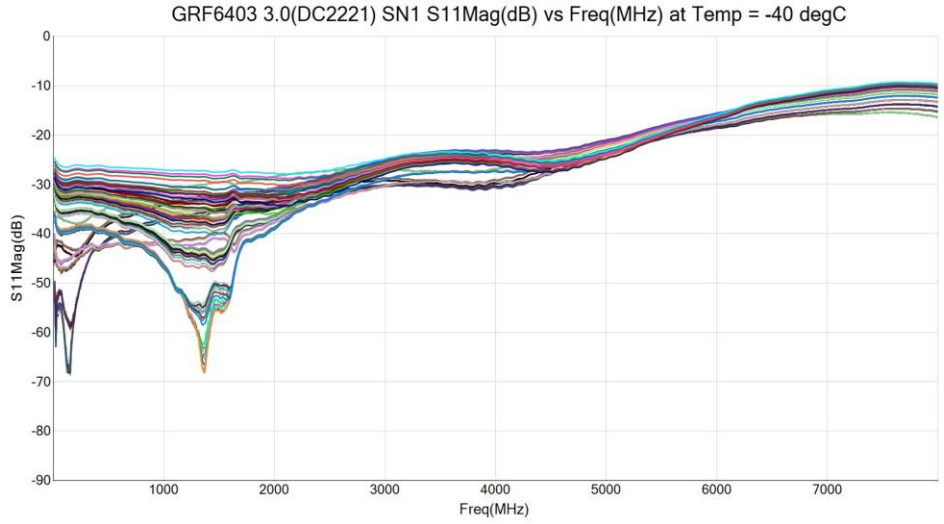


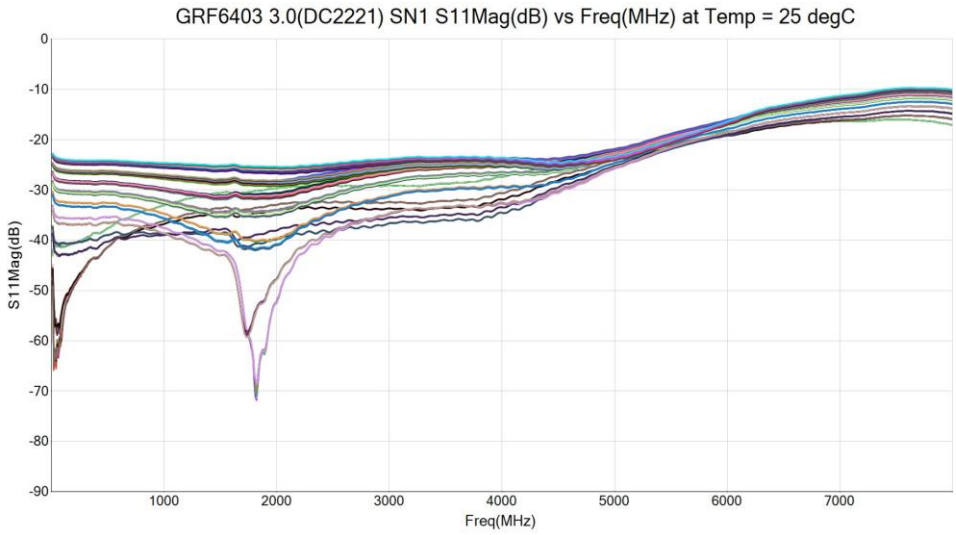

GRF6403 3.0(DC2221) SN1 S21Mag(dB) vs Freq(MHz) at Temp = 115 degC
S21Mag(dB)
Freq(MHz)

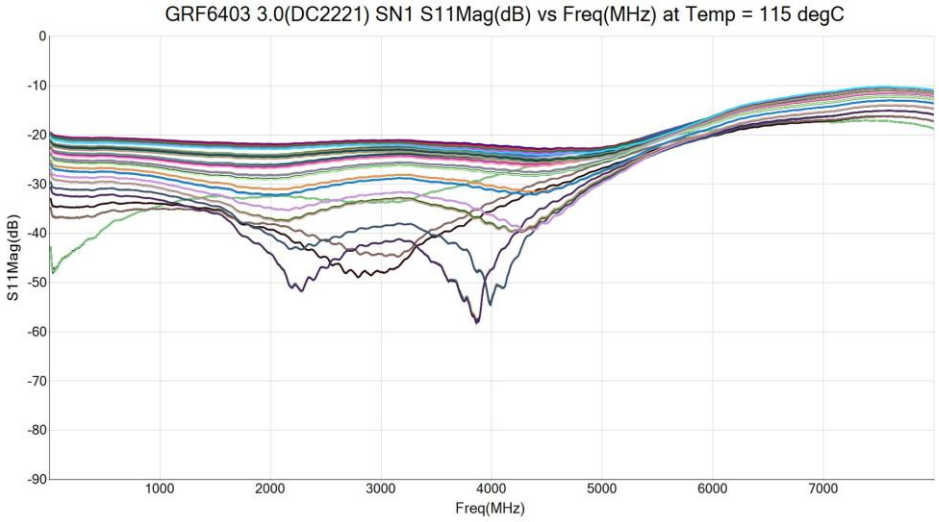

GRF6403 3.0(DC2221) SN1 S21Mag(dB) vs ProgAtten(dB) at Temp = -40 degC
S21Mag(dB)
ProgAtten(dB)
Freq(MHz)

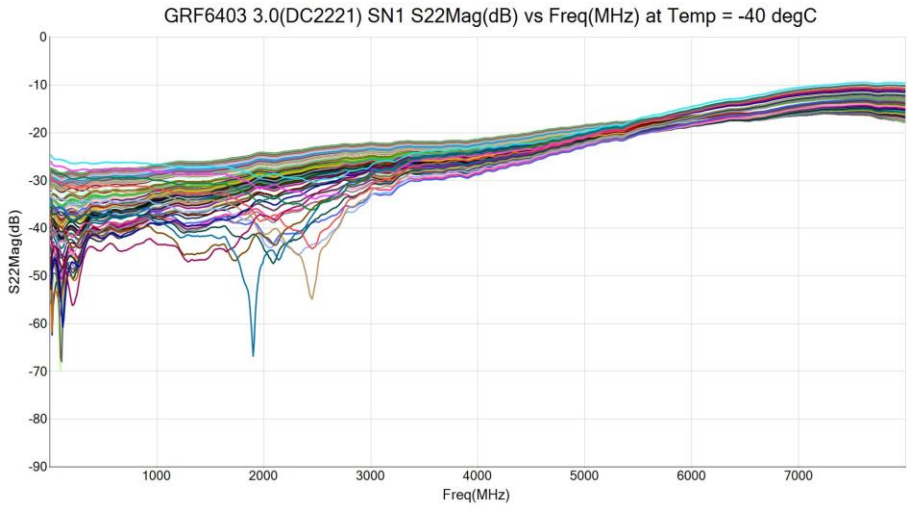

GRF6403 3.0(DC2221) SN1 S21Mag(dB) vs ProgAtten(dB) at Temp = 25 degC
S21Mag(dB)
ProgAtten(dB)
Freq(MHz)

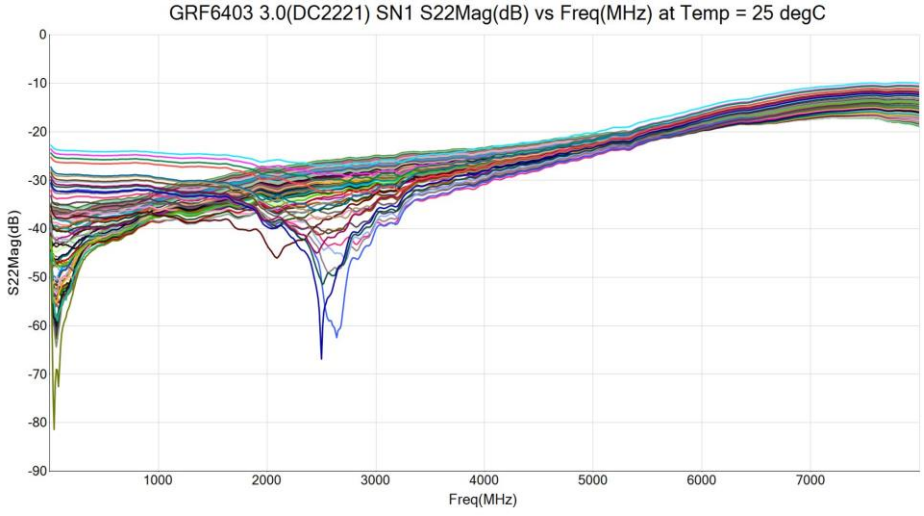


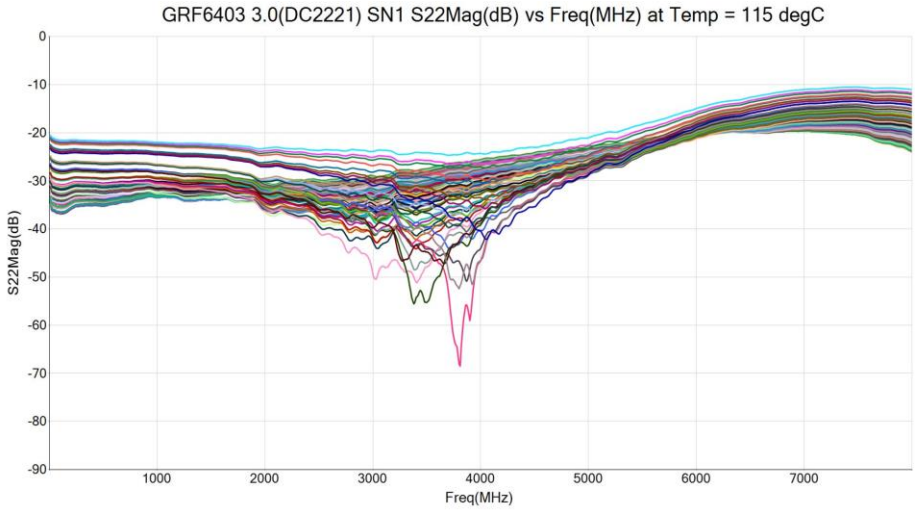


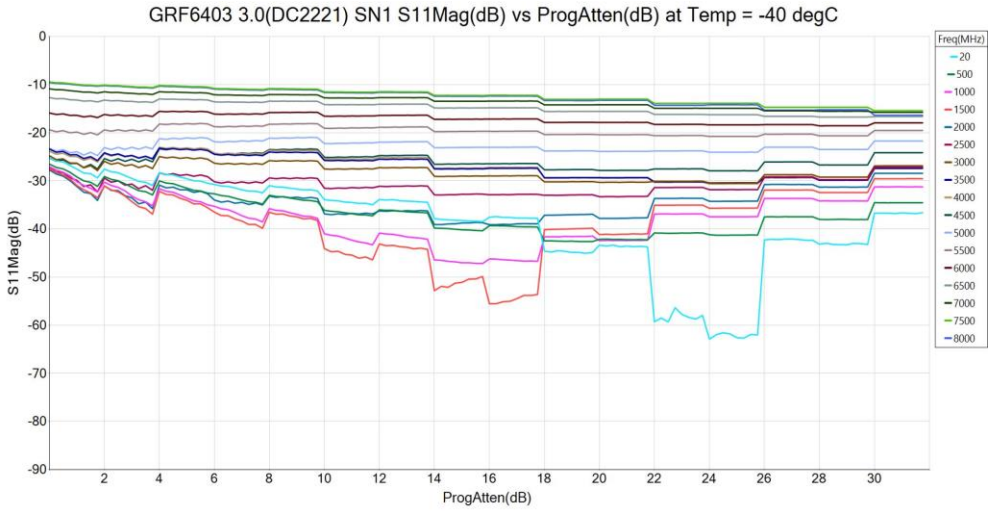


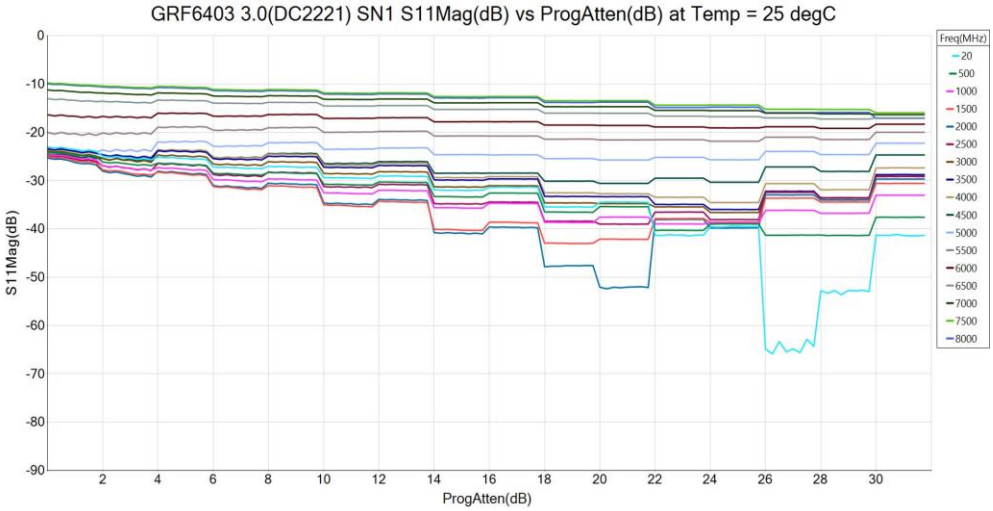


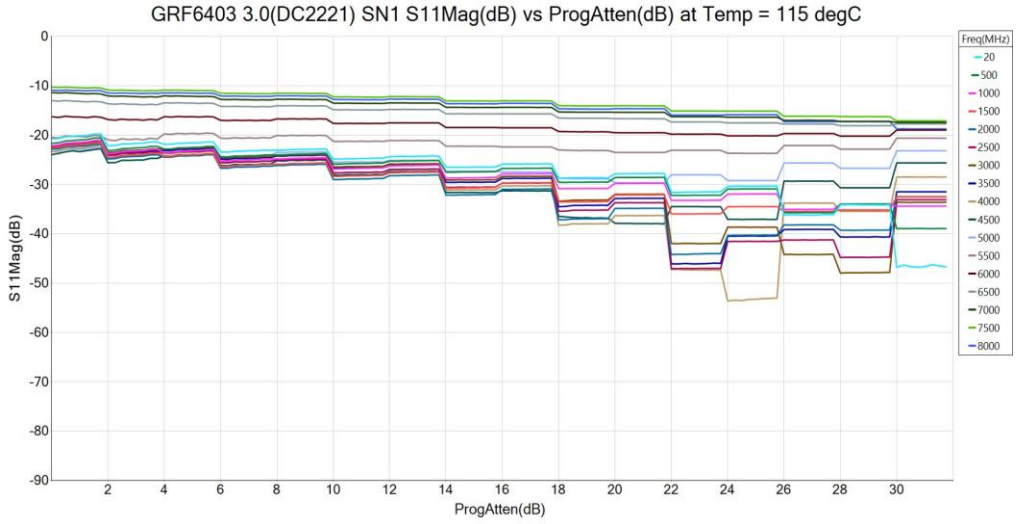


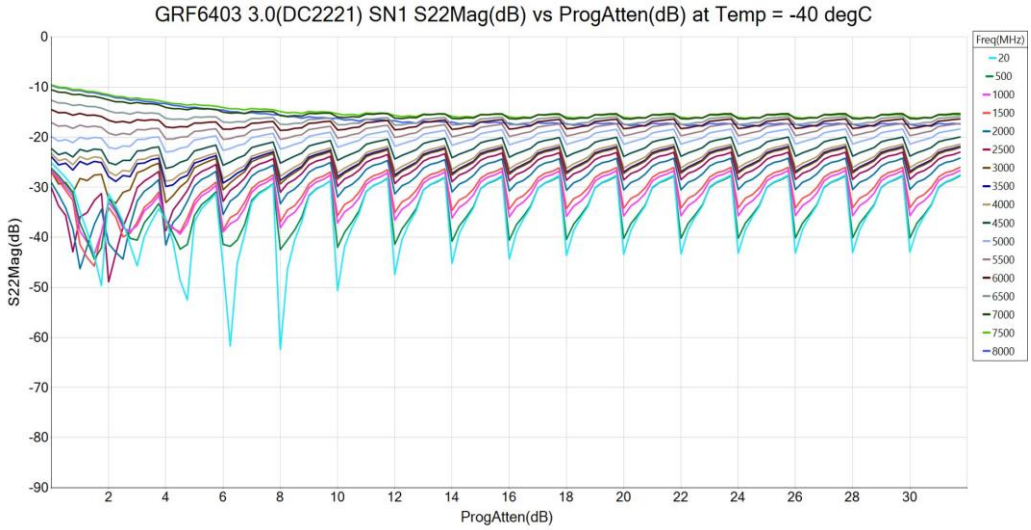


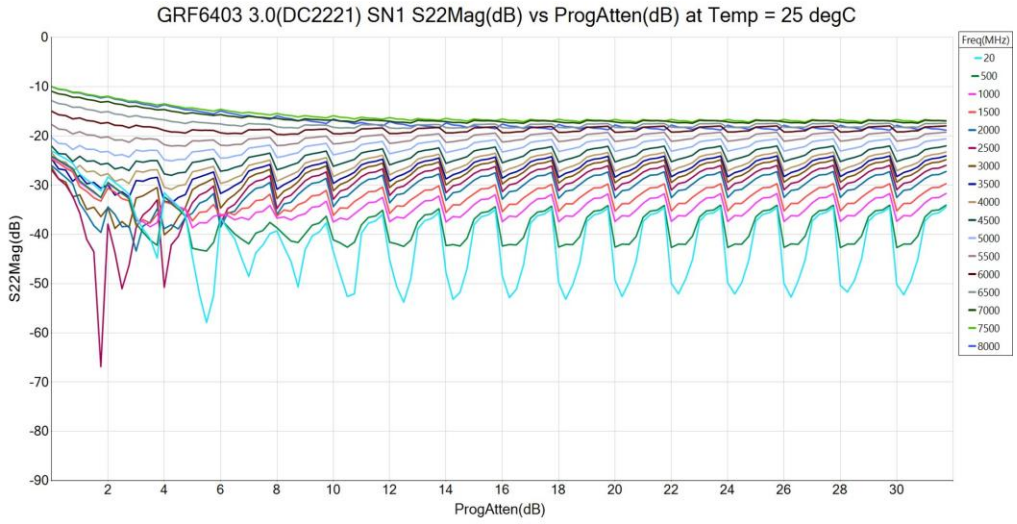


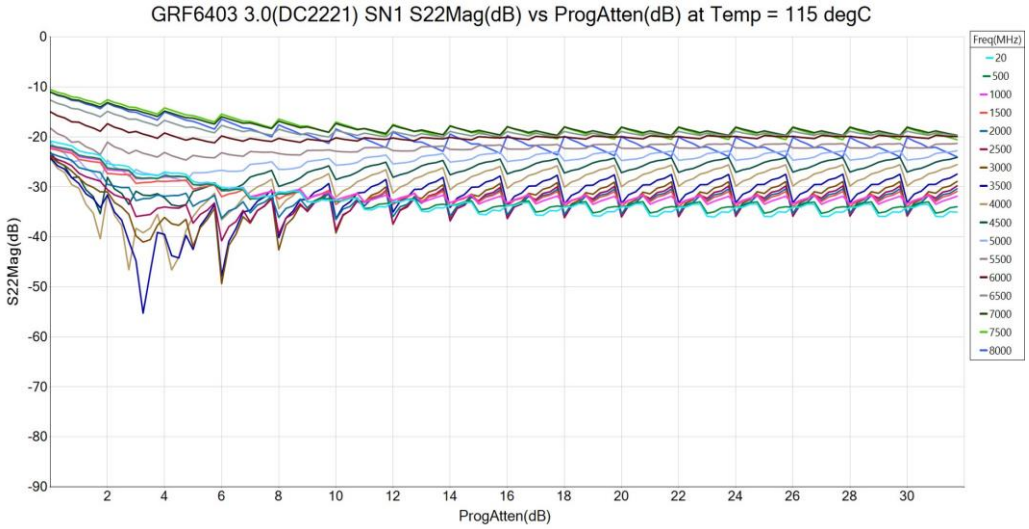


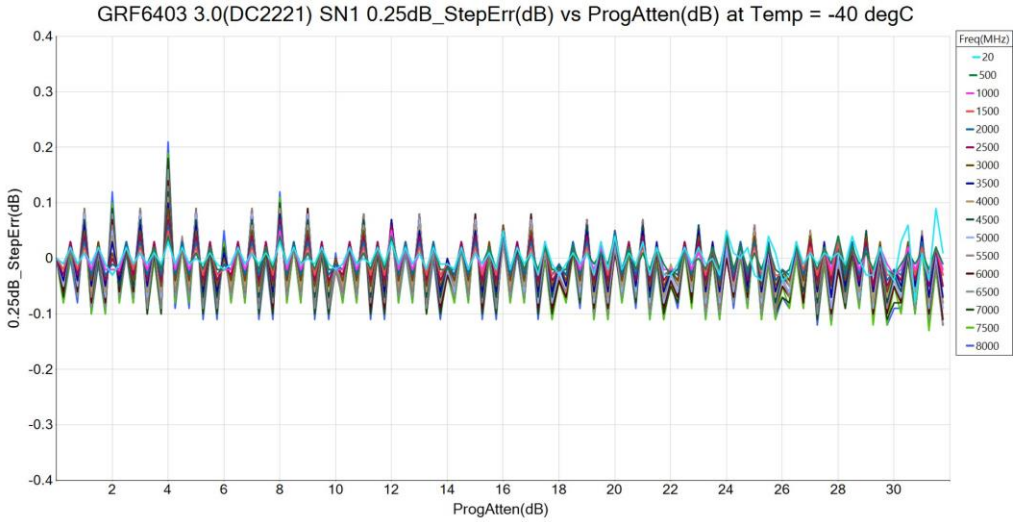


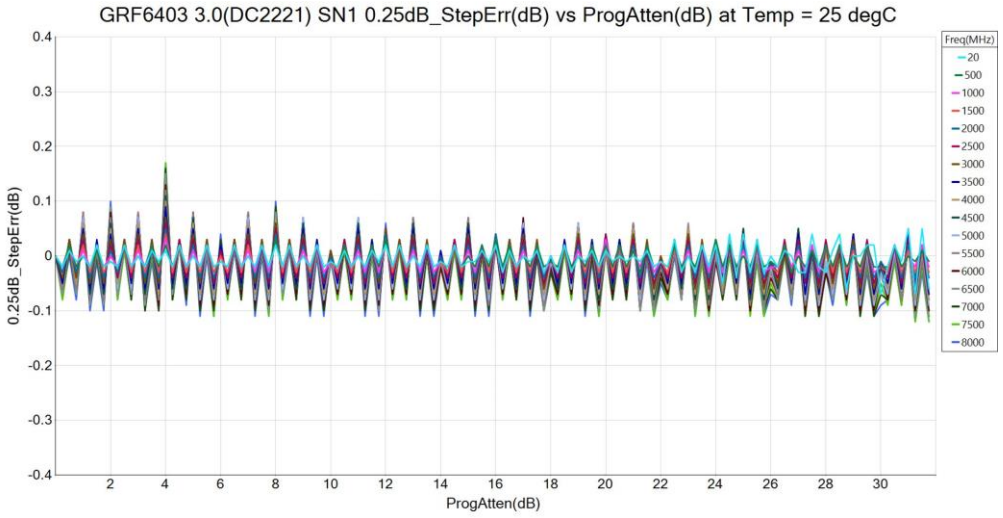


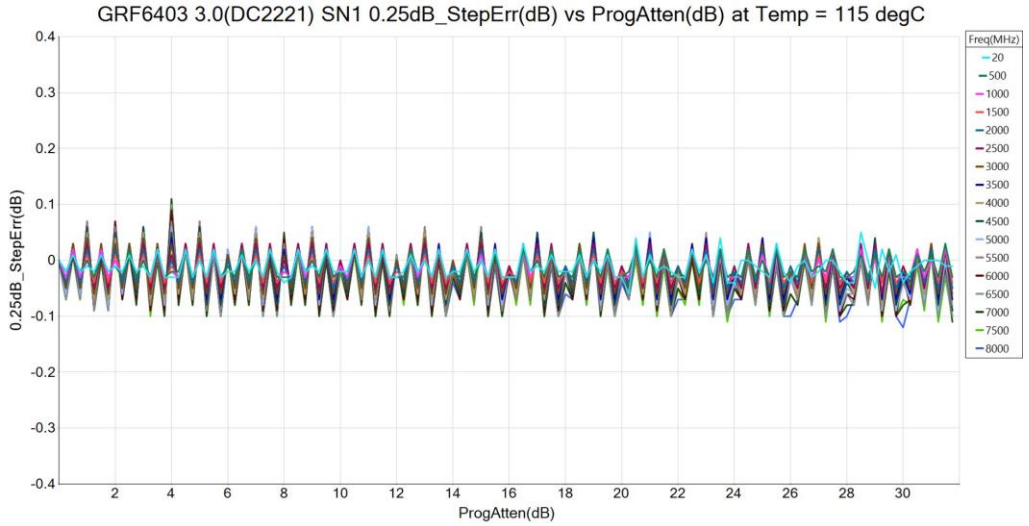


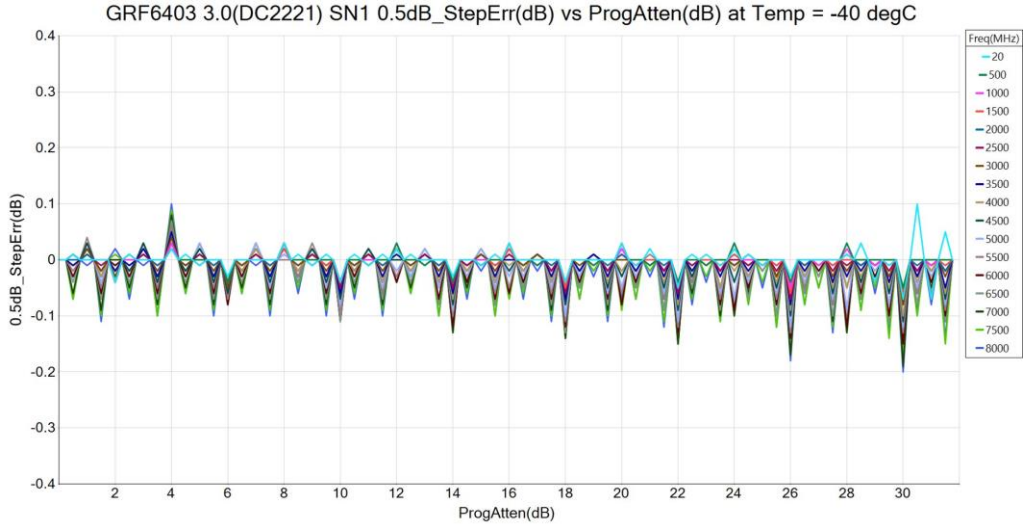


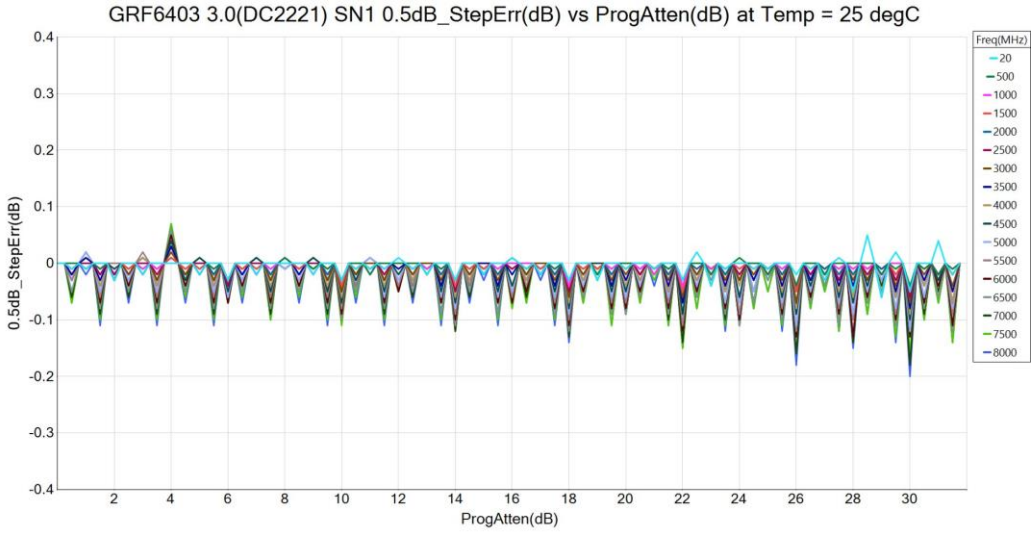


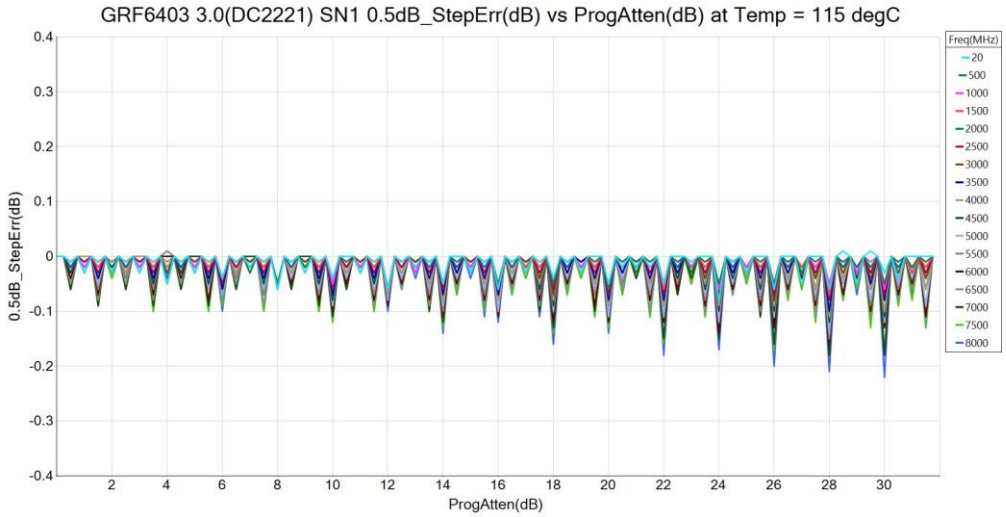


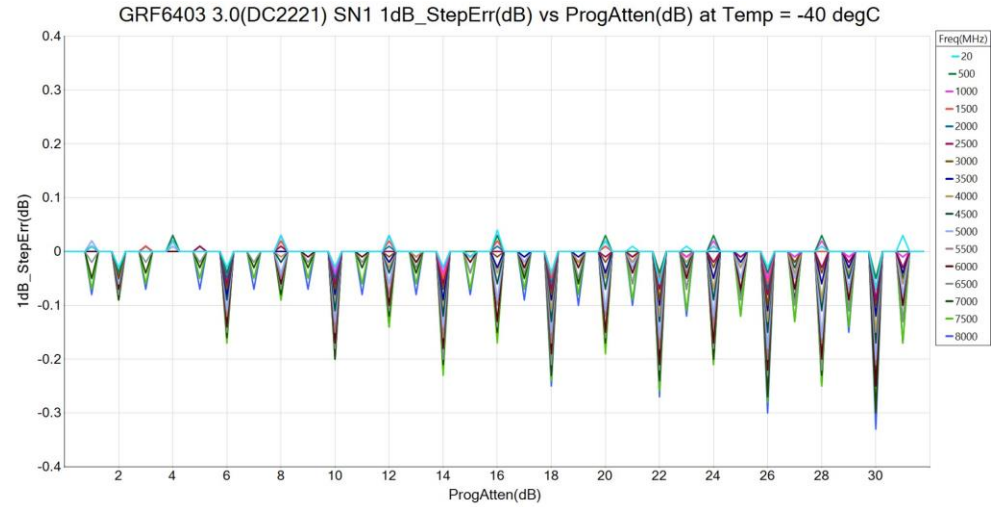


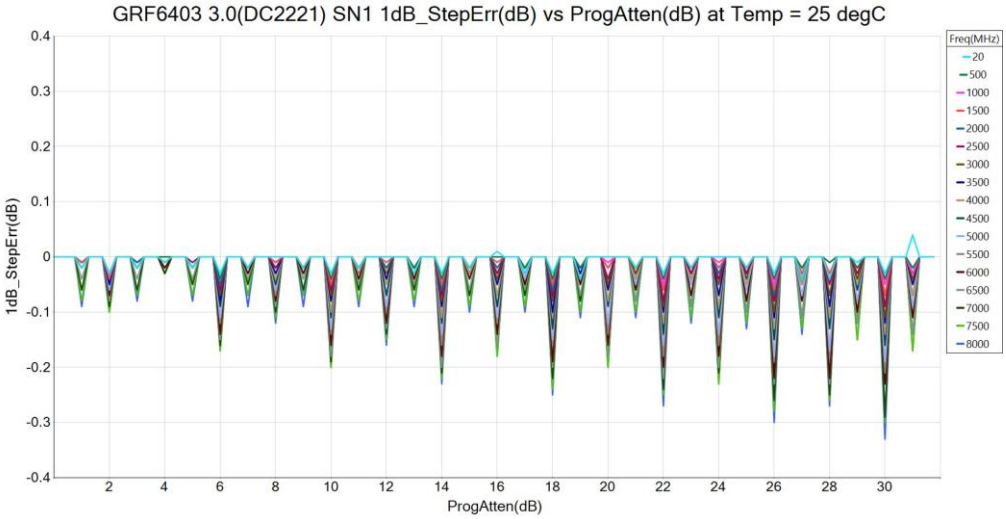


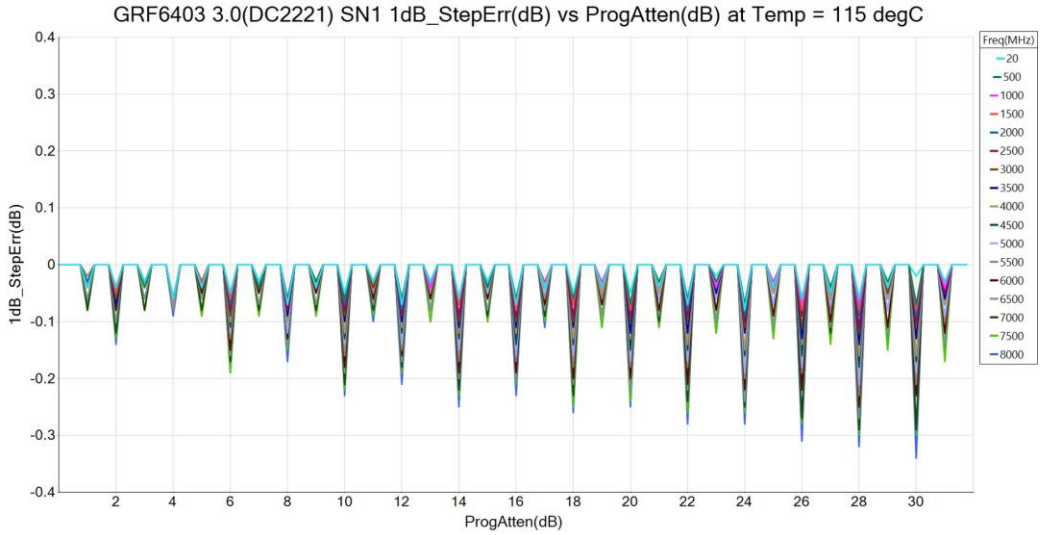


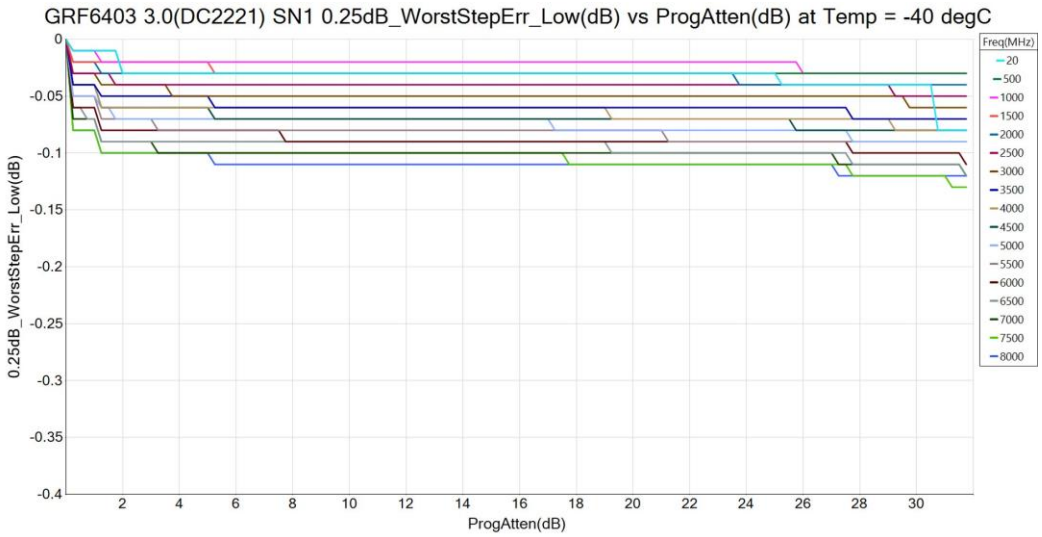


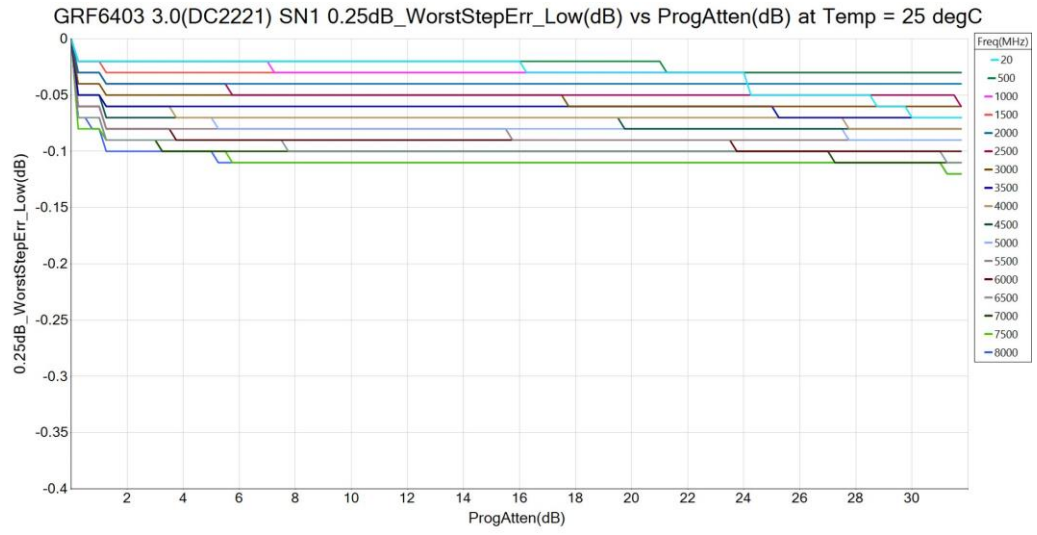


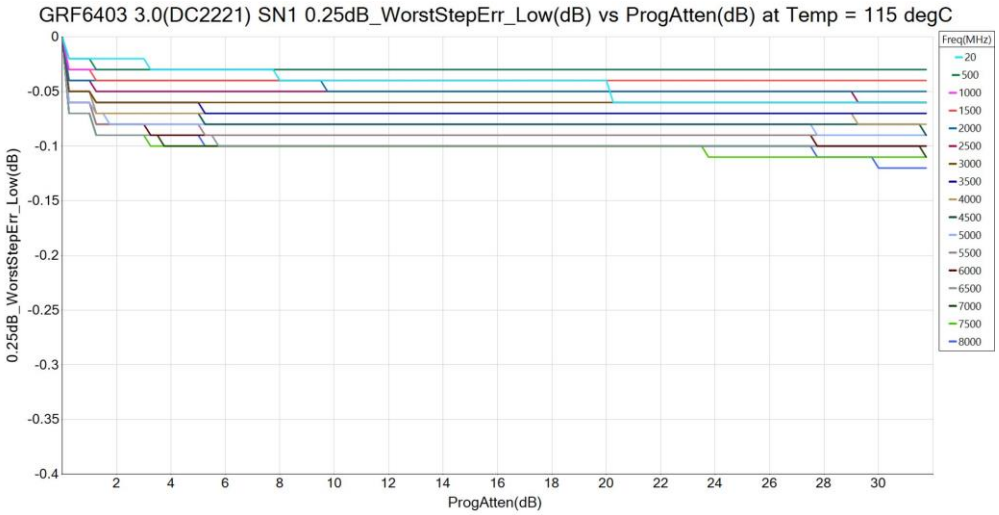


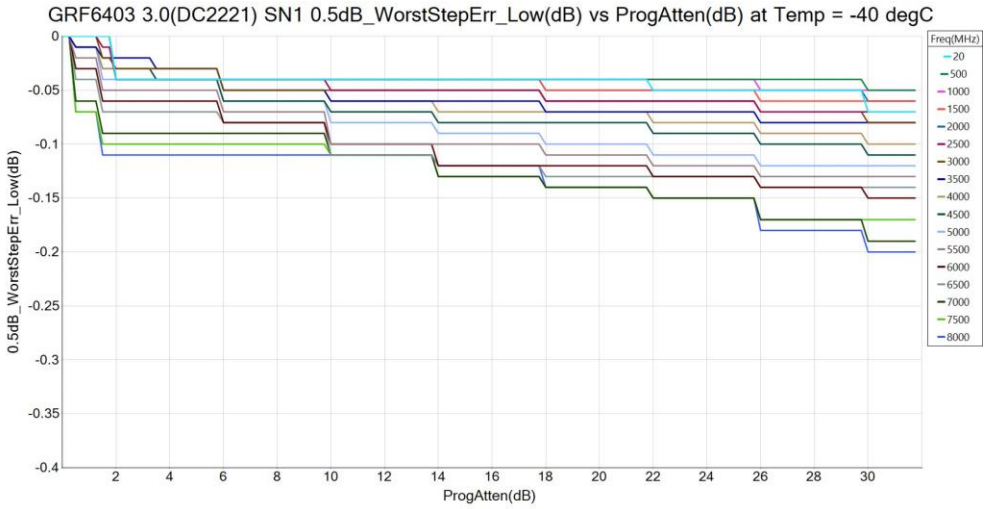


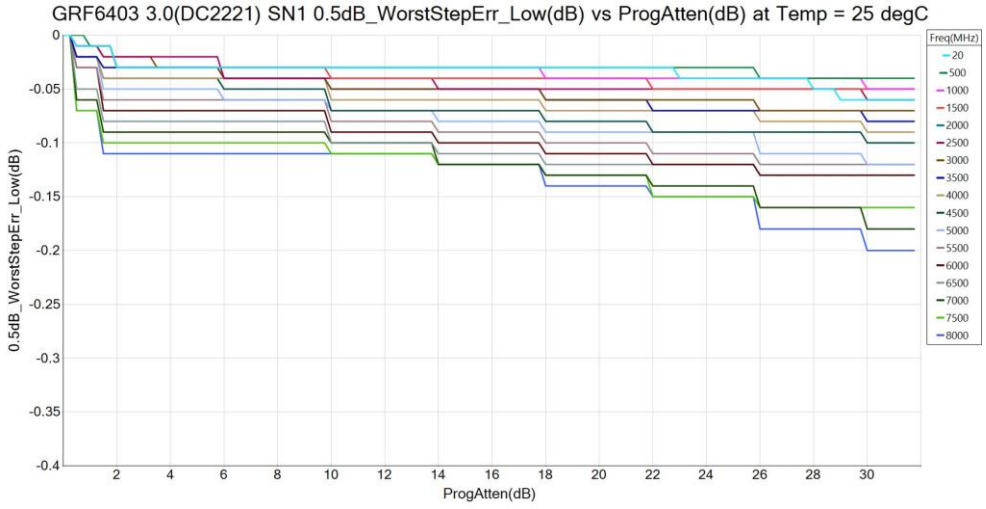


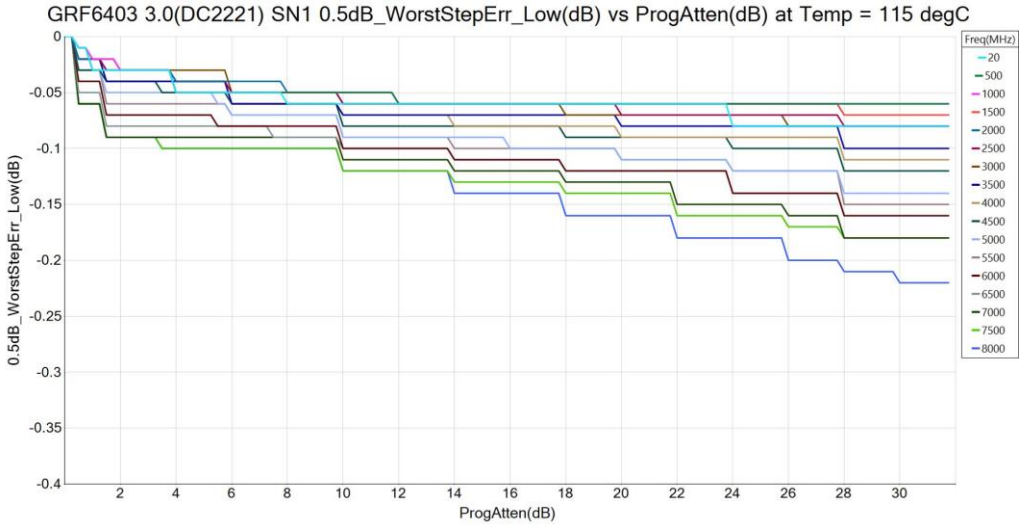


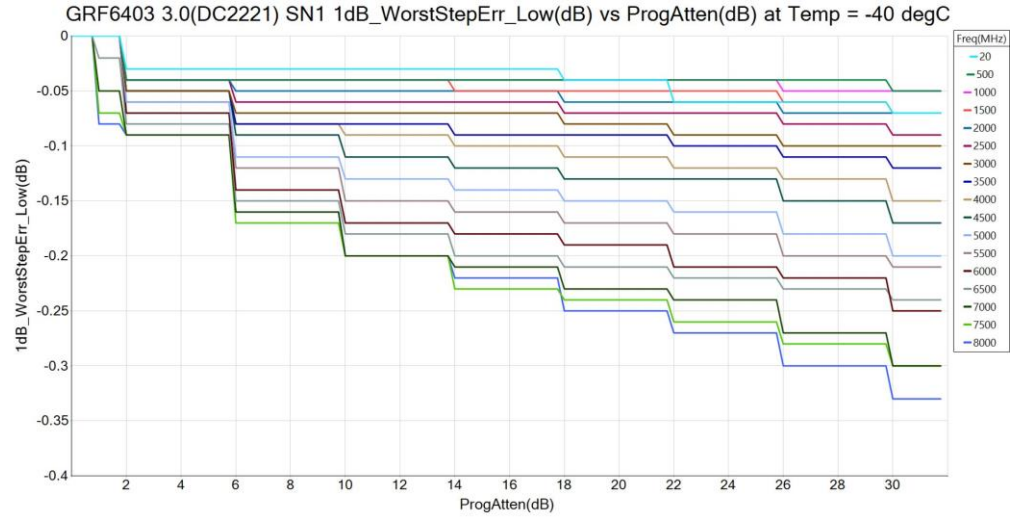


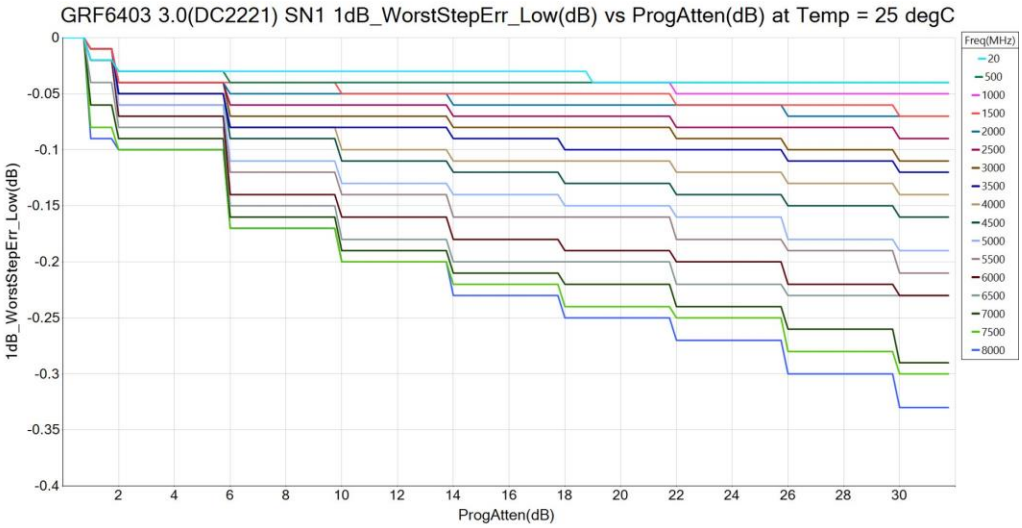


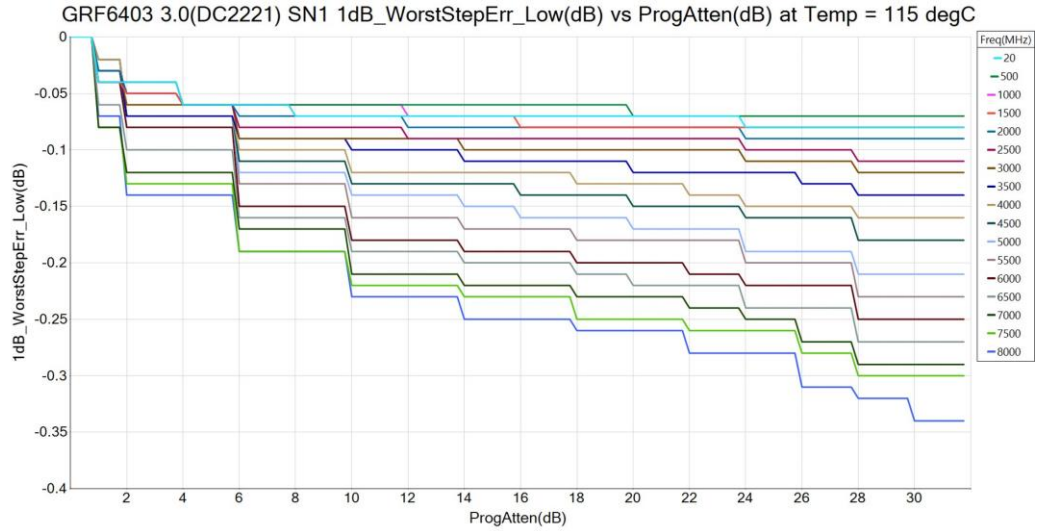


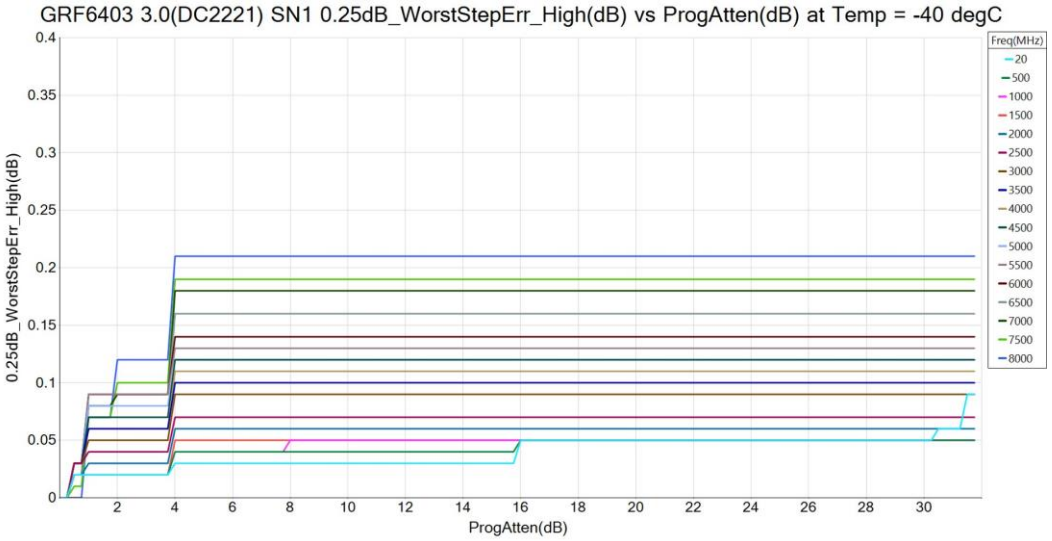


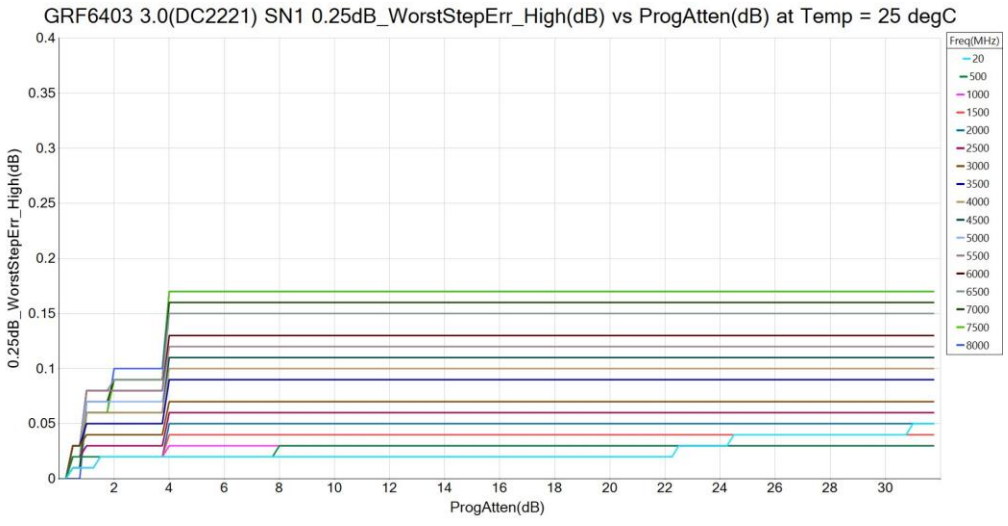


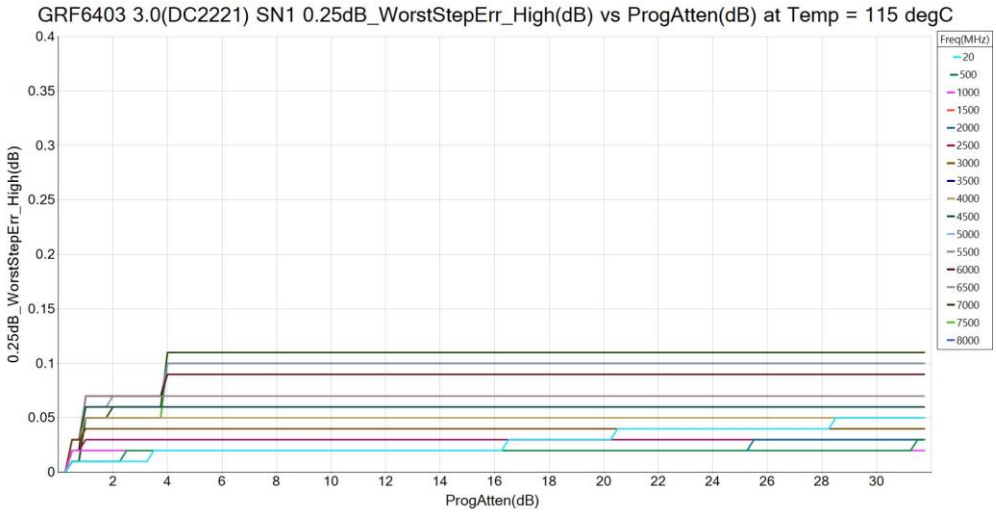


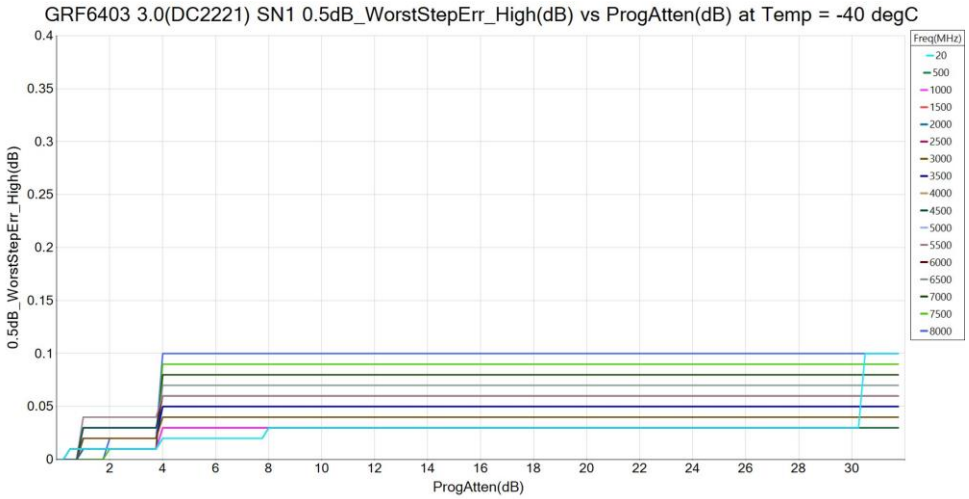


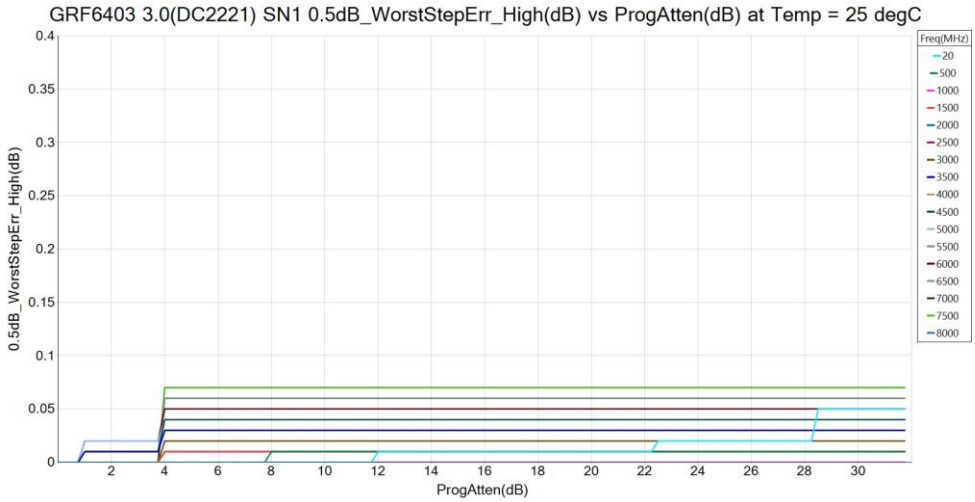


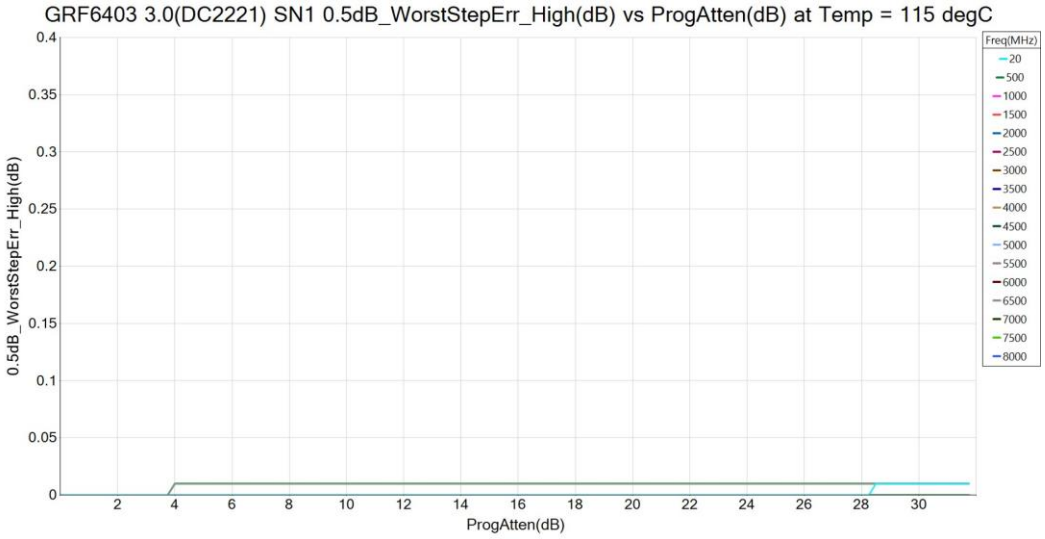


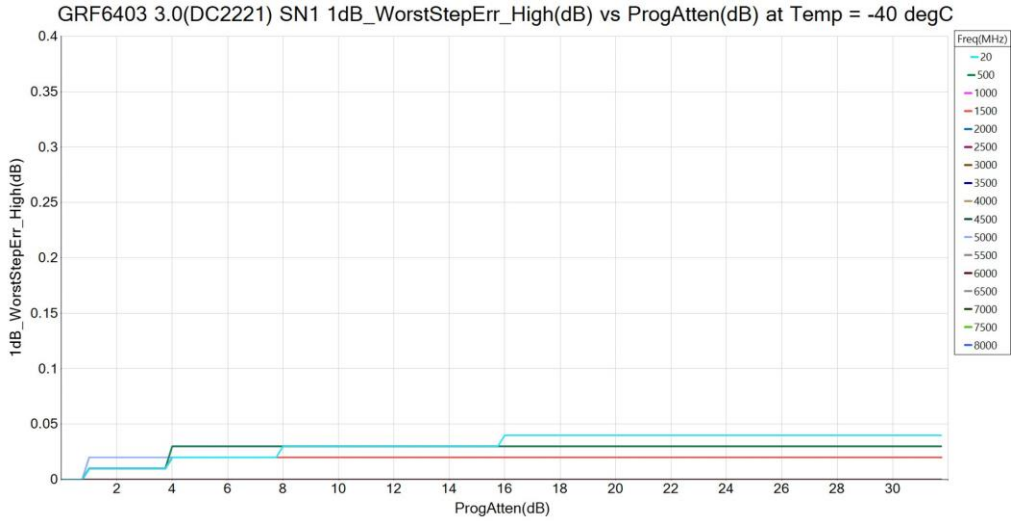


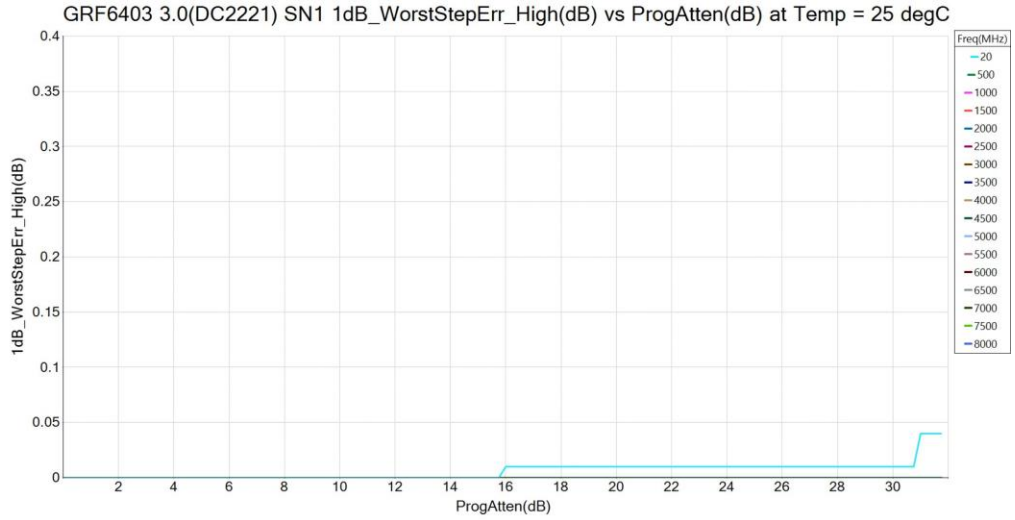


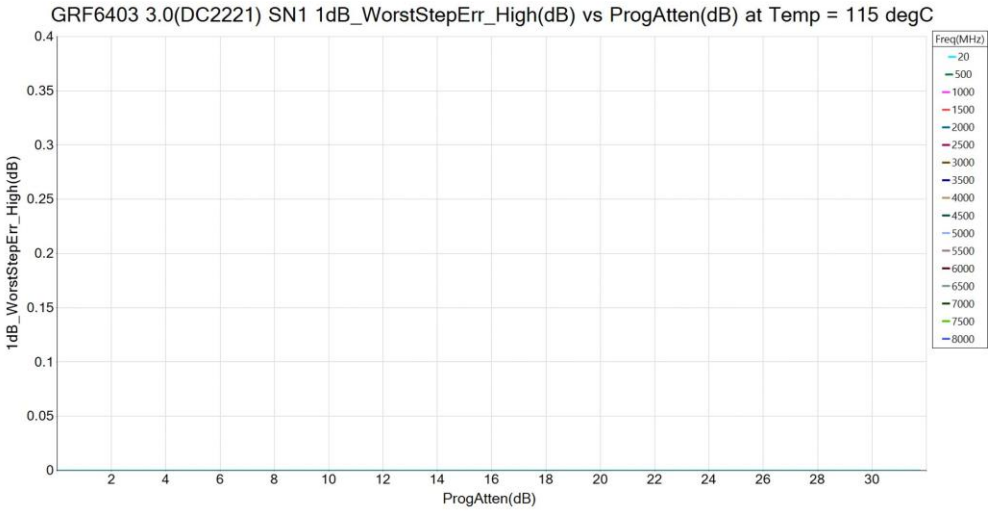


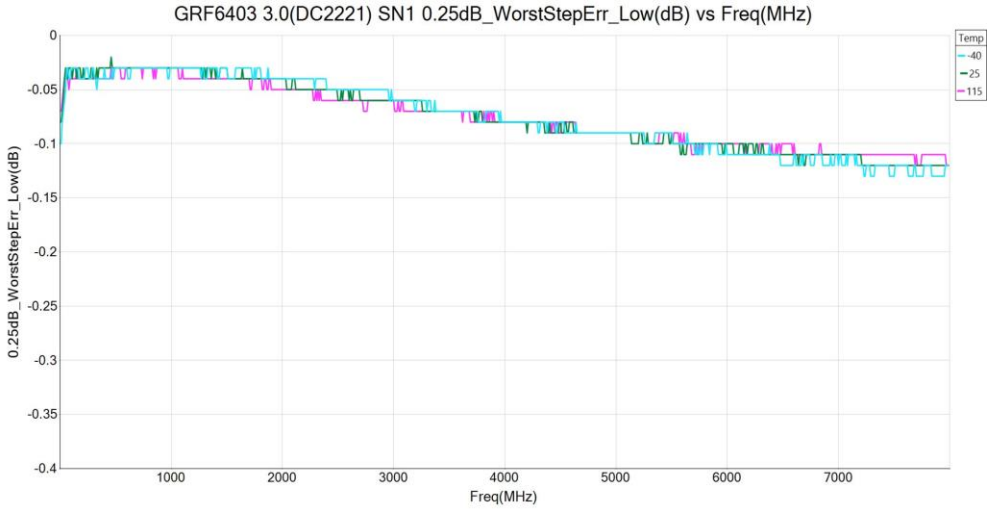


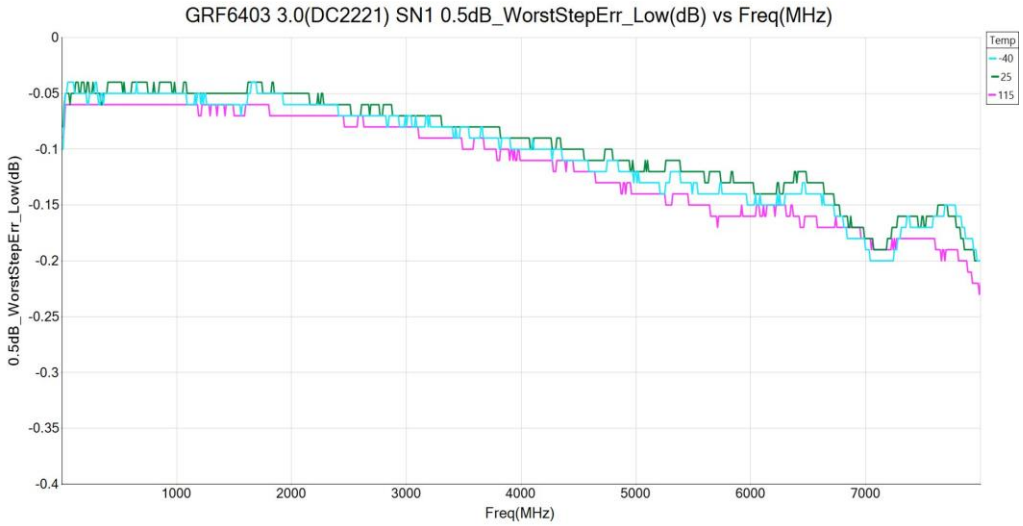


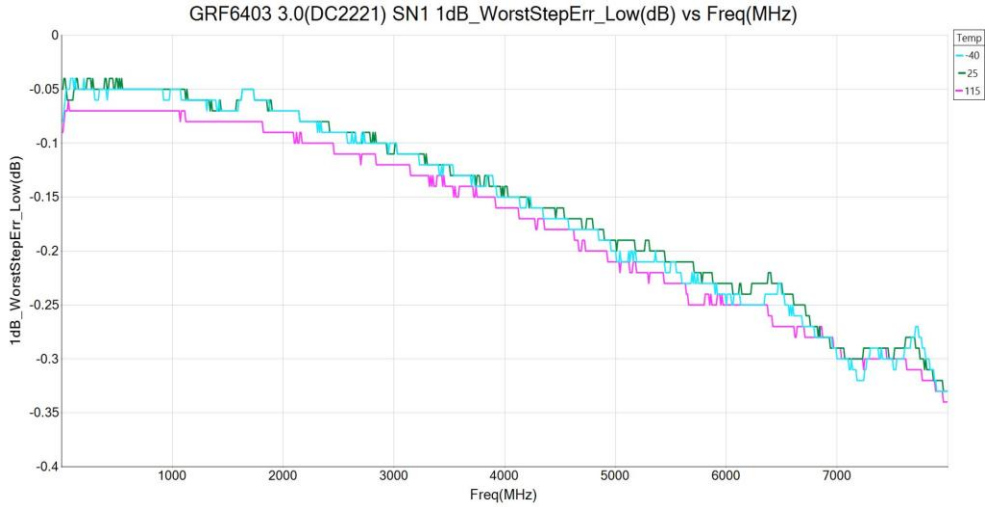


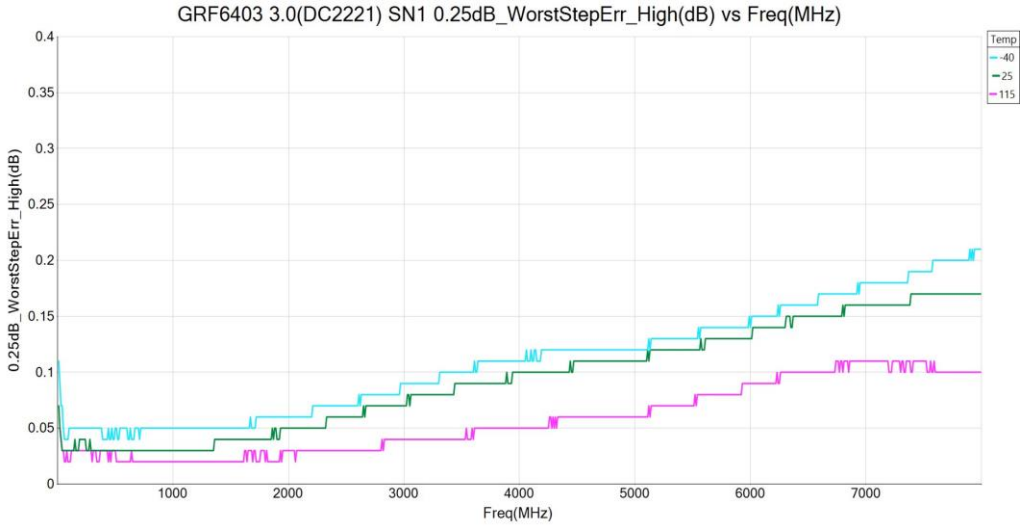


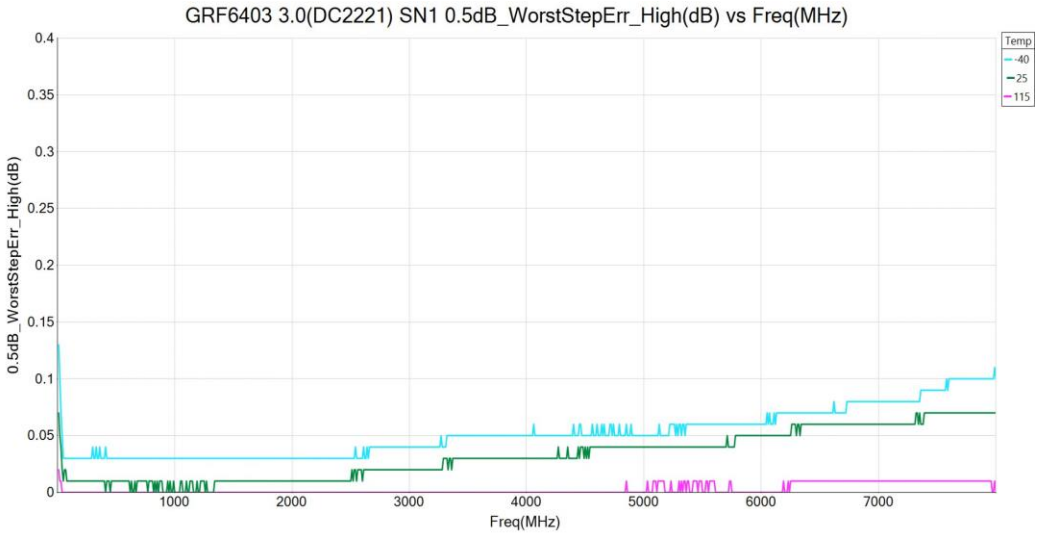


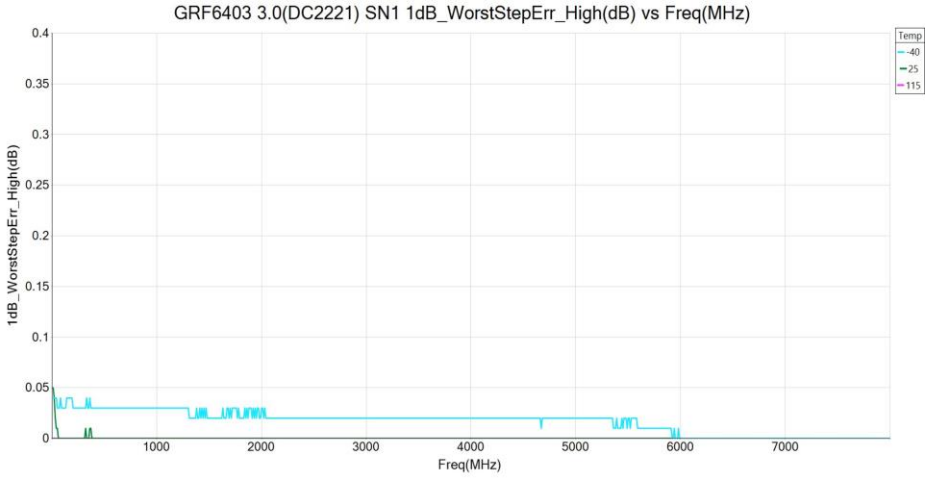


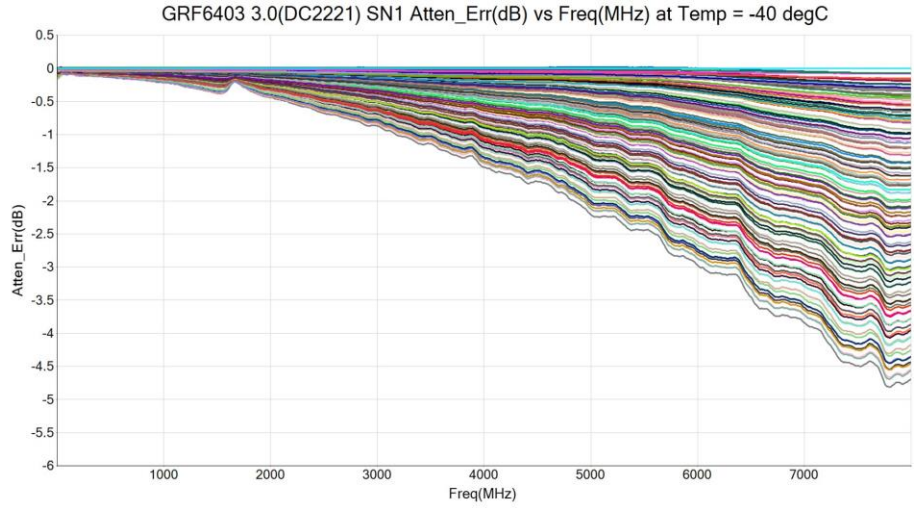


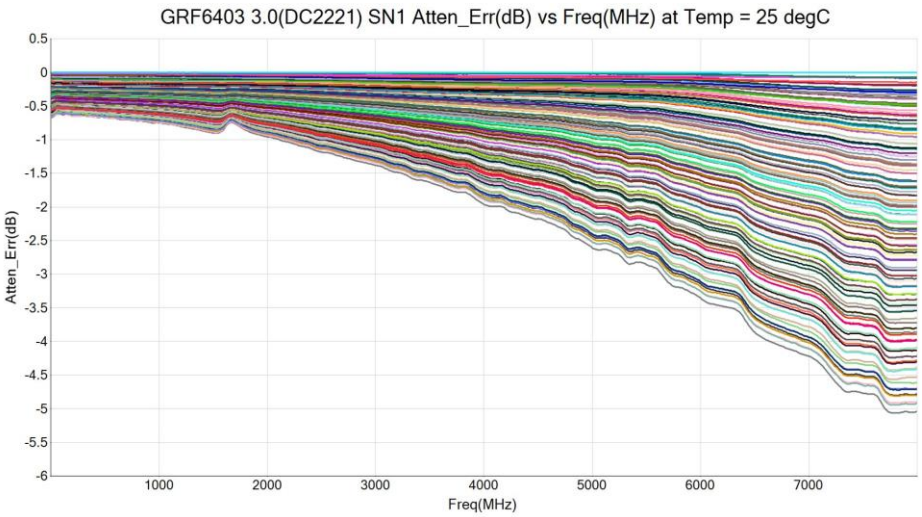


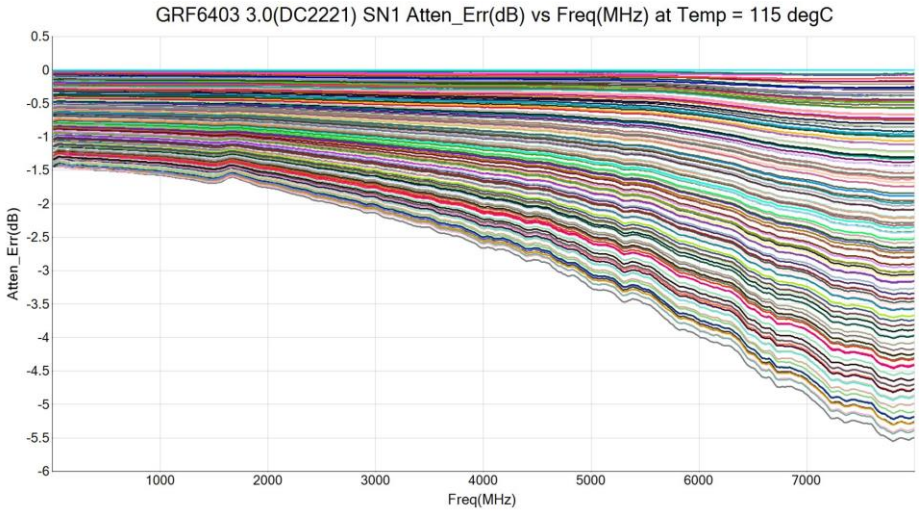


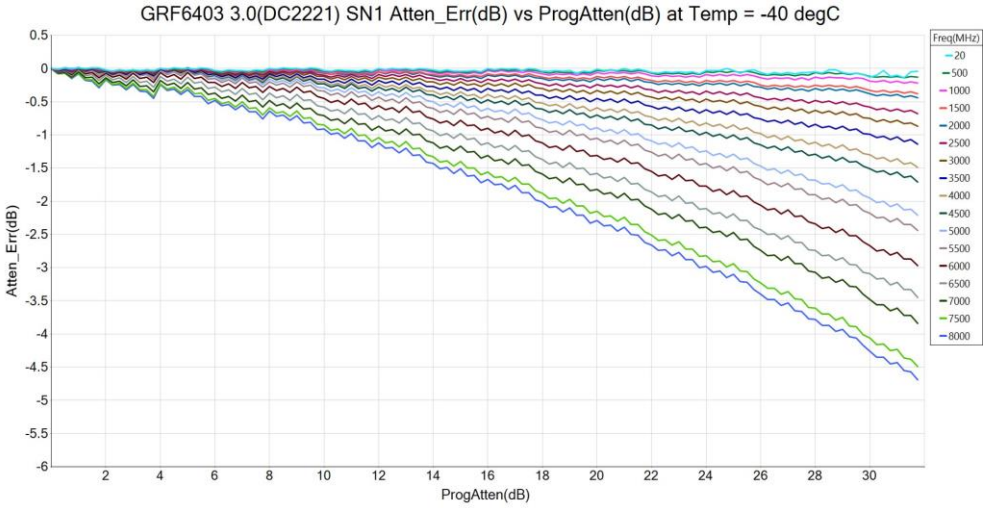


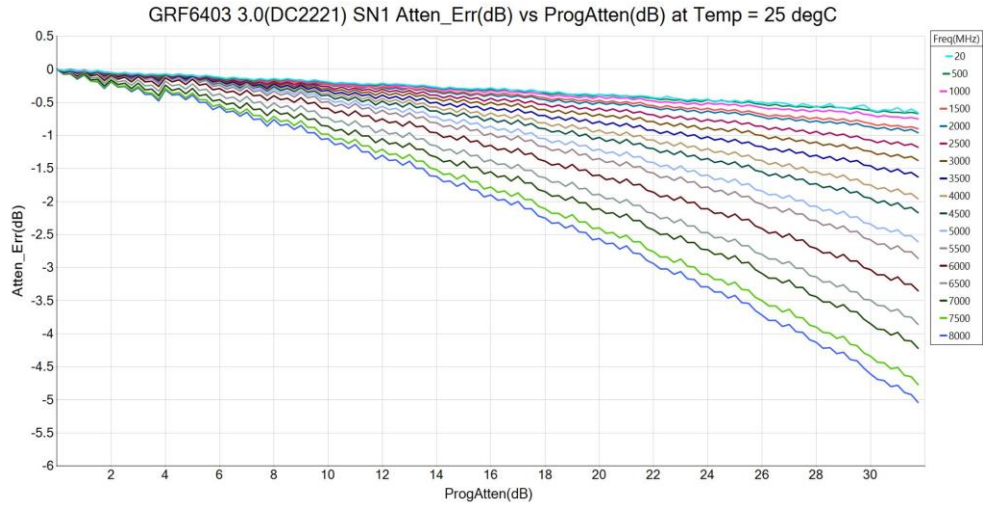

GRF6403 3.0(DC2221) SN1 1dB_WorstStepErr_High(dB) vs Freq(MHz)
Temp
-40
25
115
1dB_WorstStepErr_High(dB)
Freq(MHz)

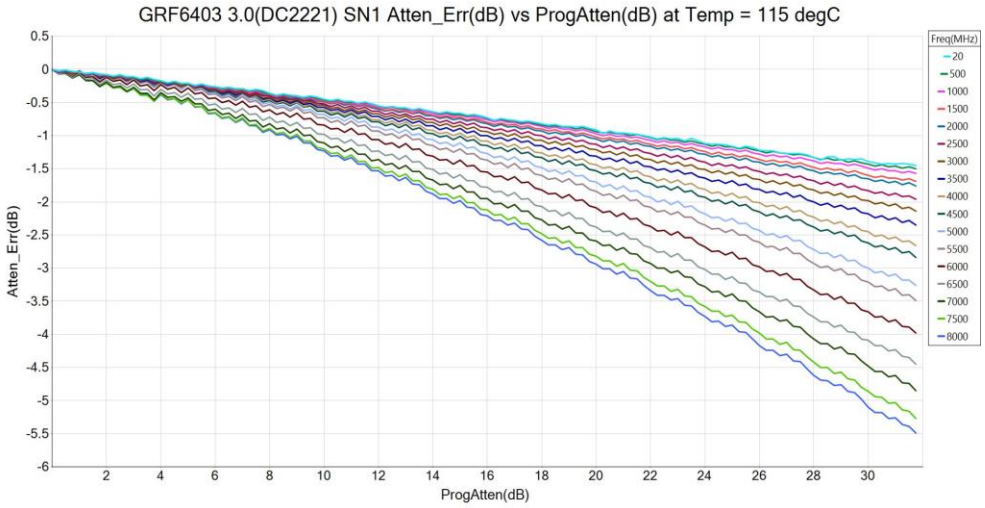

GRF6403 3.0(DC2221) SN1 Atten_Err(dB) vs Freq(MHz) at Temp = -40 degC
Atten_Err(dB)
Freq(MHz)

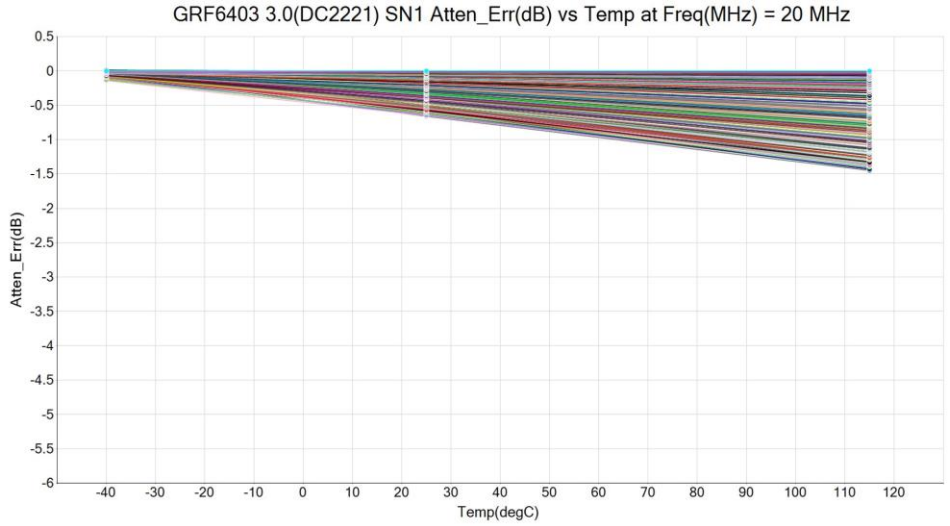

GRF6403 3.0(DC2221) SN1 Atten_Err(dB) vs Freq(MHz) at Temp = 25 degC
Atten_Err(dB)
Freq(MHz)

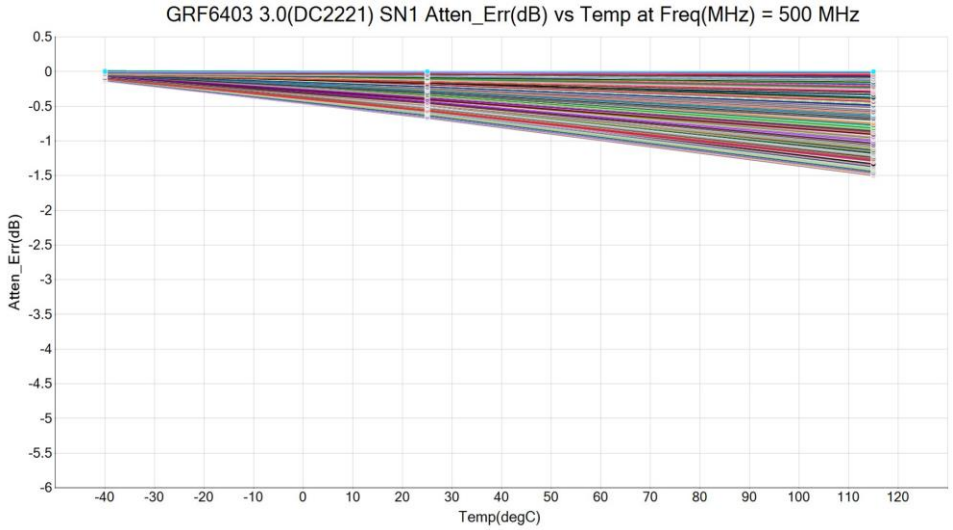


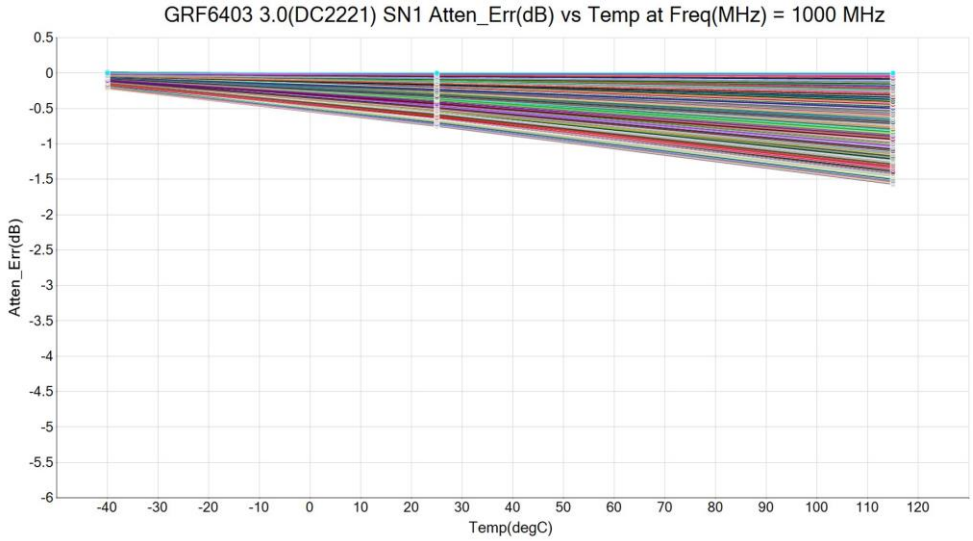


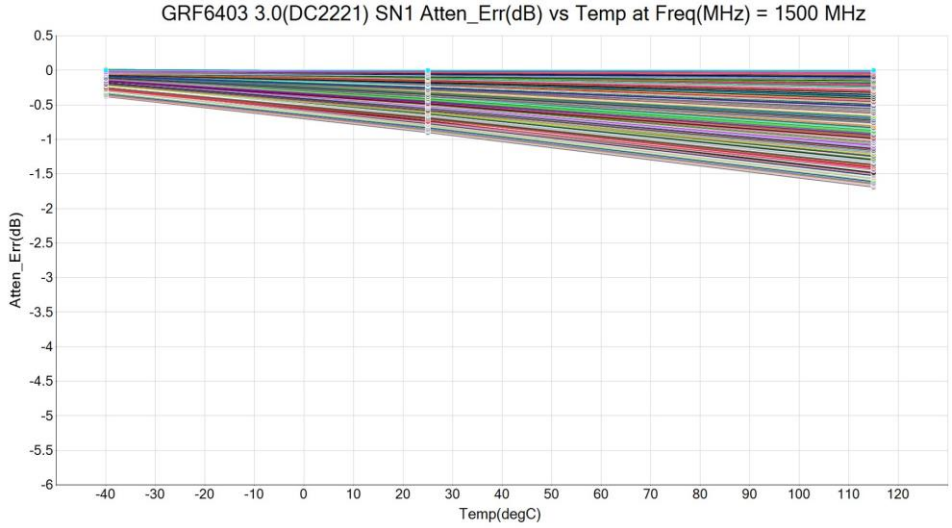


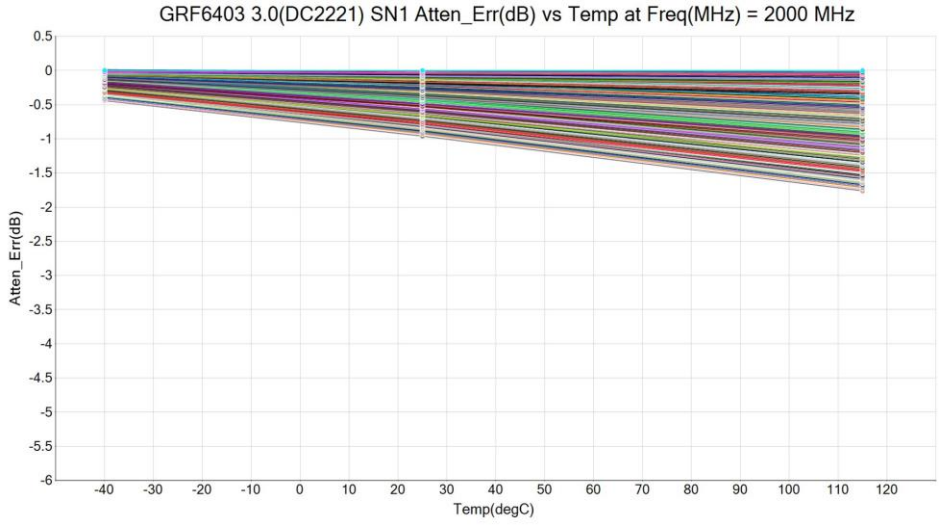












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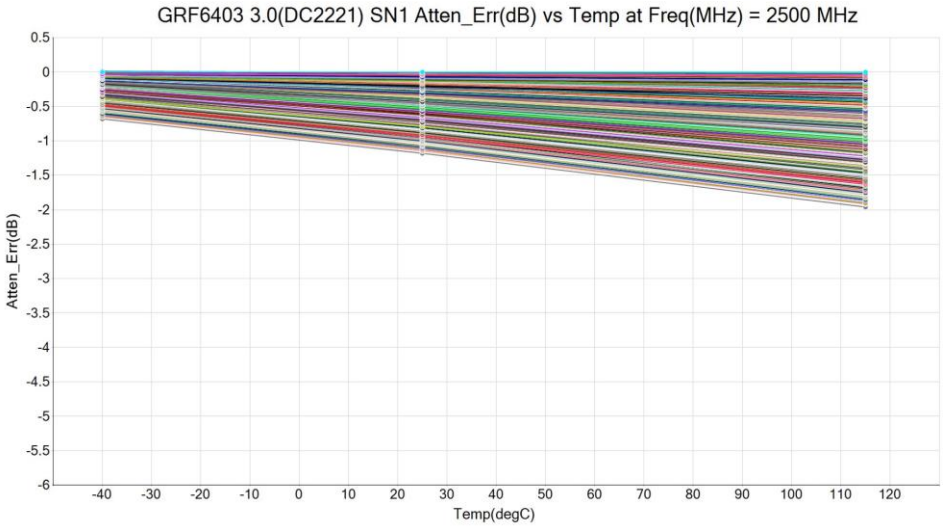

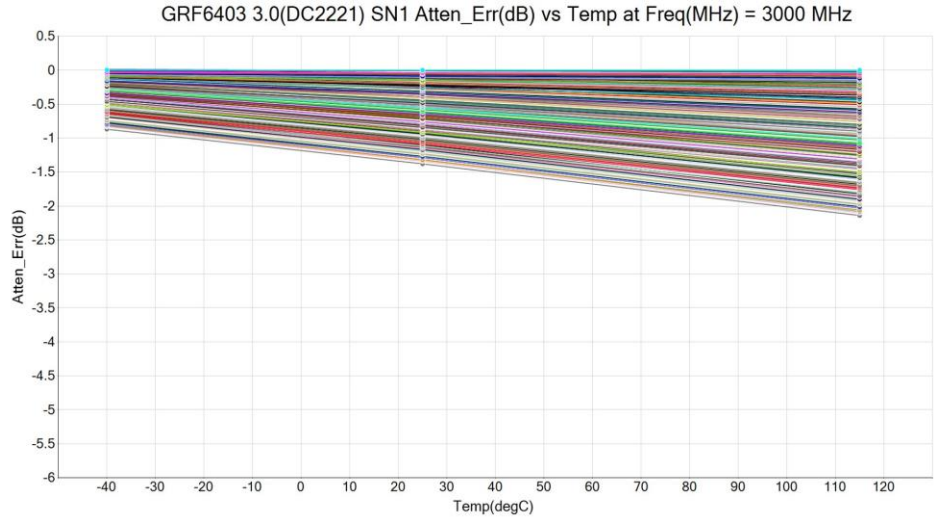

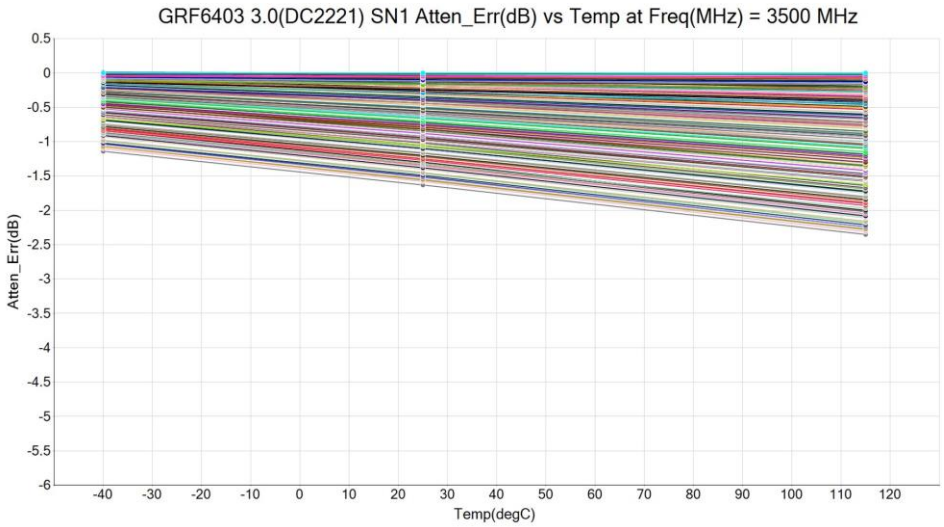

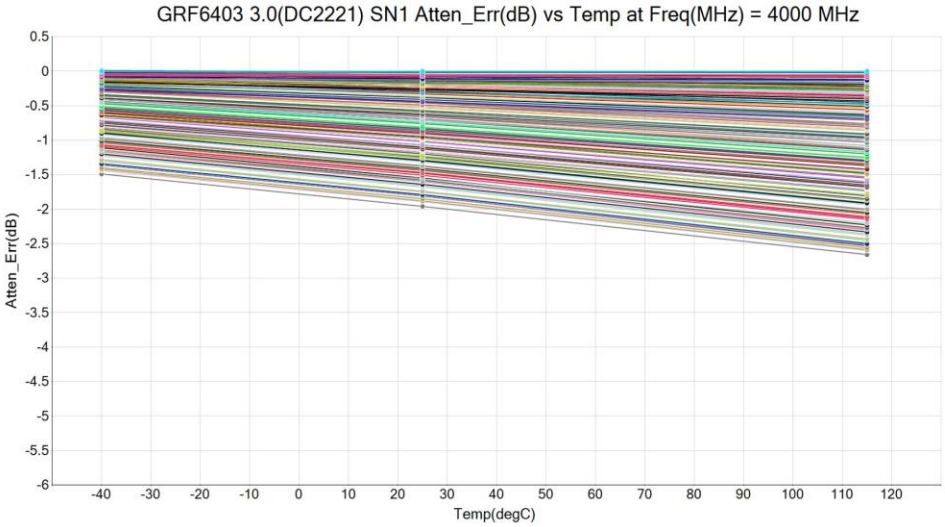

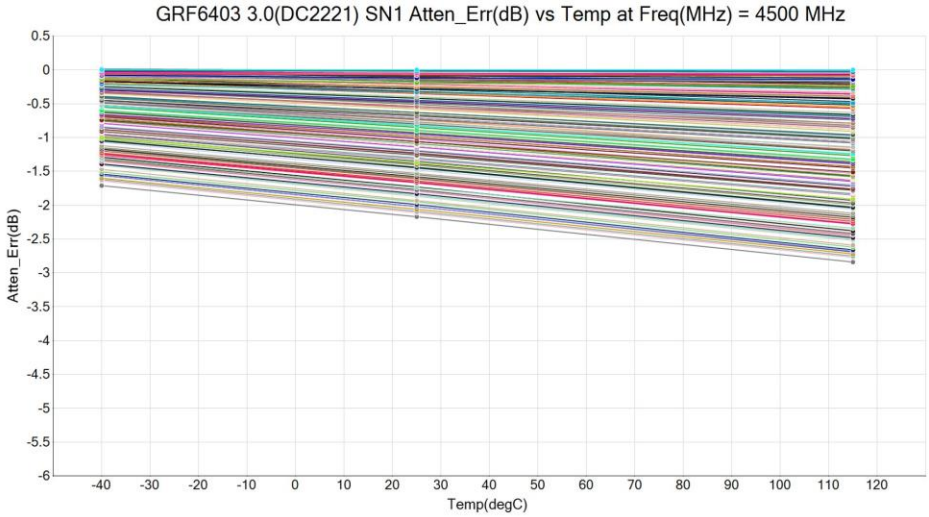

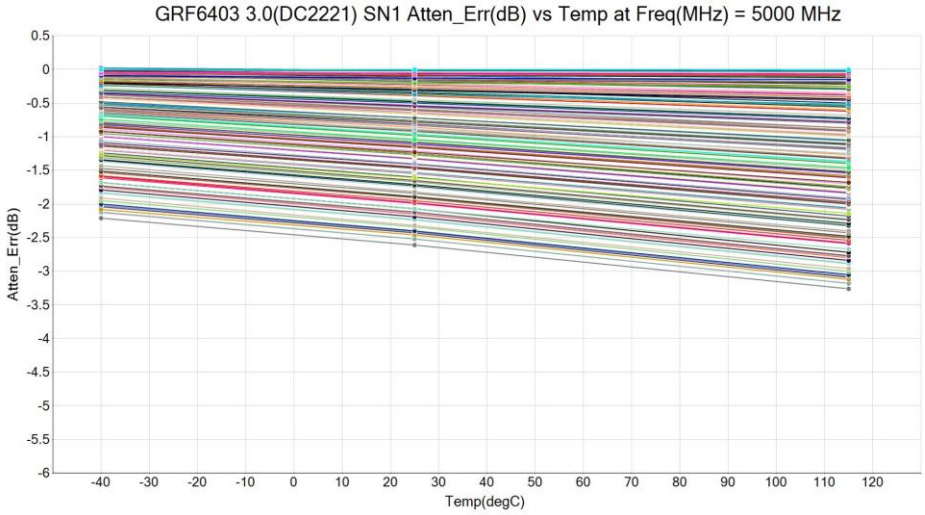

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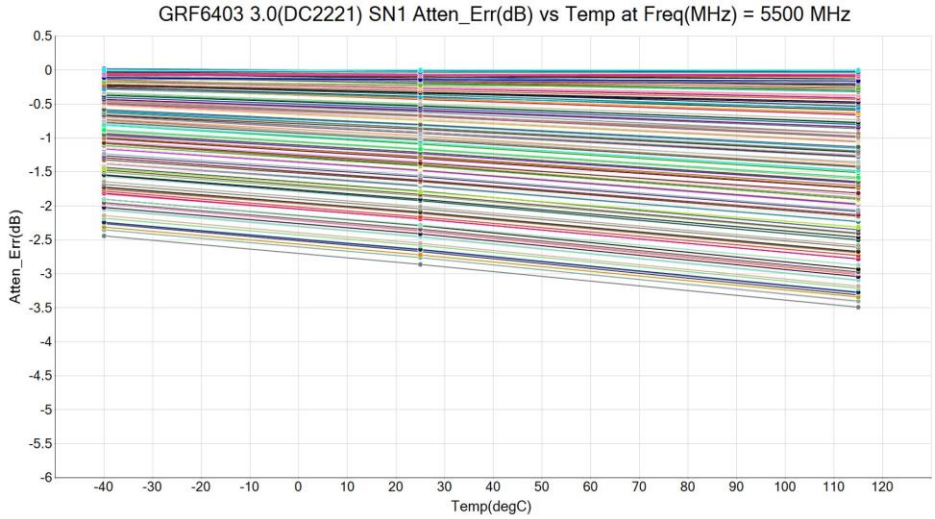
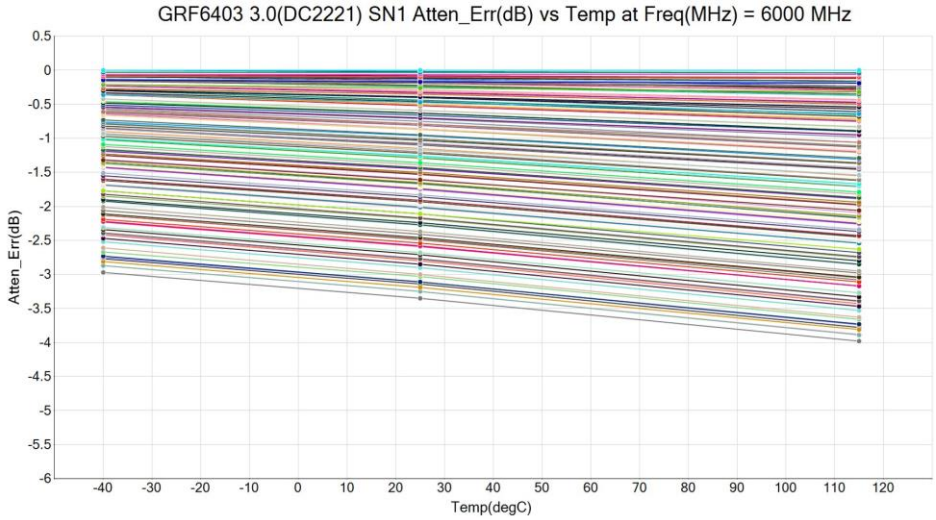
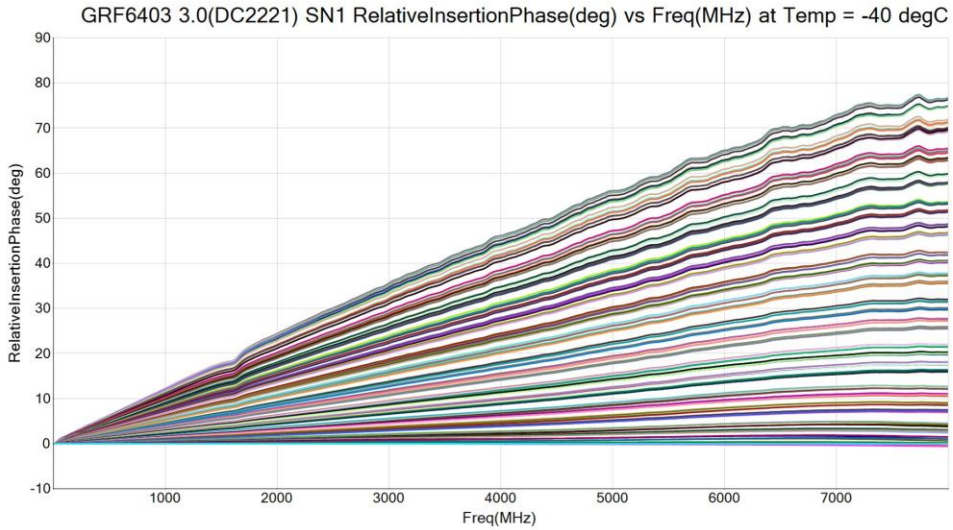
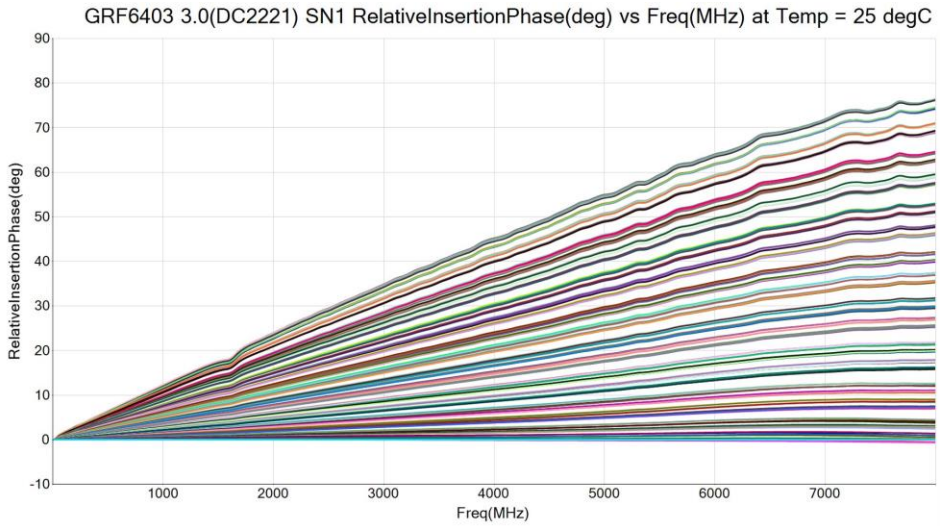
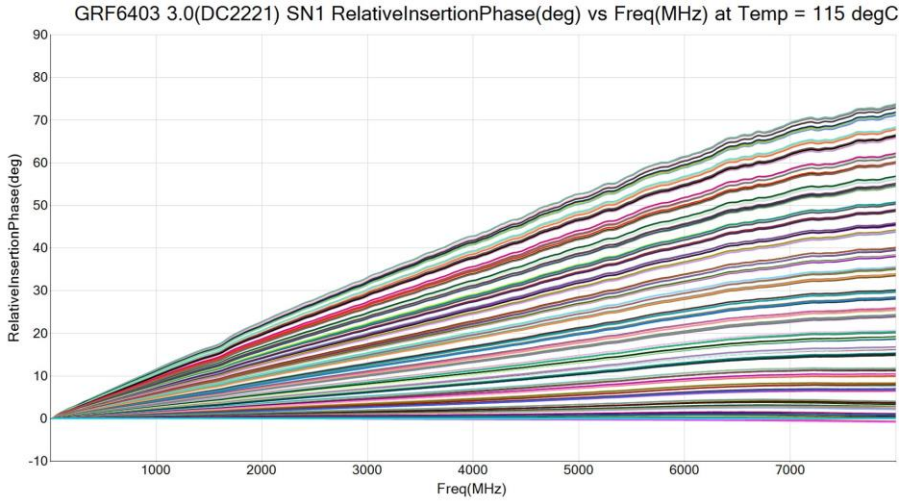
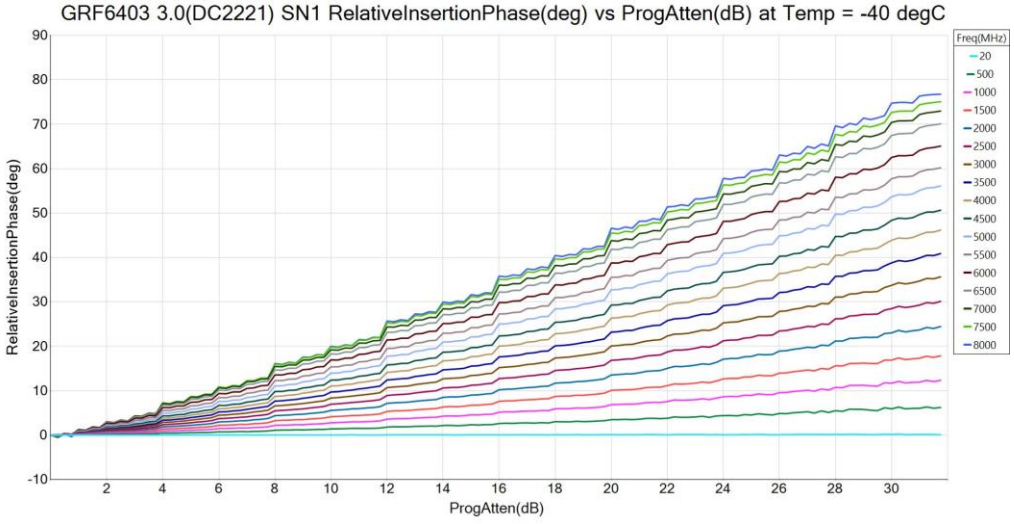


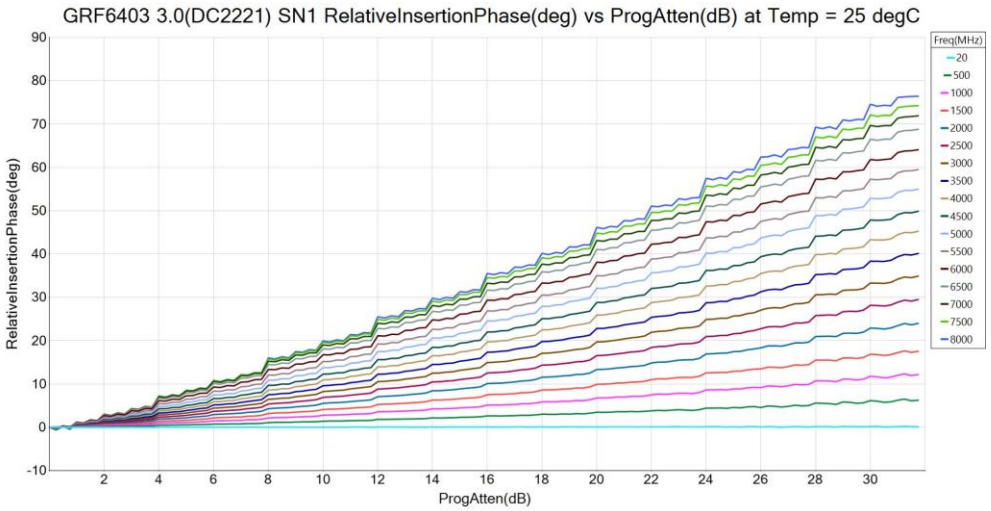


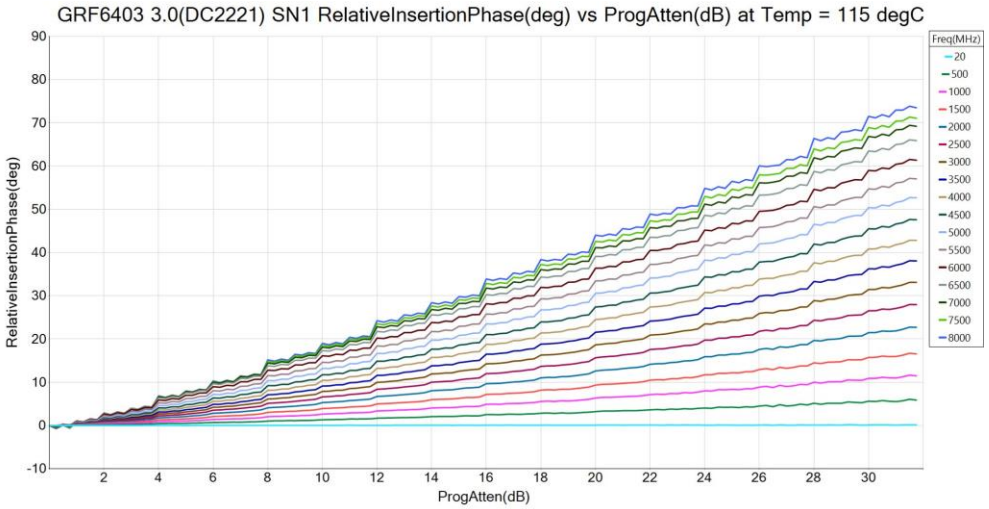


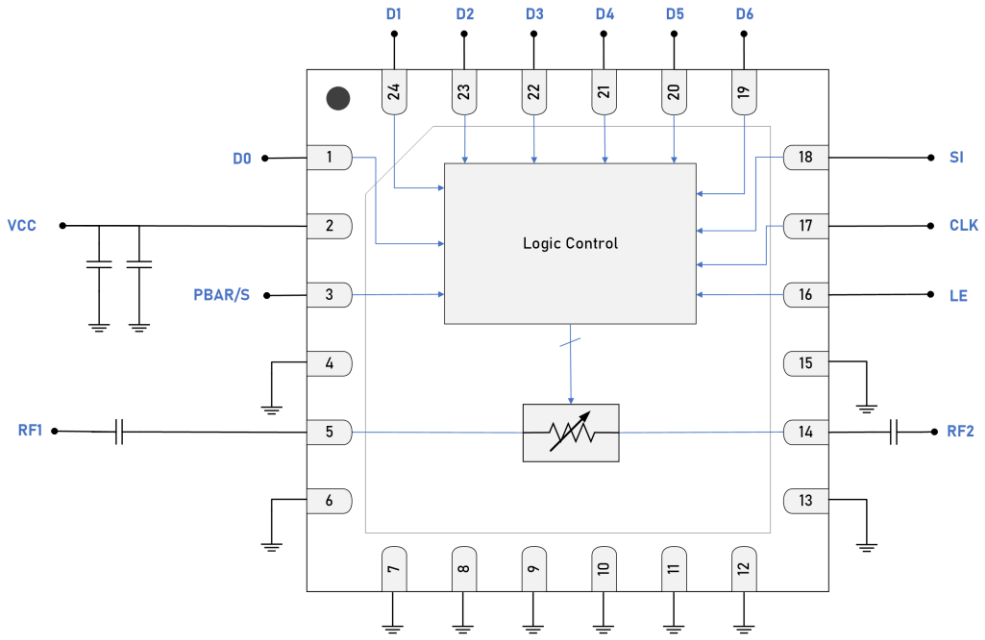








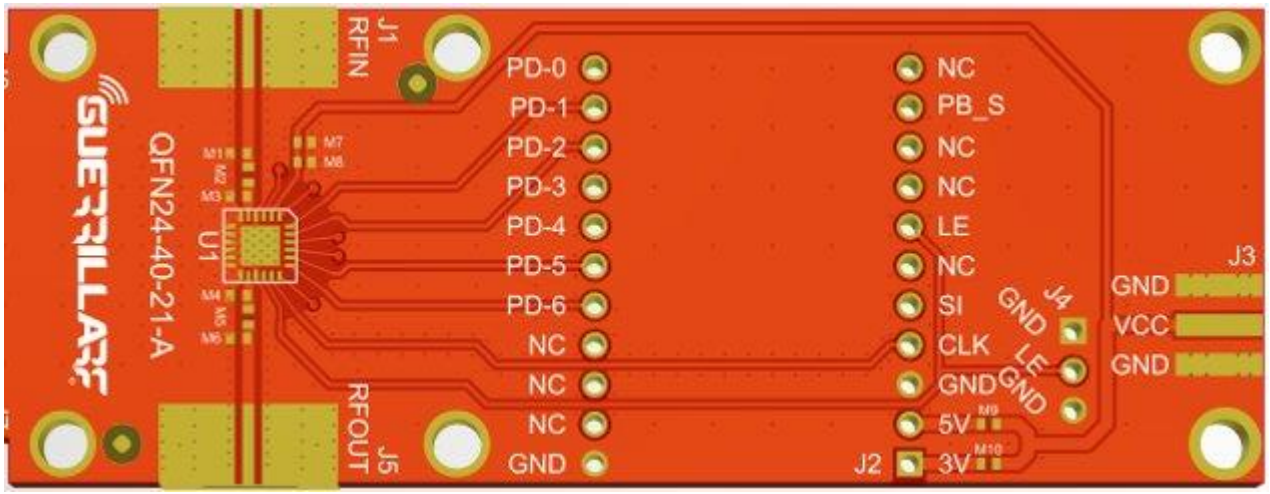




NOTE: *Do not apply DC voltage to pins 4 (RF1) and 9 (RF2).* DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages. As a matter of good practice, it is recommended that DC blocks be used as a precaution.

The DSA will not generate DC voltages on either pins 1 and 9; as such, the blocking capacitors can be omitted in cases where it can be *guaranteed* that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the RF1 and RF2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these safeguard components.

GRF6403 Application Schematic

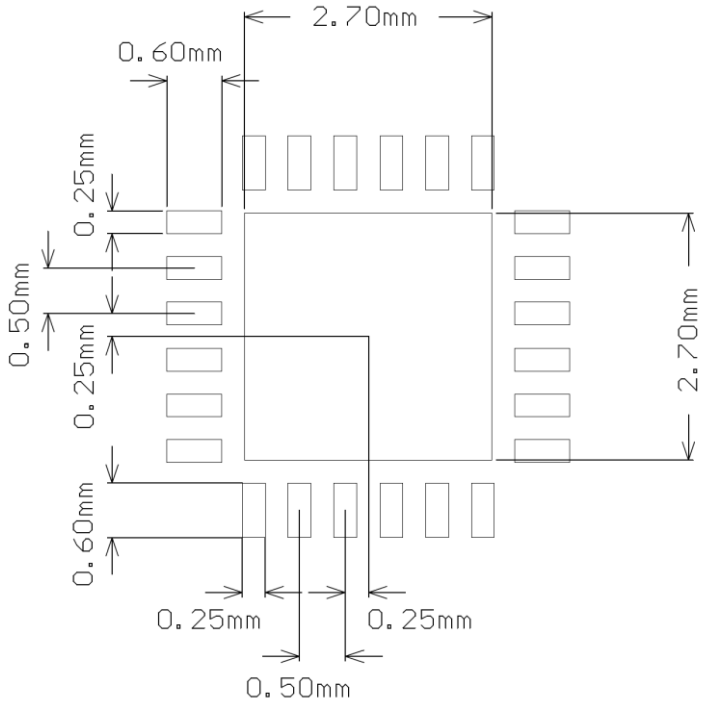


GRF6403 Evaluation Board Assembly Diagram

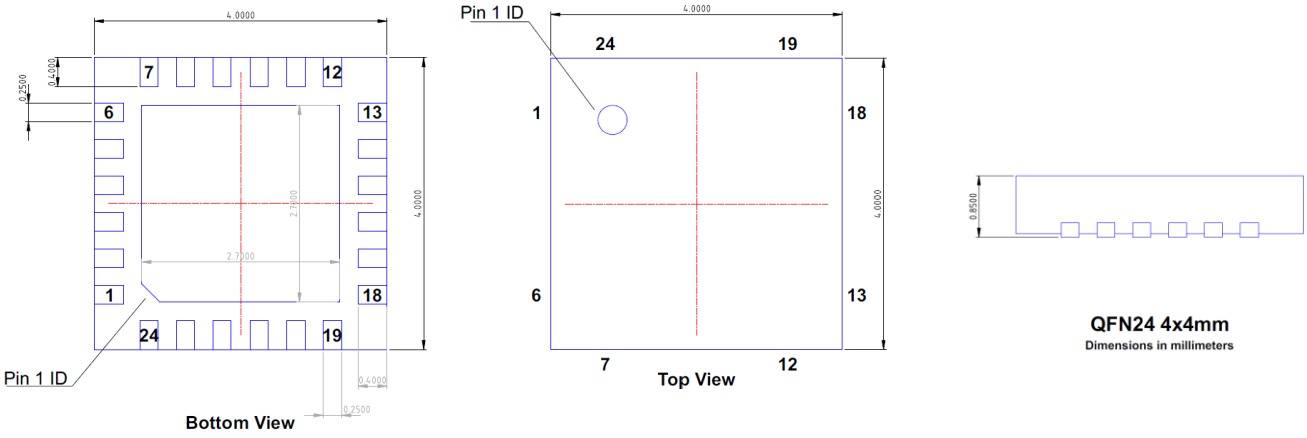
GRF6403 Evaluation Board Assembly Diagram Reference

Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1					DNP	
M2	Jumper, Solid Copper	Koa/Speer	TLRZ1ETTB	0 Ω	0402	OK
M3					DNP	
M4					DNP	
M5	Jumper, Solid Copper	Koa/Speer	TLRZ1ETTB	0 Ω	0402	OK
M6					DNP	
M7	Capacitor	Murata	GRM	10 nF	0402	OK
M8	Capacitor	Murata	GRM	1 µF	0402	OK
J1	RF Jack, 10 GHz	Johnson	SMA	142-0701-851		OK
J5	RF Jack, 10 GHz	Johnson	SMA	142-0701-851		OK
Control Board	FT232H USB-C to GPIO, SPI and I2C Controller	Adafruit				
Evaluation Board	QFN24-40-21-A					

Note: Standard evaluation board bias: V_{CC} = 5.0 V



4 x 4 mm QFN-24 Suggested PCB Footprint (Top View)



4 x 4 mm QFN-24 Package Dimensions

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Package Marking Diagram

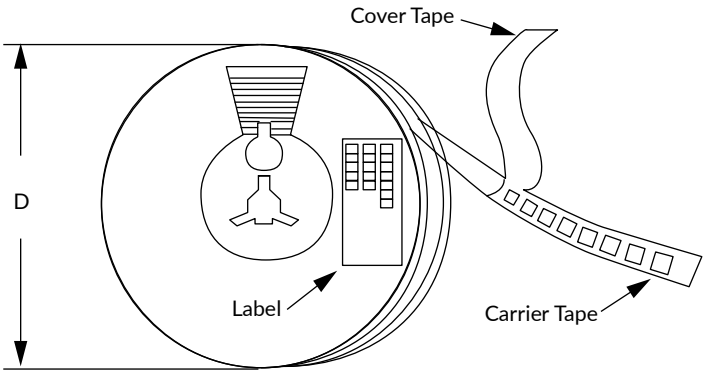
Line 1 *"XXXX"* = *PART NUMBER*

Line 2 *"YY"* = *YEAR and "WW"* = *WEEK* that the part was assembled.

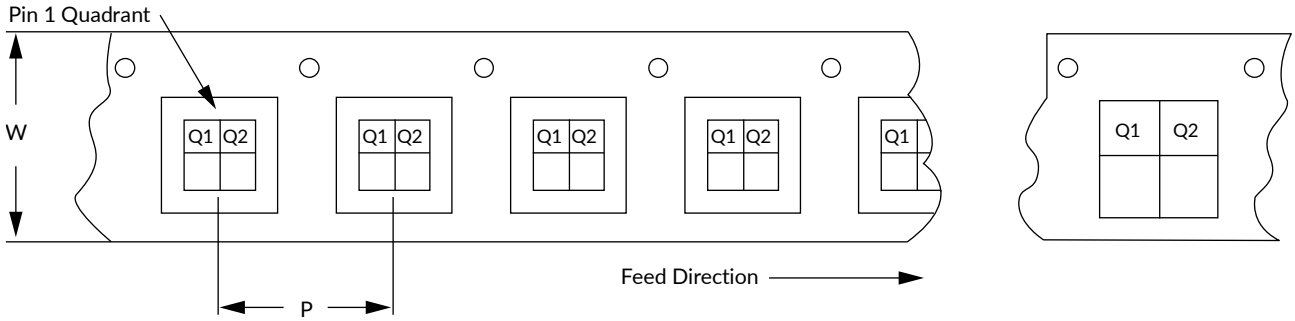
Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

Tape and Reel Specification and Device Package Information

Package			Carrier Tape			Reel	
Type	Dimensions (mm)	Leads	Width (W) (mm)	Pocket Pitch (P) (mm)	Pin 1 Quadrant	Diameter (D) (Inches)	Units per Reel
QFN	2.0 x 2.0 x 0.50	12	8	4	Q1	7	2500
QFN	3.0 x 3.0 x 0.85	16	12	8	Q1	7	1500
QFN	4.0 x 4.0 x 0.85	24	12	8	Q1	7	1500
DFN	1.5 x 1.5 x 0.45	6	8	4	Q1	7	2500
DFN	2.0 x 2.0 x 0.75	8	8	4	Q1	7	2500
LFM	3.5 x 3.5 x 0.85	See Note	12	8	Q1	7	1500
LFM	4.0 x 4.0 x 0.75	See Note	12	8	Q2	7	1500

Note: Lead count may vary. Reference applicable product data sheet.

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Revision History

Revision Date	Description of Change
November 7, 2022	Preliminary Datasheet – Initial Draft. All TYP values updated to correspond with data taken from bench measurements. Updated the SPI programming sequence to reflect the fact that LSBs are clocked in first / MSBs last. Added typical operating curves.

Datasheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on evaluation board measurements taken within the Guerrilla RF Applications Lab. Any MIN/MAX limits represented within the datasheet are based solely on *estimated* part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.