DATA SHEET

# GRF2176

## LNA with Selectable Gain 2.3 to 6 GHz

PRELIMINARY DATA SHEET

### FEATURES

- Two Selectable Gain Modes: 32.4 & 15.8 dB
- Excellent Linearity Performance Over Wide Bandwidths
- 2.7 to 6 V Supply Voltage
- Flexible Biasing Provides Latitude for Linearity Optimization
- 66 mA Native Mode Quiescent Current Consumption
- 50 Ω Single-Ended Input and Output Impedances
- RoHS Compliant

**Reference: High Gain Mode 5 V / 66 mA / 3.75 GHz**

- Gain: 32.4 dB
- OP1dB: 20.9 dB
- OIP3: 32 dBm
- Evaluation Board NF: 0.68 dB

**Reference: Low Gain Mode 5 V / 28 mA / 3.75 GHz**

- Gain: 15.8 dB
- OP1dB: 13.9 dBm
- OIP3: 24.9 dBm
- Evaluation Board NF: 0.65 dB

### APPLICATIONS

- 5G Sub-6 GHz Massive MIMO Base Stations
- TDD Small Cells and Cellular Repeaters
- High-Performance RF Infrastructure

### ORDERING INFORMATION

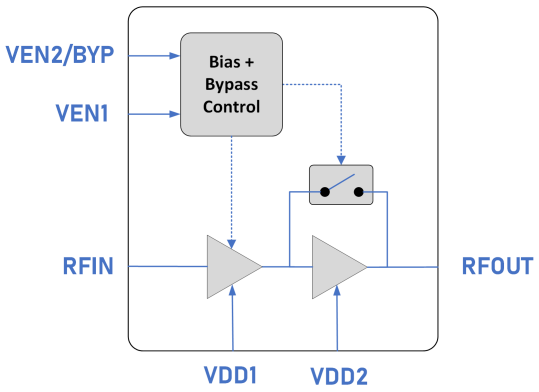
Buy it Now

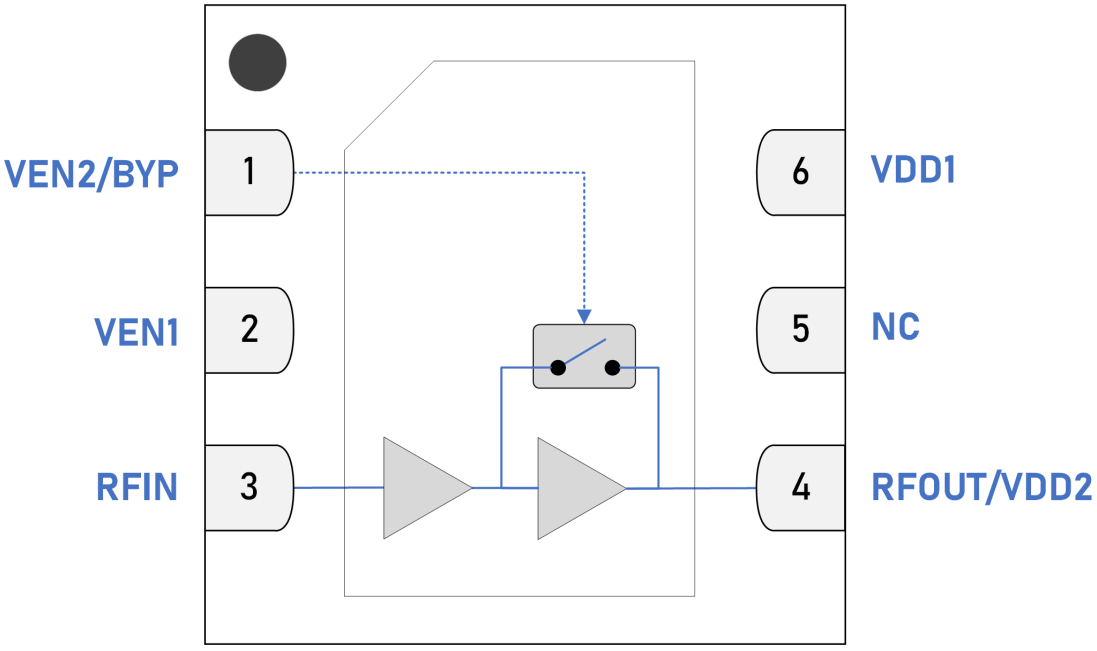
### DESCRIPTION

The GRF2176 is a two-stage GaAs pHEMT low noise amplifier targeting high-performance wireless infrastructure applications. The second stage can be bypassed with an independent control pin, thus allowing the device to support high and low gain modes of 32.4 and 15.8 dB, respectively.

For optimal efficiency and linearity, the amplifier was designed to operate with a single 5 V supply voltage while using only 66 mA of quiescent current. Supply voltages ranging from 2.7 to 6 V are also supported. Similarly, $I_{DDQ}$ can be increased beyond the native biasing point for enhanced linearity performance.

### BLOCK DIAGRAM






**Pin Out (Top View)**

## Pin Assignments

| Pin | Name | Description | Note |
|---|---|---|---|
| 1 | VEN2/BYP | 2nd Stage Enable/Bypass | VEN2/BYP ≤ 0.2 volts sets Bypass Mode. VEN2/BYP and external series resistor controls the second stage $I_{DDQ}$ when VEN2/BYP is high. |
| 2 | VEN1 | 1st Stage Enable | VEN1 ≤ 0.2 disables the first stage. VEN1 and external series resistor control the first stage $I_{DDQ}$ when VEN1 is high. |
| 3 | RFIN | RF Input | Internally matched 50 Ω. An external DC blocking cap must be used. |
| 4 | RFOUT/VDD2 | RF Output/2nd Stage Bias | Internally matched 50 Ω. $V_{DD}$ must be applied through a choke to this pin. |
| 5 | NC | No Connect | No internal connection. This pin can be left unconnected, or be connected to the ground (recommended). Use a via as close to the pin as possible if grounded. |
| 6 | VDD1 | 1st Stage Bias | Pull up to $V_{DD}$ through the inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the first stage of the device with a DC voltage, there is also an RF signal present. |
| PKG BASE | GND | Ground | Provides DC and RF ground for amplifiers, as well as thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page. |

## Absolute Ratings

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 0 | 6 | V |
| RF Input Power - RX Mode: 50 Ω, $V_{DD}$ < 6.0 V average power rating, LTE 20 MHz waveform with 8 dB PAR, 100% DC, 115 °C | $P_{IN\ MAX}$ | | TBD | dBm |
| Operating Temperature (Package Heat Sink) | $T_{PKG\ BASE}$ | -40 | 115 | °C |
| Maximum Channel Temperature (MTTF > $10^6$ Hours) | $T_{MAX}$ | | 170 | °C |
| Maximum Dissipated Power | $P_{DISS\ MAX}$ | | TBD | W |
| **Electrostatic Discharge** | | | | |
| Charged Device Model | CDM | TBD | | kV |
| Human Body Model | HBM | TBD | | V |
| **Storage** | | | | |
| Storage Temperature | $T_{STG}$ | -65 | 150 | °C |
| Moisture Sensitivity Level | | | 1 | -- |

**Caution! ESD Sensitive Device.**

**Exceeding Absolute Maximum Rating conditions may cause permanent damage.**

Note: For additional information, please refer to Manufacturing Note MN-001 - Packaging and Manufacturing Information.

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the Certificate of RoHS Compliance.

## Recommended Operating Conditions

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | $V_{CC}$ | 4.75 | 5 | 5.25 | V | |
| Operating Temperature Range | $T_{PKG\ BASE}$ | -40 | | +115 | °C | |
| RF Frequency Range **(note 1)** | $F_{RF}$ | 2.3 | | 2.7 | GHz | 2.5 GHz tuning set. |
| | | 3.3 | | 4.2 | | 3.75 GHz tuning set. |
| | | 4.4 | | 5.0 | | 4.7 GHz tuning set. |
| RF_IN Port Impedance | $Z_{RFIN}$ | | 50 | | Ω | Single ended, with respective matching elements from each tuning set. |
| RF_OUT Port Impedance | $Z_{RFOUT}$ | | 50 | | Ω | Single ended, with respective matching elements from each turning set. |

**Note1:** Operation outside of this range is possible but with the degraded performance of some parameters.

## Nominal Operating Parameters - General

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Logic Input Low | $V_{IL}$ | 0 | | 0.2 | V | VEN1 and VEN2/BYP inputs. |
| Logic Input High | $V_{IH}$ | 1.5 | | $V_{DD}$ | V | VEN1 and VEN2/BYP inputs. |
| Logic Current | $I_{IL}$, $I_{IH}$ | | TBD | | µA | VEN1 and VEN2/BYP inputs. |
| VEN1 Switching Rise Time | $t_{VEN1-RISE}$ | | 200 | | ns | Turn ON time (VEN1 Low to High, **note 2**). |
| VEN1 Switching Fall Time | $t_{VEN1-FALL}$ | | 50 | | ns | Turn OFF time (VEN1 High to Low, **note 3**). |
| VEN2/BYP Switching Rise Time | $t_{GAIN-RISE}$ | | 200 | | ns | Low to High gain mode switching (VEN2/BYP Low to High, **note 4**). |
| VEN2/BYP Switching Fall Time | $t_{GAIN-FALL}$ | | 50 | | ns | High to Low gain mode switching (VEN2/BYP High to Low, **note 5**). |

### Disabled Mode

| | | | | | | |
|---|---|---|---|---|---|---|
| Standby Current | $I_{STBY}$ | | TBD | | µA | $V_{DD}$ = 5 V, VEN1 = Low, VEN2/BYP = Low. |

### Thermal Data

| | | | | | | |
|---|---|---|---|---|---|---|
| Thermal Resistance (Infrared Scan) | $\theta_{JC}$ | | TBD | | °C/W | On Standard Evaluation Board |
| Channel Temp @ +115 °C (Reference Package Heat Sink) | $T_{CHAN}$ | | TBD | | °C | $V_{DD}$ = 5 V, $I_{DDQ}$ = 66 mA, $P_{DISS}$ = TBD. No RF applied **(note 6).** |

**Note 2:** Switching Rise Time: 50% of VEN1 to 90% of $P_{OUT}$.

**Note 3:** Switching Fall Time: 50% of VEN1 to 10% of $P_{OUT}$.

**Note 4:** Switching Rise Time: 50% of VEN2/BYP to 90% of $P_{OUT}$.

**Note 5:** Switching Fall Time: 50% of VEN2/BYP to 10% of $P_{OUT}$.

**Note 6:** MTTF > $10^6$ hours for $T_{CHAN}$ < 170 °C.

# Nominal Operating Parameters - RF

## 3.3 to 4.2 GHz, 5 V Supply, High Gain Configuration

The following conditions apply unless noted otherwise: typical application schematic using the 3.3 to 4.2 GHz tuning set, VEN1 = 3 V, VEN2/BYP = 3 V (high gain mode), $R_{BIAS1}$ = 2 kΩ, $R_{BIAS2}$ = 2 kΩ (low bias mode), 50 Ω system impedance, $V_{DD}$ = 5 V, $P_{OUT}$ = 0 dBm, $F_{TEST}$ = 3.75 GHz, $T_{PKG\ BASE}$ = 25 °C. MIN/MAX values in *italics* are guaranteed by test; all other parameters are guaranteed by design and characterization. Evaluation board losses are included within the specifications.

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Quiescent Current (High Bias Mode) | $I_{DDQ-HIGH}$ | | TBD | | mA | $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Quiescent Current (Low Bias Mode) | $I_{DD-LOW}$ | | 66 | | | $R_{BIAS}$ = 2 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Supply Current with RF applied (High Bias Mode) | $I_{DD-HIGH}$ | | TBD | | mA | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Current with RF applied (Low Bias Mode) | $I_{DD-LOW}$ | | TBD | | | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = 2 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Gain | S21 | | 32.4 | | dB | $F_{RF}$ = 3.75 GHz |
| Gain Flatness | $S21_{FLAT}$ | | 1.9 | | dB | $F_{RF}$ = 3.3 to 4.2 GHz |
| Gain Variation Over Temp | $S21_{TEMP}$ | | 1/-1.25 | | dB | $T_{PKG\ BASE}$ = -40 to 115 °C, Referenced to $T_{PKG\ BASE}$ = 25 °C |
| Standby Mode Gain | $S21_{STBY}$ | | TBD | | dB | VEN1 = VEN2/BYP = 0 V |
| Input Return Loss | S11 | | > 5.5 | | dB | $F_{RF}$ = 3.3 to 4.2 GHz |
| Output Return Loss | S22 | | > 6.2 | | dB | $F_{RF}$ = 3.3 to 4.2 GHz |
| Reverse Isolation | S12 | | > 44 | | dB | $F_{RF}$ = 3.3 to 3.8 GHz |
| De-Embedded Noise Figure | NF | | TBD | | dB | $F_{RF}$ = 3.75 GHz |
| Evaluation Board Noise Figure | | | 0.68 | | | $F_{RF}$ = 3.75 GHz |
| Output 3rd Order Intercept Point | $OIP3_{HI\ BIAS}$ | | TBD | | dBm | $I_{DDQ}$ = TBD, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| | $OIP3_{LO\ BIAS}$ | | 32 | | | $I_{DDQ}$ = 66 mA, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| Output 1 dB Compression Power | $OP1dB_{HI\ BIAS}$ | | TBD | | dB | $I_{DDQ}$ = TBD |
| | $OP1dB_{LO\ BIAS}$ | | 22 | | | $I_{DDQ}$ = 66 mA |

# Nominal Operating Parameters - RF

## 3.3 to 4.2 GHz, 5 V Supply, Low Gain Configuration

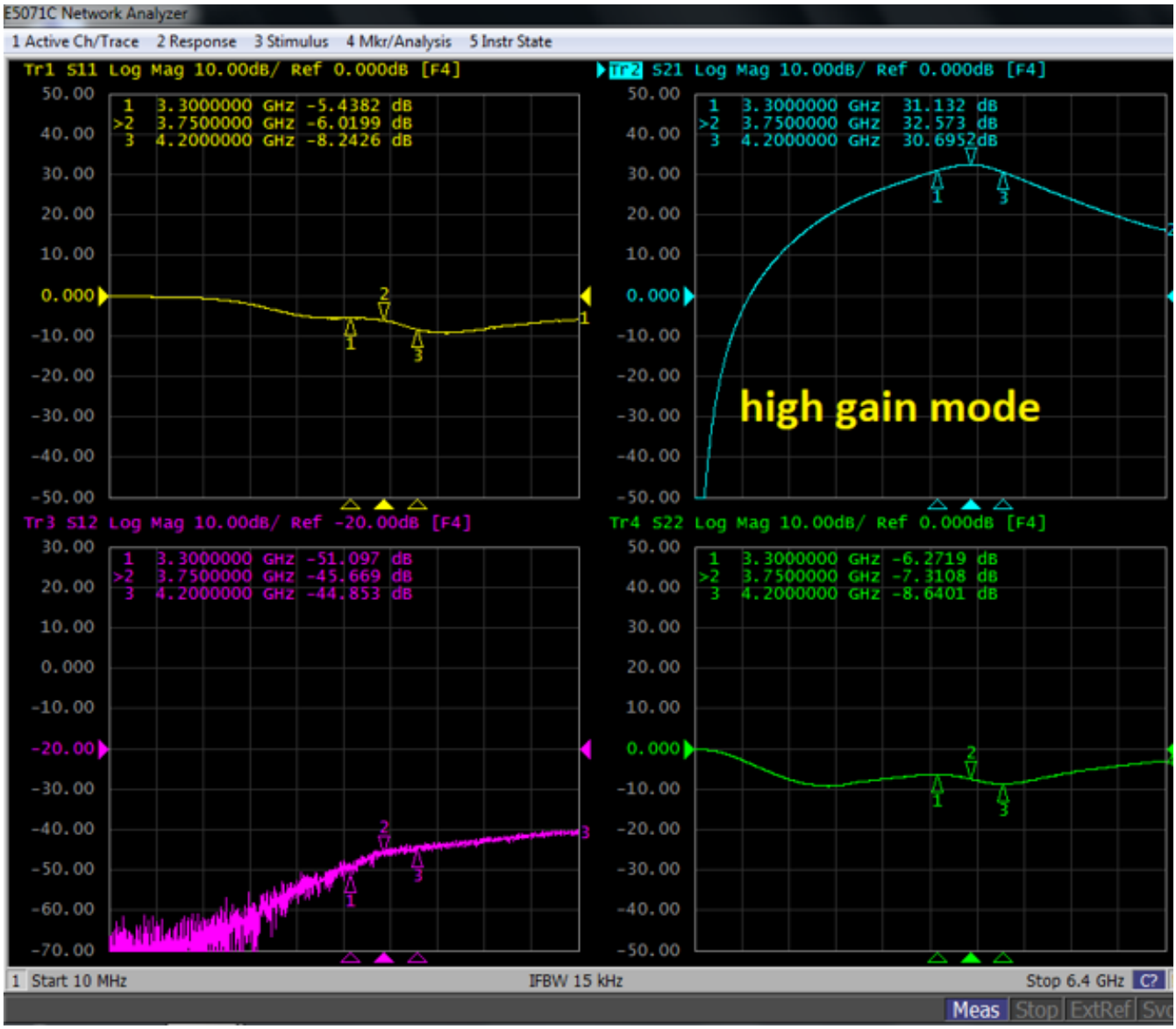
The following conditions apply unless noted otherwise: typical application schematic using the 3.3 to 4.2 GHz tuning set, VEN1 = 3 V, VEN2/BYP = 0 V (low gain mode), $R_{BIAS1}$ = 2 kΩ, $R_{BIAS2}$ = 2 kΩ (low bias mode), 50 Ω system impedance, $V_{DD}$ = 5 V, $P_{OUT}$ = 0 dBm, $F_{TEST}$ = 3.75 GHz, $T_{PKG\ BASE}$ = 25 °C. MIN/MAX values in *italics* are guaranteed by test; all other parameters are guaranteed by design and characterization. Evaluation board losses are included within the specifications.

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Quiescent Current (High Bias Mode) | $I_{DDQ-HIGH}$ | | TBD | | mA | $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Quiescent Current (Low Bias Mode) | $I_{DD-LOW}$ | | 28 | | | $R_{BIAS}$ = 2 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Supply Current with RF applied (High Bias Mode) | $I_{DD-HIGH}$ | | TBD | | mA | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Current with RF applied (Low Bias Mode) | $I_{DD-LOW}$ | | TBD | | | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = 2 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Gain | S21 | | 15.8 | | dB | $F_{RF}$ = 3.75 GHz |
| Gain Flatness | $S21_{FLAT}$ | | 1.4 | | dB | $F_{RF}$ = 3.3 to 4.2 GHz |
| Gain Variation Over Temp | $S21_{TEMP}$ | | 0.6/-1.2 | | dB | $T_{PKG\ BASE}$ = -40 to 115 °C, Referenced to $T_{PKG\ BASE}$ = 25 °C |
| Standby Mode Gain | $S21_{STBY}$ | | TBD | | dB | VEN1 = VEN2/BYP = 0 V |
| Input Return Loss | S11 | | > 6.7 | | dB | $F_{RF}$ = 3.3 to 4.2 GHz |
| Output Return Loss | S22 | | > 6.8 | | dB | $F_{RF}$ = 3.3 to 4.2 GHz |
| Reverse Isolation | S12 | | > 30 | | dB | $F_{RF}$ = 3.3 to 3.8 GHz |
| De-Embedded Noise Figure | NF | | TBD | | dB | $F_{RF}$ = 3.75 GHz |
| Evaluation Board Noise Figure | | | 0.65 | | | $F_{RF}$ = 3.75 GHz |
| Output 3rd Order Intercept Point | $OIP3_{HI\ BIAS}$ | | TBD | | dBm | $I_{DDQ}$ = TBD, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| | $OIP3_{LO\ BIAS}$ | | 24.9 | | | $I_{DDQ}$ = 66 mA, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| Output 1 dB Compression Power | $OP1dB_{HI\ BIAS}$ | | TBD | | dB | $I_{DDQ}$ = TBD |
| | $OP1dB_{LO\ BIAS}$ | | 13.9 | | | $I_{DDQ}$ = 66 mA |

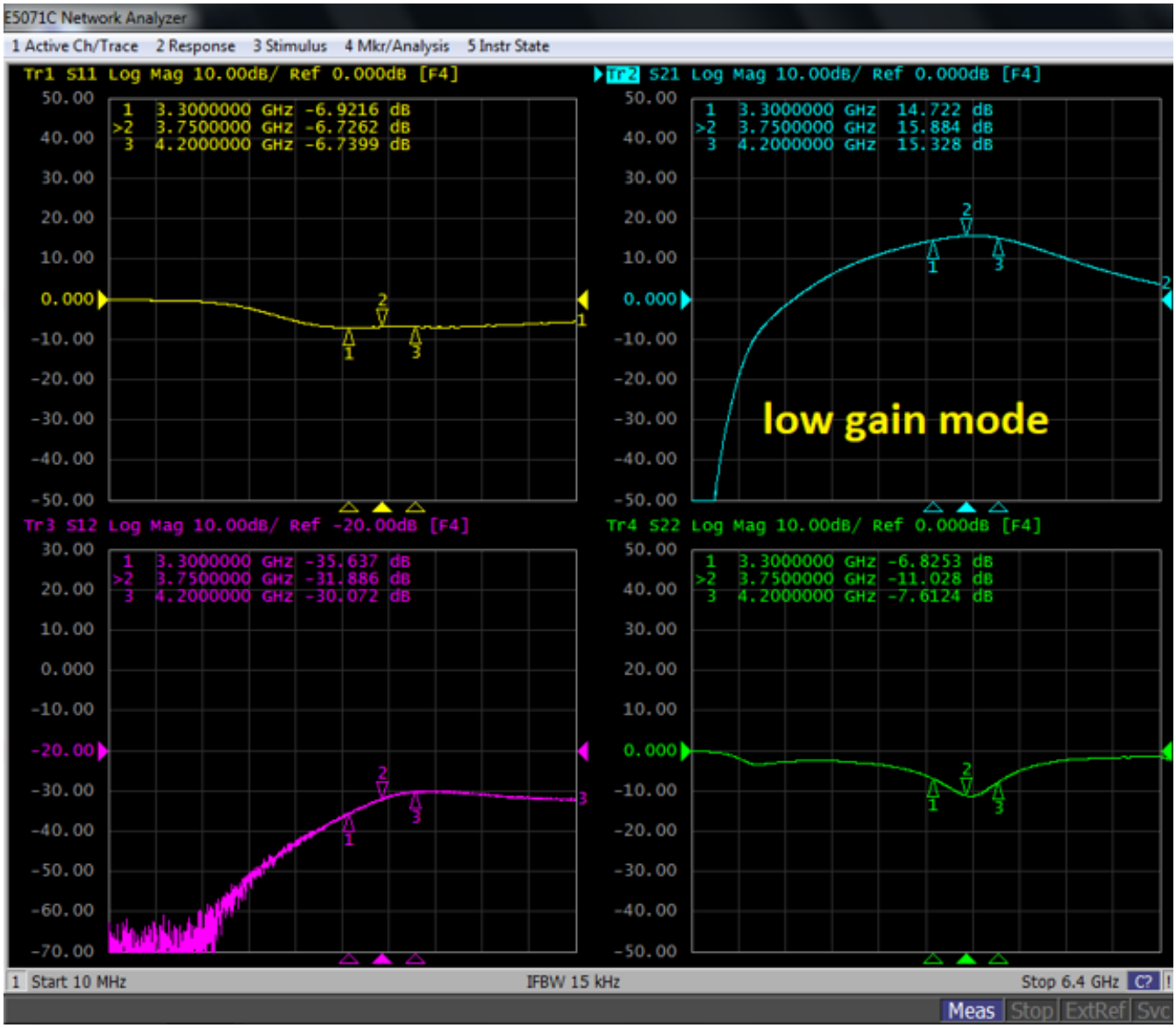
## TRUTH TABLE

| Mode | Pin Logic | |
|---|---|---|
| | VEN1 | VEN2/BYP |
| High Gain | HIGH | HIGH |
| Low Gain (2nd Stage Bypass) | HIGH | LOW |
| Standby | LOW | LOW |

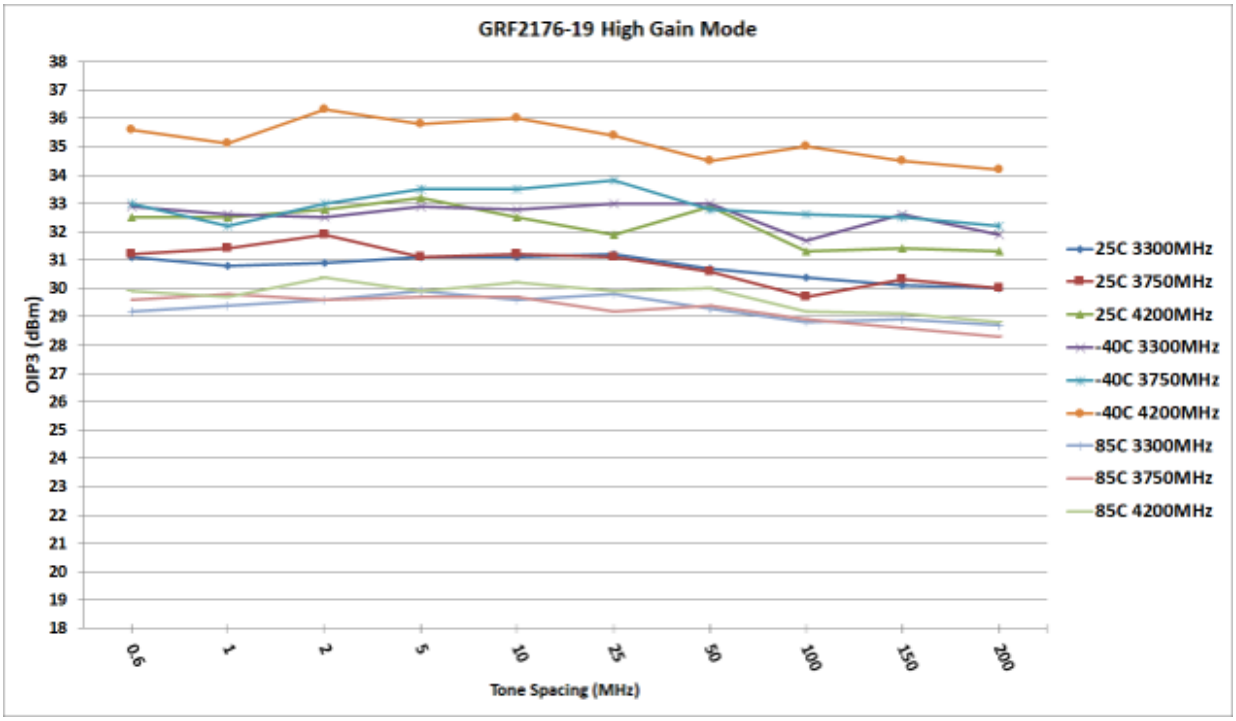
## S-Parameters - HIGH GAIN MODE



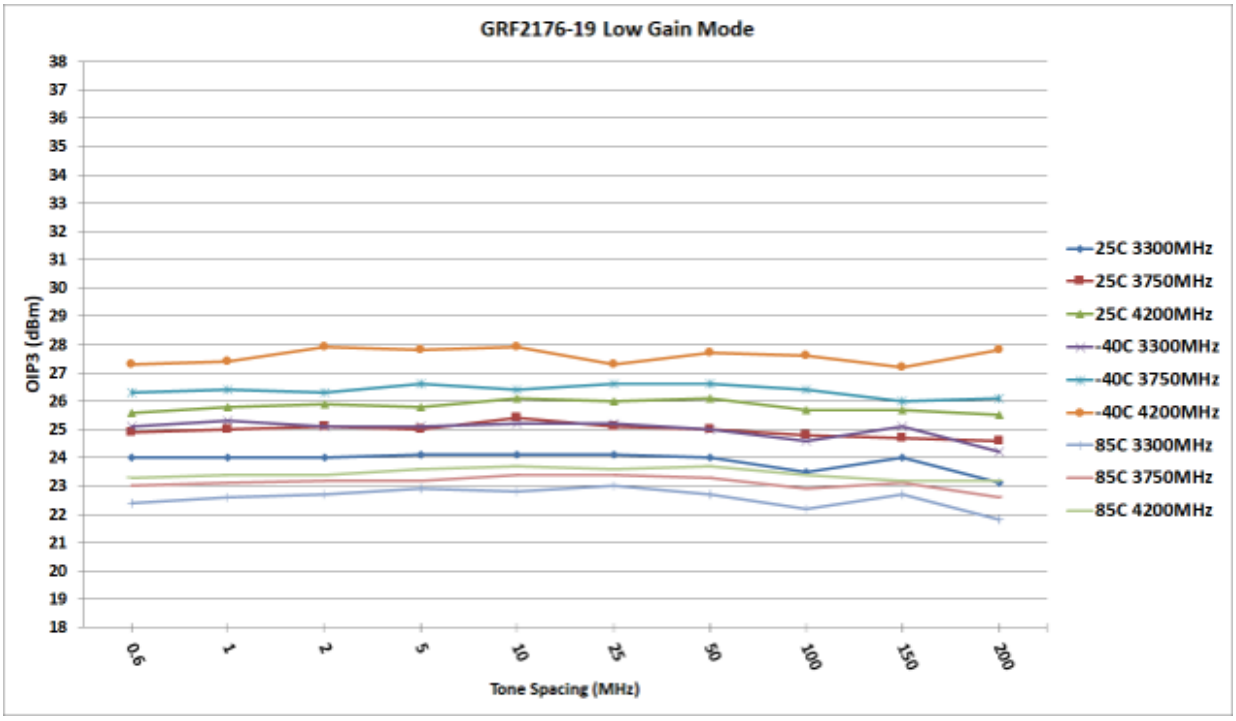
## S-Parameters - LOW GAIN MODE

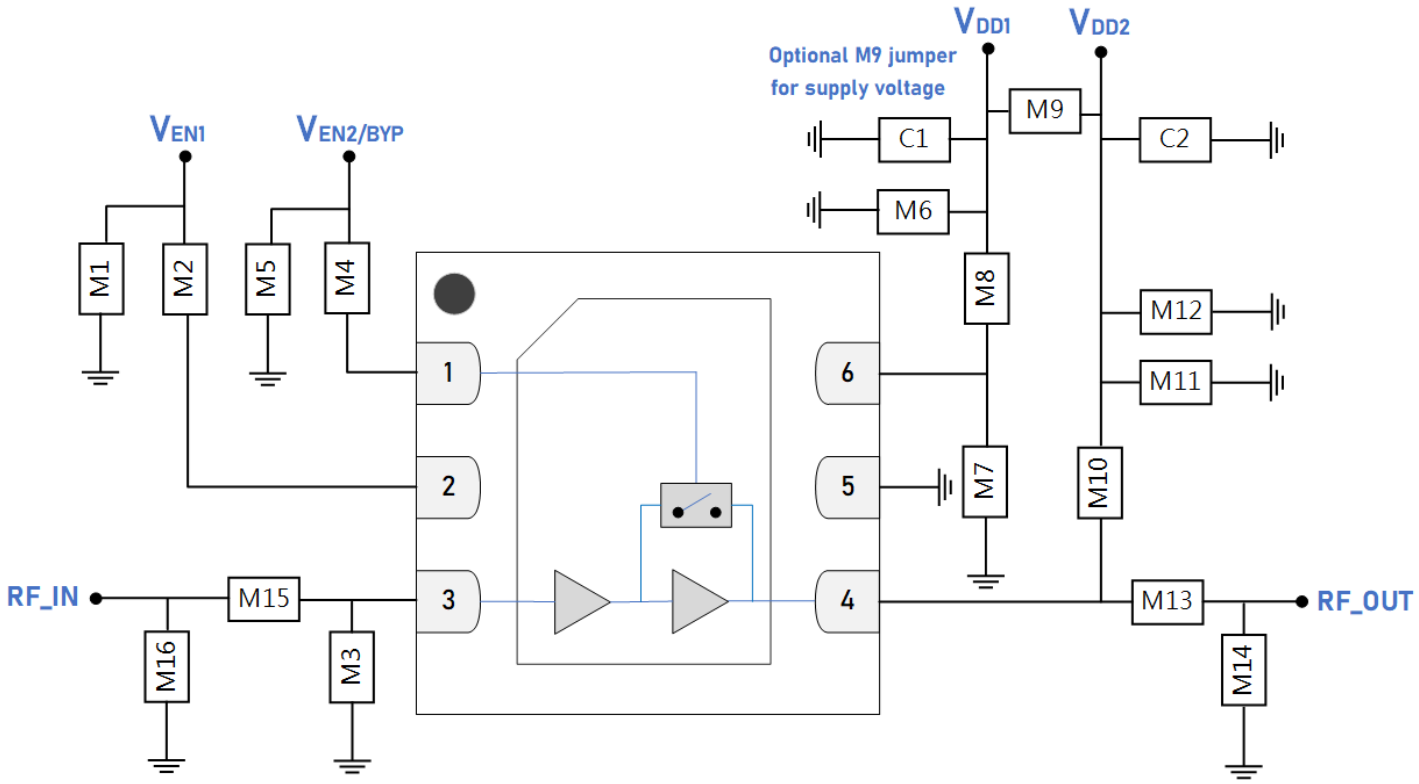


## OIP3 - HIGH GAIN MODE

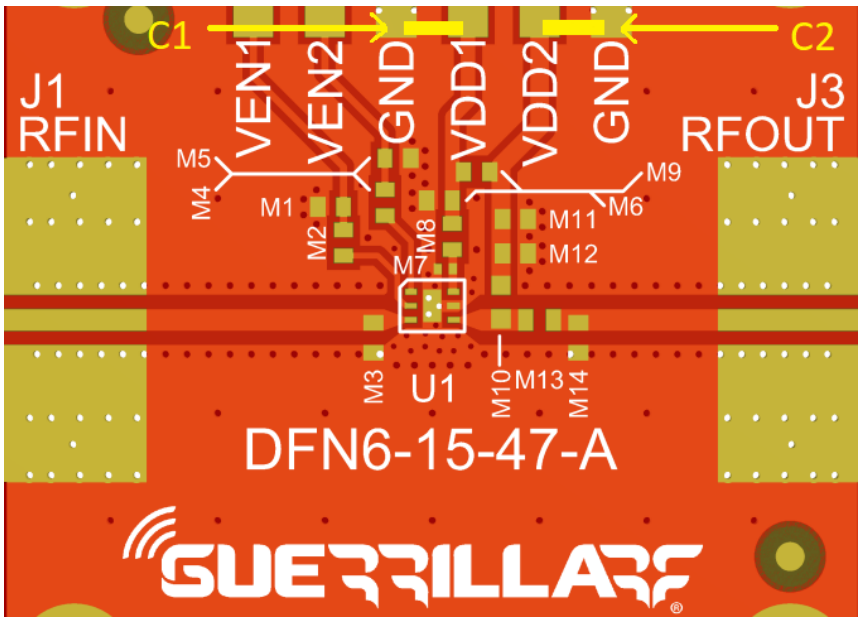



## OIP3 - LOW GAIN MODE






**GRF2176 Standard Test Schematic**

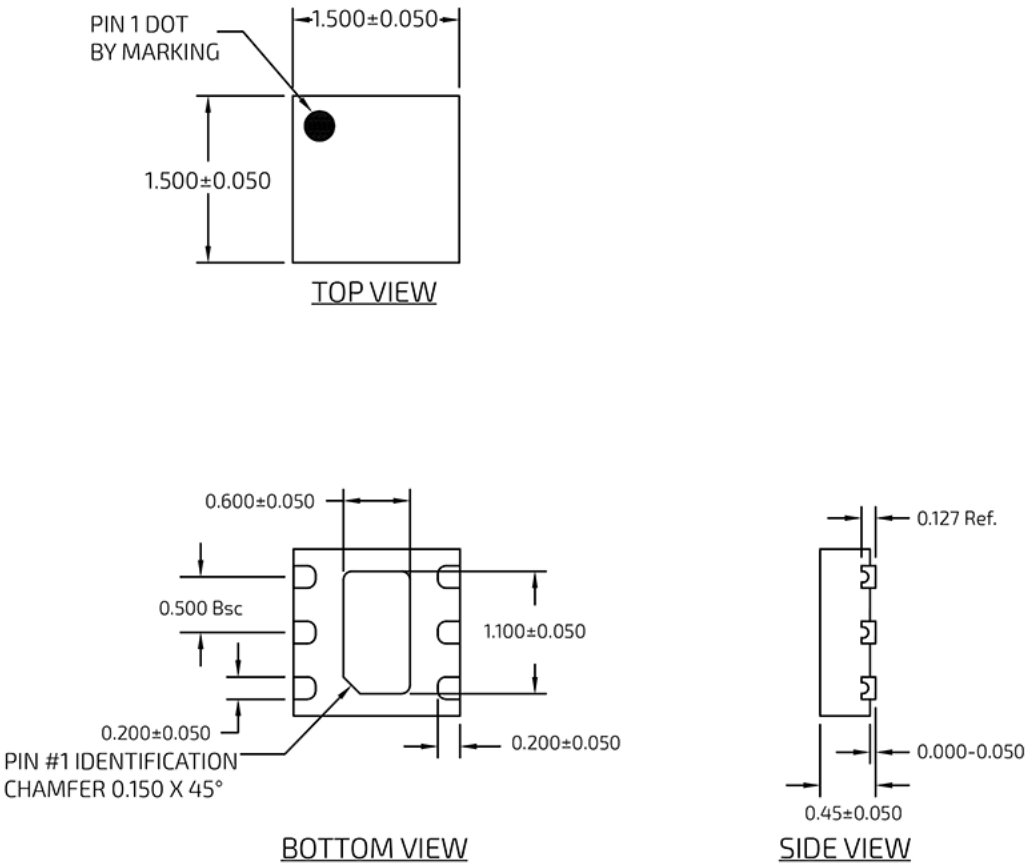



**GRF2176 Evaluation Board Assembly Drawing**

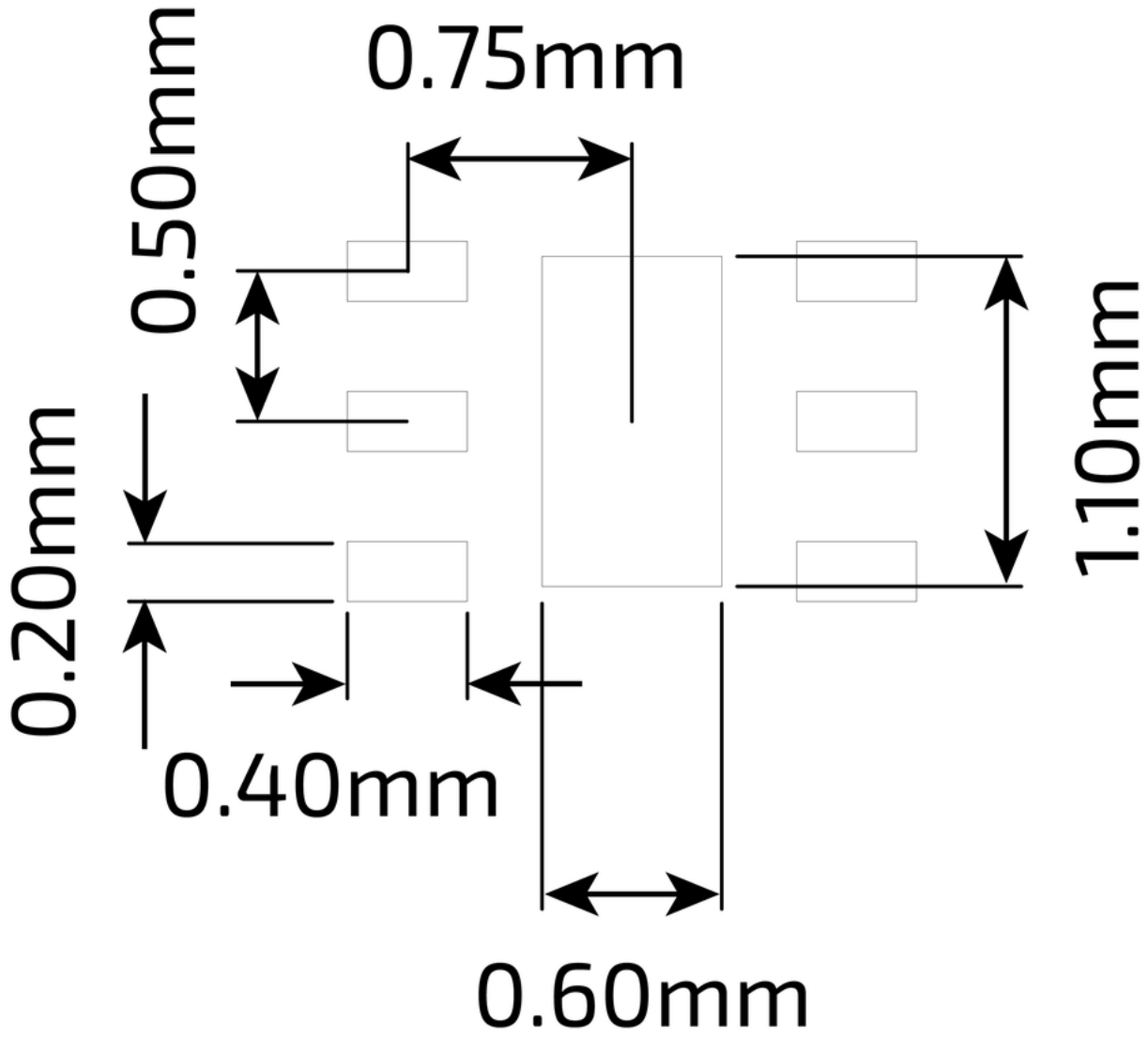
## GRF2176 Evaluation Board Assembly Diagram Reference

| Component | Type | Manufacturer | Family | Value | Package Size | Substitution |
|---|---|---|---|---|---|---|
| C1 | Capacitor | Murata | GJM | 100 pF | 0402 | Ok |
| C2 | Capacitor | Murata | GJM | 100 pF | 0402 | Ok |
| M1, M3, M5, M6 M11, M14 | DNP | -- | -- | -- | -- | -- |
| M2 | Resistor | Various | 5% | 2 kΩ | 0402 | Ok |
| M4 | Resistor | Various | 5% | 2 kΩ | 0402 | Ok |
| M7 | Capacitor | Murata | GJM | 0.1 µF | 0402 | Ok |
| M8 | Inductor | Murata | LQG | 15 nH | 0402 | Ok |
| M9 | Resistor | Various | 5% | 0 Ω | 0402 | Ok |
| M10 | Inductor | Murata | LQG | 6.8 nH | 0402 | Ok |
| M12 | Capacitor | Murata | GJM | 0.1 µF | 0402 | Ok |
| M13 | Capacitor | Murata | GJM | 10 pF | 0402 | Ok |
| M15 | Capacitor | Murata | GJM | 1.8 pF | 0402 | Ok |
| M16 | Inductor | Murata | LQG | 3.3 nH | 0402 | Ok |
| Evaluation Board | DFN6-15-47-A | | | | | |

**Note:** Standard evaluation board bias: $V_{DD}$ = 5 V.




**DFN 6 1.5x1.5mm Package Dimensions**



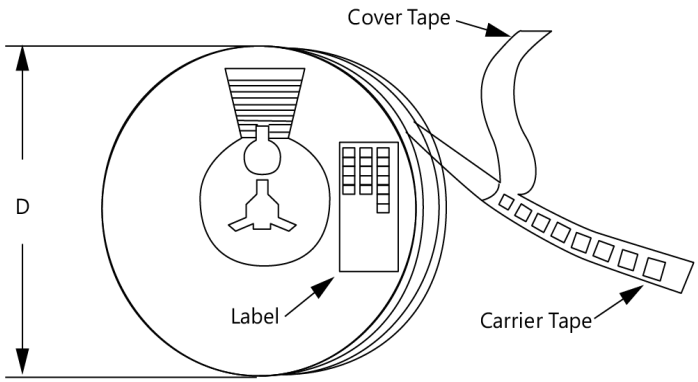

**DFN 6 1.5x1.5mm Suggested PCB Footprint (Top View)**

### Package Marking Diagram

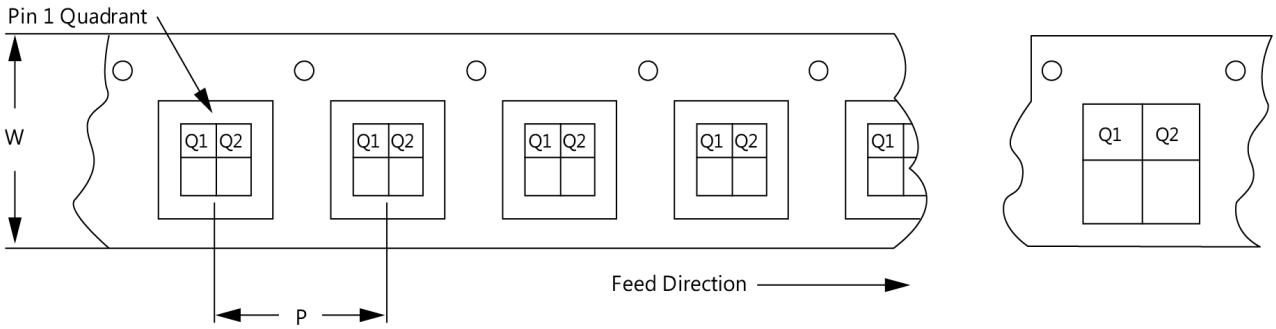

Line 1: "Y" = YEAR (single digit). "WW" = WORK WEEK the Device was assembled.
Line 2: "XXXX" = Device Part Number.

### Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag, and the outside surface of the box. For the latest reel specifications and package information (including units/reel), please visit Package Manufacturing Information | Guerrilla RF (guerrilla-rf.com).




Tape and Reel Packaging with Reel Diameter Noted (D)




Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

## Revision History

| Revision Date | Description of Change |
|---|---|
| November 24, 2020 | Advance data sheet - Initial Release. |
| February 13, 2023 | Preliminary data sheet - Initial Release. |
| July 31, 2023 | Upgraded to new Data Sheet format.<br>Removed M1 and M5 from EVB BOM and added Capacitors C1 and C2. |
| October 6, 2023 | Added "RoHS Compliant" to Features list on Page-1. |

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**Data Sheet Classifications**

| Data Sheet Status | Notes |
|---|---|
| Advance | S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices. |
| Preliminary | All data based on evaluation board measurements taken within the Gurerrilla RF Applications Lab. Any MIN/MAX limits represented within the data sheet are based solely on *estimated* part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data. |
| Release Ø | All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory. |
| Release A-Z | All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads. |






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