

GLDBOX REAL TIME DRIVER EXAMPLE ENABLEMENT GUIDE



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Hardware Requirement and Software Installation

Hardware Requirement

- S32G-VNP-RDB2
- S32 Debug Probe
- AD/DC power supply
- Serial port cable for UART example

Software Installation

- S32DS3.4 according to [S32G-VNP-GLDBOX Software Enablement Guide](#)
- SW32_RTD_4.4_1.0.0(RTD) according to [S32G-VNP-GLDBOX Software Enablement Guide](#)



01.

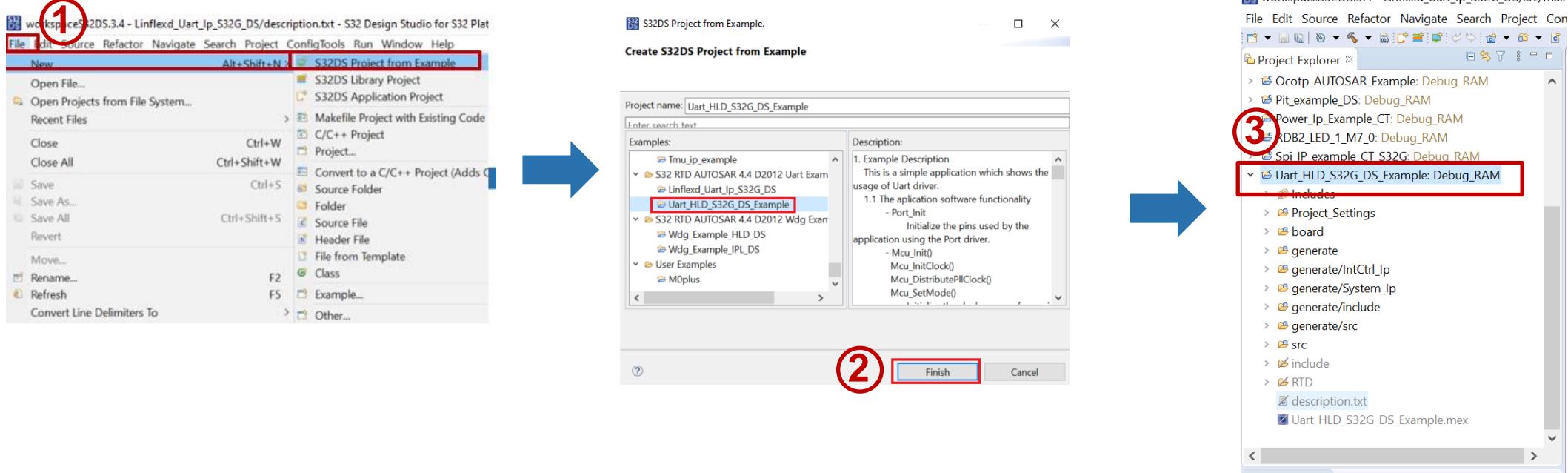
Hands on UART Example

Hands on UART: Objective

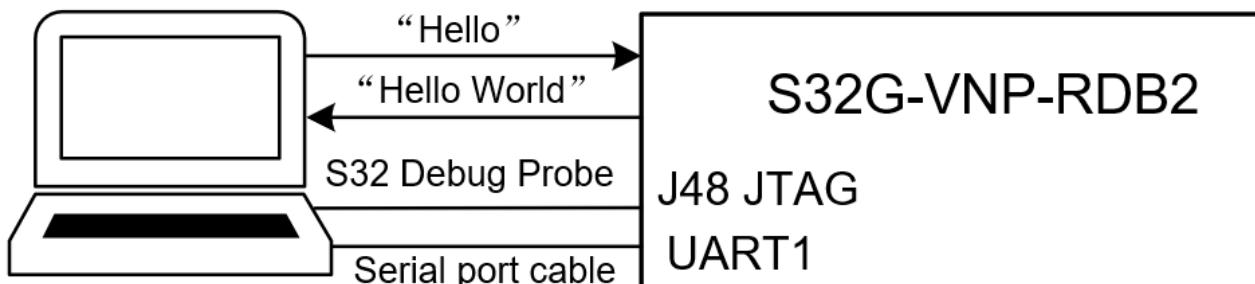
- How to import the UART example into S32DS
- How to configure the clock of UART via S32DS
- How to configure the UART setting via S32DS
- How to debug the UART example with S32 debug probe

Hands on UART: Import UART example project

Open S32DS3.4, go to “File -> New -> S32DS Project From Example”. Select “Uart_HLD_S32G_DS_Example” example, Then click on “Finish”. The project should now be copied into current workspace.



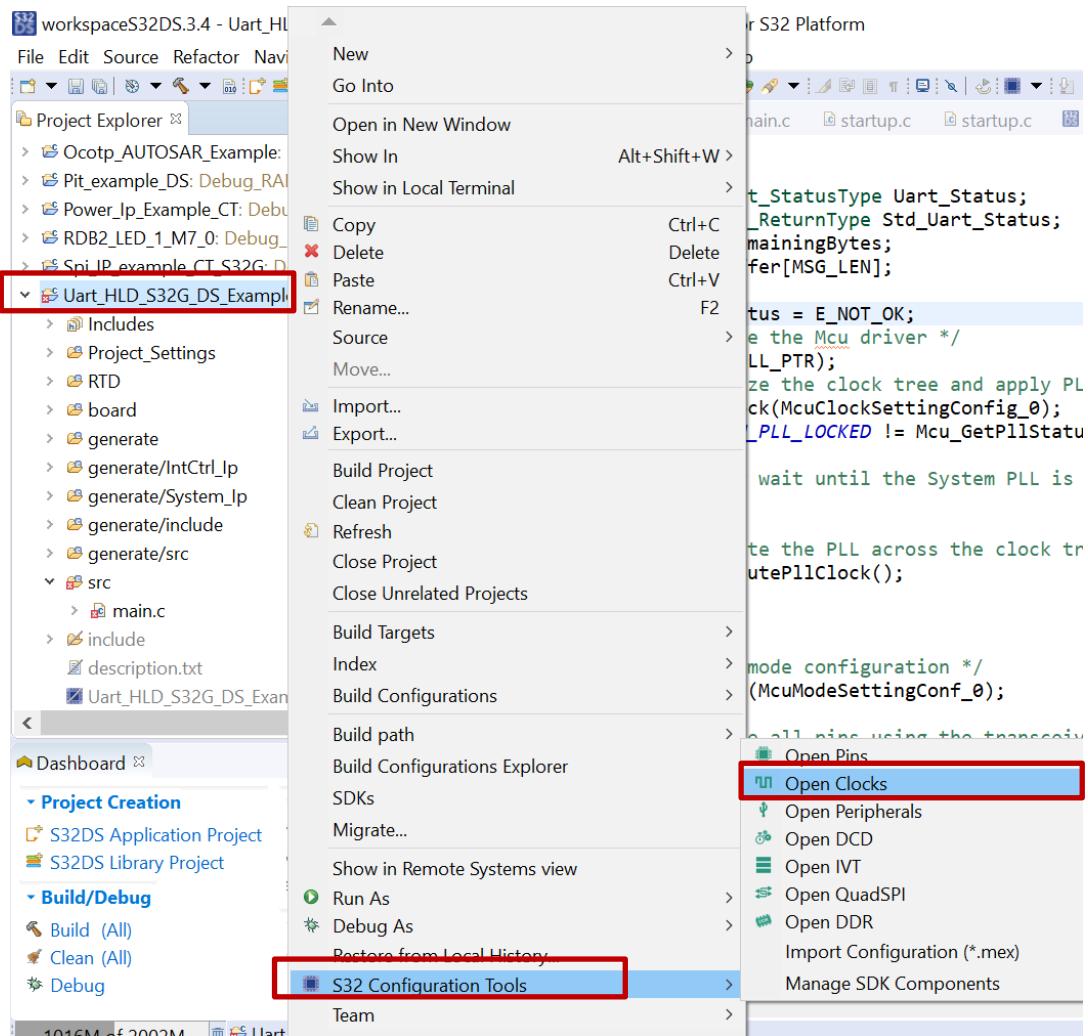
The purpose of “Uart_HLD_S32G_DS_Example” example is a simple application which shows the usage of UART driver.



Hands on UART: Clock Configuration 1

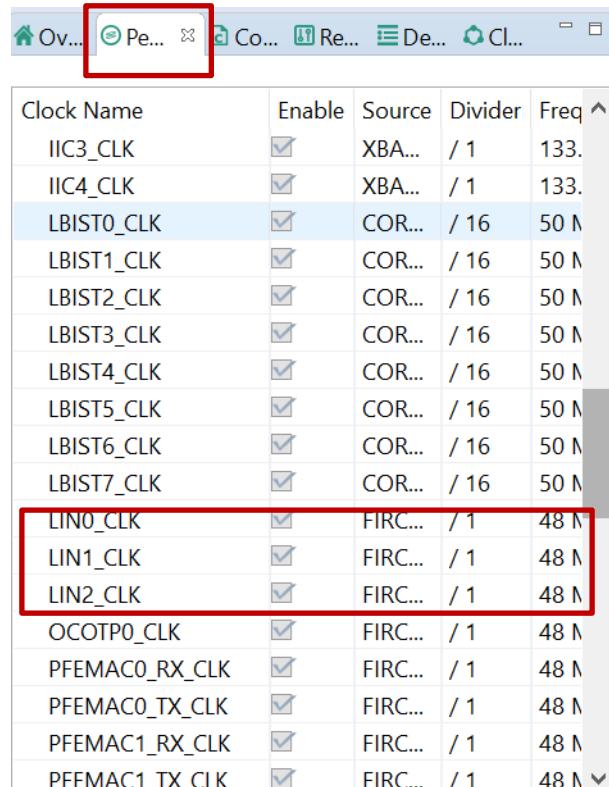
Go to desired configuration tool:

- Right click on Project,
- Select S32 Configuration Tool...
- Select Open Clocks



Hands on UART: Clock Configuration 2

Open the [Peripheral Clock View](#), Double click the Lin module. The [Clocks Diagram](#) will show the power tree .In Uart_HLD_S32G_DS_Example project. The default clock configuration of UART is 48 MHZ which comes from FIRC directly



The screenshot shows a software interface for managing peripheral clocks. At the top, there are tabs for Overview, Peripheral Clock View (which is selected and highlighted with a red box), Configuration, Reference, Details, and Clocks. Below the tabs is a table with columns: Clock Name, Enable, Source, Divider, and Freq. The table lists various clocks, with three specific ones highlighted by a red box: LIN0_CLK, LIN1_CLK, and LIN2_CLK, all of which are derived from FIRC at 48 MHz.

Clock Name	Enable	Source	Divider	Freq
IIC3_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.
IIC4_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.
LBIST0_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST1_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST2_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST3_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST4_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST5_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST6_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LBIST7_CLK	<input checked="" type="checkbox"/>	COR...	/ 16	50 M
LIN0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
LIN1_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
LIN2_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
OCOTP0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
PFEMAC0_RX_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
PFEMAC0_TX_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
PFEMAC1_RX_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
PFEMAC1 TX CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M

Fig. Peripheral Clock View

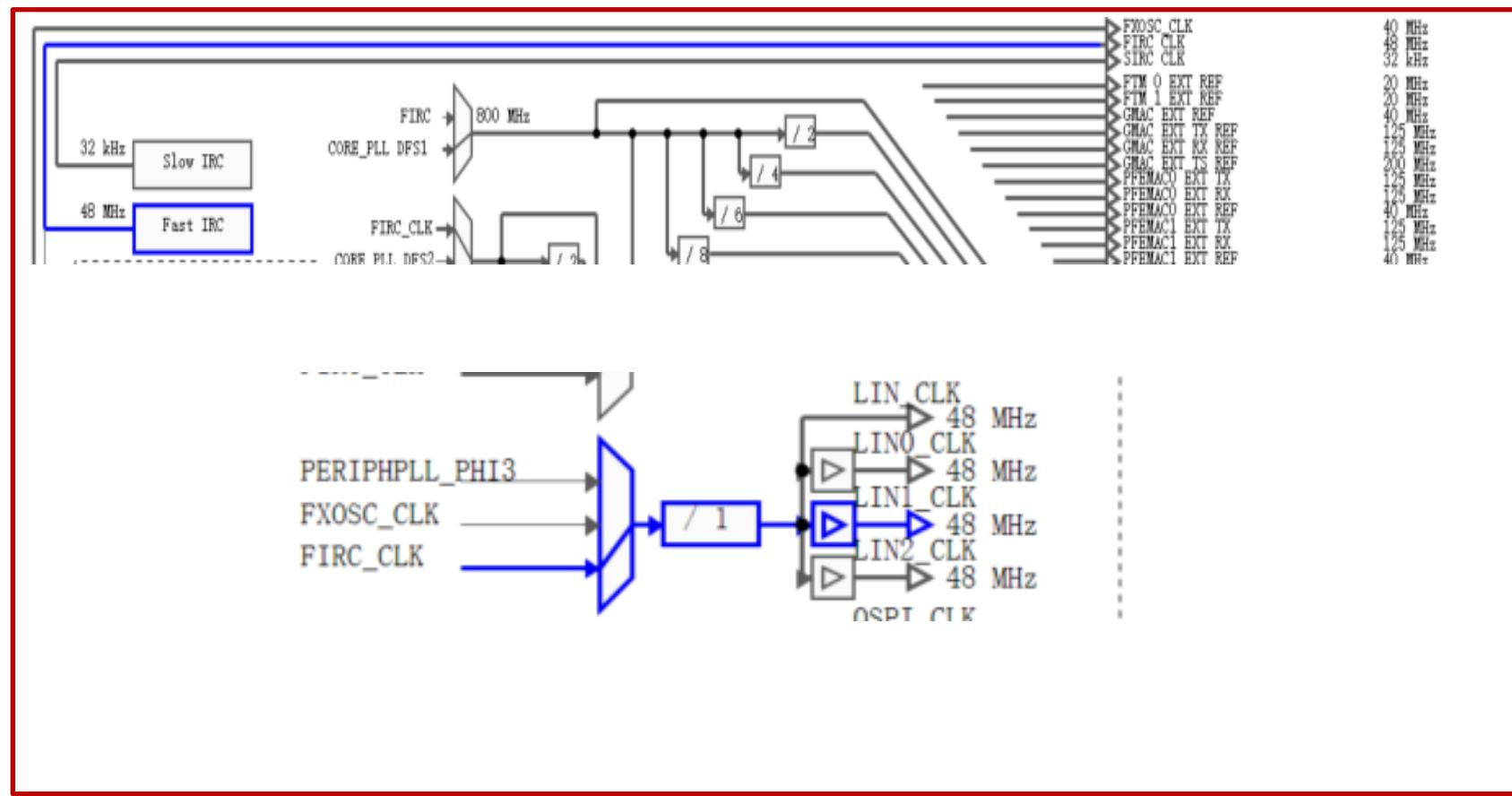
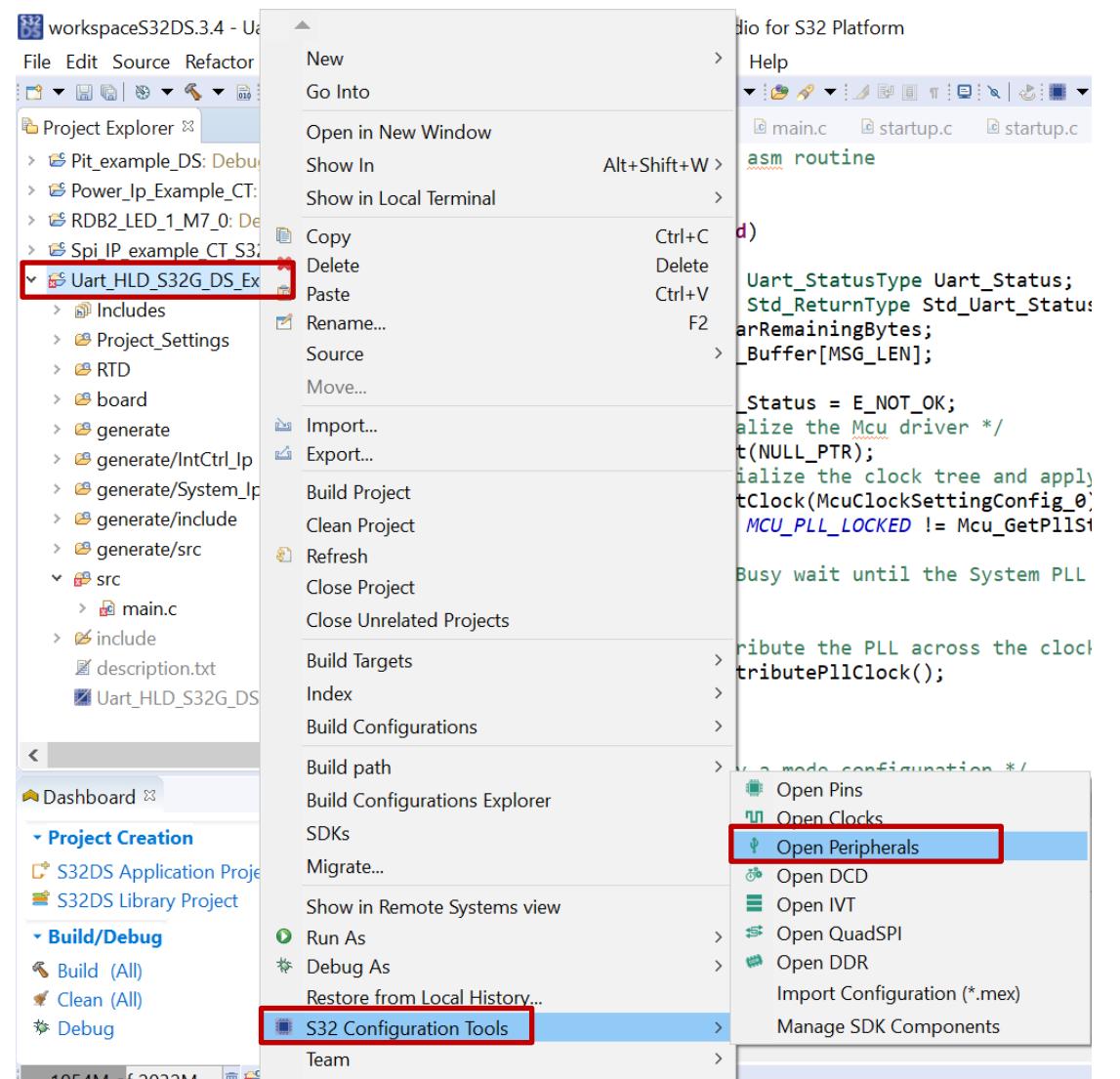


Fig. Clocks Diagram

Hands on UART: UART Configuration 1

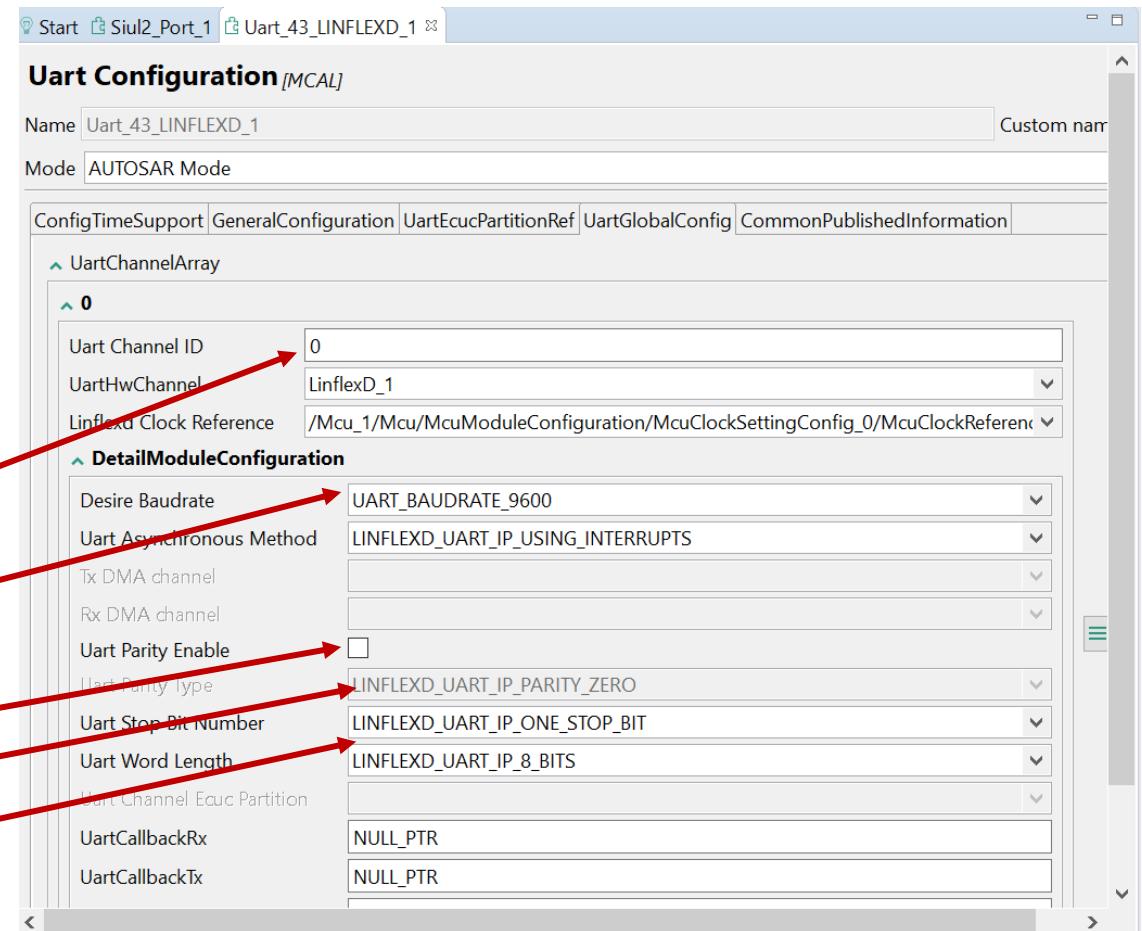
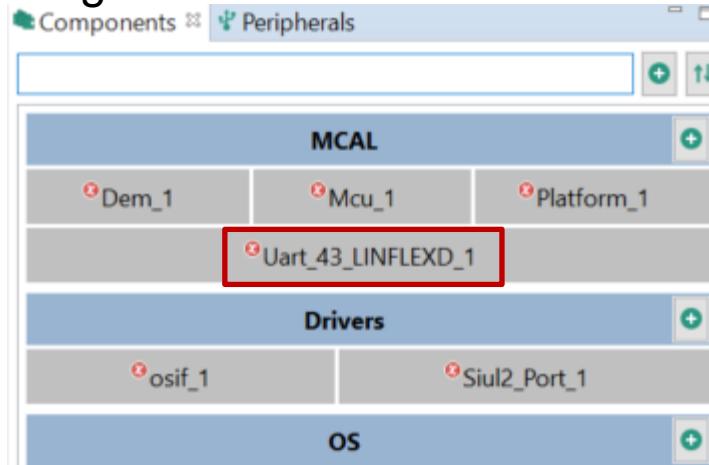
Open the Clocks Diagram:

- Right click on Project,
- Select S32 Configuration Tool...
- Select Peripherals



Hands on UART: UART Configuration 2

The [Components](#) shows all drivers which used by this example, the [UART_43_LINFLEXD_1](#) includes the configuration of UART driver



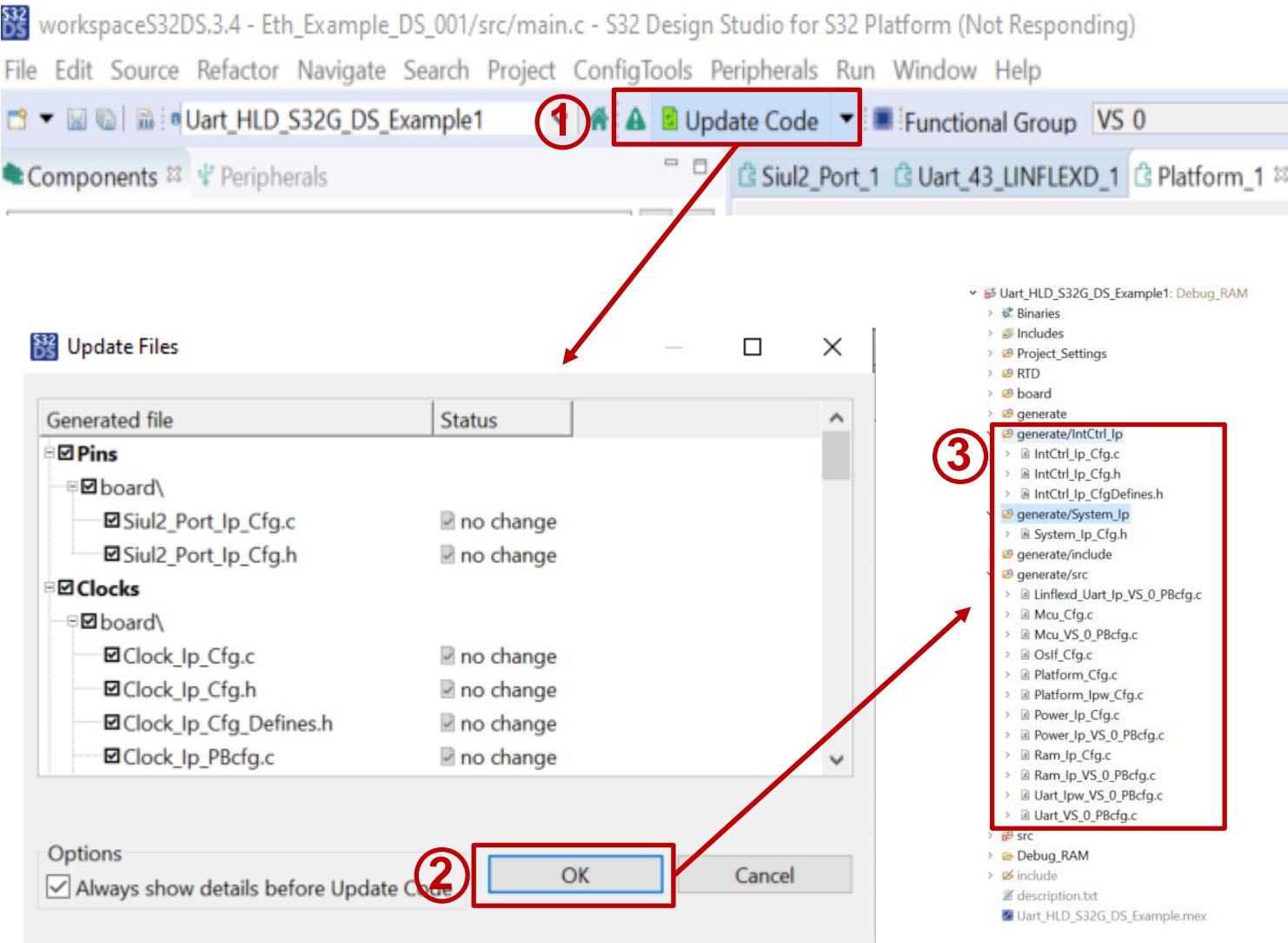
UART default configuration:

- - Select correct COM Port
- - Select Baudrate of 9600
- - Select none parity checking
- - Select 1 stop bits
- - Select 8 data bits

Hands on UART: Update code

Generate code method:

- 1.Click on any configuration tool, like Pins
Then click **Update Code** (ensure desired project is selected!)
- 2.The Update Files window pops up. It shows the detail update information. Click **ok** button.
- 3.The configuration .c and .h file will be generated at “generate” folder.



Hands on UART: Application code 1

Open the main.c file in S32DS

```
int main(void)
{
    volatile Uart_StatusType Uart_Status;
    volatile Std_ReturnType Std_Uart_Status;
    uint32 varRemainingBytes;
    uint8 Rx_Buffer[MSG_LEN];

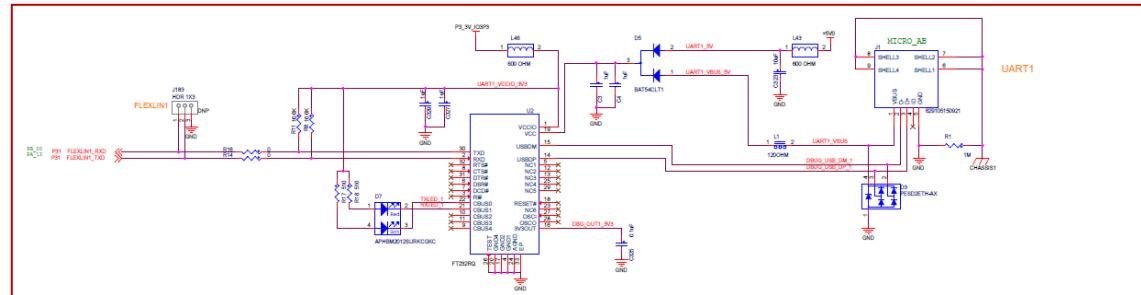
    Std_Uart_Status = E_NOT_OK;
    /* Initialize the Mcu driver */
    Mcu_Init(NULL_PTR);
    /* Initialize the clock tree and apply PLL as system clock */
    Mcu_InitClock(McuClockSettingConfig_0);
    while (MCU_PLL_LOCKED != Mcu_GetPllStatus())
    {
        /* Busy wait until the System PLL is locked */
    }
    /* Distribute the PLL across the clock tree */
    Mcu_DistributePllClock();

    /* Apply a mode configuration */
    Mcu_SetMode(McuModeSettingConf_0);

    /* Initialize all pins using the transceiver */
    Uart_Setup_Pins();

    /* Initialize IRQs */
    Platform_Init(NULL_PTR);
    Platform_InstallIrqHandler(LINFLEXD1_IRQn, LINFLEXD1_UART_IRQHandler, NULL_PTR);
```

MCU clock initiation



```
/* Init Pins */
void Uart_Setup_Pins(void)
{
    /* LINFLEXD1_TX: PA_13 */
    t_reg_write(0x4009C274, 0x00200002);
    /* LINFLEXD1_RX: PB_00 */
    t_reg_write(0x4009C280, 0x00008000);
    t_reg_write(0x44010DC0, 0x02);
}
```

In Uart_HLD_S32G_DS_Example Project.
Initialization of pins is writing register directly.

Hands on UART: Application code 2

```
while (1)
{
    /* Receive and store data byte by byte until new line character is received,
     * or the buffer becomes full
    */
    (void)Uart_AsyncReceive(UART_CHANNEL, Rx_Buffer, strlen(EXPECT_RX_MSG));
    /* Wait for transfer to be completed */
    while(Uart_GetStatus(UART_CHANNEL, &varRemainingBytes, UART_RECEIVE) == UART_OPERATION_ONGOING);

    /* Check the status */
    Uart_Status = Uart_GetStatus(UART_CHANNEL, &varRemainingBytes, UART_RECEIVE);

    if (Uart_Status != UART_NO_ERROR)
    {
        /* If an error occurred, send the error message and exit the loop */
        (void)Uart_AsyncSend(UART_CHANNEL, (const uint8 *)ERROR_MSG, strlen(ERROR_MSG));
        while(Uart_GetStatus(UART_CHANNEL, &varRemainingBytes, UART_SEND) == UART_OPERATION_ONGOING);
        break;
    }

    /* Send the received data back */
    Std_Uart_Status = Uart_AsyncSend(UART_CHANNEL, (const uint8 *)SEND_MSG, strlen(SEND_MSG));
    while(Uart_GetStatus(UART_CHANNEL, &varRemainingBytes, UART_SEND) == UART_OPERATION_ONGOING);
    break;
}
```

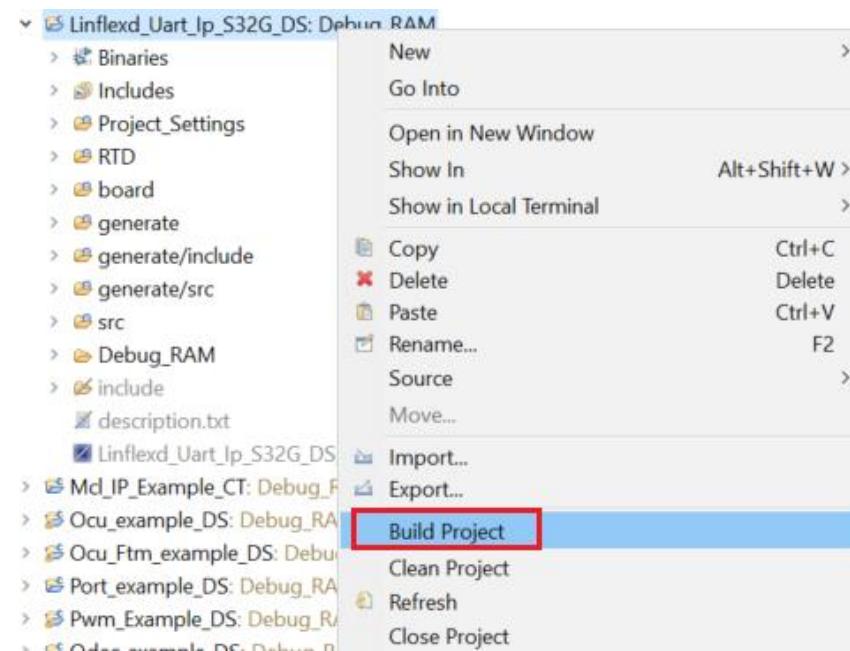
Receive data from user

Echo the received data back

Hands on UART: Build and Debug 1

Build the target :

- Right click on Project,
- Select Build Project
- Print Build information on Console window
- Uart_HLD_S32G_DS_Example1.elf is generated



The screenshot shows the build output window in the NXP Studio IDE. At the top, the project tree shows 'Uart_HLD_S32G_DS_Example: Debug_RAM' expanded, with 'Binaries' selected. Inside 'Binaries', 'Uart_HLD_S32G_DS_Example1.elf - [arm/le]' is highlighted with a red box. Below the tree is a 'Problems' tab bar. The main area displays the build log:

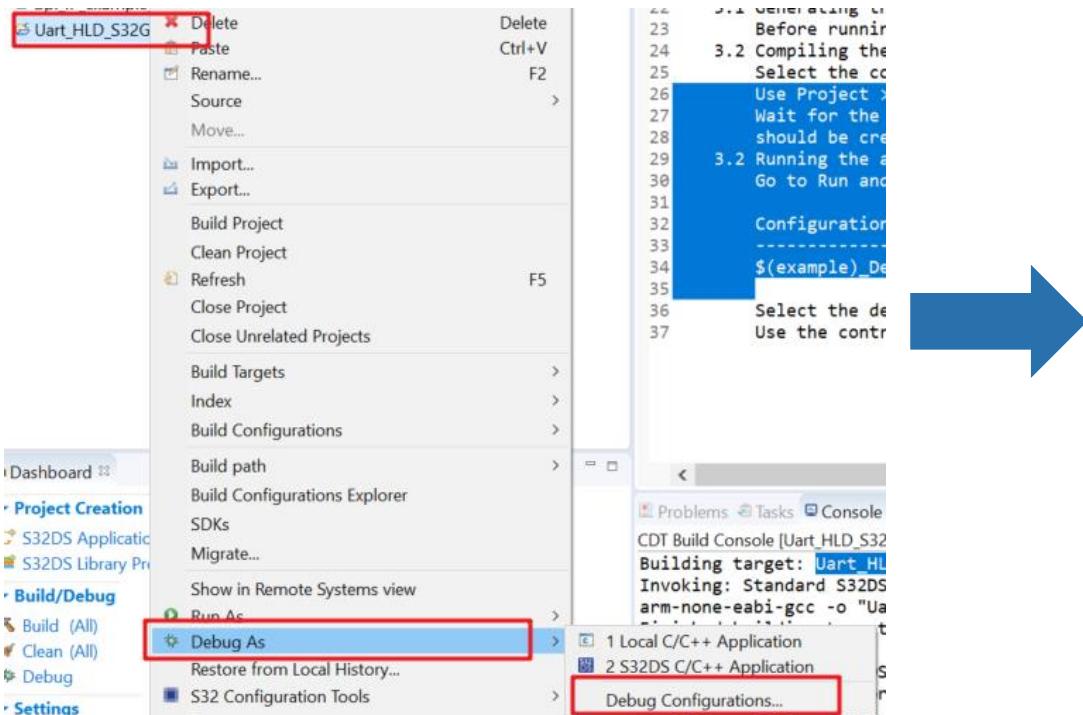
```
CDT Build Console [Uart_HLD_S32G_DS_Example1]
Building target: Uart_HLD_S32G_DS_Example1.elf
Invoking: Standard S32DS C Linker
arm-none-eabi-gcc -o "Uart_HLD_S32G_DS_Example1.elf" "@Uart_HLD_S32G_DS_Example1.args"
Finished building target: Uart_HLD_S32G_DS_Example1.elf
|
Invoking: Standard S32DS Print Size
arm-none-eabi-size --format=berkeley Uart_HLD_S32G_DS_Example1.elf
    text      data      bss      dec      hex filename
  309808        0   12288   322096   4ea30 Uart_HLD_S32G_DS_Example1.elf
Finished building: Uart_HLD_S32G_DS_Example1.siz

10:04:55 Build Finished. 0 errors, 0 warnings. (took 6s.982ms)
```

Hands on UART: Build and Debug 2

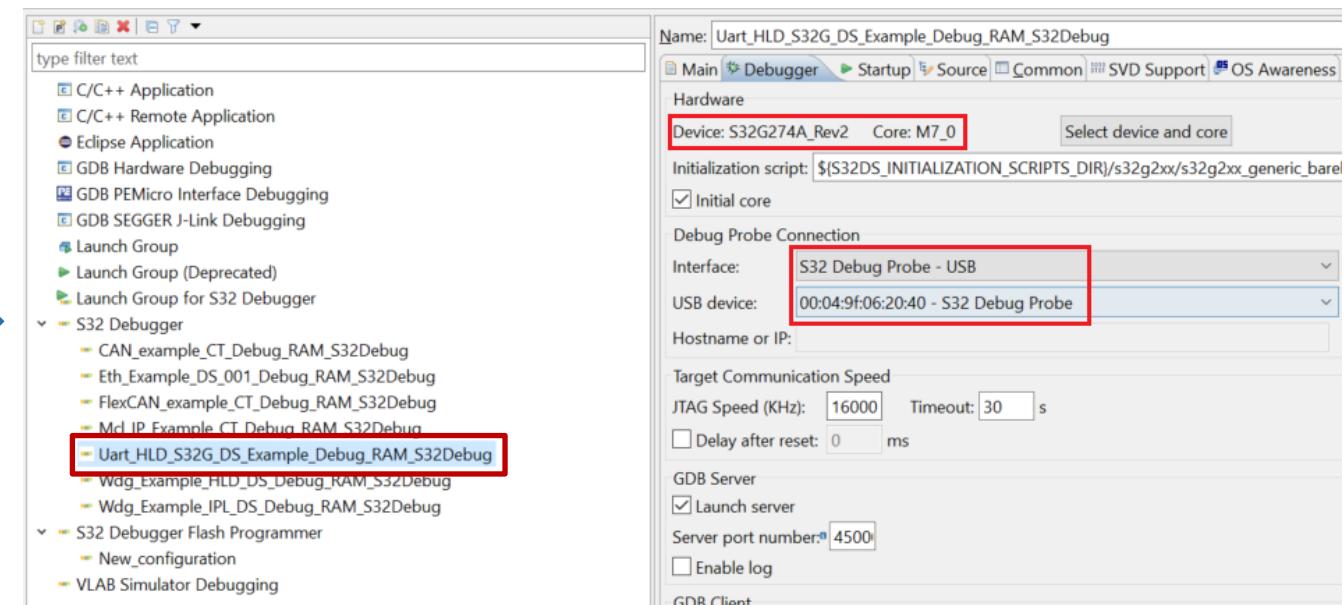
Go to debug configuration:

- Right click on Project,
- Select the Debug As
- Click Configurations



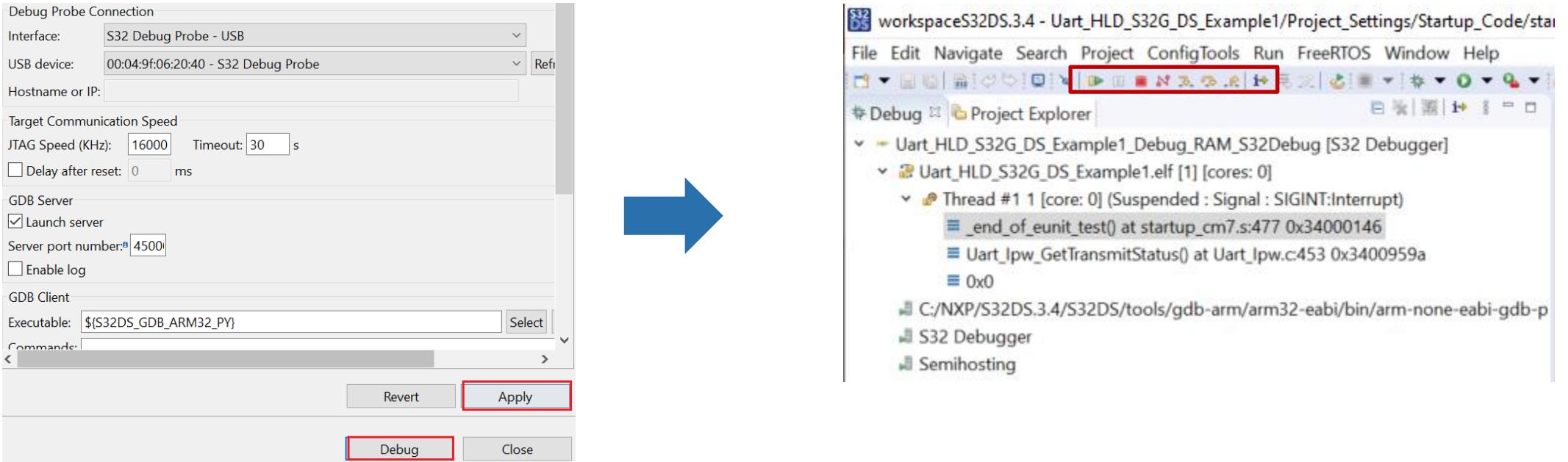
Debug configuration set:

- Click target project ,
- Select the target device
- Select target S32 Debug Probe



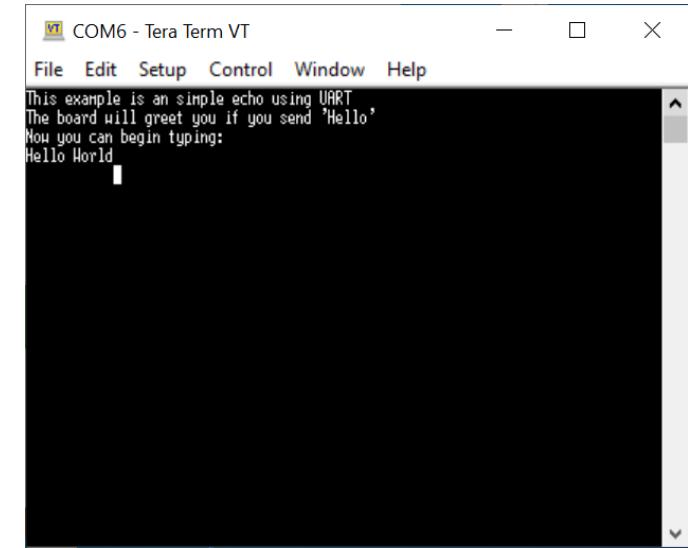
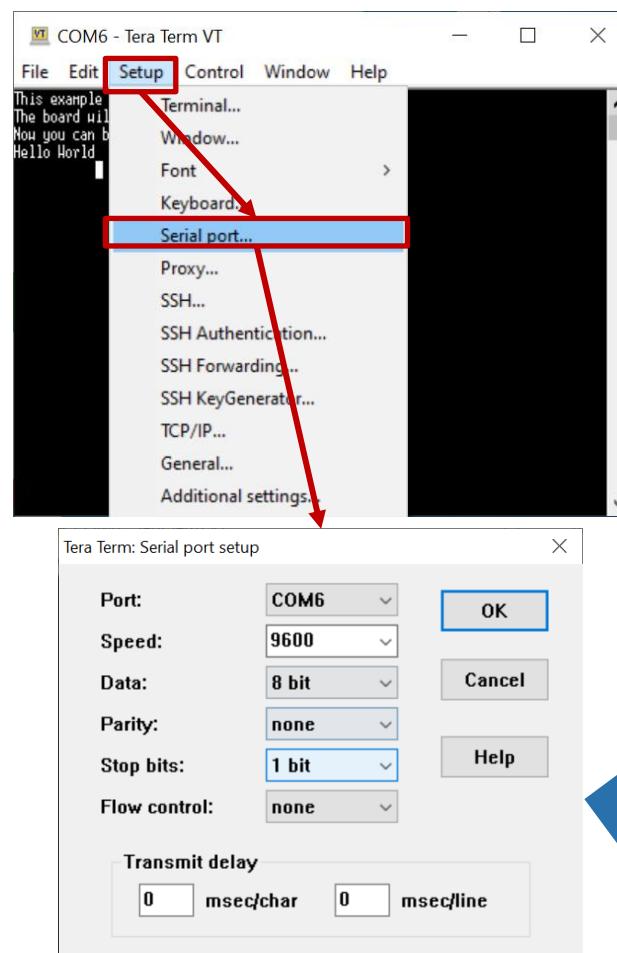
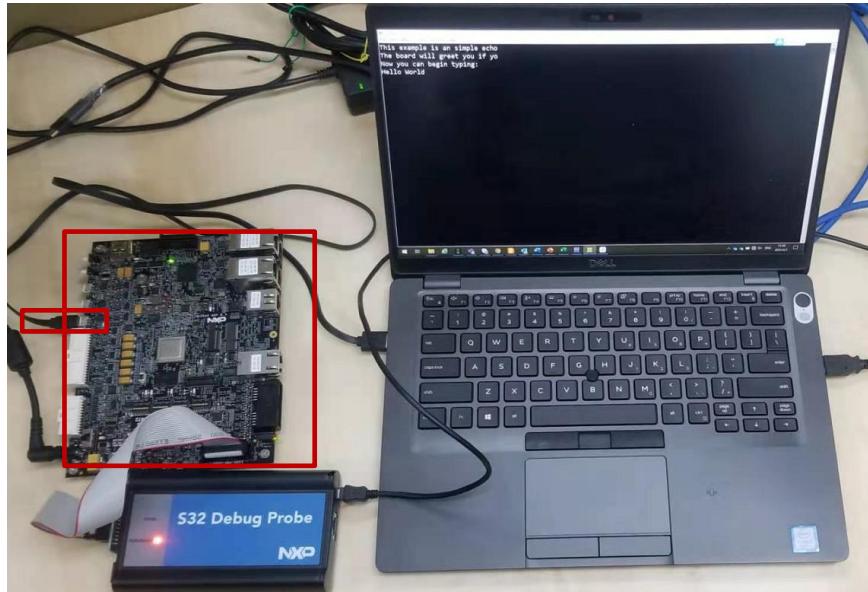
Hands on UART : Debug and run

Click on “Apply”, then click on “Debug”. the perspective will jump to the Debug Perspective, and you can use the controls to control the program flow.



Hands on UART: Test result

- Connect the PC and UART1
- Open Tera Term and Set the serial port
- the terminal software will show the below messages. input “Hello”, UART output “Hello World”





04.

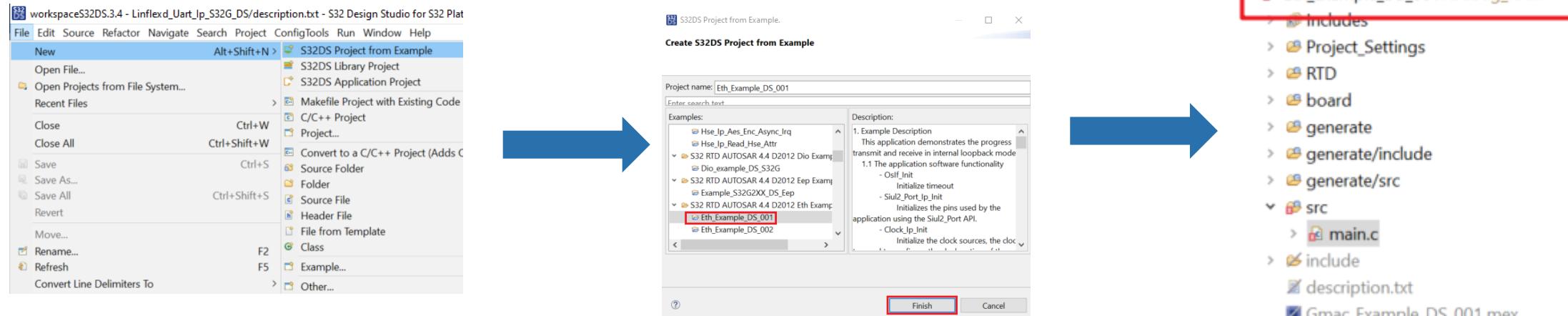
Hands on ETH Example

Hands on ETH – Objective

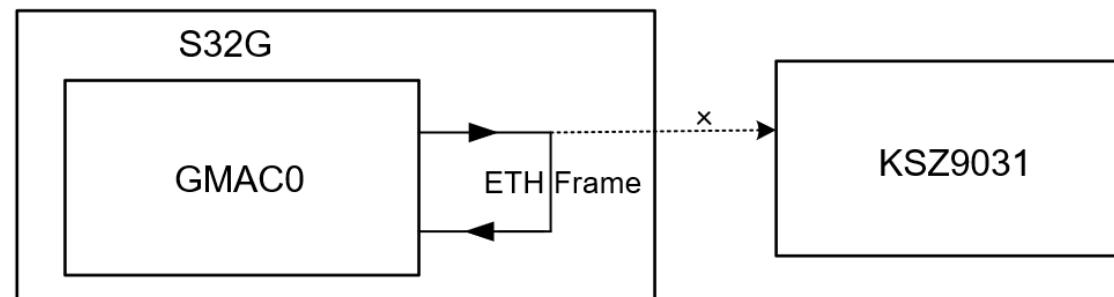
- How to import the ETH example into S32DS
- How to configure the clock of ETH via S32DS
- How to configure the port of ETH via S32DS
- How to use the ETH module to transmit/receive ETH frame
- How to debug the ETH example with S32 debug probe

Hands on ETH: Import ETH example project

Open S32 Design Studio, go to “File -> New -> S32DS Project From Example”. Select “Eth_Example_DS_001” example, then click on “Finish”. The project is copied into current workspace.



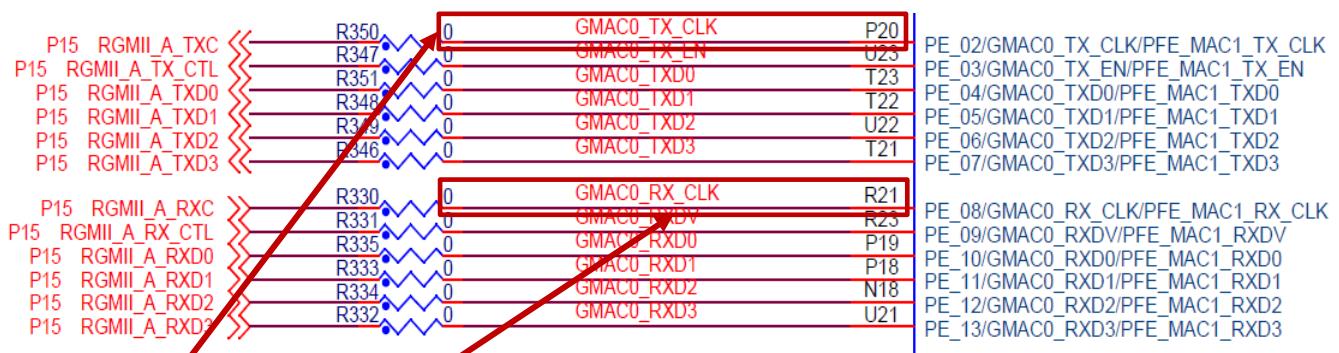
This “Gmac_Example_DS_001” example demonstrates the GMAC transmit and receive in internal loopback mode. The ETH frame is transmitted back directly through GMAC, and the frame will not be transmitted to PHY.



Hands on ETH : Port Configuration 1

Go to desired configuration tool:

- Right click on Project,
- Select S32 Configuration Tool...
- Select Open Pins
- Configure pins to provide the external clock to Tx, Rx signals



```

/* Payload = Frame - (Ds
*((uint32 *)txBuffer.da
)
/* Send the ETH frame */
txBuffer.length = 64U - .
if (GMAC_STATUS_SUCCESS
{
    result = FALSE;
}

/* Wait for the frame to
do {
    status = Gmac_Ip_Get
} while (status == GMAC_
/* Check the frame statu
if ((GMAC_STATUS_SUCCESS
{
    result = FALSE;
}

/* Wait for the frame to
do {
    status = Gmac_Ip_Rea
} while (status == GMAC_
/* Check the frame statu
if ((GMAC_STATUS_SUCCESS
{
    result = FALSE;
}

Gmac_Ip_ProvideRxBuff(IN
Gmac_Ip_DisableControlle
Exit_Example(result);
return 0;

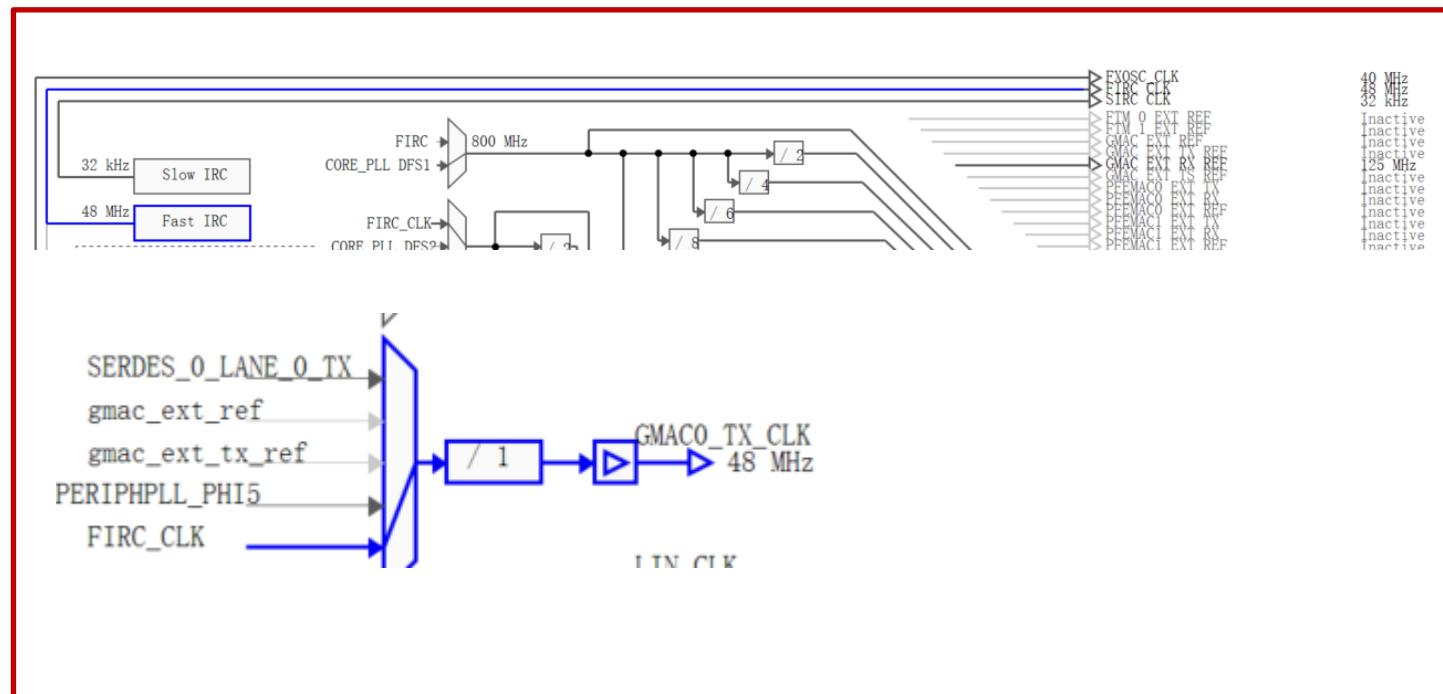
```

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	Output Buffer	Open Drain	Input Buffer	Slew Rate Control	Pullup Enable
	GMAC_0	tx_clk_o	PE_02		n/a	VDD_IO_GMAC0 (0V)	Output	Enabled	Disabled	Disabled	SIUL2_0: FAST pad: 166MHz(1.8V), 150MHz(3.3V) - GPIO pad: 166MHz(1.8V), 50Mhz(3.3V) / SIUL2_1: 150MHz or lower	Disabled
	GMAC_0	rx_clk_i	PE_08		n/a	VDD_IO_GMAC0 (0V)	Input	Disabled	Disabled	Enabled	SIUL2_0: FAST pad: 166MHz(1.8V), 150MHz(3.3V) - GPIO pad: 166MHz(1.8V), 50Mhz(3.3V) / SIUL2_1: 150MHz or lower	Disabled

Hands on ETH : Clock Configuration 1

Open the [Peripheral Clock View](#), Double click the GMAC0 module. The [Clocks Diagram](#) shows the power tree of GMAC module

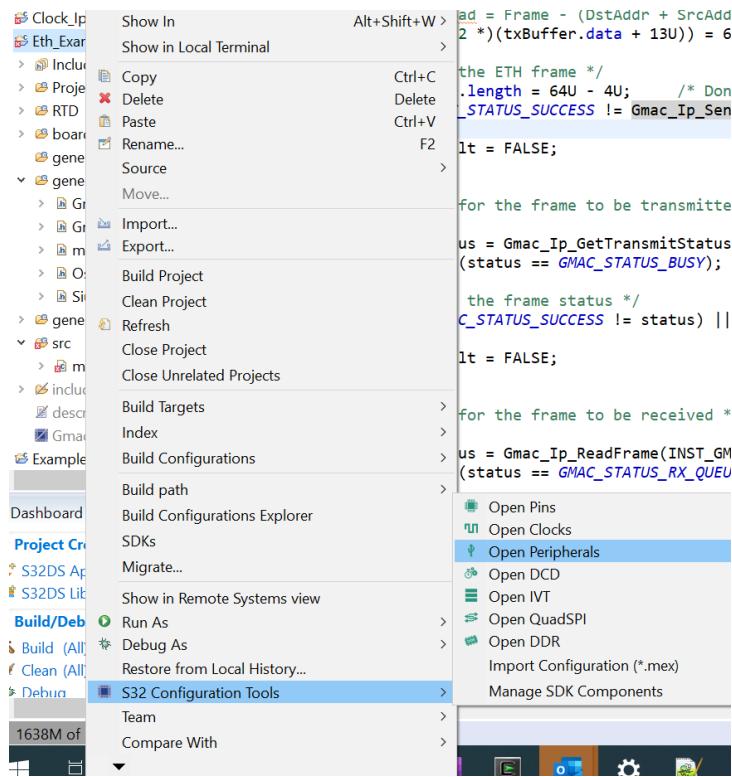
Clock Name	Enable	Source	Divider	Frequency	Monitor
EIM3_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.66....	
EIM_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.66....	
ERM0_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.66....	
FLEXCAN0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
FLEXCAN1_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
FLEXCAN2_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
FLEXCAN3_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
FRAY0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
FTIMER0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
FTIMER1_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
GMAC0_RX_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
GMAC0_TS_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
GMAC0_TX_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 MHz	
IIC0_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.33.....	
IIC1_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.33.....	
IIC2_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.33.....	
IIC3_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.33.....	



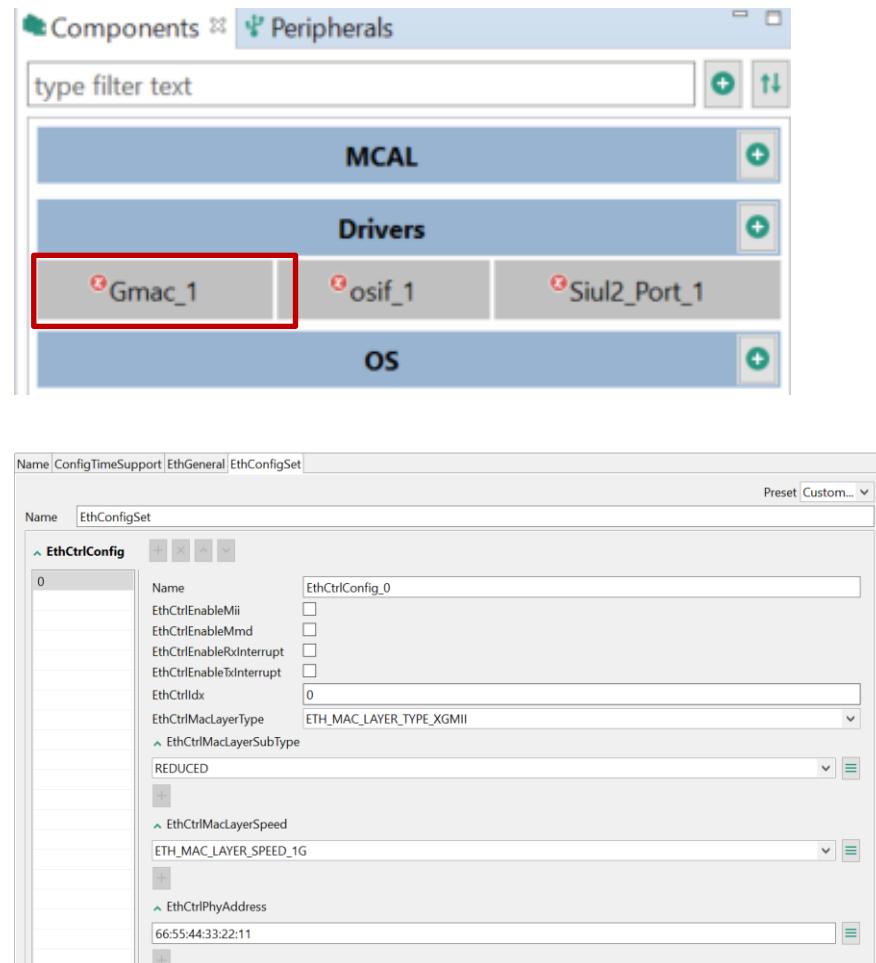
Hands on ETH: ETH configuration

Open the peripheral configuration:

- Right click on Project,
- Select S32 Configuration Tool...
- Select Peripherals



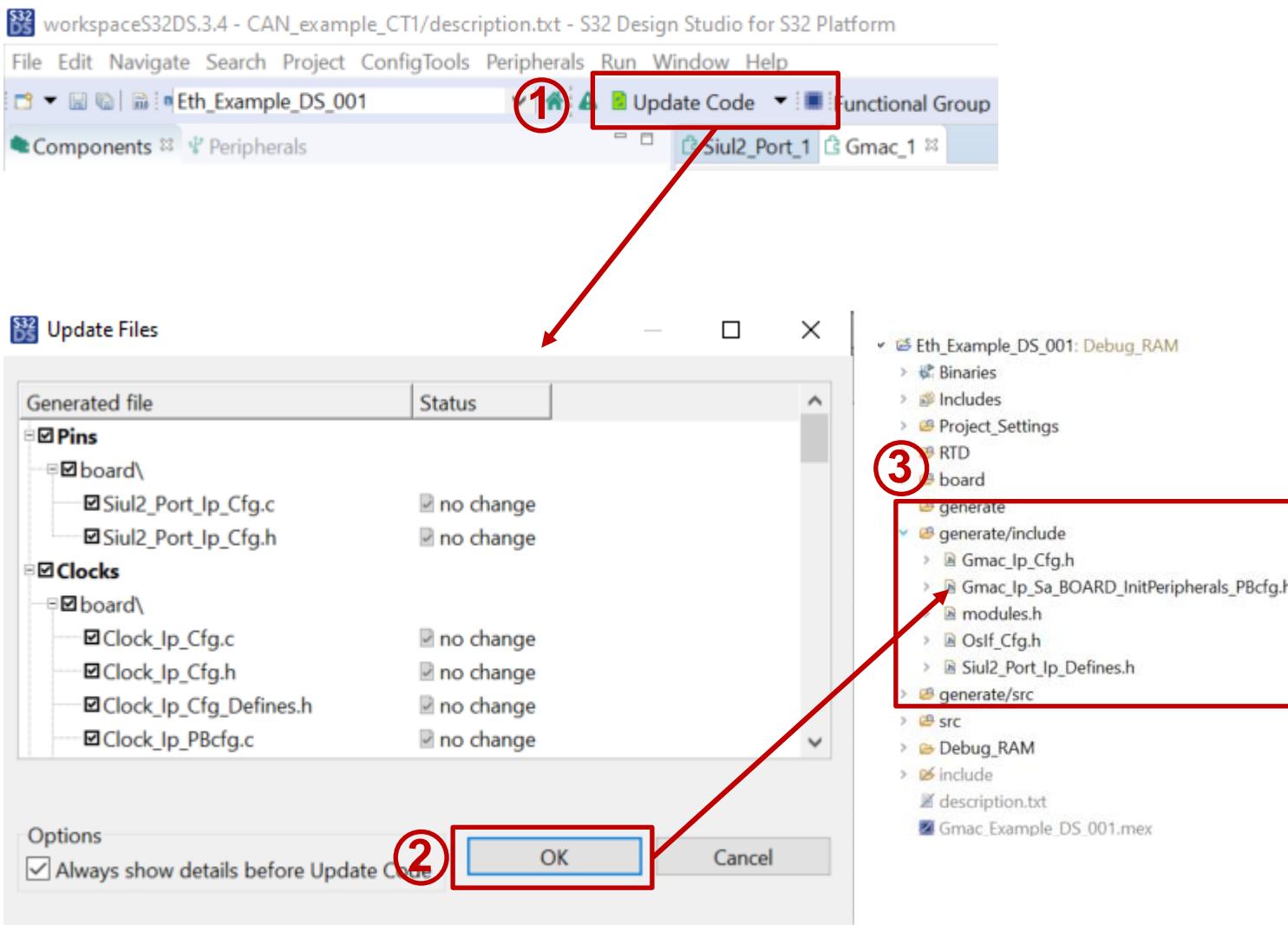
Select **Components** to find out **GMAC_1** Driver and double click



Hands on ETH: Update code

Generate code method:

- 1.Click on any configuration tool, like Pins
Then click **Update Code** (ensure desired project is selected!)
- 2.The Update Files widow pops up. It shows the detail update information. Click **ok** button.
- 3.The configuration .c and .h file will be generated at “generate” folder.



Hands on ETH: Application code 1

```
int main(void)
{
    Gmac_Ip_TxOptionsType txOptions = {TRUE, GMAC_CRC_AND_PAD_INSERTION, GMAC_CHECKSUM_INSERTION_DISABLE};
    Gmac_Ip_BufferType txBuffer = {0};
    Gmac_Ip_BufferType rxBuffer = {0};
    Gmac_Ip_TxInfoType txInfo;
    Gmac_Ip_RxInfoType rxInfo;
    Gmac_Ip_StatusType status;
    uint8 macAddr[6U] = {0U};
    uint8 i;
    uint8 j = 0U;
    boolean result = TRUE;

    OsIf_Init(NULL_PTR);

    Siul2_Port_Ip_Init(NUM_OF_CONFIGURED_PINS0, g_pin_mux_InitConfigArr0);
    Clock_Ip_Init(&Mcu_aClockConfigPB[0]);

    Gmac_Ip_Init(INST_GMAC_0, &Gmac_0_ConfigPB_BOARD_INITPERIPHERALS);

    /* Setup the frame with the Mac address and size */
    Gmac_Ip_GetMacAddr(INST_GMAC_0, macAddr);

    /* Request a buffer of at least 64 bytes */
    txBuffer.length = 64U;
    if ((GMAC_STATUS_SUCCESS != Gmac_Ip_GetTxBuff(INST_GMAC_0, 0U, &txBuffer, NULL_PTR)) || (txBuffer.length < 64U))
    {
        result = FALSE;
    }

    for (i = 0U; i < 12U; i++)
    {
        *((uint8 *)&(txBuffer.data[0U] + i)) = macAddr[0 + j];
        if (j < 5U)
        {
            j++;
        }
        else
        {
            j = 0U;
        }
    }
}
```

Initialize pins to provide the external clock to Tx, Rx signals via the function Siul2_Port_Ip_Init
Initialize clock to Tx, Rx signals via the function Clock_Ip_Init
Enable controller, initialize Tx and Rx buffer via the function Gmac_Ip_Init

initialize transmit buffer and Borrow transmit area to load frame via the function Gmac_Ip_GetTxBuff

Hands on ETH: Application code 2

```
/* Payload = Frame - (DstAddr + SrcAddr + EtherType/Length + FCS) */  
*((uint32 *)(&txBuffer.data[13U])) = 64U - (6U + 6U + 2U + 4U);  
  
/* Send the ETH frame */  
txBuffer.length = 64U - 4U; /* Don't count FCS, because it is automatically inserted by the controller in this example */  
if (GMAC_STATUS_SUCCESS != Gmac_Ip_SendFrame(INST_GMAC_0, 0U, &txBuffer, &txOptions))  
{  
    result = FALSE;  
}  
  
/* Wait for the frame to be transmitted */  
do {  
    status = Gmac_Ip_GetTransmitStatus(INST_GMAC_0, 0U, &txBuffer, &txInfo);  
} while (status == GMAC_STATUS_BUSY);  
  
/* Check the frame status */  
if ((GMAC_STATUS_SUCCESS != status) || (0U != txInfo.errMask))  
{  
    result = FALSE;  
}  
  
/* Wait for the frame to be received */  
do {  
    status = Gmac_Ip_ReadFrame(INST_GMAC_0, 0U, &rxBuffer, &rxInfo);  
} while (status == GMAC_STATUS_RX_QUEUE_EMPTY);  
  
/* Check the frame status */  
if ((GMAC_STATUS_SUCCESS != status) || (0U != rxInfo.errMask))  
{  
    result = FALSE;  
}  
  
Gmac_Ip_ProvideRxBuff(INST_GMAC_0, 0U, &rxBuffer);  
  
Gmac_Ip_DisableController(INST_GMAC_0);
```

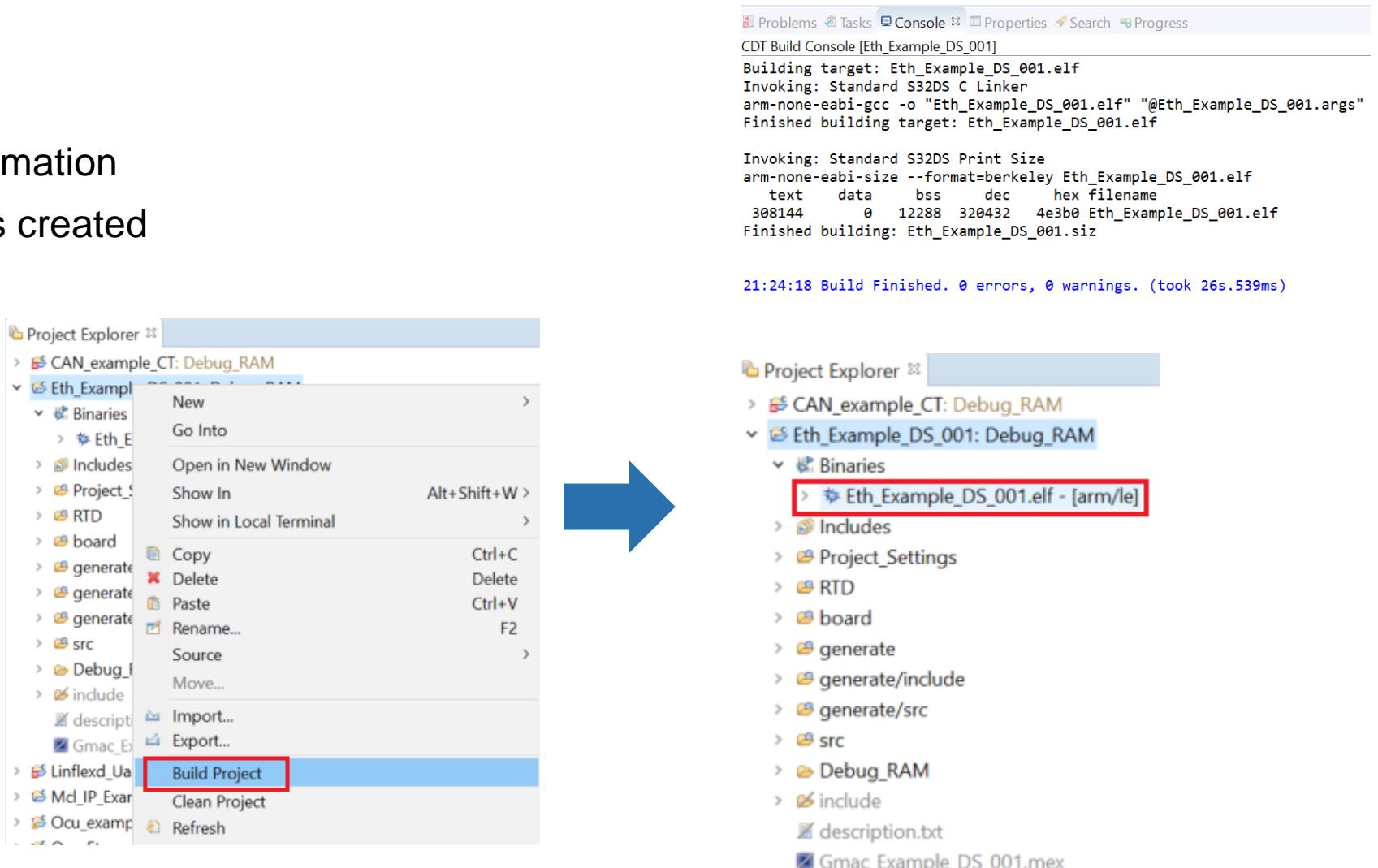
Trigger the transmit frame via Gmac_Ip_SendFrame

Verify frame is transmitted/ received

Hands on ETH: Build and Debug 1

Build target Project:

- Right click on Project,
- Build Project
- The console print build information
- Eth_Example_DS_001.elf is created



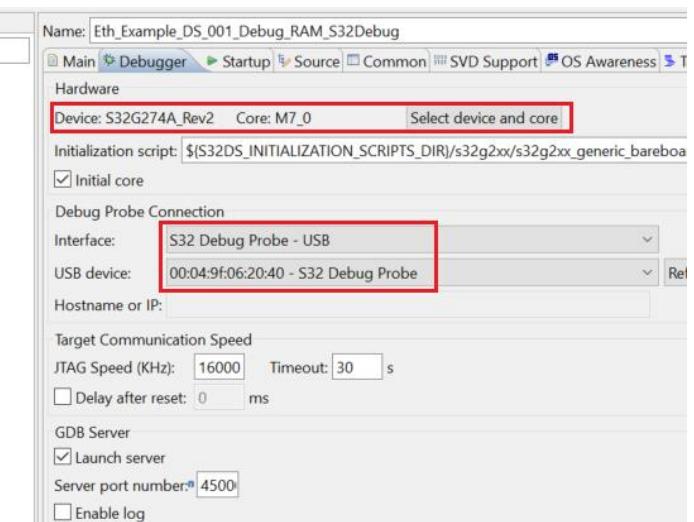
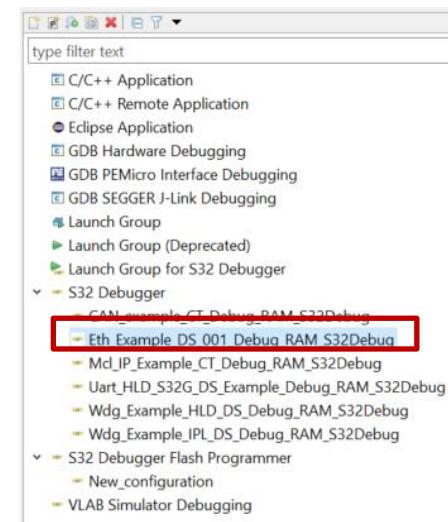
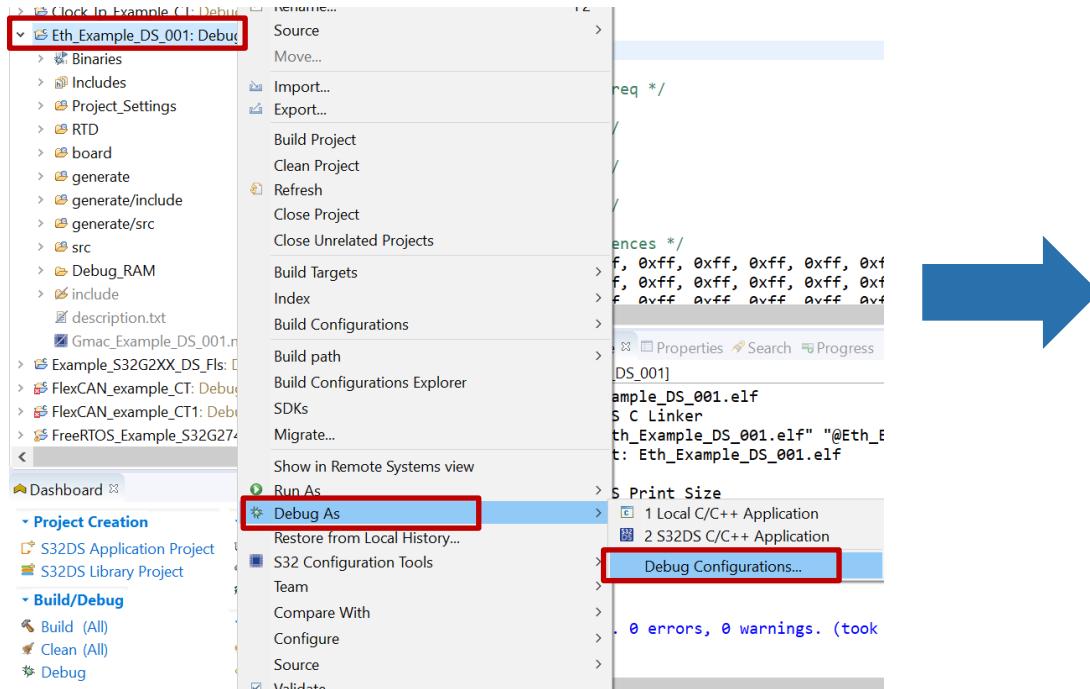
Hands on ETH: Build and Debug 2

Go to debug configuration:

- Right click on Project,
- Select the Debug As
- Click Configurations

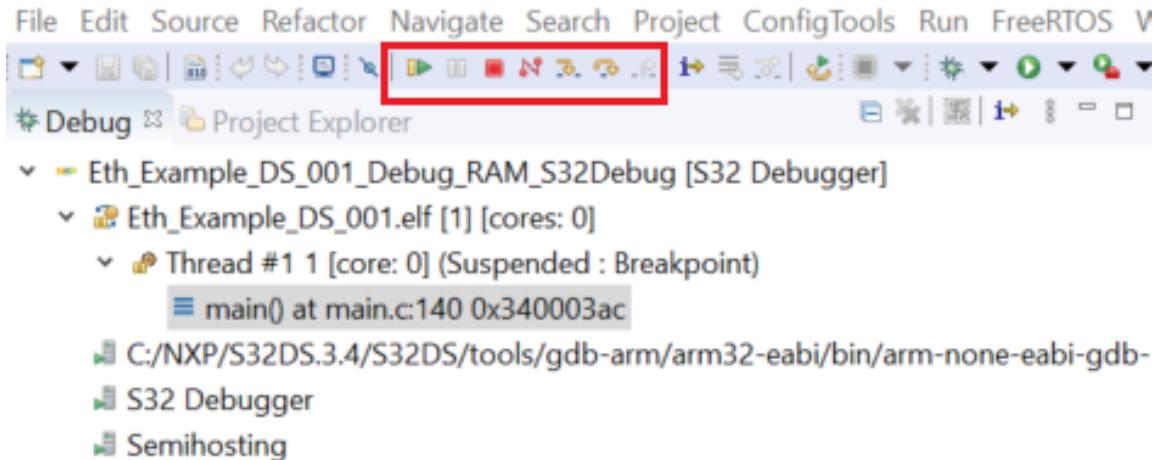
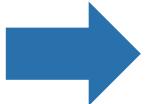
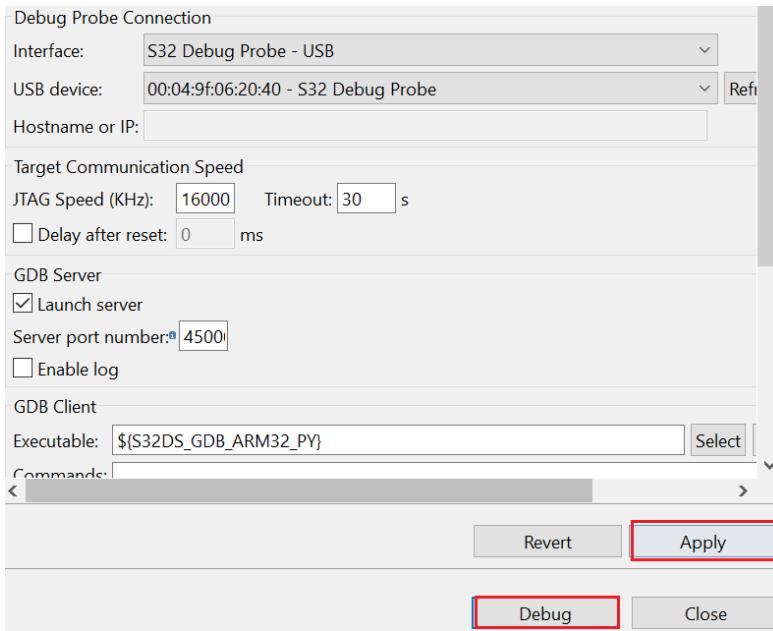
Debug configuration set:

- Click target project ,
- Select the target device
- Select target S32 Debug Probe



Hands on ETH: Debug and run

Click on “Apply”, then click on “Debug”. the perspective will jump to the Debug Perspective, and you can use the controls to control the program flow.



Hands on ETH: Test result

In this project. The eth frame of Transmit & receive in internal loopback mode. The rxBuffer shows the received frame.

The screenshot shows a debugger interface with two main windows. The top window is a 'Monitors' table showing the state of the variable `rxBuffer`. The bottom window is a 'Memory' dump showing the contents of memory starting at address `0x34501700`.

Monitors Table:

Expression	Type	Value
<code>rxBuffer</code>	<code>Gmac_Ip_BufferType</code>	[...]
<code>> * data</code>	<code>uint8 *</code>	<code>0x34501700 <GMAC_0_RxRing_0_DataBuffer> "fUD3\0"</code>
<code>>> length</code>	<code>uint16</code>	64

Memory Dump:

Address	0	3	4	7	8	B	C - F
34501700	66554433	22116655	44332211	002E0000			
34501710	00000000	00000000	00000000	00000000			
34501720	00000000	00000000	00000000	00000000			
34501730	00000000	00000000	00000000	65EA1543			
34501740	00000000	00000000	00000000	00000000			
34501750	00000000	00000000	00000000	00000000			
34501760	00000000	00000000	00000000	00000000			
34501770	00000000	00000000	00000000	00000000			
34501780	00000000	00000000	00000000	00000000			



03.

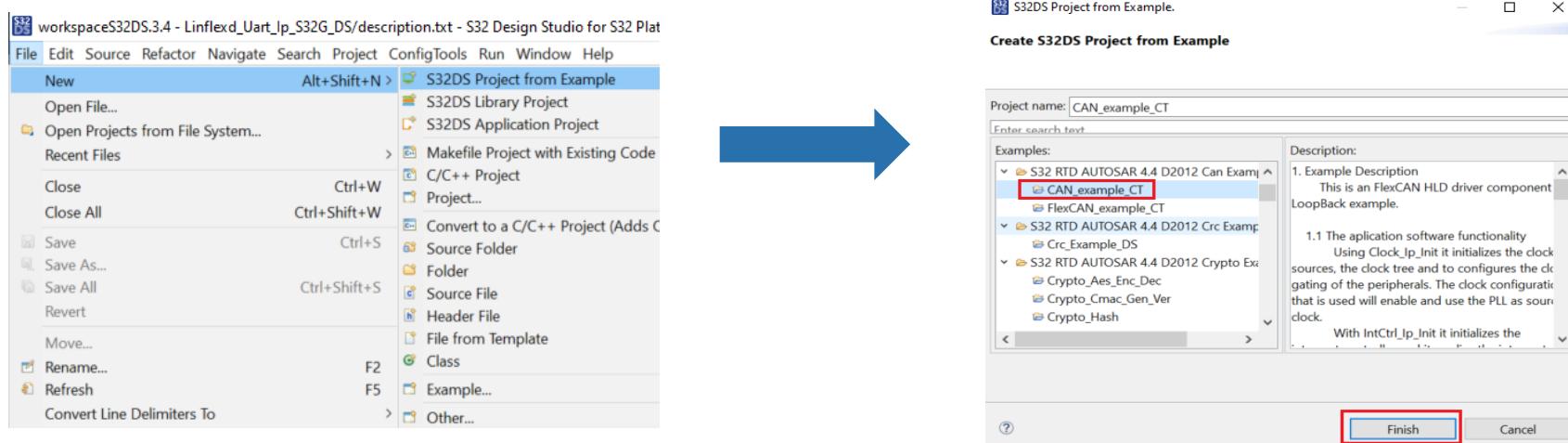
Hands on CAN Example

Hands on CAN – Objective

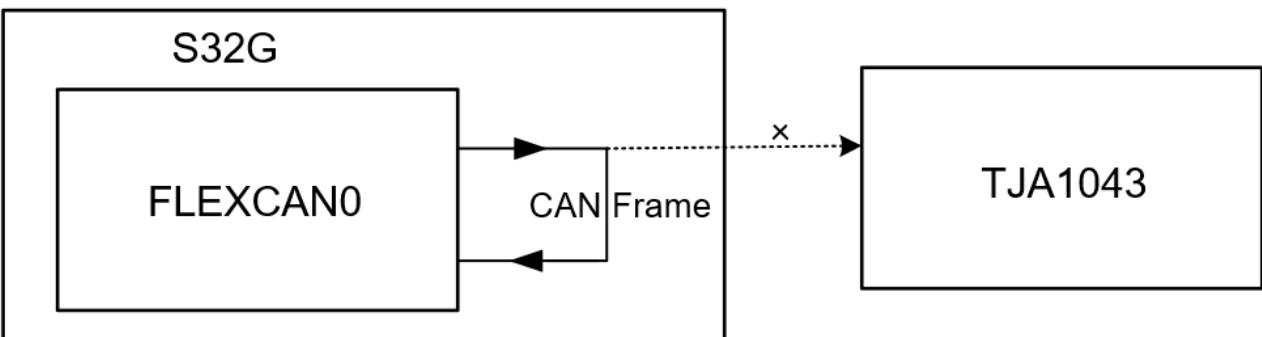
- How to import the CAN example into S32DS
- How to configure the clock of CAN via S32DS
- How to configure the port of CAN via S32DS
- How to modify the CAN loopback
- How to debug the CAN example with S32 debug probe

Hands on CAN : Import CAN example project

Open S32DS3.4, go to “File -> New -> S32DS Project From Example”. Select “CAN_example_CT” example, then click on “Finish”. The project is copied into current workspace.

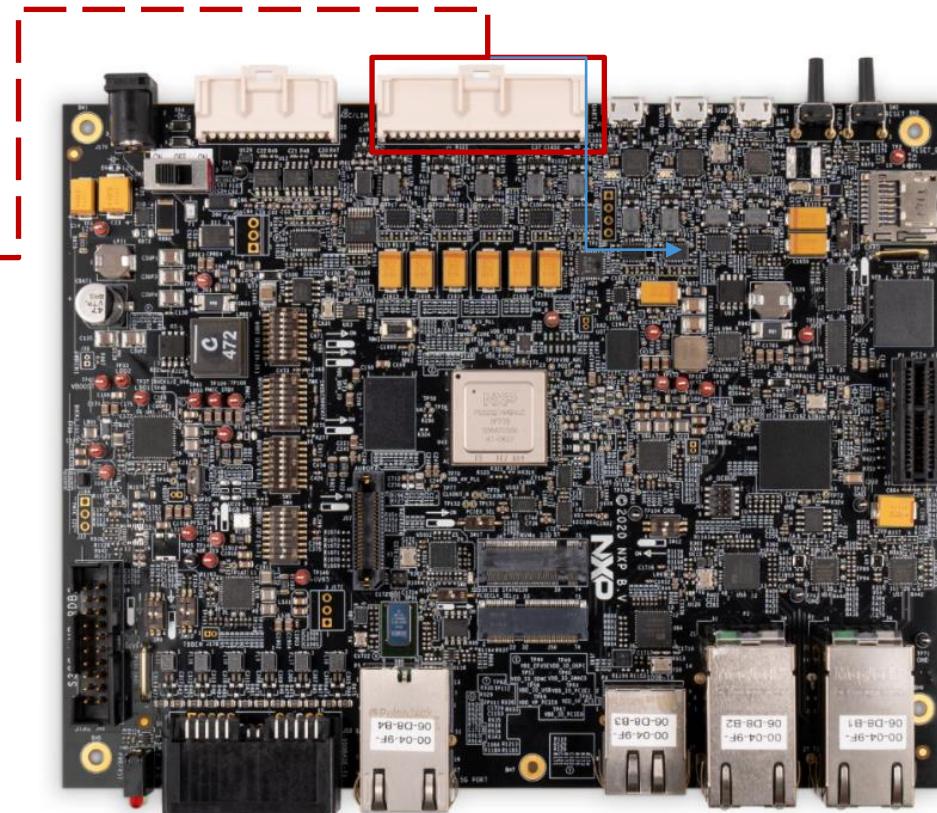
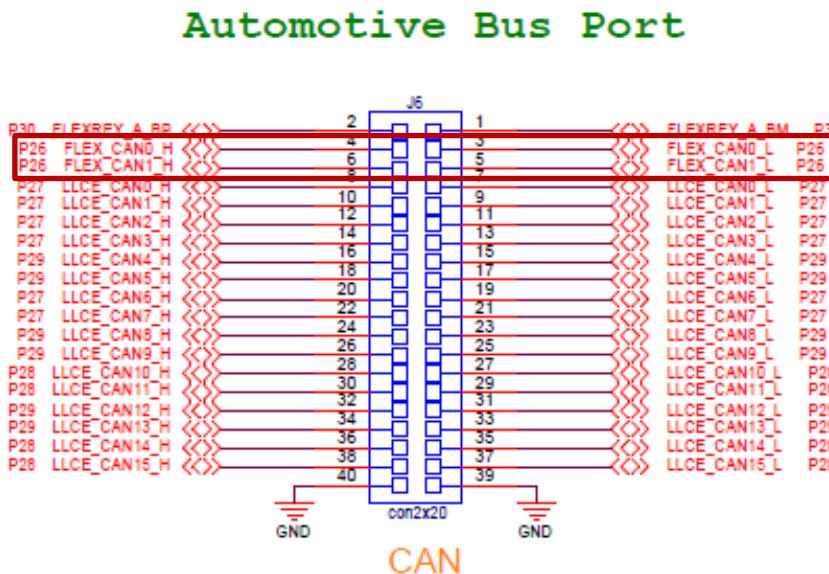


“CAN_example_CT” project is a FlexCAN HLD driver component LoopBack project.



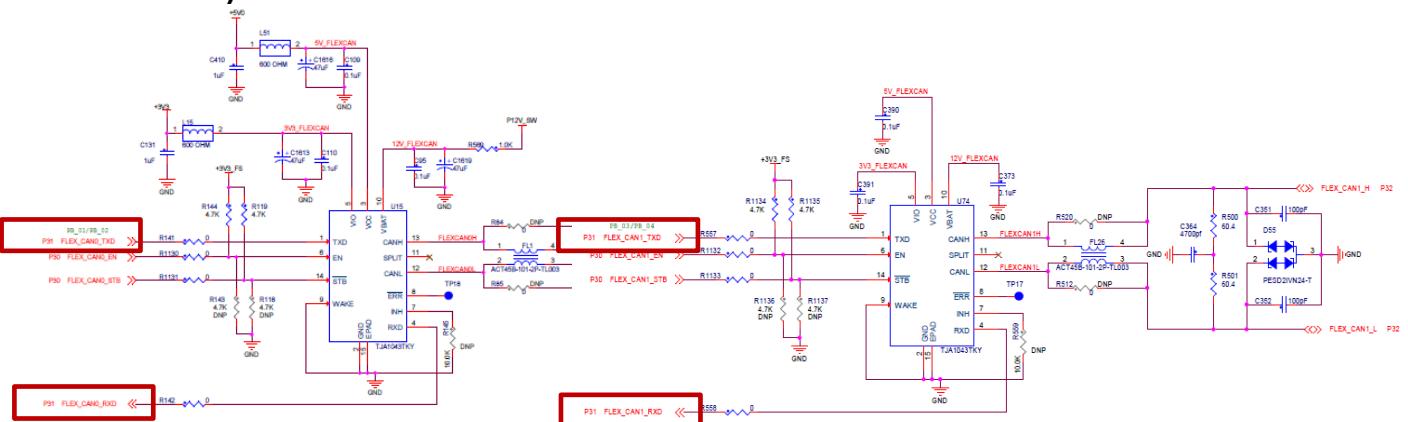
Hands on CAN: the proposed demo need to modify

The “CAN_example_CT” project only support loopback model. modify this default project configuration to build transmit/receive CAN frame from FlexCAN_0 to FlexCAN_1

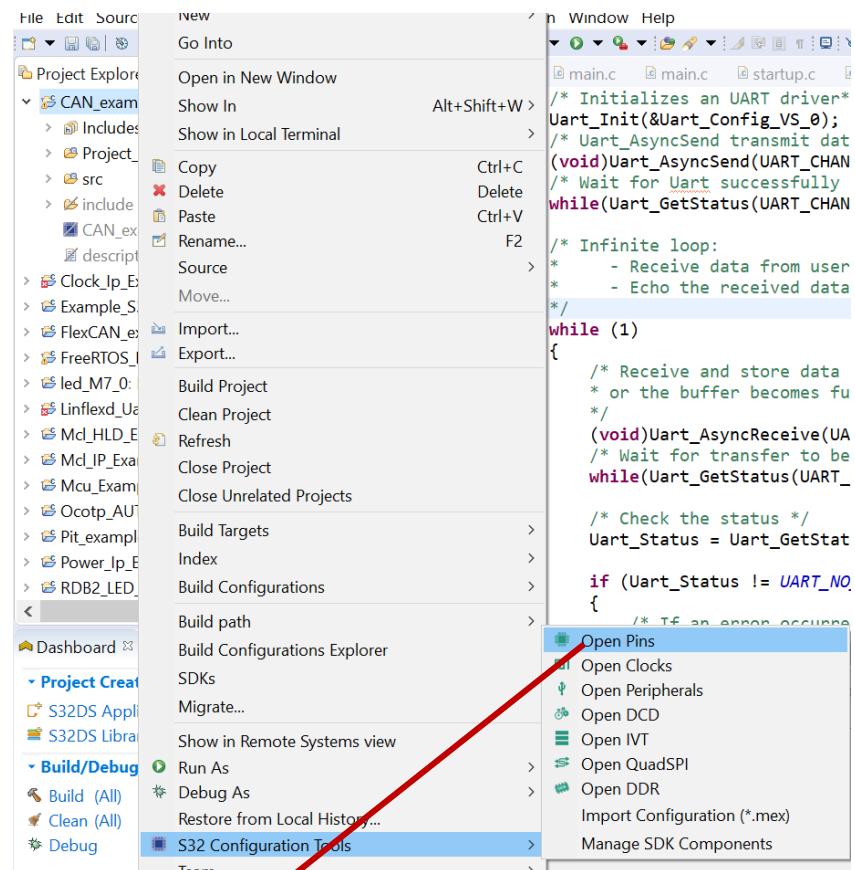


Hands on CAN: Port Configuration 1

- Go to desired configuration tool:
 - Right click on Project,
 - Select S32 Configuration Tool...
 - Select Open Pins
 - Modify the Pins as the schematic of CAN0 and CAN 1

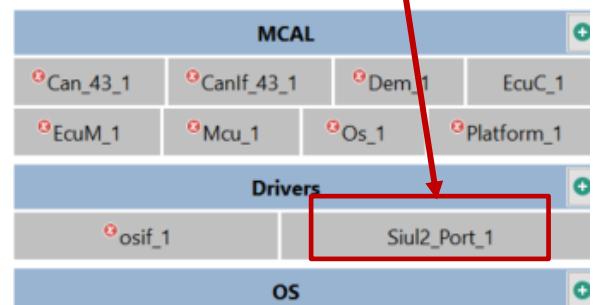
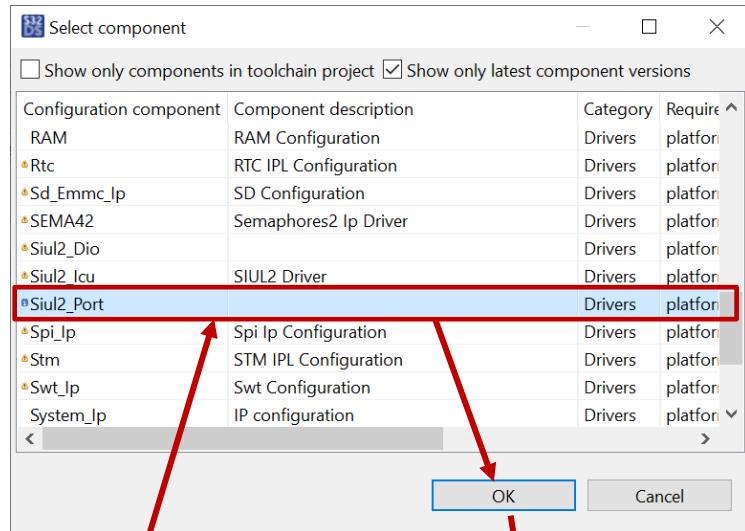
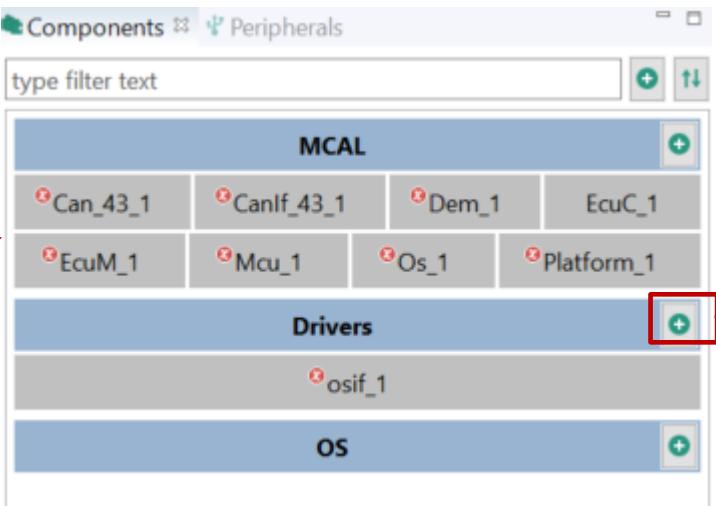
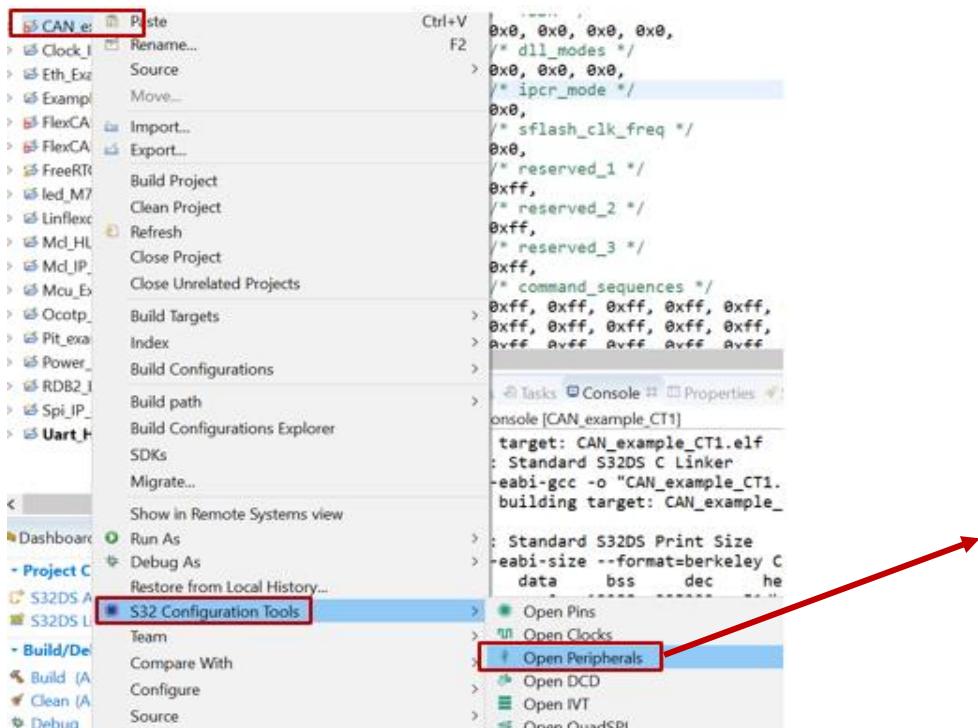


Routed Pins for BOARD...										
#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	Output Buffer	Open Drain	Input Buffer
D7	CAN_0	rxd	PB_02		n/a	VDD_IO_B (0V)	Input	Disabled	Disabled	Enabled
E7	CAN_0	txd	PB_01		n/a	VDD_IO_B (0V)	Output	Enabled	Disabled	Disabled
E8	CAN_1	rxd	PB_04		n/a	VDD_IO_B (0V)	Input	Disabled	Disabled	Enabled
C6	CAN_1	txd	PB_03		n/a	VDD_IO_B (0V)	Output	Enabled	Disabled	Disabled



Hands on CAN: Port Configuration 2

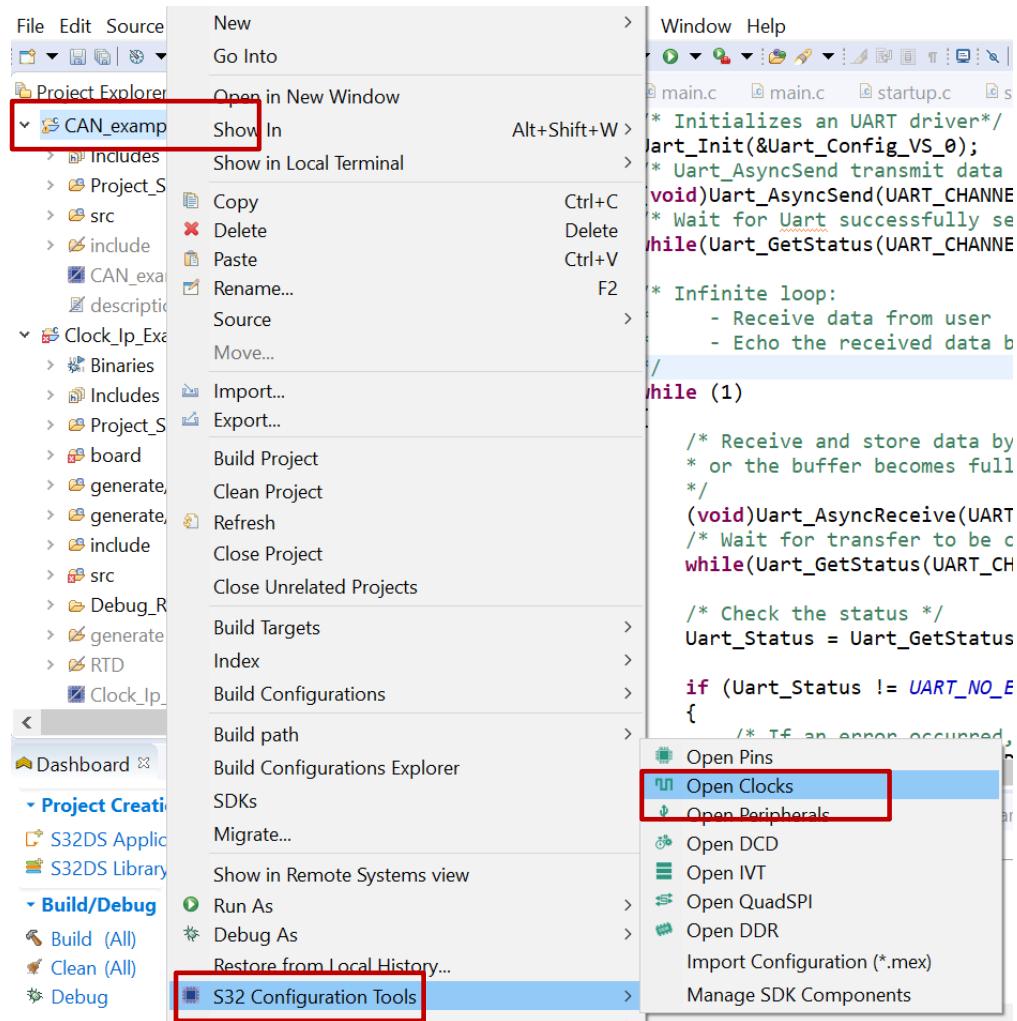
- Add the Port configuration:
 - Right click on Project,
 - Select S32 Configuration Tool...
 - Select Open Peripherals
- Click the plus button
- Click the Siul2_Port component
- The Siul2_Port_1 will be added



Hands on CAN: Clock Configuration 1

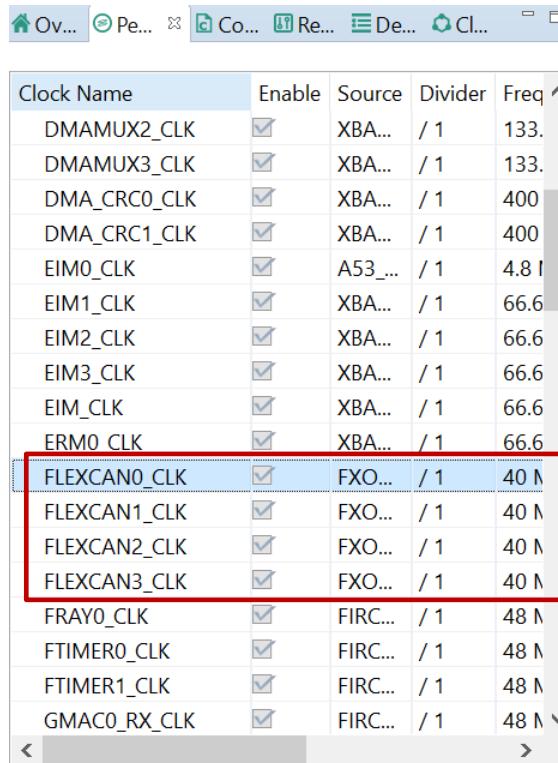
Go to desired configuration tool:

- Right click on Project,
- Select S32 Configuration Tool...
- Select Open Clocks

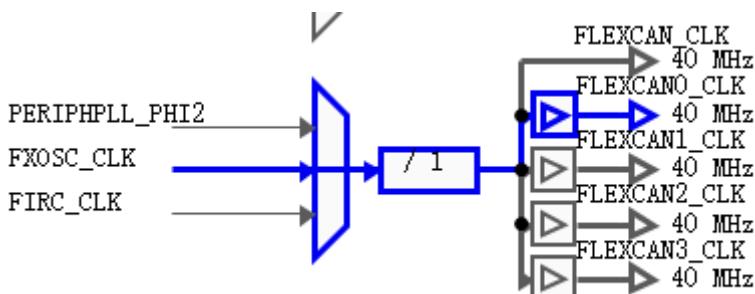
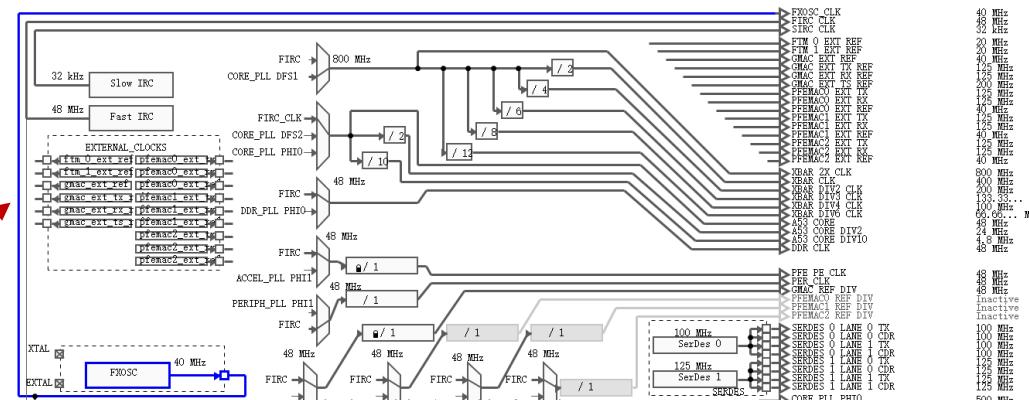


Hands on CAN: Clock Configuration 2

Open the [Peripheral Clock View](#), double click the **FLEXCAN0_CLK**. The [Clocks Diagram](#) will show the power tree and the key node can be re-set. The default clock configuration of CAN is 40 MHZ. the CAN PE clock source comes from FXOSC



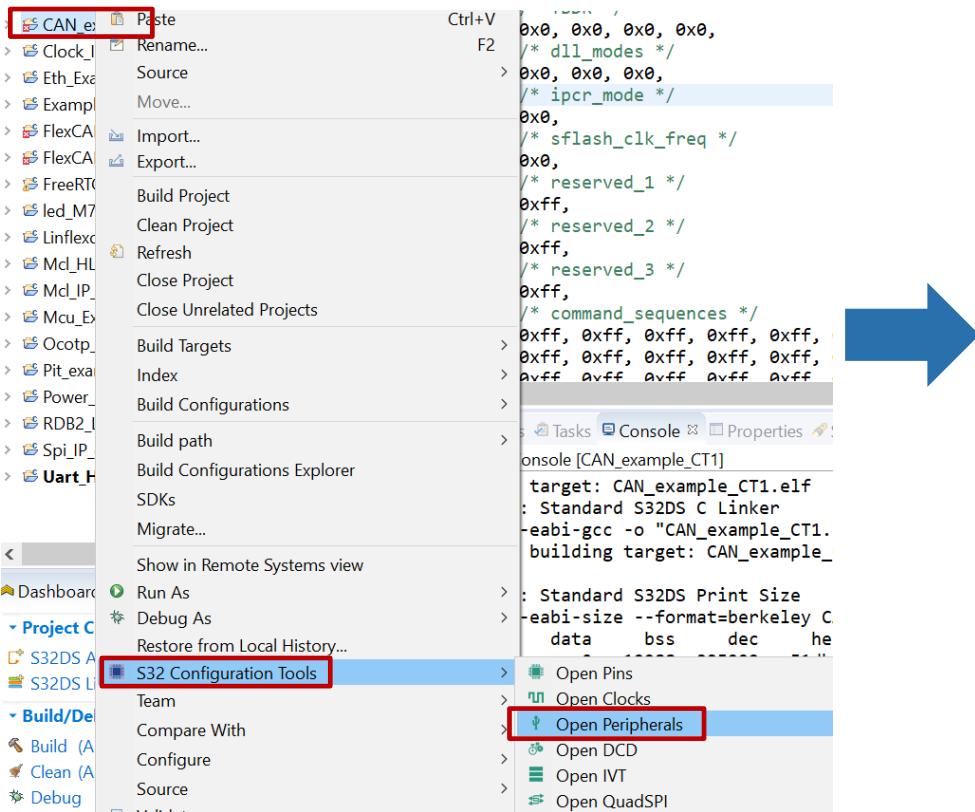
Clock Name	Enable	Source	Divider	Freq
DMAMUX2_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.
DMAMUX3_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	133.
DMA_CRC0_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	400
DMA_CRC1_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	400
EIM0_CLK	<input checked="" type="checkbox"/>	A53...	/ 1	4.8 I
EIM1_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.6
EIM2_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.6
EIM3_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.6
EIM_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.6
ERMO_CLK	<input checked="" type="checkbox"/>	XBA...	/ 1	66.6
FLEXCAN0_CLK	<input checked="" type="checkbox"/>	FXO...	/ 1	40 M
FLEXCAN1_CLK	<input checked="" type="checkbox"/>	FXO...	/ 1	40 M
FLEXCAN2_CLK	<input checked="" type="checkbox"/>	FXO...	/ 1	40 M
FLEXCAN3_CLK	<input checked="" type="checkbox"/>	FXO...	/ 1	40 M
FRAY0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
FTIMER0_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
FTIMER1_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M
GMAC0_RX_CLK	<input checked="" type="checkbox"/>	FIRC...	/ 1	48 M



Hands on CAN: CAN Configuration 1

Open the Clocks Diagram:

- Right click on Project,
- Select S32 Configuration Tool...
- Select Peripherals

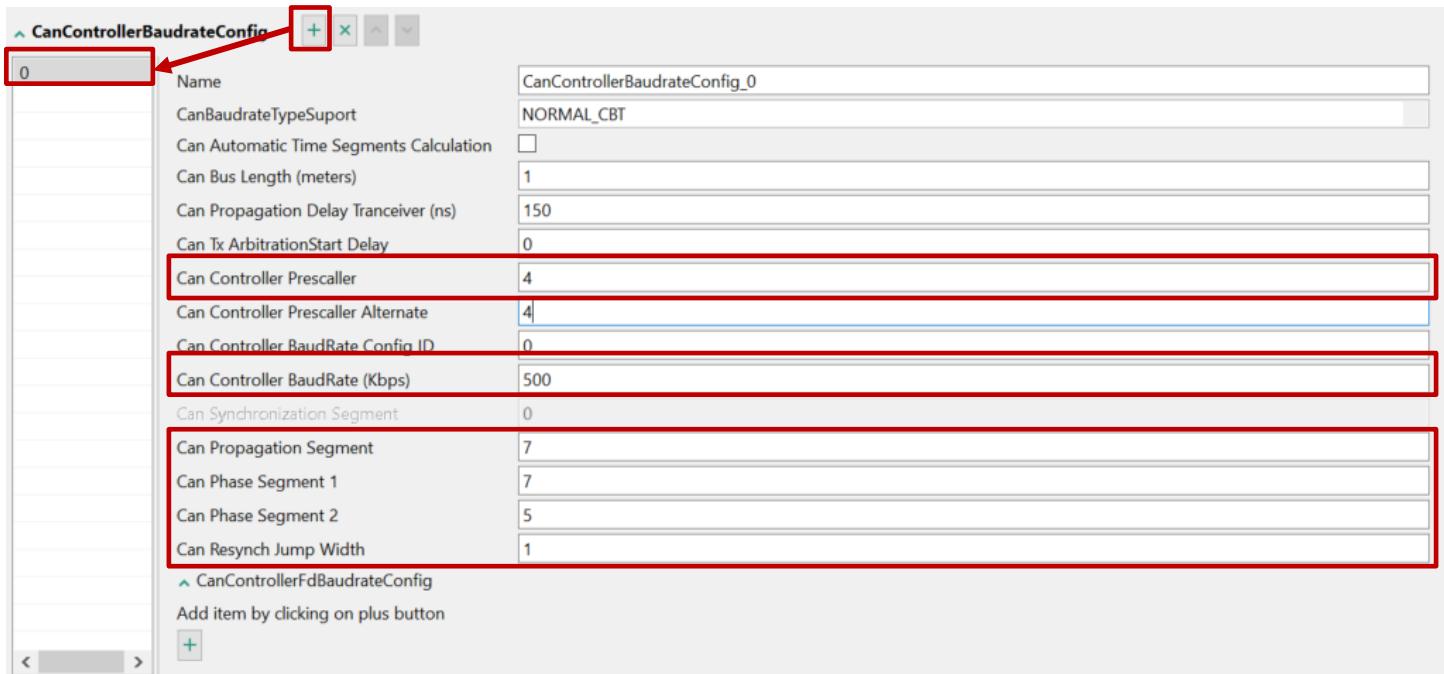


The screenshot shows the MCAL Peripheral Configuration tool. At the top, there are tabs for Components (Components, Peripherals) and a search bar. Below is a tree view under MCAL, showing nodes like Can_43_1, CanIf_43_1, Dem_1, EcuC_1, EcuM_1, Mcu_1, Os_1, and Platform_1. A detailed configuration dialog for the CanController_0 peripheral is open at the bottom. The 'Name' field is set to 'CanController_0'. Under the 'Can Controller Activation' section, the 'Can Loop Back Mode' checkbox is checked and highlighted with a red border. A red annotation text 'disable Loop Back Mode' is placed next to this checkbox. Other configuration options include Can Controller ID (0), Can Rx Processing Type (POLLING), Can Tx Processing Type (POLLING), Can BusOff Processing Type (INTERRUPT), Can Wakeup Functionality API (unchecked), Can Wakeup Processing Type (unchecked), and Can Wakeup Support (unchecked).

Hands on CAN: CAN Configuration 2

Configure the Baud rate as 500Kbps for Controller 0

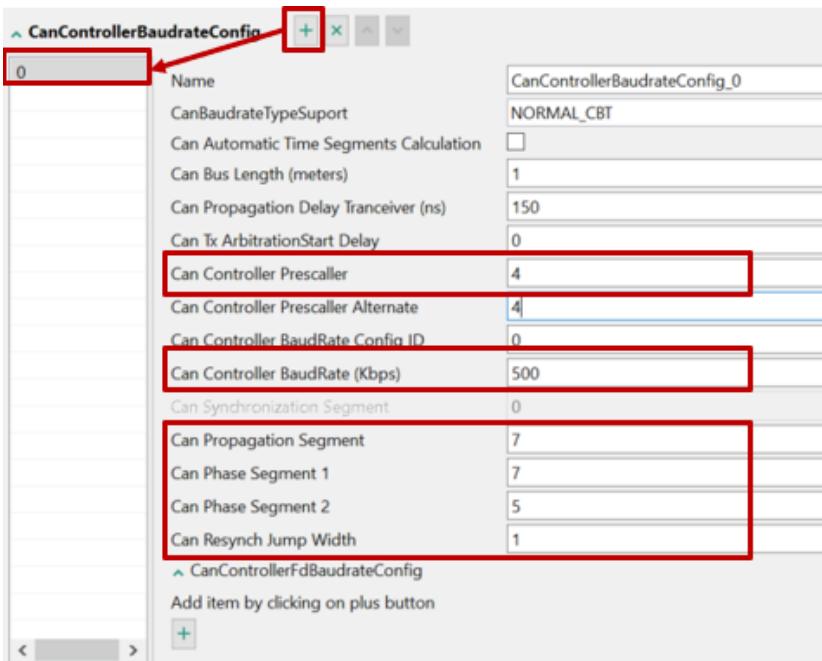
- TimeQuantum (seconds) = Prescaler / CanClockFrequency
- No. of CanTimeQuantas = (1 / CancontrollerBaudRate) / TimeQuantum
- No. of CanTimeQuantas = 1 + CanControllerPropSeg + CanControllerSeg1 + CanControllerSeg2



Hands on CAN: CAN Configuration 3

Open the peripheral configuration view

- add a new CanController for FLEXCAN_1
- Set Hardware Channel as FLEXCAN_1
- Set CAN Rx/TX Processing Type as POLLING
- Set CanCpuClockRef as 40Mhz
- Set Baudrate as 500kbps



Set Baudrate

AUTOSAR CAN Driver [MCAL]

Name: Can_43_1
Mode: General Mode

Name	Value
Can Controller Activation	1
Can Controller Base Address	
Can Controller ID	
Can Rx Processing Type	POLLING
Can Tx Processing Type	POLLING
Can BusOff Processing Type	
Can Wakeup Functionality API	
Can Wakeup Processing Type	
Can Wakeup Support	
Can Loop Back Mode	
Can Auto BusOff Recovery	
Can Three Samples	
Can Protocol Exception	
Can Edge Filter	
Can FD ISO	
Can Controller Default Baudrate	
Can Controller Ecuc Partition Ref	
CanCpuClockRef	/Mcu_1/Mcu/McuModuleConfiguration/McuClockSettingConfig_0/McuClockReferencePoint_0
CanCpuClockRefAlternate	/Mcu_1/Mcu/McuModuleConfiguration/McuClockSettingConfig_0/McuClockReferencePoint_0

Hands on CAN: CAN Configuration 3

Modify the CanHardwareObjects Configuration for CanController 0 and CanController 1

Set the CanHardwareObjects_0 reference to CanController 1

Set the CanHardwareObjects_1 reference to CanController 0

Name	CanController	CanHardwareObject																																			
0		<table border="1"><tr><td>Name</td><td>CanHardwareObject_0</td></tr><tr><td>FD padding value</td><td>0</td></tr><tr><td>Can Implementation Type</td><td>BASIC</td></tr><tr><td>Can ID Message Type</td><td>STANDARD</td></tr><tr><td>Can Object ID</td><td>2</td></tr><tr><td>Can Object Type</td><td>RECEIVE</td></tr><tr><td>Hardware Object Uses Polling.</td><td><input checked="" type="checkbox"/></td></tr><tr><td>CanTriggerTransmitEnable</td><td><input type="checkbox"/></td></tr><tr><td>Can Controller Reference</td><td>/Can_43_1/Can/CanConfigSet/CanController_1</td></tr><tr><td>Can MainFunction RW Period Reference</td><td>/Can_43_1/Can/CanGeneral/CanMainFunctionRWPerio</td></tr><tr><td>Can HwObject Uses Block</td><td>CAN_RAM_BLOCK_0</td></tr><tr><td>Can Hw Object Count</td><td>1</td></tr><tr><td colspan="2">CanHwFilterArray</td></tr><tr><td>0</td><td>Name</td><td>Can_aHwFilter_Object_0</td></tr><tr><td></td><td>Can Hw Filter Code</td><td>0</td></tr><tr><td></td><td>Can Hw Filter Mask</td><td>0</td></tr></table>	Name	CanHardwareObject_0	FD padding value	0	Can Implementation Type	BASIC	Can ID Message Type	STANDARD	Can Object ID	2	Can Object Type	RECEIVE	Hardware Object Uses Polling.	<input checked="" type="checkbox"/>	CanTriggerTransmitEnable	<input type="checkbox"/>	Can Controller Reference	/Can_43_1/Can/CanConfigSet/CanController_1	Can MainFunction RW Period Reference	/Can_43_1/Can/CanGeneral/CanMainFunctionRWPerio	Can HwObject Uses Block	CAN_RAM_BLOCK_0	Can Hw Object Count	1	CanHwFilterArray		0	Name	Can_aHwFilter_Object_0		Can Hw Filter Code	0		Can Hw Filter Mask	0
Name	CanHardwareObject_0																																				
FD padding value	0																																				
Can Implementation Type	BASIC																																				
Can ID Message Type	STANDARD																																				
Can Object ID	2																																				
Can Object Type	RECEIVE																																				
Hardware Object Uses Polling.	<input checked="" type="checkbox"/>																																				
CanTriggerTransmitEnable	<input type="checkbox"/>																																				
Can Controller Reference	/Can_43_1/Can/CanConfigSet/CanController_1																																				
Can MainFunction RW Period Reference	/Can_43_1/Can/CanGeneral/CanMainFunctionRWPerio																																				
Can HwObject Uses Block	CAN_RAM_BLOCK_0																																				
Can Hw Object Count	1																																				
CanHwFilterArray																																					
0	Name	Can_aHwFilter_Object_0																																			
	Can Hw Filter Code	0																																			
	Can Hw Filter Mask	0																																			
1																																					

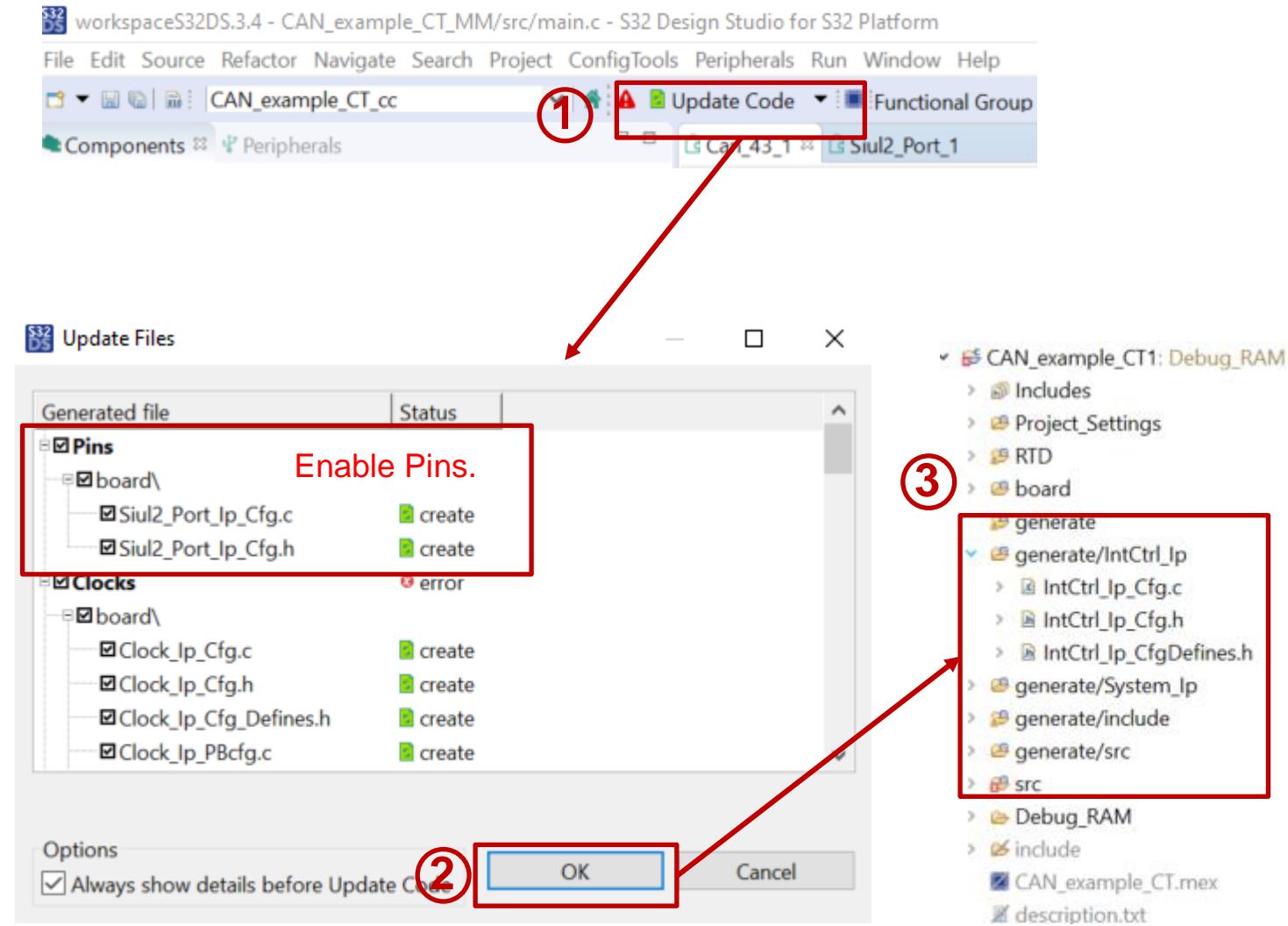
Name	CanController	CanHardwareObject																																		
0		<table border="1"><tr><td>Name</td><td>CanHardwareObject_1</td></tr><tr><td>FD padding value</td><td>0</td></tr><tr><td>Can Implementation Type</td><td>BASIC</td></tr><tr><td>Can ID Message Type</td><td>STANDARD</td></tr><tr><td>Can Object ID</td><td>1</td></tr><tr><td>Can Object Type</td><td>TRANSMIT</td></tr><tr><td>Hardware Object Uses Polling.</td><td><input checked="" type="checkbox"/></td></tr><tr><td>CanTriggerTransmitEnable</td><td><input type="checkbox"/></td></tr><tr><td>Can Controller Reference</td><td>/Can_43_1/Can/CanConfigSet/CanController_0</td></tr><tr><td>Can MainFunction RW Period Reference</td><td>/Can_43_1/Can/CanGeneral/CanMainFunctionRWPerio</td></tr><tr><td>Can HwObject Uses Block</td><td>CAN_RAM_BLOCK_0</td></tr><tr><td>Can Hw Object Count</td><td>1</td></tr><tr><td colspan="2">CanHwFilterArray</td></tr><tr><td>Add item by clicking on plus button</td><td colspan="2"></td></tr><tr><td colspan="2">CanTTHardwareObjectTriggerArray</td></tr><tr><td>Add item by clicking on plus button</td><td colspan="2"></td></tr></table>	Name	CanHardwareObject_1	FD padding value	0	Can Implementation Type	BASIC	Can ID Message Type	STANDARD	Can Object ID	1	Can Object Type	TRANSMIT	Hardware Object Uses Polling.	<input checked="" type="checkbox"/>	CanTriggerTransmitEnable	<input type="checkbox"/>	Can Controller Reference	/Can_43_1/Can/CanConfigSet/CanController_0	Can MainFunction RW Period Reference	/Can_43_1/Can/CanGeneral/CanMainFunctionRWPerio	Can HwObject Uses Block	CAN_RAM_BLOCK_0	Can Hw Object Count	1	CanHwFilterArray		Add item by clicking on plus button			CanTTHardwareObjectTriggerArray		Add item by clicking on plus button		
Name	CanHardwareObject_1																																			
FD padding value	0																																			
Can Implementation Type	BASIC																																			
Can ID Message Type	STANDARD																																			
Can Object ID	1																																			
Can Object Type	TRANSMIT																																			
Hardware Object Uses Polling.	<input checked="" type="checkbox"/>																																			
CanTriggerTransmitEnable	<input type="checkbox"/>																																			
Can Controller Reference	/Can_43_1/Can/CanConfigSet/CanController_0																																			
Can MainFunction RW Period Reference	/Can_43_1/Can/CanGeneral/CanMainFunctionRWPerio																																			
Can HwObject Uses Block	CAN_RAM_BLOCK_0																																			
Can Hw Object Count	1																																			
CanHwFilterArray																																				
Add item by clicking on plus button																																				
CanTTHardwareObjectTriggerArray																																				
Add item by clicking on plus button																																				

| 1 | | |

Hands on ETH: Update code

Generate code method:

- 1.Click on any configuration tool, like Pins
Then click **Update Code** (ensure desired project is selected!)
- 2.The Update Files widow pops up. It shows the detail update information. Click **ok** button.
- 3.The configuration .c and .h file will be generated at “generate” folder.



Hands on CAN: Application code

```
20/*=====
21 *          INCLUDE FILES
22 * 1) system and project includes
23 * 2) needed interfaces from external units
24 * 3) internal and external interfaces from this unit
25 =====
26 #include "Mcu.h"
27 #include "Platform.h"
28 #include "Can.h"
29 #include "SchM_Can.h"
30 #include "check_example.h"
31
32 #include "Siul2_Port_Ip.h"
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127
128 int main(void)
129 {
130     uint8 u8TimeOut = 100U;
131     CanIf_bTxFlag = FALSE;
132     CanIf_bRxFlag = FALSE;
133     /* Initialize the Mcu driver */
134     Mcu_Init(NULL_PTR);
135
136     /* Initialize the clock tree and apply PLL as system clock */
137     Mcu_InitClock(McuClockSettingConfig_0);
138
139     while (MCU_PLL_LOCKED != Mcu_GetPllStatus())
140     {
141         /* Busy wait until the System PLL is locked */
142     }
143
144     Mcu_DistributePllClock();
145     Mcu_SetMode(McuModeSettingConf_0);
146     /* Initialize Platform driver */
147     Platform_Init(NULL_PTR);
148     static Can_PduType Can_PduInfo;
149
150     Siul2_Port_Ip_Init(NUM_OF_CONFIGURED_PINS0, g_pin_mux_InitConfigArr0);
151     /* Can_CreatePduInfo(id, swPduHandle,length, sdu) */
```

Add the Port configuration and initiation function

Add the Can_SetControllerMode for CanController_1

```
/* Can_CreatePduInfo(id, swPduHandle,length, sdu) */
Can_PduInfo = Can_CreatePduInfo(0U, 0U, 8U, Can_au8Sdu8bytes);
/* Initialize Can driver */
Can_Init(&Can_Config_VS_0);
Can_SetControllerMode(CanController_0, CAN_CS_STARTED);
Can_SetControllerMode(CanController_1, CAN_CS_STARTED);
if((Can_Write(CanHardwareObject_1, &Can_PduInfo) == E_OK))
while(!CanIf_bTxFlag) && (u8TimeOut != 0U))

    Can_MainFunction_Write();
    Can_DummyDelay(100U);
    u8TimeOut--;

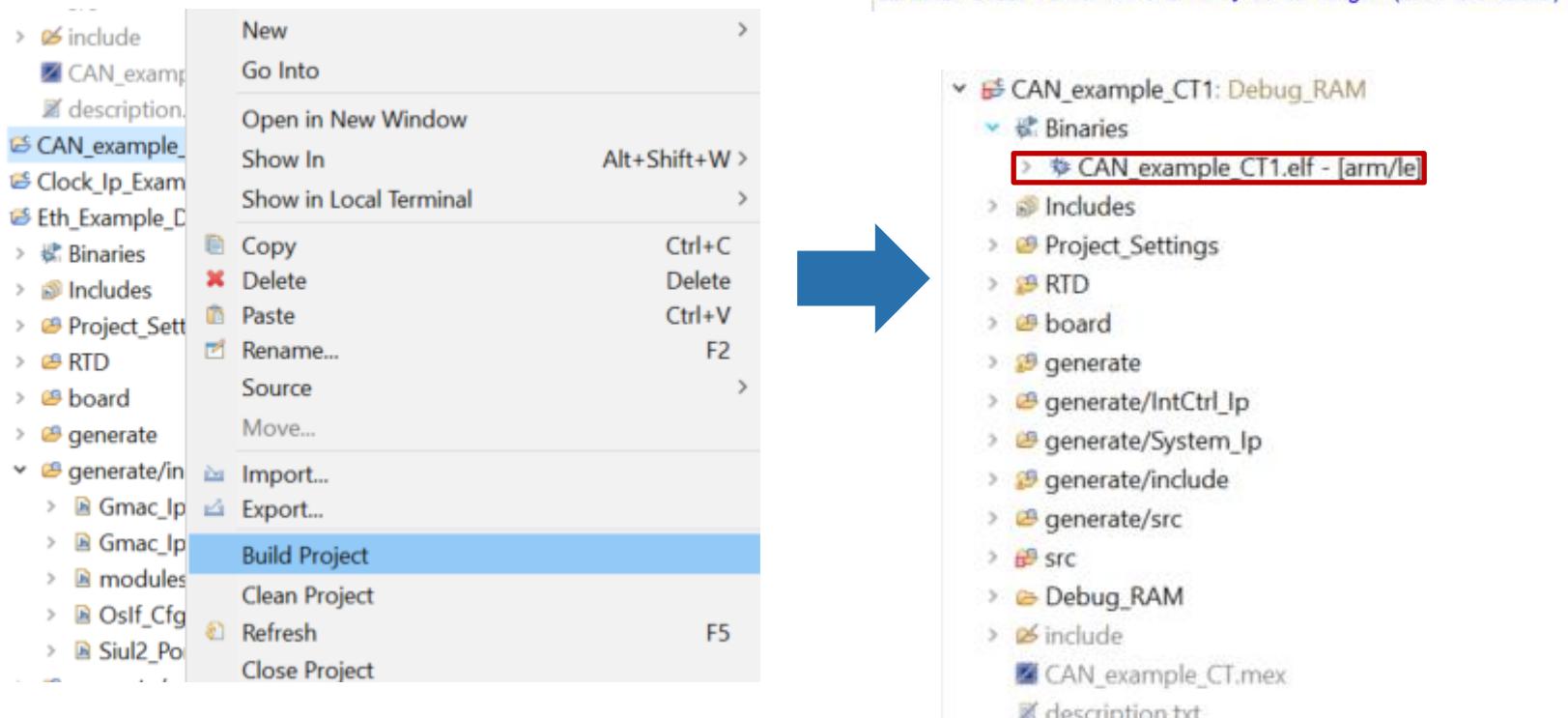
}

u8TimeOut = 100U;
while(!CanIf_bRxFlag) && (u8TimeOut != 0U)
{
    Can_MainFunction_Read();
    Can_DummyDelay(100U);
    u8TimeOut--;
}
Can_SetControllerMode(CanController_0, CAN_CS_STOPPED);
Can_SetControllerMode(CanController_1, CAN_CS_STOPPED);
Can_DeInit();
```

Hands on CAN: Build and Debug

Build target Project:

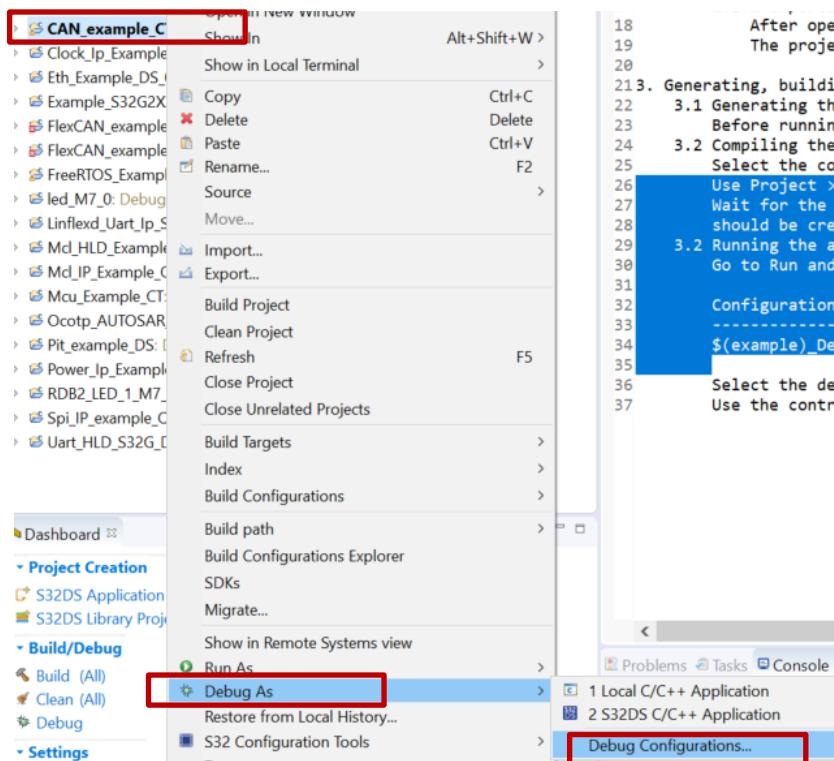
- Right click on Project
- Build Project
- The console print build information
- CAN_example_CT1.elf is created



Hands on CAN: Build and Debug

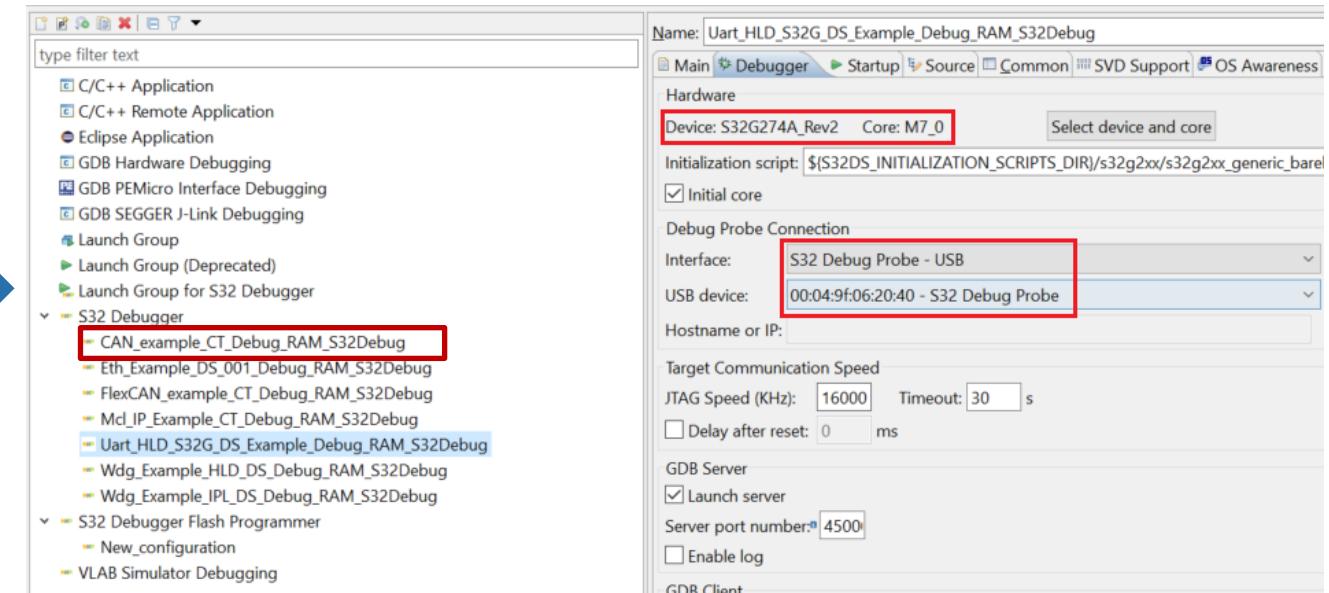
Go to debug configuration:

- Right click on Project,
- Select the Debug As
- Click Configurations



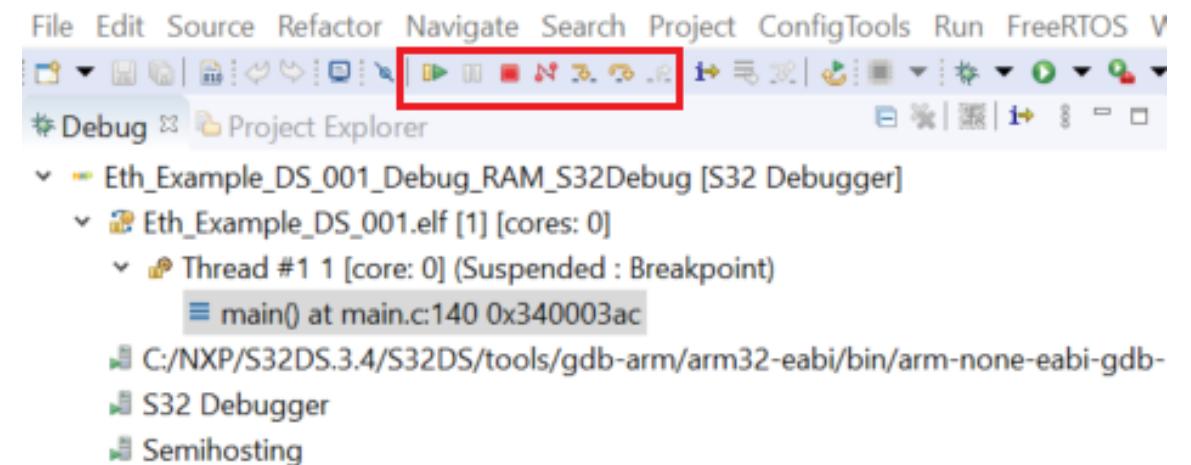
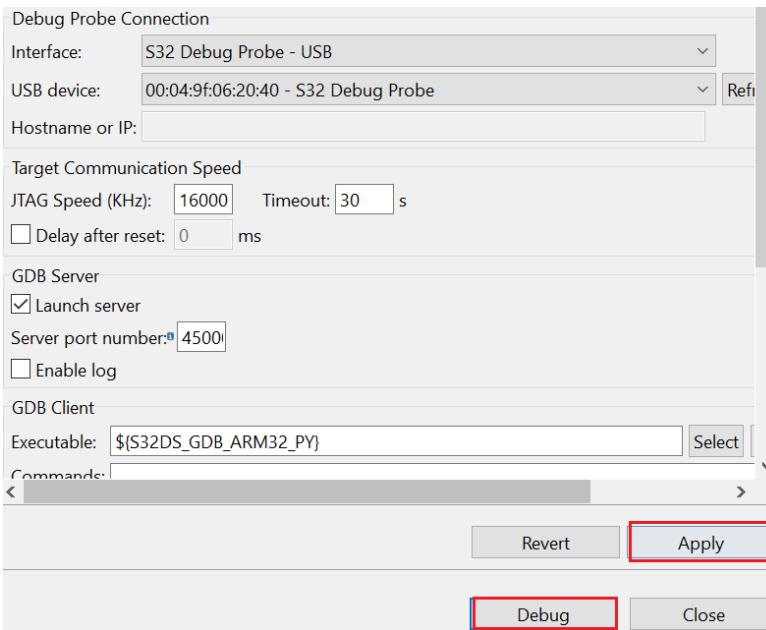
Debug configuration set:

- Click target project ,
- Select the target board
- Select target debugger



Hands on CAN: Debug and run

Click on “Apply”, then click on “Debug”. the perspective will jump to the Debug Perspective, and you can use the controls to control the program flow.

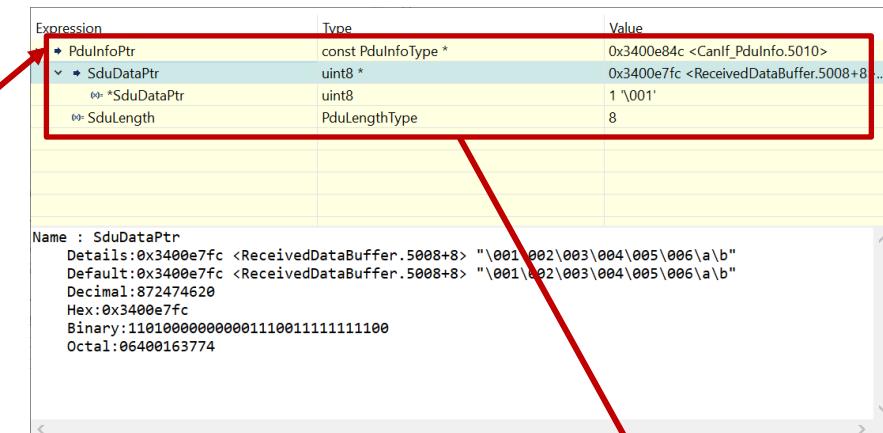


Hands on CAN: Test result

Through the modification, the CAN frame transmits from CAN0 to CAN1. the callback function **CanIf_RxIndication** capture the received CAN frame.

```
void CanIf_TxConfirmation(PduIdType CanTxPduId)
{
    CanIf_u8TxConfirmCnt++;
    CanIf_bTxFlag = TRUE;
}

void CanIf_RxIndication(const Can_HwType* Mailbox,
const PduInfoType* PduInfoPtr)
{
    CanIf_u8RxIndicationCnt++;
    CanIf_bRxFlag = TRUE;
}
```



The screenshot shows a debugger's memory dump window for address 0x3400e7fc. A red box highlights the byte at address 0x3400E800, which is 0560708. The dump table has columns for Address, 0 - 3, 4 - 7, 8 - B, and C - F.

Address	0 - 3	4 - 7	8 - B	C - F
3400E7F0	00000000	0F000802	00000000	01020304
3400E800	0560708	00000000	00000000	00000000
3400E810	00000000	00000000	00000000	00000000
3400E820	00000000	00000000	00000000	00000000
3400E830	00000000	00000000	00000000	08000000
3400E840	0F000000	00000000	00000000	FCE70034
3400E850	08000000	D0E00034	01000000	D0E00034
3400E860	00000000	409C0000	80BB0000	D5080200
3400E870	00000000	00000000	10000000	00000000
3400E880	0F000000	000A0000	0065CD1D	006CDC02
3400E890	006CDC02	005A6202	006CDC02	006CDC02



SECURE CONNECTIONS
FOR A SMARTER WORLD