

# Dual Port USB Type-C & PD Controller

## FUSB15201

The FUSB15201 is a highly integrated dual port USB Type-C and Power Delivery Controller optimized for automotive and industrial power sourcing applications. The FUSB15201 enables a complete solution for USB power sources through optimized hardware peripherals and complete open-source embedded firmware all in a compact solution. Maximizing total system power budgets is enabled through both hardware and firmware of the FUSB15201.

onsemi offers a complete open-source embedded firmware solution that draws inputs from various hardware peripherals and system level USB-PD identifiers to provide the most optimal power sharing across ports while staying within the total power budget.

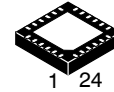
System designers can easily tailor this algorithm to meet the specific needs of their end application through an easy to use API for the embedded firmware. The FUSB15201 also provides a completely USB PD3.1 compliant solution with interoperability with leading mobile and computing devices in the market.

### Key Features

- Small Footprint Dual-port USB PD Controller Supporting the most Popular Peripherals
  - ◆ USB PD 3.1 & USB Type-C 2.1
  - ◆ I<sup>2</sup>C Master/Slave
  - ◆ Dual USB BC1.2 Provider Emulation
- Fully Programmable and Upgradable Open-source Firmware providing API for Customer Specific Device Policy Manager Development
- High Voltage Protection on CC and D+/- Pins
- Supports Firmware Upgrades via USB-C
- 10-bit ADC for Accurate Monitoring of VBUS, External Temperature and Voltages
- External Temperature Monitoring via NTC Resistors
- 24-Pin QFNW Package (4 mm x 4 mm, 0.5 mm Pitch)
- Grade 2 AEC-Q100 Qualified
- These are Pb-free Devices

### Typical Applications

- Automotive
- Power Outlets
- Wall Chargers



QFNW24 4x4, 0.5P  
CASE 484AU

### MARKING DIAGRAM



FUSB15201V = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device            | Package | Shipping <sup>†</sup> |
|-------------------|---------|-----------------------|
| FUSB15201VMNWTWG  | QFNW24  | 4,000 / Tape & Reel   |
| FUSB15201DVMNWTWG | QFNW24  | 4,000 / Tape & Reel   |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# FUSB15201

## Features

- **Arm Cortex-M0+:** A 32-bit core with flexible clocking up to 24 MHz
- **Memories:** A total of 132 kB of flash is available to store program code. 6 kB of SRAM program memory.
- **USB Type-C and PD:** Integrated USB PD PHY and Type-C termination/comparators supporting latest USB-IF specification.
- **Integrated VCONN Switch:** Provides the full 1.5 W power to interrogate cable eMarkers and power active cables.
- **BC1.2 Support:** Fully programmable USB BC1.2 interface is capable of presenting as CDP, DCP or SDP.
- **High Voltage Protection:** Robust USB-C connector interface with 28 V DC tolerant VBUS and CC. 20 V DC D+/- for FUSB15201 and 28 V DC D+/- for FUSB15201D
- **ADC:** Multi-channel 10-bit ADC for accurate monitoring of VBUS, external temperature and voltages.
- **I<sup>2</sup>C:** Serial communication port capable of acting as a host or device allowing control of external system peripherals by FUSB15201.
- **GPIOs:** Fully programmable I/Os with internal terminations. Configurable as input or output (CMOS or open-drain).
- **Programmable VBUS discharge:** Internal programmable resistors capable of discharging up to 100  $\mu$ F
- **Multiple Timers:** Four independent 32-bit timers are available: 2 General Purpose, 1 Watchdog, and 1 Wake-up / General Purpose
- **External NTC:** Integrated current sources are used in conjunction with the ADC to monitor a variety of NTC resistors.
- **Low Power Operation Modes:** Programmable sleep modes allowing device to minimize power usage as needed. Automatic USB-C detection and wake-up functionality from sleep modes.
- **Automotive Ready:** Grade 2 temperature range performance and AECQ-100 Qualified. QFN package with 0.5 mm pitch and wettable flank.

## FUSB15201 INTERNAL BLOCK DIAGRAM

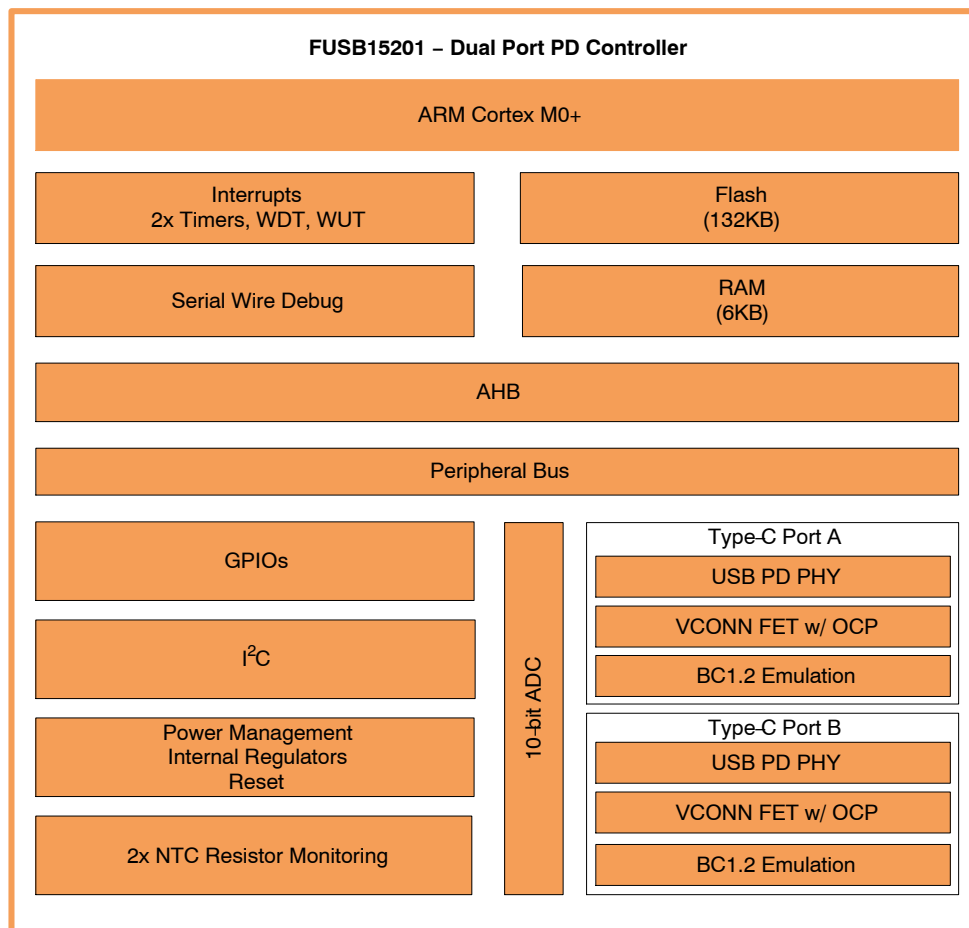
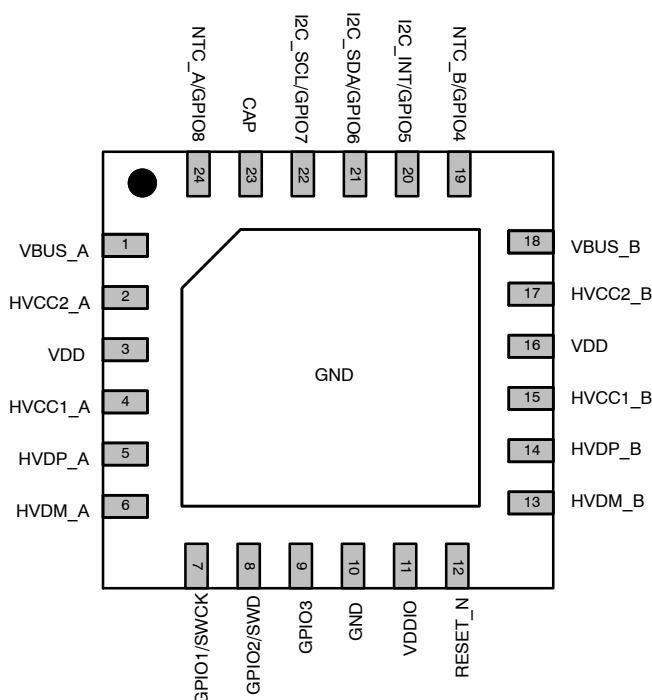


Figure 1. FUSB15201 Block Diagram

# FUSB15201



**Figure 2. Pin Diagram**

**Table 1. FUNCTION DESCRIPTION**

| Pin # | Name           | Port   | Description                                                        |
|-------|----------------|--------|--------------------------------------------------------------------|
| 1     | VBUS_A         | Analog | Port A VBUS. Monitoring Discharge (28 V)                           |
| 2     | HVCC2_A        | Analog | Port A High Voltage Configuration Channel 2 (28 V)                 |
| 3     | VDD            | Power  | Power Supply                                                       |
| 4     | HVCC1_A        | Analog | Port A High Voltage Configuration Channel 1 (28 V)                 |
| 5     | HVDP_A         | Analog | Port A High Voltage USB 2.0 D+ (FUSB15201: 20 V; FUSB15201D: 28 V) |
| 6     | HVDM_A         | Analog | Port A High Voltage USB 2.0 D- (FUSB15201: 20 V; FUSB15201D: 28 V) |
| 7     | GPIO1/SWCK     | PA1    | General Purpose I/O/ Serial Wire Debug Port Clock                  |
| 8     | GPIO2/SWD      | PA2    | General Purpose I/O/ Serial Wire Debug Port Data                   |
| 9     | GPIO3          | PA3    | General Purpose I/O                                                |
| 10    | GND            | Ground | Ground                                                             |
| 11    | VDDIO          | Power  | I/O Power Supply                                                   |
| 12    | RESET_N        | Input  | Reset                                                              |
| 13    | HVDM_B         | Analog | Port B High Voltage USB 2.0 D- (FUSB15201: 20 V; FUSB15201D: 28 V) |
| 14    | HVDP_B         | Analog | Port B High Voltage USB 2.0 D+ (FUSB15201: 20 V; FUSB15201D: 28 V) |
| 15    | HVCC1_B        | Analog | Port B High Voltage Configuration Channel 1 (28 V)                 |
| 16    | VDD            | Power  | Power Supply                                                       |
| 17    | HVCC2_B        | Analog | Port B High Voltage Configuration Channel 2 (28 V)                 |
| 18    | VBUS_B         | Analog | Port B VBUS. Monitoring Discharge (28 V)                           |
| 19    | NTC_B/GPIO4    | PA4    | Port B External NTC sense Pin / General Purpose I/O                |
| 20    | I2C_INT1/GPIO5 | PA5    | I2C Port Interrupt / General Purpose I/O                           |
| 21    | I2C_SDA/GPIO6  | PA6    | I2C Port Data / General Purpose I/O                                |
| 22    | I2C_SCL/GPIO7  | PA7    | I2C Port Clock / General Purpose I/O                               |
| 23    | CAP            | Analog | 1.5V capacitor                                                     |
| 24    | NTC_A/GPIO8    | PA8    | Port A External NTC sense Pin / General Purpose I/O                |
| DAP   | GND            | Ground | Ground                                                             |

# FUSB15201

## APPLICATIONS DIAGRAM

The figure below shows a typical dual port automotive source application. The FUSB15201 communicates to the DC-DC controllers via integrated I<sup>2</sup>C host peripheral.

External NTC resistors monitor temperature at each port and is used for over-temperature protection or to dynamically change power capabilities.

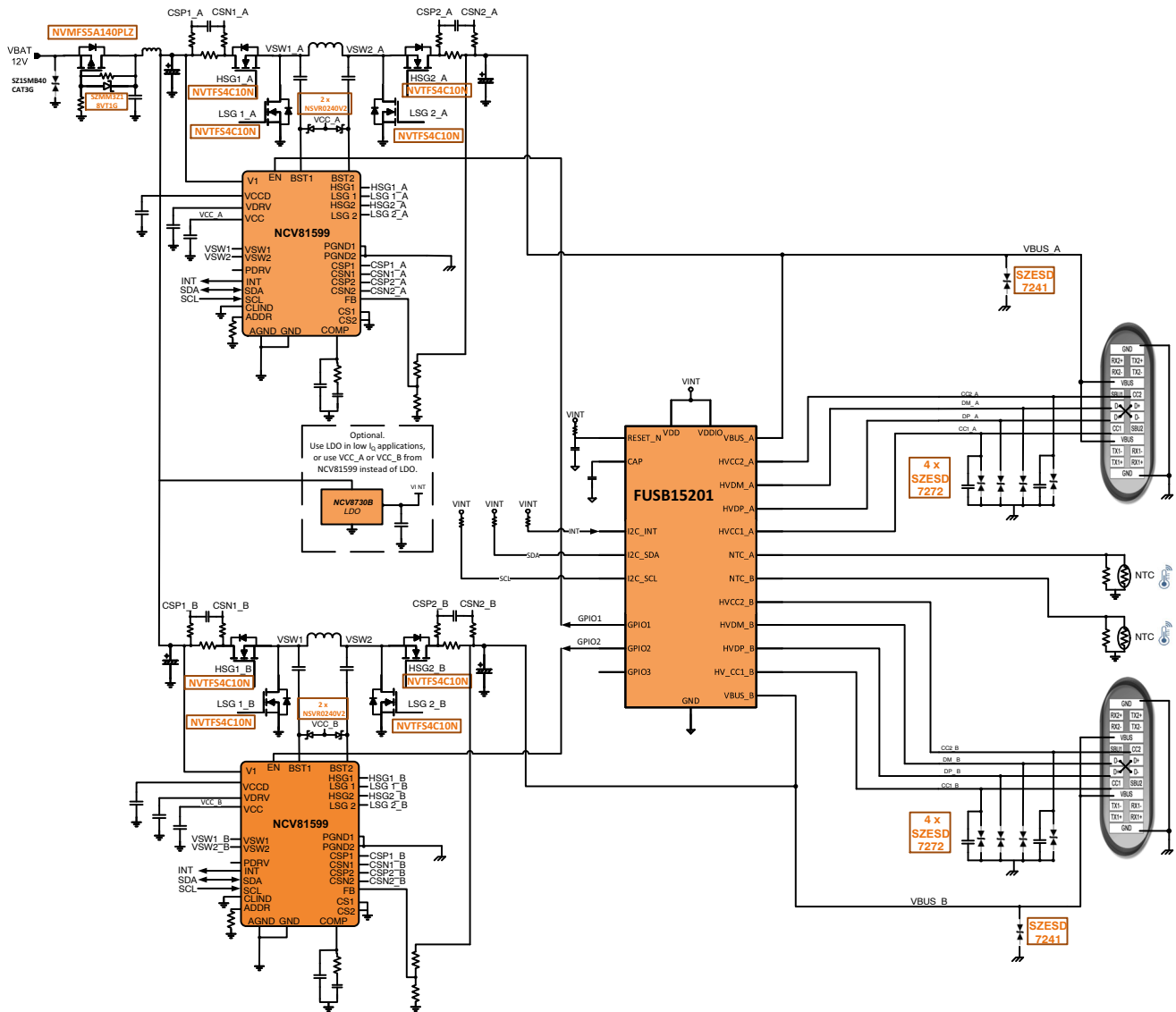


Figure 3. Automotive Application Schematic

# FUSB15201

## ELECTRICAL SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Notes 1, 2, 3)

| Symbol                 | Parameter                                              | Minimum | Maximum | Unit |
|------------------------|--------------------------------------------------------|---------|---------|------|
| VBUS                   | VBUS Pin Voltage                                       | -0.3    | 28      | V    |
| V <sub>CONNECTOR</sub> | HVCC1, HVCC2 Connector Pins                            | -0.3    | 28      | V    |
| V <sub>USB</sub>       | HVDP, HVDM Connector Pins (FUSB15201)                  | -0.3    | 20      | V    |
|                        | HVDP, HVDM Connector Pins (FUSB15201D)                 | -0.3    | 28      | V    |
| VIO                    | I/O Voltage                                            | -0.5    | 6.0     | V    |
| VDD                    | Supply Voltage                                         | -0.5    | 6.0     | V    |
| VDDIO                  | VDDIO Supply                                           | -0.3    | 6.0     | V    |
| VCAP                   | CAP Pin                                                | -0.5    | 2.0     | V    |
| T <sub>J</sub>         | Junction Temperature                                   | -40     | 150     | °C   |
| T <sub>STG</sub>       | Storage Temperature                                    | -40     | 150     | °C   |
| TL                     | Lead Temperature (Soldering, 10 Seconds)               |         | 260     | °C   |
| ESD <sub>HBM</sub>     | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 (Note 3) | 2       |         | kV   |
| ESD <sub>CDM</sub>     | Charged Device Model, JEDEC22-C101 (Note 3)            | 750     |         | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND Pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS-001-2012 and JEDEC 22-C101.

**Table 3. RECOMMENDED ESD DEVICES**

| Function                  | Manufacturer | Part Number |
|---------------------------|--------------|-------------|
| Type-C Connector Pins ESD | onsemi       | TBD         |

**Table 4. THERMAL RATINGS** (Note 4)

| Symbol        | Parameter                              | Min | Typ | Max | Unit |
|---------------|----------------------------------------|-----|-----|-----|------|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance |     | 57  |     | °C/W |

4. T<sub>A</sub> = 25°C unless otherwise specified with JEDEC 2S2P board with no thermal vias.

**Table 5. OPERATING RATINGS**

| Symbol             | Parameter                     | Min | Typ | Max   | Unit |
|--------------------|-------------------------------|-----|-----|-------|------|
| V <sub>DD</sub>    | Supply Voltage Range          | 3.0 | 3.3 | 5.5   | V    |
| V <sub>BUS</sub>   | VBUS Voltage                  | 3.1 |     | 22.05 | V    |
| V <sub>DDIO</sub>  | I/O Supply Voltage            | 1.7 |     | 5.5   | V    |
| V <sub>HVCCx</sub> | Communication Channel Pins    | 0   |     | 5.5   | V    |
| V <sub>HVUSB</sub> | HVDM, HVDP Pins               | 0   |     | 3.6   | V    |
| V <sub>IO</sub>    | GPIO, I <sup>2</sup> C, RESET | 0   |     | 5.5   | V    |
| T <sub>A</sub>     | Operating Ambient Temperature | -40 |     | +105  | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# FUSB15201

**Table 6. ELECTRICAL CHARACTERISTICS**

Minimum and maximum values are at  $V_{DD} = 2.8 \text{ V}$  to  $5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  unless otherwise noted.  
Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V}$

| TYPE-C AND PD SECTION |                                                                                                                         |            |      |       |      |               |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------|------------|------|-------|------|---------------|
| USB PD PHY            |                                                                                                                         |            |      |       |      |               |
| TRANSMITTER           |                                                                                                                         |            |      |       |      |               |
| Symbol                | Parameter                                                                                                               | Conditions | Min  | Typ   | Max  | Units         |
| UI                    | Unit Interval                                                                                                           |            | 3.03 | 3.33  | 3.7  | $\mu\text{s}$ |
| pBitRate              | Maximum difference between the bit-rate during the payload and last 32 bits of preamble                                 |            |      |       | 0.25 | %             |
| tEndDriveBMC          | Time to cease driving the line after the end of the last bit of the Frame                                               |            |      |       | 23   | $\mu\text{s}$ |
| tHoldLowBMC           | Time to cease driving the line after the final high-to-low transition                                                   |            | 1    |       |      | $\mu\text{s}$ |
| tInterFrameGap        | Any PD transmission cannot be sent out before a dead time of at least tInterFrameGap from receiving or sending a packet |            | 25   |       |      | $\mu\text{s}$ |
| tFall                 | Fall Time                                                                                                               |            | 300  |       |      | ns            |
| tRise                 | Rise Time                                                                                                               |            | 300  |       |      | ns            |
| tStartDrive           | Time before the start of the first bit of the preamble when the transmitter shall start driving the line                |            | -1   |       | 1    | $\mu\text{s}$ |
| vSwing                | BMC voltage swing                                                                                                       |            | 1.05 | 1.125 | 1.2  | V             |
| zDriver               | TX output impedance at 750 kHz with an external 220 pF or equivalent load                                               |            | 33   |       | 75   | $\Omega$      |

## RECEIVER

|                   |                                                                                           |                                                        |     |     |     |               |
|-------------------|-------------------------------------------------------------------------------------------|--------------------------------------------------------|-----|-----|-----|---------------|
| cReceiver         | Receiver capacitance when driver isn't turned on                                          | $V_{rms}=0.371$ ; $V_{dc}=0.5 \text{ V}$ ; Freq.=1 MHz |     | 75  |     | pF            |
| tRxFilter         | Rx bandwidth limiting filter                                                              |                                                        | 100 |     |     | ns            |
| tTransitionWindow | Time window for detecting non-idle                                                        |                                                        | 12  |     | 20  | $\mu\text{s}$ |
| vFRSwapCableTx    | The Fast Role Swap Request has to be below this voltage threshold to be detected.         |                                                        | 490 | 520 | 550 | mV            |
| zBmcRx            | Receiver Input Impedance (cannot be tested but can be simulated and guaranteed by design) |                                                        | 1   |     |     | M $\Omega$    |

## TYPE-C FRONT END

|                 |                                                           |                                                              |      |      |      |               |
|-----------------|-----------------------------------------------------------|--------------------------------------------------------------|------|------|------|---------------|
| $R_{VBUS-LEAK}$ | VBUS Leakage Impedance to ground when VBUS is not sourced |                                                              | 72.4 |      |      | k $\Omega$    |
| $I_{80\_CCX}$   | SRC 80 $\mu\text{A}$ CC current (Default)                 |                                                              | 64   | 80   | 96   | $\mu\text{A}$ |
| $I_{180\_CCX}$  | SRC 180 $\mu\text{A}$ CC current (1.5 A)                  |                                                              | 166  | 180  | 194  | $\mu\text{A}$ |
| $I_{330\_CCX}$  | SRC 330 $\mu\text{A}$ CC current (3 A)                    |                                                              | 304  | 330  | 356  | $\mu\text{A}$ |
| $R_{DEVICE}$    | Device pull-down resistance                               |                                                              | 4.6  | 5.1  | 5.6  | k $\Omega$    |
| $R_A$           | Powered Cable Termination                                 |                                                              | 800  |      | 1200 | $\Omega$      |
| zOPEN           | CC resistance for disabled state, when Vdd is valid       |                                                              | 126  |      |      | k $\Omega$    |
| $R_{SW\_CCx}$   | Rdson for VDD to CC1 or VDD to CC2                        | $I_{SW\_CCx} = 0$ to 600 mA, $V_{CONN\_OCP} > 80 \text{ mA}$ |      | 0.85 | 1.8  | $\Omega$      |

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**Table 6. ELECTRICAL CHARACTERISTICS** (continued)

Minimum and maximum values are at  $V_{DD} = 2.8 \text{ V}$  to  $5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V}$

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------|------------|-----|-----|-----|-------|
|--------|-----------|------------|-----|-----|-----|-------|

## TYPE-C FRONT END

|                         |                                                                                                         |                                                                              |      |      |      |          |
|-------------------------|---------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|------|------|------|----------|
| $R_{SW\_CCx\_LOW\_OCP}$ | Low OCP setting $R_{dson}$ for VDD to CC1 or VDD to CC2                                                 | $I_{SW\_CCx} = 0$ to $80 \text{ mA}$ ,<br>$V_{CONN\_OCP} \leq 80 \text{ mA}$ |      | 2.7  | 5    | $\Omega$ |
| $I_{SW\_CCx}$           | Over Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range | $V_{CONN\_OCP} = 800 \text{ mA}$                                             | 600  | 800  | 1000 | mA       |
| $V_{CCx\_OVP}$          | CC1/2 Over-Voltage Protection                                                                           |                                                                              | 5.6  |      | 6.0  | V        |
| $vRdSRCUSB$             | Source attach threshold for CC Pin at default current                                                   |                                                                              | 1.5  | 1.6  | 1.65 | V        |
| $vRdSRC1.5$             | Source attach threshold for CC Pin at 1.5 A current                                                     |                                                                              | 1.5  | 1.6  | 1.65 | V        |
| $vRdSRC3.0$             | Source attach threshold for CC Pin at 3 A current                                                       |                                                                              | 2.45 | 2.6  | 2.75 | V        |
| $vRaSRCUSB$             | Source $R_a$ threshold for CC Pin at default current                                                    |                                                                              | 0.15 | 0.2  | 0.25 | V        |
| $vRaSRC1.5$             | Source $R_a$ threshold for CC Pin at 1.5 A current                                                      |                                                                              | 0.35 | 0.4  | 0.45 | V        |
| $vRaSRC3.0$             | Source $R_a$ threshold for CC Pin at 3 A current                                                        |                                                                              | 0.75 | 0.8  | 0.85 | V        |
| $vRdSNKUSB$             | Attach threshold for CC Pin SNK (default current)                                                       |                                                                              | 0.61 | 0.66 | 0.7  | V        |
| $vRdSNK1.5$             | Attach threshold for CC Pin SNK (1.5 A current)                                                         |                                                                              | 1.16 | 1.23 | 1.31 | V        |
| $vRdSNK3.0$             | Attach threshold for CC Pin SNK (3 A current)                                                           |                                                                              | 2.04 | 2.11 | 2.18 | V        |
| $vRaSNK$                | Attach threshold for CC Pin SRC or SNK                                                                  |                                                                              | 0.15 | 0.2  | 0.25 | V        |
| $V_{Safe0V}$            | Safe Operating Voltage at 0 V                                                                           |                                                                              | 0.6  |      | 0.8  | V        |

## VBUS DISCHARGE

|                      |                                                    |                                            |      |      |      |            |
|----------------------|----------------------------------------------------|--------------------------------------------|------|------|------|------------|
| $R_{VBUS\_DISCH\ 0}$ | Pull-down Resistance applied to VBUS when selected | $VBUS = 0.8 \text{ V}$ to $21.5 \text{ V}$ | 315  | 450  | 585  | $\Omega$   |
| $R_{VBUS\_DISCH\ 1}$ |                                                    | $VBUS = 0.8 \text{ V}$ to $21.5 \text{ V}$ | 420  | 600  | 780  |            |
| $R_{VBUS\_DISCH\ 2}$ |                                                    | $VBUS = 0.8 \text{ V}$ to $21.5 \text{ V}$ | 525  | 750  | 975  |            |
| $R_{VBUS\_DISCH\ 3}$ |                                                    | $VBUS = 0.8 \text{ V}$ to $21.5 \text{ V}$ | 700  | 1000 | 1300 |            |
| $R_{VBUS\_DISCH\ 4}$ |                                                    | $VBUS = 0.8 \text{ V}$ to $21.5 \text{ V}$ | 1400 | 2000 | 2600 |            |
| $R_{VBUS\_DISCH\ 5}$ |                                                    | $VBUS = 0.8 \text{ V}$ to $21.5 \text{ V}$ | 4.20 | 6.00 | 7.80 | k $\Omega$ |

## CURRENT CONSUMPTION

|                        |                                        |                                                                                                                                                        |  |     |    |               |
|------------------------|----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|--|-----|----|---------------|
| $I_{SLEEP-UNATTACHED}$ | Current consumption when in deep sleep | $V_{DD} = V_{DDIO} = 3.0$ to $5.5 \text{ V}$ $VBUS = 0 \text{ V}$ ;<br>Not Type-C attached,<br>DRP Toggling; LSOSC enabled; BC1.2 disabled             |  |     | 75 | $\mu\text{A}$ |
| $I_{SLEEP}$            | Sleep Current                          | $V_{DD} = V_{DDIO} = 3.0$ to $5.5 \text{ V}$ $VBUS = 0 \text{ V}$ ;<br>No $I^2C$ traffic, LSOSC running; PD Peripheral and ADC enabled. No PD traffic. |  | 700 |    | $\mu\text{A}$ |

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**Table 6. ELECTRICAL CHARACTERISTICS** (continued)

Minimum and maximum values are at  $V_{DD} = 2.8 \text{ V}$  to  $5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V}$

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------|------------|-----|-----|-----|-------|
|--------|-----------|------------|-----|-----|-----|-------|

## CURRENT CONSUMPTION

|                 |                      |                                                                                      |  |     |  |    |
|-----------------|----------------------|--------------------------------------------------------------------------------------|--|-----|--|----|
| $I_{PD-ACTIVE}$ | Port with PD traffic | Active and communicating via USB PD transmitting and receiving packets on both ports |  | 4.0 |  | mA |
|-----------------|----------------------|--------------------------------------------------------------------------------------|--|-----|--|----|

## PMU

|                   |                                                                             |              |     |  |     |   |
|-------------------|-----------------------------------------------------------------------------|--------------|-----|--|-----|---|
| $V_{VDD\_POR}$    | POR Trip point                                                              | VDD Rising   | 1.0 |  | 2.4 | V |
| $V_{VDD\_GOOD}$   | Minimum VDD level for enabling device                                       | VDD Rising   | 3.0 |  |     |   |
| $V_{VDDIO\_GOOD}$ | VDDIO Detection Threshold used in asserting PMU_STS when VDDIO is above it. | VDDIO Rising |     |  | 1.0 | V |
| $V_{VDD\_BRWN}$   | VDD Brown Out Threshold                                                     | VDD Falling  | 2.6 |  | 3.0 | V |

## CLOCKS

|               |                                                  |  |      |     |      |     |
|---------------|--------------------------------------------------|--|------|-----|------|-----|
| $F_{LS\_CLK}$ | Low Speed Clock for Idle, Type-C Attach          |  | 114  | 120 | 126  | kHz |
| $F_{HS\_CLK}$ | Internal clock for Active Core and full function |  | 22.8 | 24  | 25.2 | MHz |

## INTERNAL TEMPERATURE PROTECTION

|            |                                                     |                      |  |     |  |                  |
|------------|-----------------------------------------------------|----------------------|--|-----|--|------------------|
| $T_{SHUT}$ | Temperature for internal temperature protection     | VDD = 3.0 V to 5.5 V |  | 145 |  | $^\circ\text{C}$ |
| $T_{HYS}$  | Temp hysteresis for internal temperature protection | VDD = 3.0 V to 5.5 V |  | 10  |  | $^\circ\text{C}$ |

## EXTERNAL TEMPERATURE MEASUREMENT

|            |                        |  |    |    |    |               |
|------------|------------------------|--|----|----|----|---------------|
| $I_{NTCA}$ | Current Source on NTCA |  | 55 | 60 | 65 | $\mu\text{A}$ |
| $I_{NTCB}$ | Current Source on NTCB |  | 55 | 60 | 65 | $\mu\text{A}$ |

## BC1.2 DETECTION

|                |                                       |                                                                       |      |      |      |                  |
|----------------|---------------------------------------|-----------------------------------------------------------------------|------|------|------|------------------|
| $R_{DCP}$      | DCP Emulation Resistance              | $V_{D+}/D- = 0 \text{ V}$ , $1.0 \text{ V}$ , $I_{ON} = 2 \text{ mA}$ |      | 80   | 180  | $\Omega$         |
| $R_{Dx\_DWN}$  | DP/DM pull down resistance            | $V_{D+}/- = 0 \text{ V} - 3.6 \text{ V}$                              | 16   | 19.5 | 23   | $\text{k}\Omega$ |
| $I_{DP\_SRC}$  | DCD Source Current                    | VDD = 3.0 V to 5.5 V                                                  | 7    | 10   | 13   | $\mu\text{A}$    |
| $I_{Dx\_SNK}$  | Sink Current to Dx                    | VDD = 3.0 V to 5.5 V                                                  | 25   | 75   | 175  | $\mu\text{A}$    |
| $V_{DIV}$      | Divider Mode Output Voltage           | VDD = 3.0 V to 5.5 V                                                  | 2.65 | 2.75 | 2.85 | V                |
| $R_{DIVP}$     | Divider Mode resistance on DP         | $5\mu\text{A}$ pulled out of DP                                       | 24   | 30   | 36   | $\text{k}\Omega$ |
| $R_{DIVM}$     | Divider Mode resistance on DM         | $5\mu\text{A}$ pulled out of DM                                       | 24   | 30   | 36   | $\text{k}\Omega$ |
| $R_{DAT\_LKG}$ | Resistor weak pull-down on D+ and D-  | $V_{(sw)} = 0 \text{ V}$ to $3.6 \text{ V}$                           | 300  | 700  | 1100 | $\text{k}\Omega$ |
| $V_{Dx\_SRC}$  | Source Voltage                        | VDD = 3.0 V to 5.5 V                                                  | 0.5  | 0.6  | 0.7  | V                |
| $V_{Dx\_OVP}$  | D+/D- Over-Voltage Protection         |                                                                       | 4.4  | 4.55 | 4.7  | V                |
| $R_{PU\_MOS}$  | Pull-Up Moisture Detection Resistor   |                                                                       | 288  | 320  | 352  | $\text{k}\Omega$ |
| $V_{SRC\_MOS}$ | Voltage Source for Moisture Detection |                                                                       | 0.9  | 1.0  | 1.1  | V                |

## SERIAL WIRE DEBUG INTERFACE

|              |                                         |                         |  |  |    |     |
|--------------|-----------------------------------------|-------------------------|--|--|----|-----|
| $F_{SWDCLK}$ | Serial Wire Debug Input Clock Frequency | Core frequency = 24 MHz |  |  | 10 | MHz |
|--------------|-----------------------------------------|-------------------------|--|--|----|-----|

# FUSB15201

**Table 6. ELECTRICAL CHARACTERISTICS** (continued)

Minimum and maximum values are at  $V_{DD} = 2.8 \text{ V}$  to  $5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V}$

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------|------------|-----|-----|-----|-------|
|--------|-----------|------------|-----|-----|-----|-------|

## SERIAL WIRE DEBUG INTERFACE

|                  |                                            |                                                                                                   |                            |     |                       |               |
|------------------|--------------------------------------------|---------------------------------------------------------------------------------------------------|----------------------------|-----|-----------------------|---------------|
| $T_{SWDI\_SET}$  | Serial Wire Debug Data Setup timing        |                                                                                                   | $0.25 \times (1/SWCLK)$    |     |                       | ns            |
| $T_{SWDI\_HOLD}$ | Serial Wire Debug Data Hold Timing         |                                                                                                   | $0.25 \times (1/SWCLK)$    |     |                       | ns            |
| $V_{IH-SWD}$     | Serial Wire Debug Input voltage threshold  | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$                                                     | $0.7 \times V_{DDIO}$      |     |                       | V             |
| $V_{IL-SWD}$     |                                            | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$                                                     |                            |     | $0.3 \times V_{DDIO}$ |               |
| $V_{HYS-SWD}$    | Serial Wire Debug Input Voltage Hysteresis | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$                                                     |                            | 300 |                       | mV            |
| $I_{LKG-SWD}$    | Serial Wire Debug Input Leakage            | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>Input Voltage $0 \text{ V}$ to $5.5 \text{ V}$ | -10                        |     | +10                   | $\mu\text{A}$ |
| $V_{OH-SWD}$     | Serial Wire Debug Output Voltage High      | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$I_{out} = -2 \text{ mA}$                      | $V_{DDIO} - 0.5 \text{ V}$ |     |                       | V             |
| $V_{OL-SWD}$     | Serial Wire Debug Output Voltage Low       | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$I_{out} = +4 \text{ mA}$                      |                            |     | $0.4 \text{ V}$       | V             |

## RESET

|              |                                  |                                             |                     |     |                     |               |
|--------------|----------------------------------|---------------------------------------------|---------------------|-----|---------------------|---------------|
| RESET_N_VIL1 | Low level input voltage          | $V_{DD} = 2.8 \text{ V}$ to $5.5 \text{ V}$ |                     |     | $0.3 \times V_{DD}$ | V             |
| RESET_N_VIH1 | High Level Input Voltage         | $V_{DD} = 2.8 \text{ V}$ to $5.5 \text{ V}$ | $0.7 \times V_{DD}$ |     |                     | V             |
| RESET_N_RPU  | Internal Pull-Up Resistor to VDD |                                             |                     | 100 |                     | $k\Omega$     |
| RESET_N_ILKG | Input Leakage                    |                                             | -120                |     |                     | $\mu\text{A}$ |

## GPIO

|                |                                     |                                                                                                                           |                       |     |                       |               |
|----------------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|-----------------------|---------------|
| $V_{IH-GPIO}$  | High Level Input Voltage            | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$                                                                             | $0.7 \times V_{DDIO}$ |     |                       | V             |
| $V_{IL-GPIO}$  | Low level input voltage             | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$                                                                             |                       |     | $0.3 \times V_{DDIO}$ | V             |
| $V_{OH-GPIO}$  | Output High Voltage                 | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$I_{out} = -2 \text{ mA}$                                              | $V_{DDIO} - 0.5$      |     |                       | V             |
| $V_{OL-GPIO}$  | Output Low Voltage                  | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$I_{out} = +4 \text{ mA}$                                              |                       |     | 0.4                   | V             |
| $V_{OH-NTC}$   | Output High Voltage for PA4 and PA8 | $V_{DD} = 2.8 \text{ V}$ to $5.5 \text{ V}$ ,<br>$I_{out} = -2 \text{ mA}$                                                | $V_{DD} - 0.5$        |     |                       | V             |
| $V_{OL-NTC}$   | Output Low Voltage for PA4 and PA8  | $V_{DD} = 2.8 \text{ V}$ to $5.5 \text{ V}$ ,<br>$I_{out} = +4 \text{ mA}$                                                |                       |     | 0.4                   | V             |
| $V_{HYS-GPIO}$ | Input Hysteresis                    | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>3.6 V Typ                                                              |                       | 300 |                       | mV            |
| $I_{IN-GPIO}$  | Input Leakage                       | $V_{DDIO} = 1.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>Input Voltage $0 \text{ V}$ to $5.5 \text{ V}$                         | -5                    |     | 5                     | $\mu\text{A}$ |
| $I_{OFF-GPIO}$ | Off Input Leakage                   | $V_{DDIO} = 0 \text{ V}$ ,<br>$V_{DD} = 0 \text{ V}$ to $5.5 \text{ V}$<br>Input Voltage $0 \text{ V}$ to $5.5 \text{ V}$ | -5                    |     | 5                     | $\mu\text{A}$ |
| $R_{PD-GPIO}$  | Pull-Down resistance                | PORT_PD $x$ = 1                                                                                                           |                       | 100 |                       | $k\Omega$     |
| $R_{PU-GPIO}$  | Pull-up resistance                  | PORT_PU $x$ = 1                                                                                                           |                       | 100 |                       | $k\Omega$     |
| $C_{GPIO}$     | Pin Capacitance                     |                                                                                                                           |                       | 5   |                       | pF            |

## I<sup>2</sup>C I/O

|              |                                     |                                                                     |     |  |    |               |
|--------------|-------------------------------------|---------------------------------------------------------------------|-----|--|----|---------------|
| $I_{CCTI2C}$ | VDD current when SDA or SCL is HIGH | $V_{DD} = 2.8 \text{ V}$ to $5.5$ ,<br>$V_{IN} = 1.8 \text{ V}$     | -10 |  | 10 | $\mu\text{A}$ |
| $I_{I2C}$    | Input Current of SDA and SCL Pins   | $V_{DD} = 2.8 \text{ V}$ to $5.5$ ,<br>$V_I = 0$ to $5.5 \text{ V}$ | -10 |  | 10 | $\mu\text{A}$ |
| $V_{IH-I2C}$ | High-Level Input Voltage            | $V_{DD} = 2.8 \text{ V}$ to $5.5 \text{ V}$                         | 1.2 |  |    | V             |

# FUSB15201

**Table 6. ELECTRICAL CHARACTERISTICS** (continued)

Minimum and maximum values are at  $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +105^\circ\text{C}$  unless otherwise noted.  
Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V}$

| Symbol                    | Parameter                                                         | Conditions                                                                           | Min | Typ | Max | Units |
|---------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------------------------|-----|-----|-----|-------|
| <b>I<sup>2</sup>C I/O</b> |                                                                   |                                                                                      |     |     |     |       |
| $V_{IL-I2C}$              | Low-Level Input Voltage                                           | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           |     |     | 0.4 | V     |
| $V_{OL1-I2C}$             | Low-Level Output Voltage at 3mA Sink Current (Open-Drain)         | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           | 0   |     | 0.3 | V     |
| $V_{OL2-I2C}$             | Low-Level Output Voltage at 2mA Sink Current (Open-Drain)         | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           | 0   |     | 0.3 | V     |
| $V_{HYS-I2C}$             | Hysteresis of Schmitt Trigger Inputs                              | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           | 0.1 | 0.2 |     | V     |
| $I_{OLSDA}$               | Low-Level Output Current (Open-Drain)                             | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$ ,<br>$V_{OL} = 0.4 \text{ V}$<br>(Note 5) | 20  |     |     | mA    |
| $V_{OL\_INT}$             | INT_N Output Low Voltage                                          | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$ ,<br>$I_{OL} = 4 \text{ mA}$              |     |     | 0.4 | V     |
| $C_{I-I2C}$               | Capacitance for Each I/O Pin                                      | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           |     | 5   |     | pF    |
| $t_{SP}$                  | Pulse Width of Spikes that Must Be Suppressed by the Input Filter |                                                                                      | 0   |     | 50  | ns    |
| $V_{IH\_INT}$             | High-Level Input Voltage                                          | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           | 1.2 |     |     | V     |
| $V_{IL\_INT}$             | Low-Level Input Voltage                                           | $V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}$                                           |     |     | 0.4 | V     |

## FLASH

|          |                  |                         |        |  |  |                           |
|----------|------------------|-------------------------|--------|--|--|---------------------------|
| NEND     | Sector Endurance |                         | 20,000 |  |  | Erase/<br>write<br>cycles |
| $T_{DR}$ | Data Retention   | $T = 25^\circ\text{C}$  | 100    |  |  | years                     |
|          |                  | $T = 105^\circ\text{C}$ | 20     |  |  | years                     |
|          |                  | $T = 125^\circ\text{C}$ | 10     |  |  | years                     |

5. (20 mA guaranteed over  $-40^\circ\text{C to } 85^\circ\text{C}$ )

# FUSB15201

## Arm Cortex-M0+ Processor

The FUSB15201 integrates an Arm Cortex-M0+ processor with Nested Vector Interrupt Controller (NVIC), Wake-up Interrupt Controller (WIC), and Debug Access Port (DAP). The processor uses the Thumb instruction set and is optimized for high performance with reduced code size and low power operation. The Arm Cortex-M0+ efficiently handles multiple parallel peripherals and has integrated sleep modes. Test and debug capability is enhanced with the Arm Serial Wire Debug Port.

The Arm implementation in the FUSB15201 includes a 132 kB Flash RAM and 6 kB of SRAM.

The MCU, Memory and DAP are interconnected using the AMBA (Advanced Microcontroller Bus Architecture) AHB-Lite interface and peripherals are connected to the AHB via APB interface (Advanced Peripheral Bus).

In addition to the base Arm Cortex-M0+ processor interrupts, the FUSB15201 implements multiple external

source interrupts for peripheral devices. A powerful nested, pre-emptive and priority based interrupt handling system assures timely and flexible response to external events.

Low power features on FUSB15201 include the WIC, adjustable clock rates, and different software controlled power modes to maximize opportunities to save power in the final application.

## Power Management Unit

The Power Management Unit (PMU) provides appropriate power to all the blocks in the FUSB15201.

The FUSB15201 power management unit prevents system brown-outs in case VDD voltage dips below the specified minimum voltage required for reliable operation. Firmware monitors the power supply and safely shuts down the system as needed.

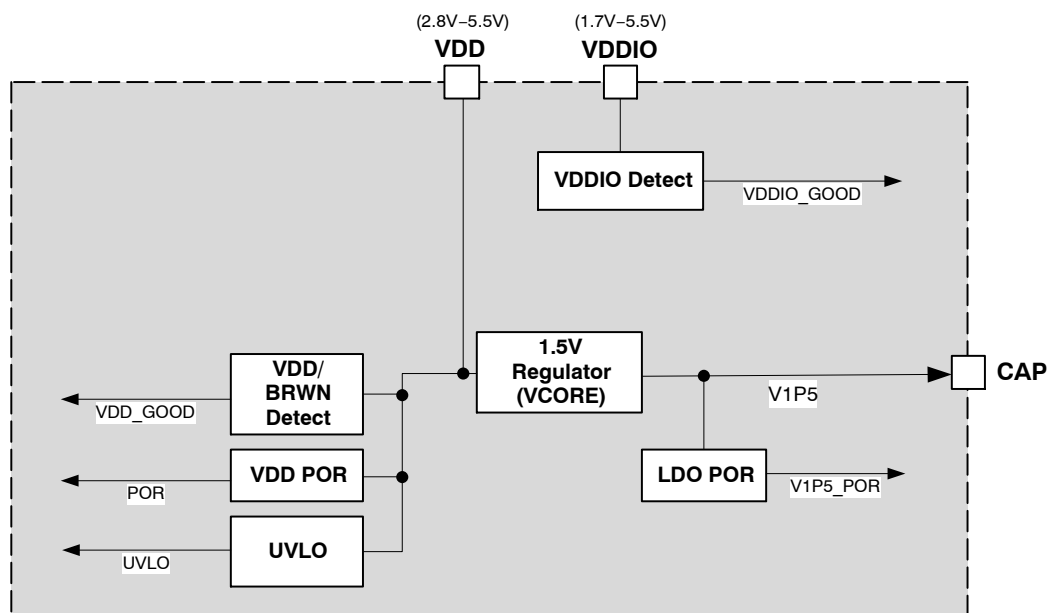


Figure 4. FUSB15201 PMU

## Reset Sources

The FUSB15201 has various sources of reset including:

- **Internal Power-On Reset (VDD\_POR)** – The VDD\_POR reset asserts when the regulated supply is below threshold levels for proper operation. The VDD\_POR resets the entire chip including core, debug port, peripherals, wakeup timer, and watchdog.
- **Software Issued Reset** – The software reset can be called by writing to a given register in the Cortex address space. It is typically called on exit from a processor exception. Software reset resets the entire chip including core, peripherals, wakeup timer, and watchdog.
- **Watchdog Timer Reset** – The watchdog timer reset is caused by the watchdog timeout and is used to prevent errant software from locking up the device. The watchdog reset resets the entire chip including core, debug port, peripherals, and watchdog. The watchdog timer is disabled upon power up and must be enabled by software. The watchdog is not paused when the debugger halts the processor.
- **External Pin Reset** – The external reset is under user control with the external RESET\_N Pin. External pin reset resets the entire chip including core, debug port, peripherals, wakeup timer, and watchdog.

## Power and Sleep Behavior

The FUSB15201 has been optimized to conserve power by utilizing peripheral interrupts and hardware autonomy. The device can be configured via firmware to enter low power states, disable unneeded peripherals and scale clock frequencies based on different application needs.

The Type-C block is designed to function at the lowest power states and will automatically wake when a Type-C attach is detected. This minimizes total power consumption when no device is attached.

## Clock Sources

FUSB15201's implements a dual oscillator architecture to minimize power consumption.

- A 24 MHz internal RC oscillator to enable full functionality.
- A 120 kHz internal RC oscillator that can be used for very low power sleep modes.

## TIMERS

### 32-bit General Purpose Timers (TIM0/1)

There are two 32-bit down-counters that generate interrupts and status when the counter reaches 0. The timing resolution depends on the programmable clock source and pre-scale ratios.

### 32-bit Wake-up Timer (WUT)

The main purpose of the wakeup timer is to facilitate scheduled exit from low power modes. It can also be used for general purpose event timing.

### 32-bit Watchdog Timer (WDT)

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog timer is disabled by default and must be enabled through software.

The watchdog is protected with a lock mechanism to prevent rogue software from disabling the watchdog functionality. A special value has to be written to the lock register to access watchdog control. The watchdog timer is clocked from the same oscillator as the core, which can be LS\_CLK or HS\_CLK.

## Serial Wire Debug Interface (SWD)

The Arm M0+ implementation includes a Debug Access Port (DAP). The debug mode implementation includes 4 hardware breakpoints and 2 hardware watch points.

The Debug Access Port interface implementation is the Arm Serial Wire Debug Port (SW-DAP) connected to Pins SWCLK and SWDIO. The Serial Wire Debug Port Interface uses a single bi-directional data connection. Each operation consists of three phases: Packet request, Acknowledge response, and Data transfer phase. Use any Serial Wire Debug (SWD) compliant hardware debugger interface to interact with the internals of the FUSB15201.

## USB Type-C & PD Peripheral Overview

The USB Type-C and PD peripheral is a fully compliant USB Type-C and PD solution.

This peripheral consists of an analog front end and a digital state machine. Firmware implements the higher level protocol and policy layers whereas the analog and digital components can perform lower level PD protocol and PHY layer functions.

The Type-C block includes all terminations and comparators required for Source/Sink/DRP operation: plug orientation detection, power capability advertisement and power role detection. If no VDD is applied, the CC Pins are high impedance.

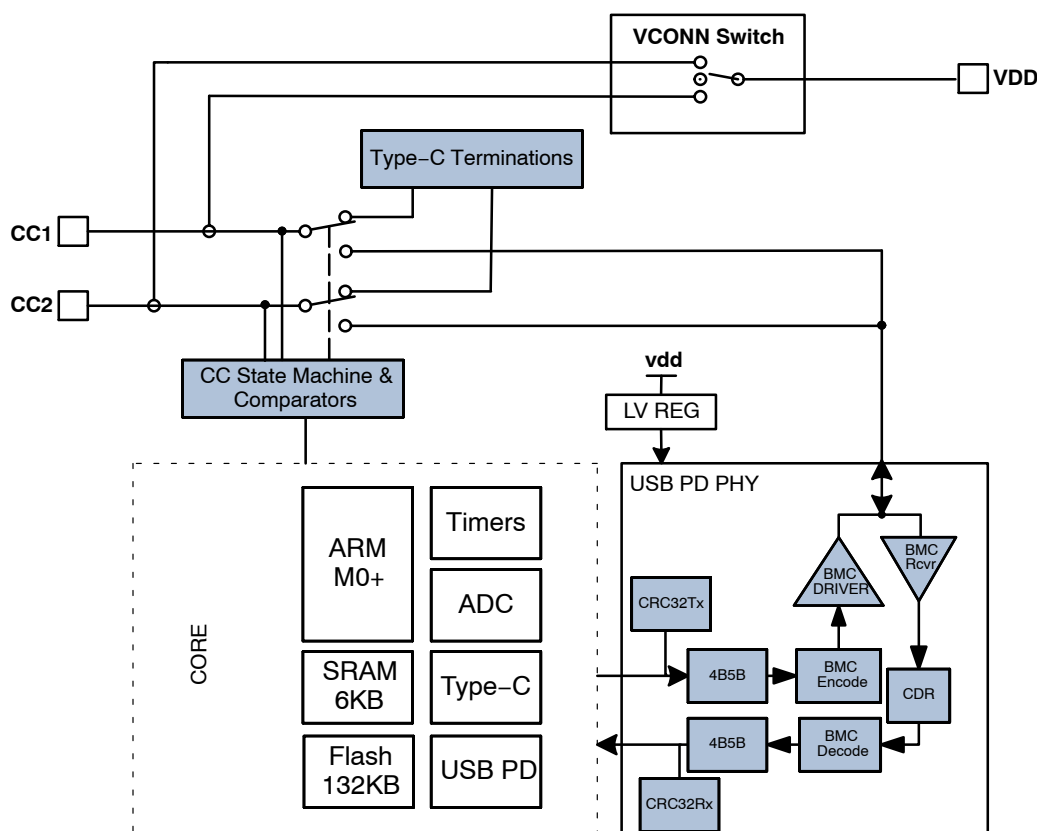


Figure 5. USB Type-C and PD

## VCONN Switch

Some applications require that a VCONN voltage be sourced in order to provide additional capabilities, such as greater than 3 A VBUS sourcing or support for full-featured Type-C cables.

The FUSB15201 can provide 1.5 W or more depending on VDD level.

## USB PD PHY State Machine Logic

The FUSB15201 PD module includes the following digital functions to enable USB PD messaging:

- Serialization and de-serialization
- Clock and data recovery (CDR)
- 4B5B coding
- BMC coding
- Packet CRC generation and checking
- Coding and detection of Power Delivery K-Codes
- Automatic GoodCRC packet response

## VBUS Discharge

The FUSB15201 is able to discharge VBUS via selectable pull-down resistors.

Typical source applications will rely on the DC-DC converter to transition between VBUS voltages.

If the application requires the FUSB15201 to discharge VBUS, the firmware may select the proper resistance of the discharge. Selection of discharge resistance needs to take into account any capacitive load on VBUS as not to violate  $V_{srcSlewNeg}$  in the USB PD spec (30 mV/μs).

Source applications, where the FUSB15201 internal discharge is utilized, will have to isolate any large bulk capacitances in order to prevent extreme internal temperature rises. Typical isolated source capacitances are around 4.7 μF.

The FUSB15201 is capable of discharging up to 100 μF from VBUS in the entire operating range.

## INTERNAL PROTECTION

The FUSB15201 integrates multiple system level protections to enable robust designs.

### VCONN Over-Current Protection

Each port's VCONN Switch provides over-current detection and protection for the switch that is enabled based on the Type-C orientation and can be software configured based on application needs. The level of OCP can be controlled via a register setting.

In case of an over-current event the switch will be opened.

### CC, DP, DM Over-Voltage Protection

Over-voltage protection on connector Pins protects the internal circuitry damage from high voltages. Interrupts can be used to inform the software that an OVP event has occurred and take appropriate actions.

### Internal Over Temperature Protection

Internal over temperature protection is always on. Two potential sources of elevated internal temperature are:

- High Current through VCONN Switch
- High current through VBUS discharge

In either case, if the over temperature is triggered ( $T > T_{shut}$ ), both ports' VCONN switches and VBUS discharge circuitry will be disabled.

## Connector Moisture Detection

If moisture or pollutants are present in the connector and the device provides VBUS, there could be a resistive short between VBUS and other connector Pins.

The FUSB15201 provides a method to detect if there is moisture or other pollutants in the connector.

Moisture detection can be turned on or off as not to conflict with cable attach detection.

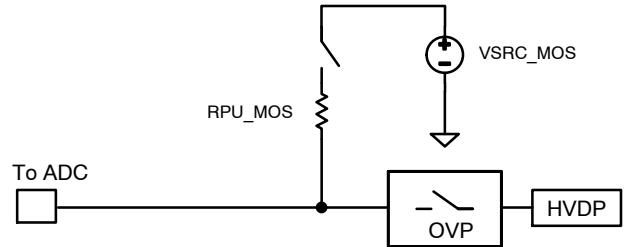


Figure 6. Moisture Detection

## Port Control and GPIOs

The FUSB15201 includes a number of Pins that can be configured to be used as standard GPIO or for use with a dedicated peripheral such as I<sup>2</sup>C. A subset of these Pins can also be connected as an input to the ADC. Internal pull-up/down resistors are programmable. Pull-up resistors are always connected to VDDIO.

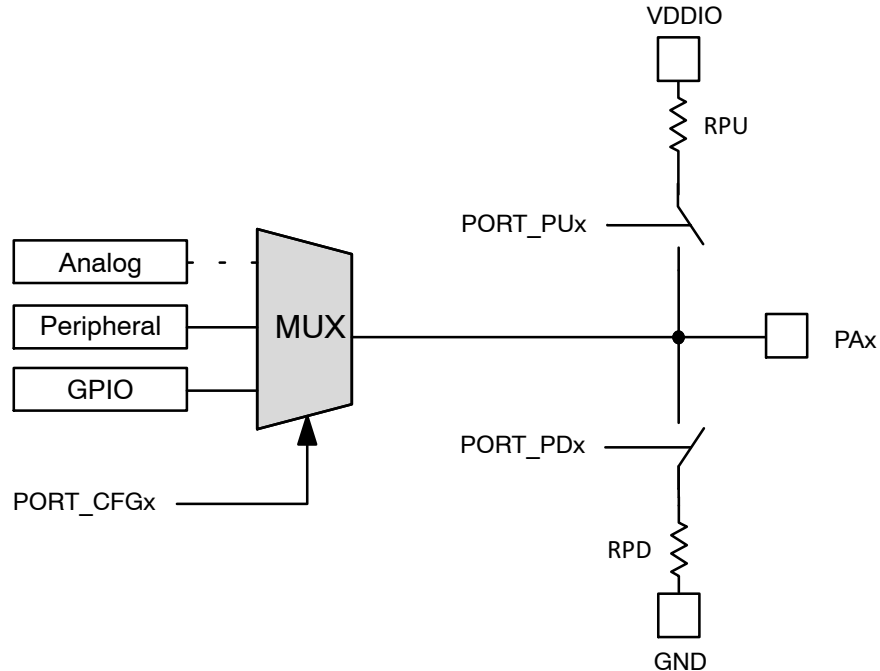


Figure 7. Typical Port Configuration

When the PORT is configured as GPIOs it will have the following capabilities:

- Bi-directional capability
- Push pull or open drain configuration
- Individually configurable interrupt lines
- Rising or Falling edge interrupt
- High or Low level interrupt

The port mapping and power domain is shown in the table below:

**Table 7. PIN – PORT CONFIGURATION AND POWER DOMAIN**

| Pin # | Name    | Port | Power Domain |
|-------|---------|------|--------------|
| 7     | GPIO1   | PA1  | VDDIO        |
|       | SWCK    |      | VDDIO        |
| 8     | GPIO2   | PA2  | VDDIO        |
|       | SWD     |      | VDDIO        |
| 9     | GPIO3   | PA2  | VDDIO        |
| 19    | GPIO4   | PA4  | VDD          |
|       | NTC_B   |      | VDD          |
| 20    | I2C_INT | PA5  | VDD          |
|       | GPIO5   |      | VDDIO        |
| 21    | I2C_SDA | PA6  | VDD          |
|       | GPIO6   |      | VDDIO        |
| 22    | I2C_SCL | PA7  | VDD          |
|       | GPIO7   |      | VDDIO        |
| 24    | GPIO8   | PA8  | VDD          |
|       | NTC_A   |      | VDD          |

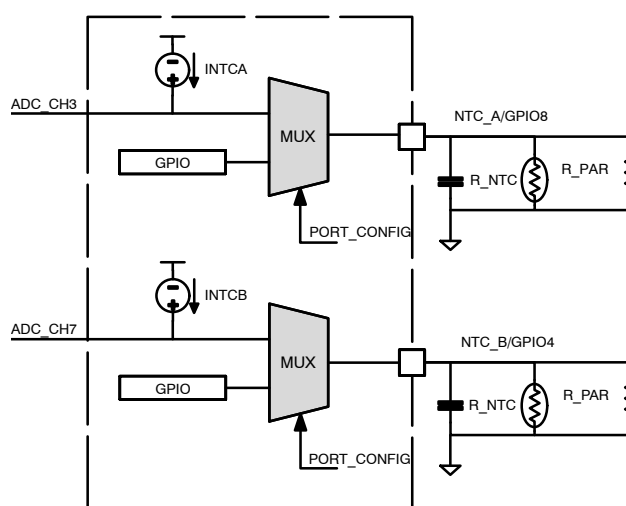
## External Temperature Measurements

There are two Pins that can be configured to monitor external NTC resistors that can be located near where high temperature devices are located. A parallel resistor is recommended for measurement linearity.

These NTC measurements are useful for reporting Source temperatures to a Sink device via FUSB15201 provided PD Status messages. Other uses include protection due to excessive thermals and dynamic power capabilities reduction.

Firmware implementation of the external temperature measurements make NTC selection flexible.

The pull-up current sources INTCA and INTCB provide a bias to the external NTC resistor networks. If desired, this current source may be turned-off.



**Figure 8. External NTC Diagram**

## BC1.2 Support

The FUSB15201 is capable of emulating and detecting BC1.2 and Divider Mode.

The following modes are supported:

- SDP
- CDP
- DCP
- 2.4 A Divider Mode (Provider only)

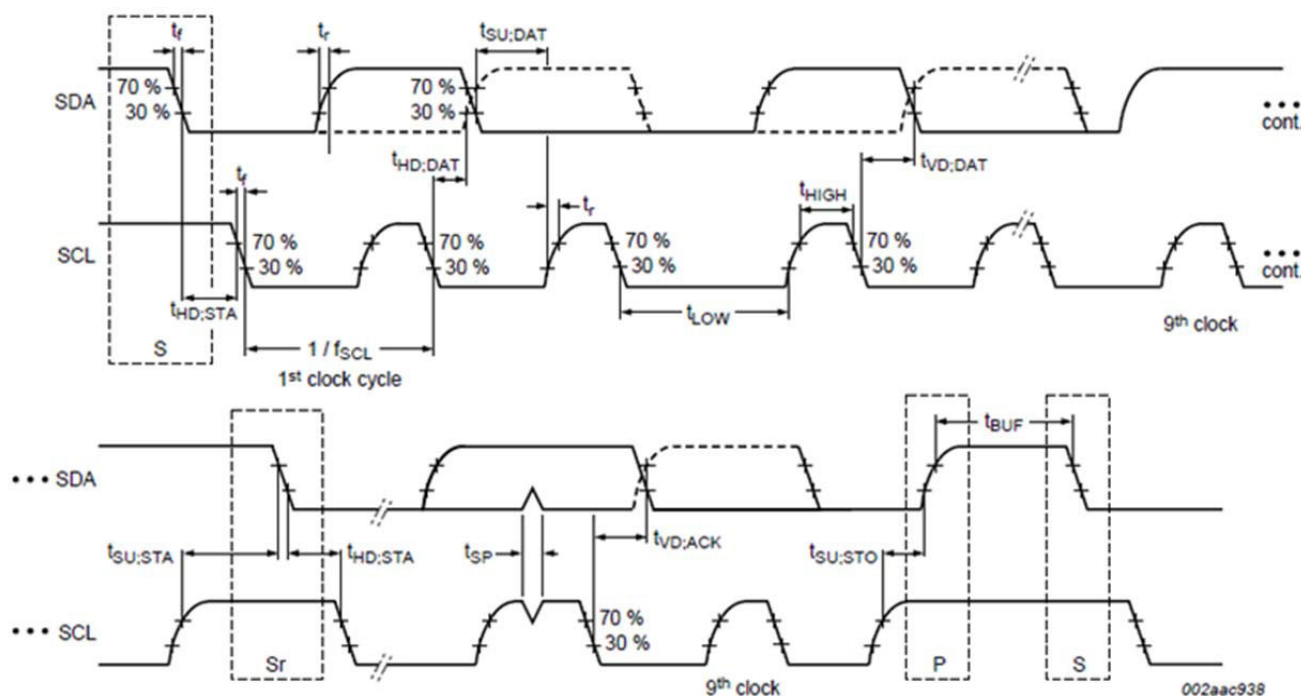
The analog circuitry is firmware configurable for the function required by the application and follows the final BC1.2 specification.

## I<sup>2</sup>C

The FUSB15201's serial interface is compatible with Standard, Fast, and Fast Mode Plus I<sup>2</sup>C bus specifications. The I<sup>2</sup>C peripheral can be configured for either host or device modes.

### Bus Timing

As shown in figure below, for data bits, SDA must be stable while SCL is HIGH. SDA may only transition when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.



$$V_{IL} = 0.3 V_{DD}$$

$$V_{IH} = 0.7 V_{DD}$$

**Figure 9. I<sup>2</sup>C Bus Timing Definition**

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH.

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH.

During a read from the FUSB15201, the host issues a Repeated Start after sending a data command and before resending the device address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH.

<sup>1</sup> Bus timing referenced from I<sup>2</sup>C-bus specification Rev. 6 – 4 April 2014

## FUSB15201

### ADC

The FUSB15201 allows for up to 12 signals to be measured and converted using the internal 10-bit ADC. For most applications, this will consist of two VBUS

voltages, two NTC temperature channels, two D+/D- BC1.2 and, optionally, two CC1/2 ports. The table below shows the typical FUSB15201 configuration along with the expected settings for the ADC module.

**Table 8. ADC CONFIGURATION**

| ADC Channel | Pin Measurement  | Resolution | Range          | Full Scale Voltage |
|-------------|------------------|------------|----------------|--------------------|
| 0           | VBUS_A           | 10 mV      | 0 V to 10.23 V | 1.024 V            |
|             |                  | 20 mV      | 0 V to 20.46 V | 2.048 V            |
|             |                  | 40 mV      | 0 V to 40.92 V | 4.096 V            |
| 1           | DP_A             | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 2           | DM_A             | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 3           | NTC1 Temperature | 1°C        | 0°C to 160°C   | 1.28 V             |
| 4           | HVCC1_A          | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 5           | HVCC2_A          | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 6           | VBUS_B           | 10 mV      | 0 V to 10.23 V | 1.024 V            |
|             |                  | 20 mV      | 0 V to 20.46 V | 2.048 V            |
|             |                  | 40 mV      | 0 V to 40.92 V | 4.096 V            |
| 7           | DP_B             | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 8           | DM_B             | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 9           | NTC2 Temperature | 1°C        | 0°C to 160°C   | 1.28 V             |
| 10          | HVCC1_B          | 4 mV       | 0 V to 4.096 V | 4.096 V            |
| 11          | HVCC2_B          | 4 mV       | 0 V to 4.096 V | 4.096 V            |

### Development Tools

FUSB15201 is supported by a full suite of comprehensive tools including:

- An easy-to-use development board
- Software Development Kit (SDK) including: USB PD protocol stacks, shared capacity algorithms, sample code, libraries, and documentation

### Specifications References

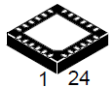
- Universal Serial Bus Power Delivery specification revision 3.1 Version 1.3, dated January 2022
- Universal Serial Bus Type C Cable and Connection Specification release 2.1, dated May 2021
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- I<sup>2</sup>C-bus specification Rev. 6 – 4 April 2014

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

ON

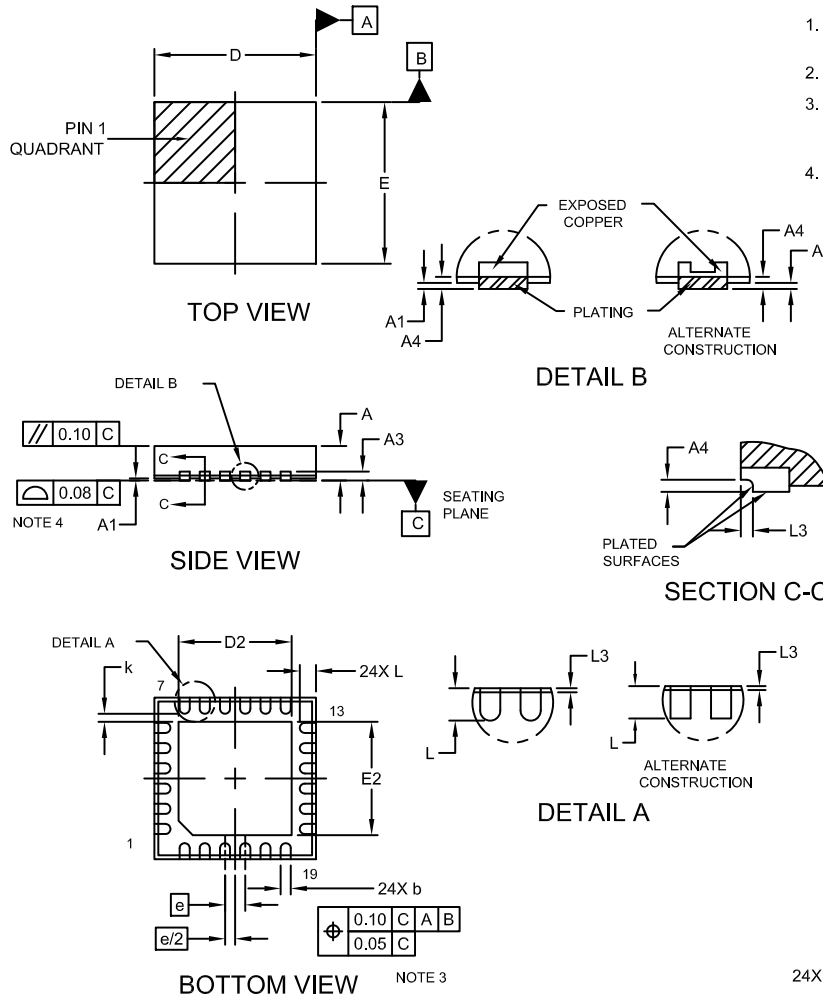


### QFNW24 4x4, 0.5P

#### CASE 484AU

#### ISSUE 0

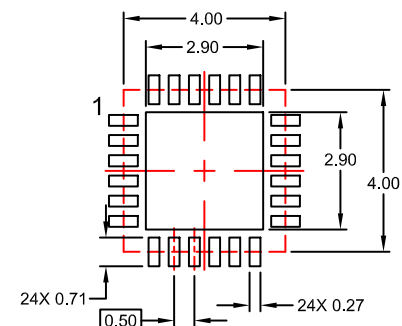
DATE 07 AUG 2020



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

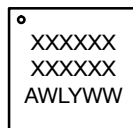
| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | 0.80        | 0.90 | 1.00 |
| A1  | --          | --   | 0.05 |
| A3  | 0.20 REF    |      |      |
| A4  | 0.10        | --   | --   |
| b   | 0.20        | 0.25 | 0.30 |
| D   | 3.90        | 4.00 | 4.10 |
| D2  | 2.70        | 2.80 | 2.90 |
| E   | 3.90        | 4.00 | 4.10 |
| E2  | 2.70        | 2.80 | 2.90 |
| e   | 0.50 BSC    |      |      |
| k   | 0.20        | --   | --   |
| L   | 0.35        | 0.40 | 0.45 |
| L3  | 0.05 REF    |      |      |



#### LAND PATTERN RECOMMENDATION\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

#### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                  |                  |                                                                                                                                                                                  |
|------------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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