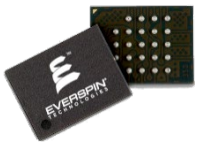
Expanded Serial Peripheral Interface (xSPI) Industrial STT-MRAM Persistent Memory

1.8V, 200MHz SPI, DSPI, QSPI and OSPI interfaces (STR & DTR)



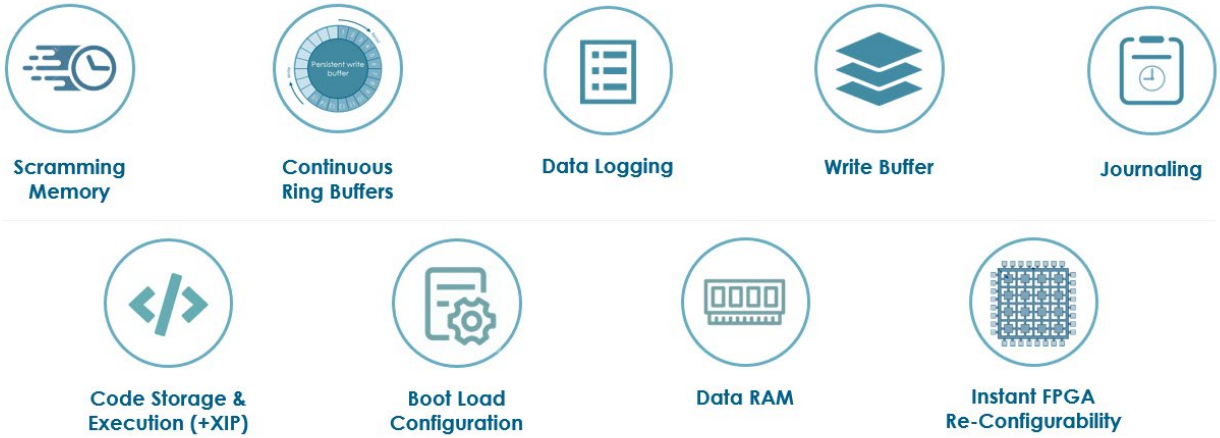
Features

- Expanded SPI bus interface supporting
  - Octal, Quad, Dual and Single SPI protocol
- Up to 200MHz single and double transfer rate (STR/DTR) for Octal SPI
- Up to 133MHz, SPI, DSPI, QSPI
- Data endurance: Unlimited read, write and erase operations for supported life of product
- Data retention: 10 Years minimum across temperature
- JEDEC compliant: JESD251, JESD251-1
- Byte level writes and reads with no erase required as persistent memory
- Data integrity: No external ECC required.
- Low Power Modes:
  - Standby < 350µA (64Mb)
  - Deep power down ~50µA w/ exit time < 100µS
- SPI compatibility: NVSRAM, FRAM, NOR, Toggle MRAM
- SPI, xSPI Commands for Program/Erase emulated NOR compatible Execute-in-place (XIP)
- Volatile and nonvolatile configuration settings
  - Nonvolatile settings are not reflow protected
- Dedicated 256-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with WRITE OTP command
  - Not reflow protected
- Erase capability
  - Chip / bulk erase and sector erase
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - 16 configurable hardware write protected regions plus top/bottom select
  - Program/erase protection during power-up
  - CRC command to detect accidental changes to user data
- Voltage
  - 1.65–2.0V (1.8V)
- Density
  - 8Mb, 16Mb, 32Mb, 64Mb
- 400MBps sustained throughput with OSPI at 200MHz , DTR, for reads and writes
- Boot mode configurations
  - Boot in x1, x2, x4, x8
- Software reset and hardware reset pin available
- 3-byte and 4-byte address modes
- Sequential (burst) read and writes
- Electronic signature
  - JEDEC-standard 3-byte signature
- JEDEC standard, RoHS compliant packages:
  - 24-ball BGA, 6mm x 8mm (5 x 5 array)
  - 8-pin DFN, 6mm x 8mm
- Operating temperature range
  - Commercial: From 0°C to +70°C
  - Industrial: From -40°C to +85°C

Device Description

The EMxxLX is the industry's first xSPI serial interface persistent memory based on Everspin's unique industrial STT MRAM technology. It is a high-performance, multiple I/O, SPI-compatible MRAM device featuring a high-speed, low pin count SPI compatible bus interface with a clock frequency of up to 200 MHz and a single 1.8V power supply. The EMxxLX delivers up to 400MBps reads and writes via eight I/O signals with a clock frequency of 200MHz.

The **EMxxLX** brings a new era of universal memory applications, replacing products such as SRAM, BBSRAM, NVSRAM and over-provisioned NOR devices and targets applications in Industrial Automation, Datacenter, Engineering Emulation, Automotive and Transportation, and Gaming. It is a great choice for the following application usage models:



BLOCK DIAGRAM

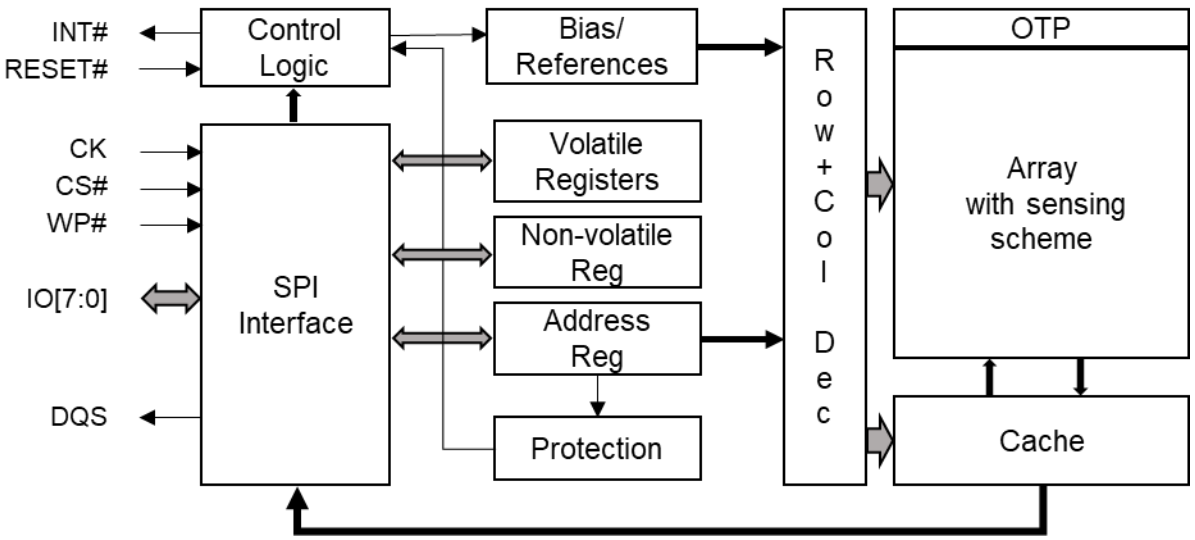
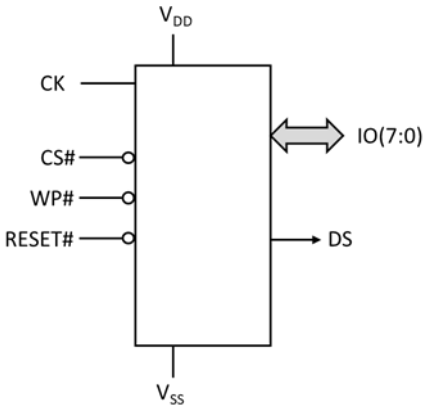
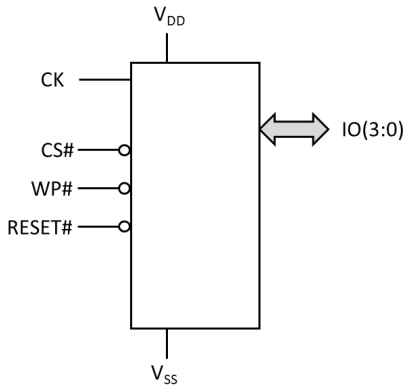


Figure 1

LOGIC DIAGRAM



OSPI, QSPI, DSPI, xSPI (24-PIN BGA)

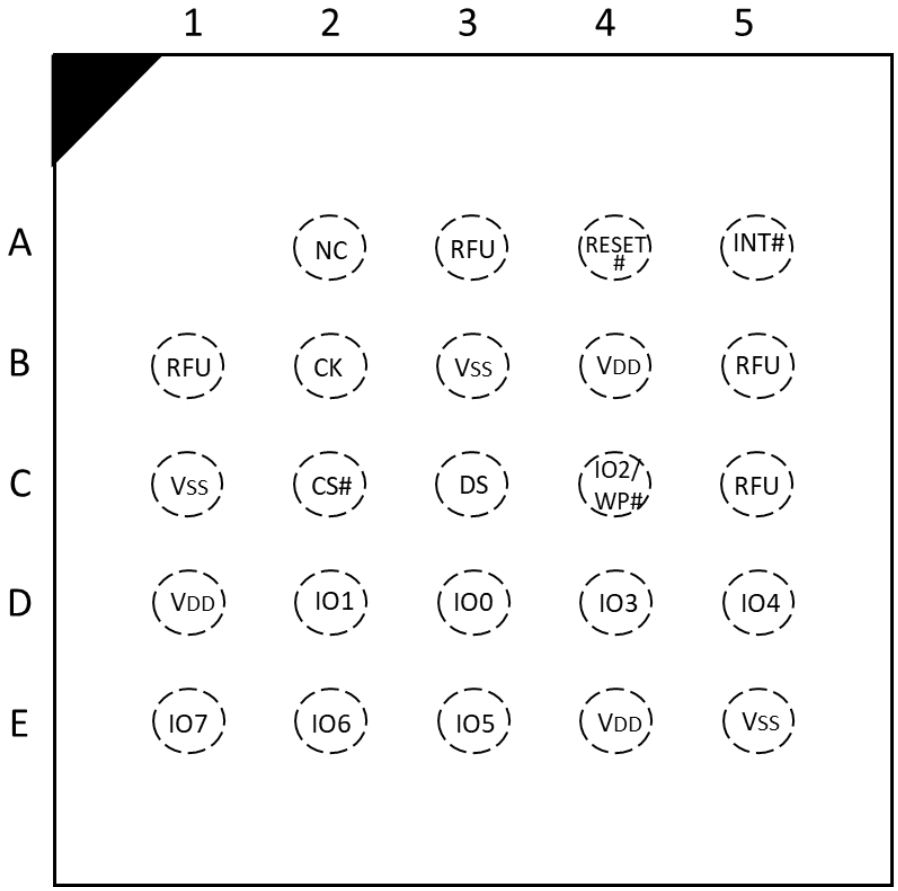


QSPI, DSPI, SPI (8-PIN DFN)

Figure 2

2. Device Pin Assignments

2.1 24 Ball BGA, 5 x 5 (Balls Down)



Octal, Quad, Dual and Single xSPI Modes

Figure 3

2.2 Signal Ball Assignment

Table 1: 24 Ball BGA xSPI, Octal, Quad, Dual and Single SPI Modes

Ball Location	xSPI Signal	Ball Location	xSPI Signal
A1	No Ball	**C4**	IO2 / WP#
A2	NC	**C5**	RFU
A3	RFU	**D1**	V_{DD}
A4	RESET#	**D2**	IO1
A5	INT#	**D3**	IO0
B1	RFU	**D4**	IO3
B2	CK	**D5**	IO4
B3	V_{SS}	**E1**	IO7
B4	V_{DD}	**E2**	IO6
B5	RFU	**E3**	IO5
C1	V_{SS}	**E4**	V_{DD}
C2	CS#	**E5**	V_{SS}
C3	DS		

Notes:

- The signals which show a "/" indicates that the pin or ball is dual function
- For C4 pin, the write protect feature (WP#) can only be used when device is in single SPI mode
- See WP# signal description for detail

Table 1

2.3 8-Pin DFN Package

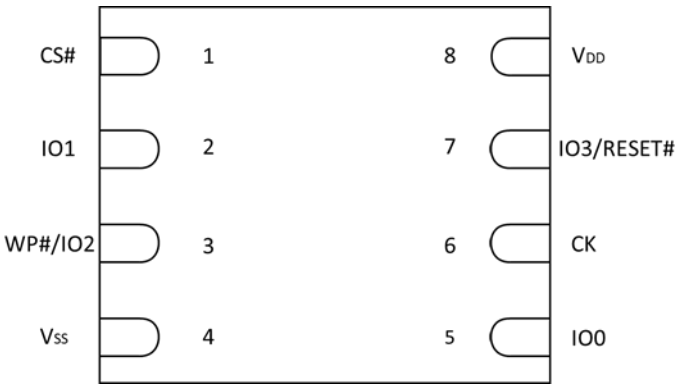


Figure 4

2.4 Signal Pinout

Table 2: xSPI, Quad, Dual and Single SPI Modes

Pin Location	Signal
1	CS#
2	IO1
3	WP#/IO2
4	V_{SS}
5	IO0
6	CK
7	IO3/RESET#
8	V_{DD}

Note:
1. Pin 7 will be IO3 in Quad SPI mode and RESET# in SPI mode or Dual SPI mode.
2. When using SPI and Dual SPI commands, IO3 must be driven high or an external pull-up resistor should be used to avoid allowing the RESET# input to float.

Table 2

3. Signal Descriptions

Signal Name	Type	Description
CS#	Input	**Chip Select.** Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a LOW to HIGH transition.
CK	Input	**Clock.** Command, Address and Data information is transferred from controller to memory with respect to the rising or falling edge of the CK. The clock is not required to be free running.
IO[7:0]	Input / Output	**Data Input/Output.** Command, Address, and Data information is transferred on these signals during Read and Write transactions.
DS	Output	**Data Strobe.** Strobe signal to capture read data sent by the memory. DS is used by a limited set of xSPI commands.
V_{DD}	Power Supply	**Power.**
V_{SS}	Power Supply	**Ground.**
RESET#	Input	**Hardware Reset.** When LOW, the memory will self-initialize and return the device to the ready state. DS and IO[7:0] are placed into the High-Z state when RESET# is LOW. The RESET# signal should not be allowed to float ; an external pull-up should be used on the PCB.
INT#	Output (Open Drain)	**Interrupt**. When LOW, the memory is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.
WP#	Input	**Write Protect**. Locks the status register in conjunction with the enable/disable bit [7] of the status register. This signal does not have internal pull-ups, it cannot be left floating and must be driven, even if neither of WP#/IO2 function is used.
RFU	Undefined	**Reserved for Future Use.** The package terminal may be connected to a circuit in the device. The function of the terminal is not currently defined or may be used for an optional signal. It is recommended to leave the terminal open and unconnected to external circuits.
NC	No Connection	**No Connection.** The package terminal has no connection to circuits in the device.
DNU	Undefined	**Do Not Use.** The package terminal must remain open and unconnected to external circuits.

Table 3

4. xSPI Signal Protocol

During the time that CS# is active (LOW) the clock signal (CK) is toggled while command information is first transferred on the data (IO) signals. The clock must be active during any period required for information access or transfer to the memory. The clock continues active during the transfer of read data from the memory to the controller or write data from the controller to the memory. When the controller has transferred the desired amount of data, CS# is driven inactive (HIGH). The period during which CS# is active is called a transaction on the bus.

While CS# is inactive, the CK is not required to toggle. CK may stop toggling when CS# is LOW as a means of lowering power consumption or inserting delay within a transaction for flow control. CK must always complete at least one rising edge and one falling edge before stopping at LOW. This requirement for a minimum of one rising and falling edge in turn requires that DTR transfers always occur in two transfer increments, e.g., two bytes (word) for 8-bit wide transfers in 8D mode. STR transfers must occur in one byte increments.

There are up to four phases of activity within each transaction:

- **Command transfer** from controller to memory
- **Command Modifier** (Address) transfer from controller to memory
- **Initial Access Latency** (also used for IO signal direction turn around in a read transaction)
- **Data transfer** (memory to controller in a read transaction or controller to memory in a write transaction)

The command transfer occurs at the beginning of every transaction. The command modifier, initial access latency, and data transfer phases are optional, and their presence depends on the protocol mode or command transferred.
The number of parallel IO signals used during the command modifier and data phases depends on the current protocol mode or command transferred. The initial access latency phase does not use the IO signals for information transfer. The protocol mode options are described by the data rate and the IO width (number of IO signals) used during the command, command modifier (address), and data phases in the following nomenclature (format):

WR-WR-WR where:
The first *WR* is the command bit width and rate
The second *WR* is the command modifier (address) bit width and rate
The third *WR* is the data bit width and rate.

The bit width *W* value may be 1, 2, 4 or 8. R has a value of S for STR, or D for DTR. STR has the same transfer value during the rising and falling edge of a clock cycle. DTR may have different transfer values during the rising and falling edges of each clock.

1S-1S-1S means that the command is 1-bit wide STR, the command modifier is 1-bit wide STR, and the data is one bit wide STR. 8D-8D-8D means that the command, the command modifier, and data transfers are always 8 bits wide DTR. The EMxxLX allows the option to repeat the command opcode which makes an 8D command look like an 8S command, but it is not required to repeat the command opcode.

Example protocol modes supported for the EMxxLX are:
1S-1S-1S; 1S-1D-1D
2S-2S-2S; 2S-2D-2D
4S-4S-4S; 4S-4D-4D
8S-8S-8S; 8D-8D-8D

Note: For full list of opcodes and modes supported by EMxxLX, please refer to section “xSPI Command Opcodes and Modes”.

The EMxxLX must be configured during the factory initialization to select the mode in which the device will boot following Power-On-Reset (POR). Supported boot modes are x1, x2, x4 or x8. For example, 8D-8D-8D mode can be made the default mode if so desired. The controller must determine the default protocol mode of the memory after POR. This may be done through prior knowledge of the system design. The controller may later reconfigure the memory to use other supported modes.

A protocol mode phase using single bit transfer uses IO[0] to transfer information from controller to memory and IO[1] to transfer information from memory to controller. On each IO, information is placed on the IO line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each u. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.

Table 4: 1S-1S-1S Bit Positions for 4 (and 3) Byte addressing

IO	Command Bits	Address Bits	Latency	Data Byte 0	Data Byte 1
0	7, 6, 5, 4, 3, 2, 1, 0	31 (23), 30 (22), … 1, 0	X …	X …	X …
1	X …	X …	X …	7, 6, 5, 4, 3, 2, 1, 0	7, 6, 5, 4, 3, 2, 1, 0
2	X …	X …	X …	X …	X …
3	X …	X …	X …	X …	X …
4	X …	X …	X …	X …	X …
5	X …	X …	X …	X …	X …
6	X …	X …	X …	X …	X …
7	X …	X …	X …	X …	X …

Table 4

A protocol mode phase using two IO signals uses IO[1:0], four IO signals using IO[3:0] and eight IO signals uses IO[7:0]. The LSb of each byte is placed on IO[0] with each higher order bit on the successively higher numbered IO signals. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes in STR are transferred in lowest address to highest address order. While in 8D mode, sequential data bytes in DTR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order. In 8D mode, the starting address must be even.

Table 5: 8D-8D-8D Bit Positions for 4 (and 3) Byte addressing

IO	Command Bits		Address Bits				Latency	Data Word 0		Data Word 1	
0	0	0	24	16	8	0	X …	0	0	0	0
1	1	1	25	17	9	1	X …	1	1	1	1
2	2	2	26	18	10	2	X …	2	2	2	2
3	3	3	27	19	11	3	X …	3	3	3	3
4	4	4	28	20	12	4	X …	4	4	4	4
5	5	5	29	21	13	5	X …	5	5	5	5
6	6	6	30	22	14	6	X …	6	6	6	6
7	7	7	31	23	15	7	X …	7	7	7	7

Table 5

IO signals not in use in a particular phase are undefined and may or may not be driven by the controller or memory, i.e., these signals may be in a high impedance state (floating and indicated by X in the bit position tables).

Note:

- In single and dual bit transfers the IO[7:2] signals may be high impedance, unless they are dual purpose such as WP# or RESET# in the DFN package
- In quad bit transfers the IO[7:4] signals may be high impedance

During the data transfer period of a read memory transaction, the Data Strobe (DS) signal is driven by the memory device and transitions edge aligned with the IO signal data transitions. DS is used as an additional output signal with the same timing characteristics as other data outputs but with the guarantee of transitioning with every data bit transferred. The DS signal transitions can be received and internally phase shifted by the controller to be used as an internal read clock/strobe to capture each data bit transferred. Data Strobe is the return of the clock, CK. It is available in all modes and makes it easier to achieve higher clock frequencies. It is required to achieve the maximum clock frequencies. DS goes low when CS# is driven low by the host controller and is driven until CS# is pulled high. DS stays low while the device is receiving command, address, and data. DS will toggle while the device is transmitting data out.

5. Registers

The EMxxLX supports various status and configuration registers for device status updates and configuration settings. These registers and their access details are discussed in the following sections.

5.1 Status Register

Read Status Register or Write Status Register commands are used to read from or write to the Status Register bits, respectively. When the status register enable/disable bit (bit 7) is set to 1 and WP# is driven LOW, the status register nonvolatile bits become read-only and the Write Status Register operation will not execute. This hardware-protected mode is exited by driving WP# high.

Table 6: Status Register

Bit	Name	Settings	Description	Type	Notes
0	WIP: Write in progress	0 = Ready 1 = Busy	Status bit to determine if a Write Status Register, Write Nonvolatile Configuration Register, Write (Program), CRC, or Erase operation is in progress. This bit is Read Only.	Volatile	2
1	WEL: Write enable latch	0 = Clear (Default) 1 = Set	The device powers up with the Write enable latch (WEL) cleared to prevent inadvertent Write (Program), or Erase operations. To enable these operations, the Write Enable command must be executed to set this bit. The Write Disable command clears this bit. This bit is Read Only.	Volatile	
2	BP[0]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1
3	BP[1]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1

4	BP[2]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1
5	Top/Bottom	0 = Top (Default) 1 = Bottom	Determines whether the top or bottom of the memory array is where the protected area as defined by the block protect bits starts from. This bit is writable.	Non-volatile	
6	BP[3]	Refer to Protected Area tables	Defines memory area to be software protected against Write (Program) or Erase operations. When one or more block protect bits are set to 1, a designated memory area is protected. This bit is writable.	Non-volatile	1
7	Status Register Write Enable/Disable	0 = Enabled (Default) 1 = Disabled	Used with WP# to enable or disable writing to the status register. This bit is writable.	Non-volatile	
Notes 1. All BP bits must be set to 0 for the Bulk Erase command execution 2. Bit 0 is the inverse of Flag Status Register Bit 7					

Table 6

Status Register Write Enable/Disable Bit [7]

This bit enables write protect for the Status register when set to '1' and the write protect (WP#) pin is driven LOW. In this mode, any instruction that changes the status register content is ignored, effectively locking the state of the device. If SR Bit [7] is set to '0', irrespective of the WP status (LOW or HIGH), status register write protection remains disabled. Refer to Table xx on page yy for the memory and status register protection options.

Top/ Bottom Protection Bit [5]

This bit defines the operation of the Block Protection bits BP3, BP2, BP1, and BP0. This bit controls the starting point of the memory array (from top or bottom) that gets protected by the Block protection bits.

Block Protection (BP3, BP2, BP1 and BP0) [6,4:2]

These bits define the memory array to be write-protected against memory write commands. When one or more of the BP bits is set to '1', the respective memory address is protected from writes. The Block Protect bits (BP3, BP2, BP1, and BP0) in combination with the T/B bit can be used to protect an address or sector range of the memory array. The size of the range is determined by the value of the BP bits and the upper or lower starting point of the range which is selected by the T/B. Table xx shows EMxxLX protected address range for BP[3:0] bits setting.

Write Enable Latch (WEL) Bit [1]

The WEL bit must be set to 1 to enable write operations to the memory array or registers, as shown in Table xx. This bit is set to '1' only by executing the Write Enable (WREN) command. The WEL bit (SR1[1]) automatically clears to '0' after a Write Disable (04h) command is executed. Write (Program) commands will not reset WEL at the completion of the command allowing for back-to-back writes to memory without loading the WREN command again. The WEL bit is volatile and returns to its default '0' state after POR, software RESET, and hardware RESET (via the RESET# pin when available).

5.2 Flag Status Register

The Read Flag Status Register command is used to read the Flag status register bits. Flag status registers bits are volatile and are reset to zero on power-up. They are set and reset automatically by the internal controller. Error bits must be cleared through the Clear Status Register command. For Soft Reset, Hardware Reset and Reset with signal sequence, bits 1, 3, 4, and 5 are set to "0"; bit 7 is set to "1". In a Reset with signal sequence, bit 0 is set to "0".

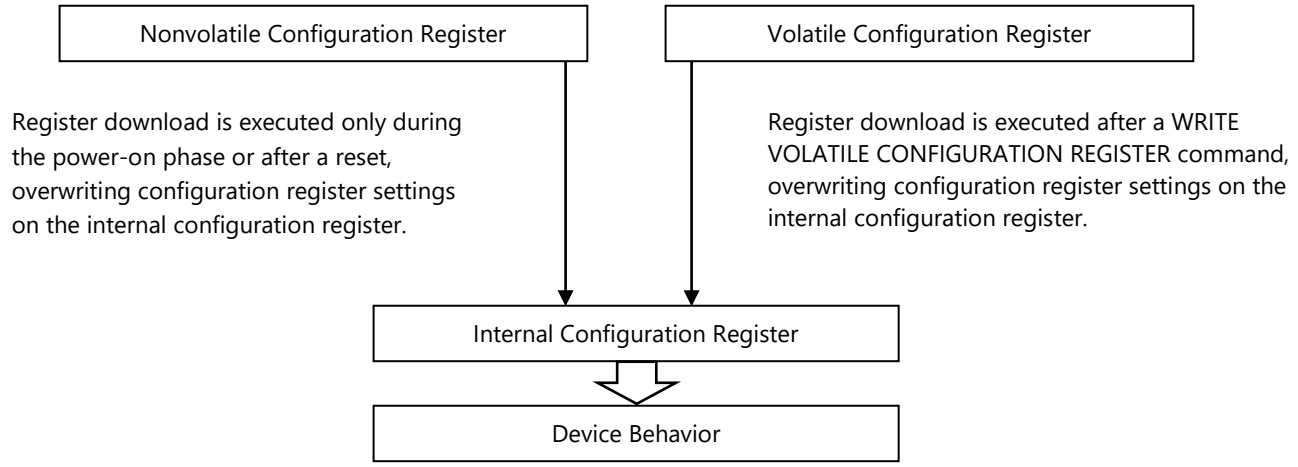
Table 9: Flag Status Register	

Bit	Name	Settings	Description	Type
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	Indicates whether 3-byte or 4-byte address mode is enabled.	Status
1	Protection	0 = Clear 1 = Protection Error	Indicates whether an Erase or Program operation has attempted to modify the protected array sector as configured by Block Protection, or whether a OTP Write operation has attempted to access the locked OTP space.	Error
2	Reserved			
3	CRC	0 = Clear 1 = Failure	Indicates that the Computed CRC did not match the user provided CRC Code.	Error
4	Write (Program)	0 = Clear 1 = Program Error	Indicates whether a Program operation has succeeded or failed. A PROGRAM or OTP Write operation will fail if WREN is not set.	Error
5	Erase	0 = Clear 1 = Erase Error	Indicates whether an Erase operation has succeeded or failed. An Erase operation will fail if WREN is not set.	Error
6	Reserved			
7	Write (Program) or Erase	0 = Busy 1 = Ready	Indicates whether one of the following command cycles is in progress: Write Status Register, Write Nonvolatile Configuration Register, Write (Program), Erase, or CRC Check.	Status

Table 9

5.3 CONFIGURATION REGISTERS

The memory configuration is set by an internal configuration register that is not directly accessible to users. The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.
The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.



5.4 NONVOLATILE CONFIGURATION REGISTER

Nonvolatile Configuration Register 0					
Address[5]	**0x0000**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	I/O Mode	1111_1111 (0xFF) 1101_1111 (0xDF) 1111_1101 (0xFD) 1101_1101 (0xDD) 1111_1011 (0xFB) 1101_1011 (0xDB) 1110_1011 (0xEB) 1100_1011 (0xCB) 1110_0111 (0xE7) 1100_0111 (0xC7) 1011_0111 (0xB7) 1001_0111 (0x97) Others	SPI with DS (default) SPI w/o DS Dual with DS Dual w/o DS Quad with DS Quad w/o DS Quad DTR with DS Quad DTR w/o DS Octal DTR with DS Octal DTR w/o DS Octal with DS Octal w/o DS SPI with DS (same as default)	6

Nonvolatile Configuration Register 1					
Address	**0x0001**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Dummy Cycle Configuration	0000_0000 0000_0001 0000_0010 . . . 0000_1111 0001_0000 . . . 0001_1110 0001_1111 1111_1111 Others	16 Dummy cycles 1 Dummy cycles 2 Dummy cycles ... 15 Dummy cycles 16 Dummy cycles ... 30 Dummy cycles 31 Dummy cycles 16 Dummy cycles 16 Dummy cycles (default)	
Nonvolatile Configuration Register 2					
Address	**0x0002**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Reserved	TBD		
Nonvolatile Configuration Register 3					
Address	**0x0003**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Driver Strength Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	50 Ohm (default) 35 Ohm 25 Ohm 18 Ohm 50 Ohm	
Nonvolatile Configuration Register 4					
Address	**0x0004**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:4	RW	TBD	TBD		
3:0	RW	DS Delay	TBD	TBD	
Nonvolatile Configuration Register 5					

Address	**0x0005**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Address Mode	1111_1111 1111_1110 Others	3-Byte Address (default) 4-Byte Address 3-Byte Address	
Nonvolatile Configuration Register 6					
Address	**0x0006**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Execute-in-Place (XIP) Configuration	1111_1111 1111_1110 1111_1100 Others	XIP Disabled (default) XIP Enable- Activated if XIP confirmation bit = 0 during FAST READ XIP BOOT- Activated at boot time XIP Disabled	1
Nonvolatile Configuration Register 7					
Address	**0x0007**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Wrap Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	Continuous (default) 64-byte wrap 32-byte wrap 16-byte wrap Continuous	2
Nonvolatile Configuration Register 8					
Address	**0x0008**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7	RW	Erase Bit Value	1 = Erase with '1' (default) 0 = Erase with '0'	Determines data state for Erase operations	
6:2	RW	TBD	TBD		
1	RW	RPE	1 = Reset Pin Disabled 0 = Reset Pin Enabled (default)	When the Reset pin is disabled, the RESET # will be ignored. The device may be reset with Soft Reset or JESD Reset. In the DFN package option, the RESET# signal is disabled automatically when the device is configured in Quad SPI mode (Register 0).	
0	RW	Write mode	1 = Persistent Memory Mode enabled (default) 0 = Persistent memory mode disabled	Persistent Memory mode or NOR Flash like mode is selected with this bit.	3
Nonvolatile Configuration Registers 9,10,11,12					
Address	**0x0009, 0x000A, 0x000B, 0x000C**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Non Volatile user scratch register	1111_1111 (default)	Four 8 bit registers available for storing any user data.	4

Table 10

Notes:

1. Only FAST READ (0Bh) supports XIP operation.
2. Wrap length affects READ commands. WRITE wrap length will depend on the mode selected in Register 8.
3. Used to select the mode for writing to the memory
4. These registers may be used for storing user configuration data that will be used for device recovery if necessary.
5. Register addresses may be either 3-byte or 4-byte depending on user selection
6. When, configuring the I/O mode, the unused IO's, if any, will be left floating. For example, if a user intends to use only the Quad SPI mode in a Octal SPI in a BGA package, IO4-7 will be floating or Hi-Z. These balls may be left unconnected on the PCB if the user never intends to activate Octal SPI. If an Octal SPI BGA device is configured in the Dual SPI mode, IO0 and IO1 will be active and the remaining IO's will be

floating except for ball C4 which is dual purpose IO2/WP#. A Quad SPI device in a DFN package which is configured as Dual SPI will use IO2 and IO3 as WP# and RESET# respectively. Similarly, if the same device is configured as SPI mode, IO1 is left floating.

5.5 VOLATILE CONFIGURATION REGISTER

Volatile Configuration Register 0					
Address[4]	**0x0000**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	I/O Mode	1111_1111 (0xFF) 1101_1111 (0xDF) 1111_1101 (0xFD) 1101_1101 (0xDD) 1111_1011 (0xFB) 1101_1011 (0xDB) 1110_1011 (0xEB) 1100_1011 (0xCB) 1110_0111 (0xE7) 1100_0111 (0xC7) 1011_0111 (0xB7) 1001_0111 (0x97) Others	SPI with DS (default) SPI w/o DS Dual with DS Dual w/o DS Quad with DS Quad w/o DS Quad DTR with DS Quad DTR w/o DS Octal DTR with DS Octal DTR w/o DS Octal with DS Octal w/o DS SPI with DS (same as default)	5
Volatile Configuration Register 1					
Address	**0x0001**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Dummy Cycle Configuration	0000_0000 0000_0001 0000_0010 . . . 0000_1111 0001_0000 . . . 0001_1110 0001_1111 Others	16 Dummy cycles 1 Dummy cycles 2 Dummy cycles ... 15 Dummy cycles 16 Dummy cycles ... 30 Dummy cycles 31 Dummy cycles 16 Dummy cycles	
Volatile Configuration Register 2					
Address	**0x0002**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Reserved	TBD		
Volatile Configuration Register 3					
Address	**0x0003**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Driver Strength Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	50 Ohm (default) 35 Ohm 25 Ohm 18 Ohm 50 Ohm	
Volatile Configuration Register 4					
Address	**0x0004**				

Bit	Op	Name	Settings	Description	Notes
7:4	RW	Reserved	TBD		
3:0	RW	DS Delay	TBD	TBD	
Volatile Configuration Register 5					
Address	**0x0005**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Address Mode	1111_1111 1111_1110 Others	3-Byte Address (default) 4-Byte Address 3-Byte Address	
Volatile Configuration Register 6					
Address	**0x0006**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Execute-in-Place (XIP) Configuration	1111_1111 1111_1110 Others	XIP Disabled (default) XIP Enable- Activated if XIP confirmation bit = 0 during FAST READ XIP Disabled	1
Volatile Configuration Register 7					
Address	**0x0007**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:0	RW	Wrap Configuration	1111_1111 1111_1110 1111_1101 1111_1100 Others	Continuous (default) 64-byte wrap 32-byte wrap 16-byte wrap Continuous	2
Volatile Configuration Register 8					
Address	**0x0008**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7	RW	Erase Bit Value	1 = Erase with '1' (default) 0 = Erase with '0'	Determines data state for Erase operations	
6:3	RW	Reserved			
2	RW	OTP Unlock	1 = OTP Lock Enable (default) 0 = OTP Lock Disable"	When OTP Lock is disabled this will override the OTP Lock Byte setting and unlock the OTP array.	
1	RW	RPE	1 = Reset Pin Enabled (default) 0 = Reset Pin Disabled	When the Reset pin is disabled, the RESET # will be ignored. The device may be reset with Soft Reset or JESD Reset. In the DFN package option, the RESET# signal is disabled automatically when the device is configured in Quad SPI mode (Register 0).	
0	RW	Write mode	1 = Persistent Memory Mode enabled (default) 0 = Persistent memory mode disabled	Persistent Memory mode or NOR Flash like mode is selected with this bit.	3

Table 11

Notes:

1. Only FAST READ (0Bh) supports XIP operation.
2. Wrap length affects READ commands. WRITE wrap length will depend on the mode selected in Register 8.
3. Used to select the mode for writing to the memory
4. Register addresses may be either 3-byte or 4-byte depending on user selection

5. When, configuring the I/O mode, the unused IO's, if any, will be left floating. For example, if a user intends to use only the Quad SPI mode in a Octal SPI in a BGA package, IO4-7 will be floating or Hi-Z. These balls may be left unconnected on the PCB is the user never intends to activate Octal SPI. If an Octal SPI BGA device is configured in the Dual SPI mode, IO0 and IO1 will be active and the remaining IO's will be floating except for ball C4 which is dual purpose IO2/WP#. A Quad SPI device in a DFN package which is configured as Dual SPI will leave IO2 and IO3 as WP# and RESET# respectively. Similarly, if the same device is configured as SPI mode, IO1 is left floating.
6. Default settings are power-on reset defaults.

Table 20

6 xSPI Command Opcodes and Modes

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of CK after CS# is driven low. Command sequences starts with a one-byte command code. The one-byte command code is shifted into the device on the IO's, and each bit is latched on the rising edges of CK. Depending on the command, this might be followed by address bytes or by data bytes, or by both or neither. CS# must be driven high after the last bit of the command sequence has been completed. For the commands Read, Read Fast, Read Status Register or Deep Power-Down exit, and Read ID, the shifted-in command sequence is followed by a data-out sequence. All read instructions can be completed after any bit of the data-out sequence is being shifted out, then CS# must be driven high to return to deselected status.

Table 21: Instruction Command Table

Instruction Command Set	Opcode (Hex)	SPI Mode	DSPI Mode	QSPI Mode		OSPI Mode		Address Bytes[6]	Latency[4] (Dummy)
				STR	DTR	STR	DTR		
RESET Enable	0x66	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
RESET Memory	0x99	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Read ID	0x9E	1s-0-1s	~	~	~	8s-0-8s	8d-0-8d	0	0,0,0,8
Read ID	0x9F	1s-0-1s	~	~	~	8s-0-8s	8d-0-8d	0	0,0,0,8
Read ID MIO	0xAF	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0,0,0,8
Read	0x03	1s-1s-1s	~	~	~	~	~	3/4	0
Read Fast (XIP)	0x0B	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
Read Fast Dual Output	0x3B	1s-1s-2s	2s-2s-2s	~	~	~	~	3/4	DCC
Read Fast Dual I/O	0xBB	1s-2s-2s	2s-2s-2s	~	~	~	~	3/4	DCC
Read Fast Quad Output	0x6B	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	DCC
Read Fast Quad I/O	0xEB	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	DCC
Read Fast DTR	0x0D	1s-1d-1d	2s-2d-2d	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC
Read Fast Dual Output DTR	0x3D	1s-1d-2d	2s-2d-2d	~	~	~	~	3/4	DCC
Read Fast Dual I/O DTR	0xBD	1s-2d-2d	2s-2d-2d	~	~	~	~	3/4	DCC
Read Fast Quad Output DTR	0x6D	1s-1d-4d	~	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC
Read Fast Quad I/O DTR	0xED	1s-4d-4d	~	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC
Read Word Quad I/O (no DTR)	0xE7	1s-4s-4s	~	4s-4s-4s	~	~	~	3/4	4
Read Fast Octal Output[3]	0x8B	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
Read Fast Octal I/O[3]	0xCB	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
Read Fast Octal Output DTR[3]	0x9D	1s-1d-8d	~	~	~	8d-8d-8d	8d-8d-8d	3/4[5]	DCC
Read Fast Octal I/O DTR[3]	0xFD	1s-8d-8d	~	~	~	8d-8d-8d	8d-8d-8d	4[5]	DCC
Read 4-byte address	0x13	1s-1s-1s	~	~	~	~	~	4	0
Read Fast 4-byte address	0x0C	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	4[5]	DCC
Read Fast Dual Output 4-Byte Address	0x3C	1s-1s-2s	2s-2s-2s	~	~	~	~	4	DCC
Read Fast Dual I/O 4-byte Address	0xBC	1s-2s-2s	2s-2s-2s	~	~	~	~	4	DCC
Read Fast Quad Output 4-Byte Address	0x6C	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	DCC
Read Fast Quad I/O 4-Byte Address	0xEC	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	DCC
Read Fast DTR 4-Byte Address	0x0E	1s-1d-1d	2s-2d-2d	4s-4d-4d	4s-4d-4d	~	~	4	DCC
Read Fast Dual I/O DTR 4-Byte Address	0xBE	1s-2d-2d	2s-2d-2d	~	~	~	~	4	DCC
Read Fast Quad I/O DTR 4-Byte Address	0xEE	1s-4d-4d	~	4s-4d-4d	4s-4d-4d	~	~	4	DCC
Read Fast Octal Output 4-byte address[3]	0x7C	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	DCC
Read Fast Octal I/O 4-byte address[3]	0xCC	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	DCC
Write Enable	0x06	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0

Instruction Command Set	Opcode (Hex)	SPI Mode	DSPI Mode	QSPI Mode		OSPI Mode		Address Bytes[6]	Latency[4] (Dummy)
				STR	DTR	STR	DTR		
Write Disable	0x04	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Read Status Register	0x05	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0,0,0,8
Read Flag Status Register	0x70	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0,0,0,8
Read Nonvolatile Configuration Register	0xB5	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0,0,0,8
Read Volatile Configuration Register	0x85	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0,0,0,8
Read General Purpose Read Register	0x96	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	8,8,8,8
Write Status Register[1]	0x01	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0
Write Nonvolatile Configuration Register[1]	0xB1	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write Volatile Configuration Register[1]	0x81	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
Clear Flag Status Register	0x50	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Write (Program Page)[1,2]	0x02	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write (Program) Fast Dual Input[1,2]	0xA2	1s-1s-2s	2s-2s-2s	~	~	~	~	3/4	0
Write (Program) Fast Dual Input Extended[1,2]	0xD2	1s-2s-2s	2s-2s-2s	~	~	~	~	3/4	0
Write (Program) Fast Quad Input[1,2]	0x32	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	0
Write (Program) Fast Quad Input Extended[1,2]	0x38	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	3/4	0
Write (Program) Fast Octal Input[1,2,3]	0x82	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write (Program) Fast Octal Input Extended[1,2,3]	0xC2	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	3/4[5]	0
Write (Program) 4-byte address[1,2]	0x12	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	4[5]	0
Write (Program) Fast Quad Input 4-byte[1,2]	0x34	1s-1s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	0
Write (Program) Fast Quad Input Ext. 4-byte[1,2]	0x3E	1s-4s-4s	~	4s-4s-4s	4s-4d-4d	~	~	4	0
Write (Program) Fast Octal Input 4-byte[1,2,3]	0x84	1s-1s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	0
Write (Prog) Fast Octal Input Extended 4-byte[1,2,3]	0x8E	1s-8s-8s	~	~	~	8s-8s-8s	8d-8d-8d	4[5]	0
Erase 32kB[1]	0x52	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	3/4[5]	0
Erase 4kB[1]	0x20	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	3/4[5]	0
Erase Sector[1]	0xD8	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	3/4[5]	0
Erase/Bulk Chip[1]	0xC7	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Erase/Bulk Chip[1]	0x60	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Erase Sector 4-byte address[1]	0xDC	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	4[5]	0
Erase 4kB 4-byte address[1]	0x21	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	4[5]	0
Erase 32kB 4-byte address[1]	0x5C	1s-1s-0	2s-2s-0	4s-4s-0	4s-4d-0	8s-8s-0	8d-8d-0	4[5]	0
OTP Read	0x4B	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
OTP Write[1]	0x42	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
4-byte address mode Enter	0xB7	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
4-byte address mode Exit	0xE9	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Deep Power Down Enter	0xB9	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Deep Power Down Exit	0xAB	1s-0-0	2s-0-0	4s-0-0	4s-0-0	8s-0-0	8d-0-0	0	0
Interface Activation (CRC)	0x9B	1s-0-1s	2s-0-2s	4s-0-4s	4s-0-4d	8s-0-8s	8d-0-8d	0	0
TDP Write[1]	0xF0	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	0
TDP Read	0xF1	1s-1s-1s	2s-2s-2s	4s-4s-4s	4s-4d-4d	8s-8s-8s	8d-8d-8d	3/4[5]	DCC
TDP Read DTR	0xF2	1s-1d-1d	2s-2d-2d	4s-4d-4d	4s-4d-4d	~	~	3/4	DCC

Table 21

Notes:

1. A Write Enable command is needed to set the WEL bit prior to this command but memory writes only require WREN the first time, subsequent writes do not require a WREN.
2. WREN is only required one time, subsequent writes do not require another WREN command
3. Octal commands are treated as a NOP in part numbers that are QSPI, including QSPI in the DFN package
4. Latency: Positions in this column, A,B,C,D, are defined as: A=SPI, B=Dual, C=Quad, D={8S|8D|4D}
5. Octal SPI with DTR operations or commands all require 4-byte address input.
6. A "0" indicates that there is no address byte required.

- "~" indicates mode not supported .
- DCC = Dummy Clock Cycles from Configuration Register

xSPI Opcode Timing Representation

Please refer to the modular timing waveform below to understand the full timing for any opcode for EMxxLX shown in section "xSPI Command Opcodes and Modes". Timing of each supported opcode can be decomposed into three key items. Command, Address, and Data as shown below:

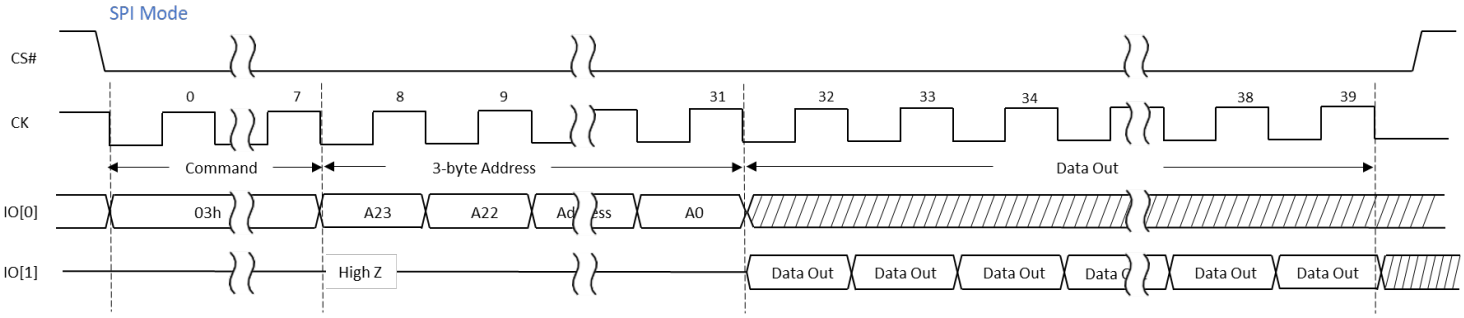
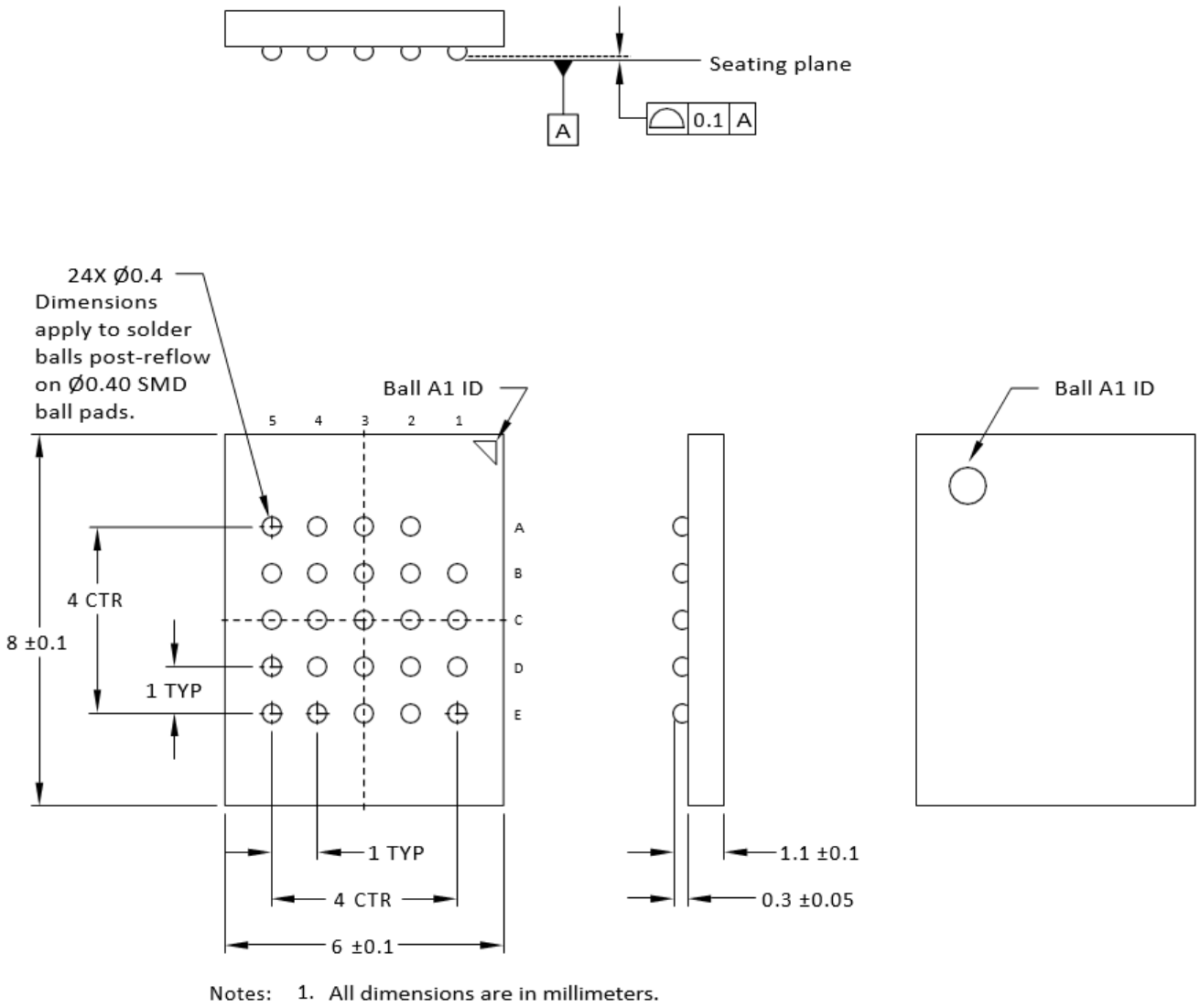


Figure 10: Opcode Timing Diagram

7 Package Information

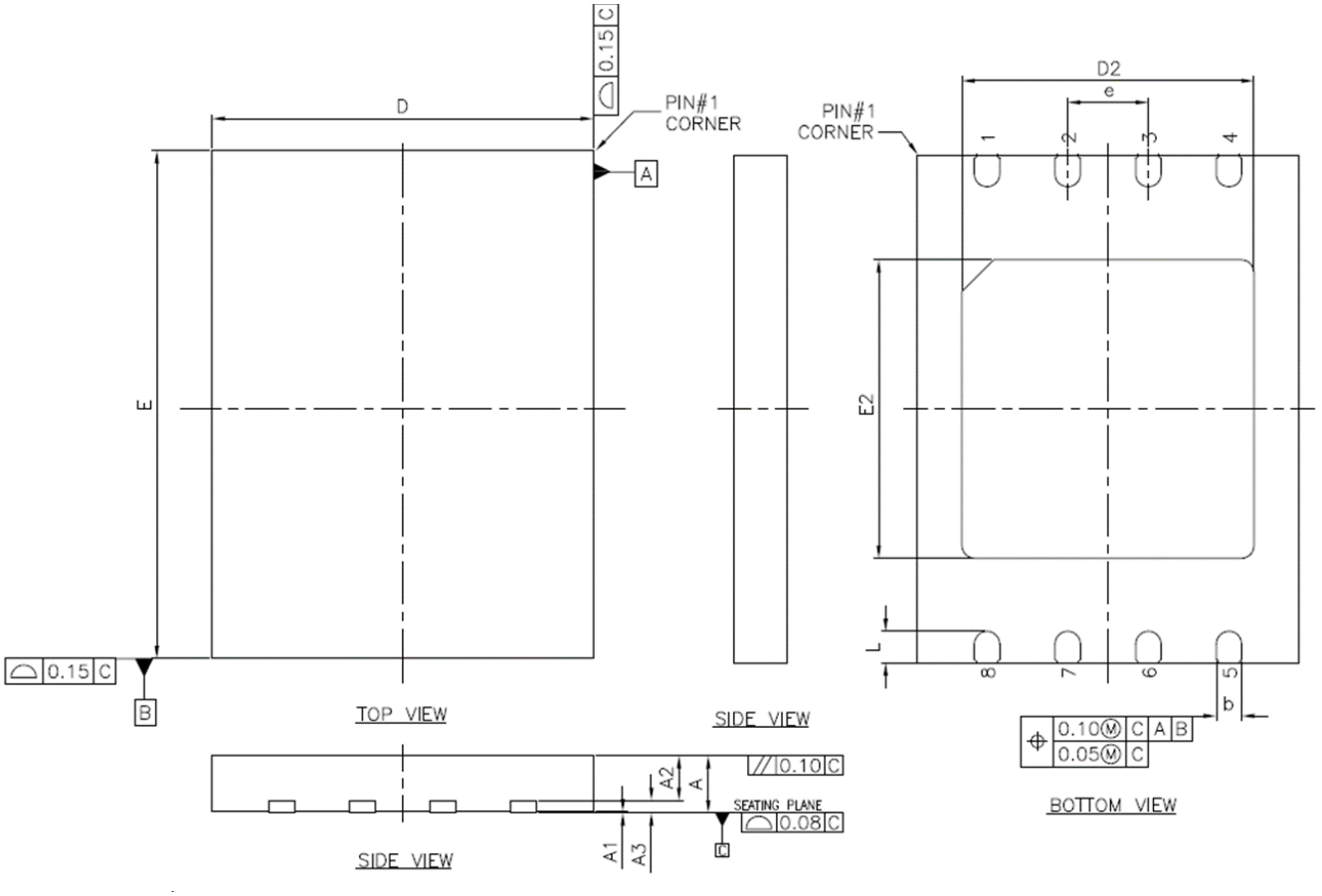
24-Ball TBGA, 5 x 5 ball array



Notes: 1. All dimensions are in millimeters.

Figure 38

8-Pin DFN Package



	Symbol	Min.	Nom.	Max.
Total thickness	A	0.85	0.90	0.95
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.65	0.70	0.75
Lead thickness	A3		0.20 REF	
Body Size	D	5.90	6.00	6.10
	E	7.90	8.00	8.10
Lead width	b	0.35	0.40	0.48
Exposed pad width	D2	4.55	4.60	4.65
Exposed pad length	E2	4.65	4.70	4.75
Lead pitch	E		1.27 BSC	
Lead length	L	0.45	0.50	0.55
Lead count	N		8L	

THIRD ANGLE PROJECTION	
UNLESS OTHERWISE SPECIFIED DECIMAL: .X ± .XX ± .10 .XXX ± .05	
ANGULAR ± 3°	
SCALE: 15:1	
JEDEC NO.: MO-229(REF.)	
DWG. NO.: PD-PR23 (OSE)	REV.: A

Figure 39

Revision History

v0 : Initial version
v1: Changed feature list on page 1.
v2: Clarified frequency for Octal, Quad and Single SPI modes. No HOLD# pin for SPI modes, Command table update.
v.3: Updated xSPI Signal Protocol section, added DSPI to package and pinouts.
v4; Updated PN, command tables, DFN drawing
v5: Register tables updated, xSPI command description updated.
v6: December 16 alignment to data sheet with updates on registers, commands and block diagrams
v7: Dec 01, 2021 Updated to reflect datasheet rev 2.0 10132021 (registers, commands, description)
v8: April 27, 2022 Updated to reflect register and command code updates