RX26T Group, RX23T Group

Differences Between the RX26T Group and the RX23T Group

Introduction

This application note is intended as a reference to points of difference in the peripheral functions, I/O registers, and pin functions between the RX26T Group and RX23T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX26T Group and the 64-pin package version of the RX23T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the *User's Manual: Hardware* for the products in question.

Target Device

RX26T Group, RX23T Group

Contents

1. Comparison of Built-In Functions of RX26T Group and RX23T Group

A comparison of the built-in functions of the RX26T Group and RX23T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX23T Group and RX26T Group.

Table 1.1 Comparison of Built-In Functions of RX23T Group and RX26T Group

Function	RX23T	RX26T
CPU	●/▲	
Operating modes	▲	
Address space	▲	
Resets	●/▲	
Option-setting memory	●/▲	
Voltage detection circuit (LVDAb for RX23T and LVDA for RX26T)	●/▲	
Clock generation circuit	●/▲	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●/■	
Register write protection function	■/▲	
Exception handling	○	
Interrupt controller (ICUb for /RX23T and ICUG for RX26T)	●/▲	
Buses	●/▲	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa)	×	○
Data transfer controller (DTCa for RX23T and DTCb for RX26T)	●/▲	
Event link controller (ELC)	×	○
I/O ports	●/▲	
Multi-function pin controller (MPC)	●/▲	
Multi-function timer pulse unit 3 (MTU3c for RX23T and MTU3d for RX26T)	●/▲	
Port output enable 3 (POE3b for RX23T and POE3D for RX26T)	●/▲	
General purpose PWM timer (GPTWa)	×	○
High resolution PWM waveform generation circuit (HRPWM)	×	○
Port output enable for GPTW (POEG)	×	○
8-bit timer (TMR for RX23T and TMRb for RX26T)	●/▲	
Compare match timer (CMT)	●/▲	
Compare match timer W (CMTW)	×	○
Watchdog timer (WDTA)	×	○
Independent watchdog timer (IWDTa)	▲	
Serial communications interface (SCIg for RX23T, and SCIk and SCIh for RX26T)	●/▲	
Serial communications interface (RSCI)	×	○
I²C bus interface (RIICa)	●	
I³C bus interface (RI3C)	×	○
CAN FD module (CANFD)	×	○
Serial peripheral interface (RSPIa for RX23T and RSPId for RX26T)	▲	
Serial peripheral interface (RSPIA)	×	○
CRC calculator (CRC for RX23T and CRCA for RX26T)	●	
Trigonometric function calculator (TFUv2)	×	○
Trusted Secure IP (TSIP-Lite)	×	○
12-bit A/D converter (S12ADE for RX23T and S12ADHa for RX26T)	●/▲	
D/A converter (DA for RX23T) 12-bit D/A converter (R12DAb for RX26T)	●/▲	

Function	RX23T	RX26T
Temperature sensor (TEMPS)	✕	○
Comparator C (CMPC for RX23T and CMPCa for RX26T)	▲	
Data operation circuit (DOC for RX23T and DOCA for RX26T)	▲	
RAM	●/▲	
Flash memory	●/▲	
Packages	●/▲	

○: Available, ✕: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specification items that have no differences between the groups are not indicated.

2.1 CPU

Table 2.1 is Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX23T	RX26T
CPU	• Maximum operating frequency: 40 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions (For products with a RAM capacity of 64 KB) • 111 instructions (For products with a RAM capacity of 48 KB) — Basic instructions: 77 — Single-precision floating point instructions: 11 — DSP instructions: 23 — Instructions for register bank save function: 2 (Only for products with a RAM capacity of 64 KB) • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits

Item	RX23T	RX26T
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparison of Operating Mode Registers.

Table 2.2 Comparison of Operating Mode Registers

Register	Bit	RX23T	RX26T
SYSCR1	—	System control register 1	System control register 1
		Initial value after a reset differs.	
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is Comparative Memory Map in Single-Chip Mode.

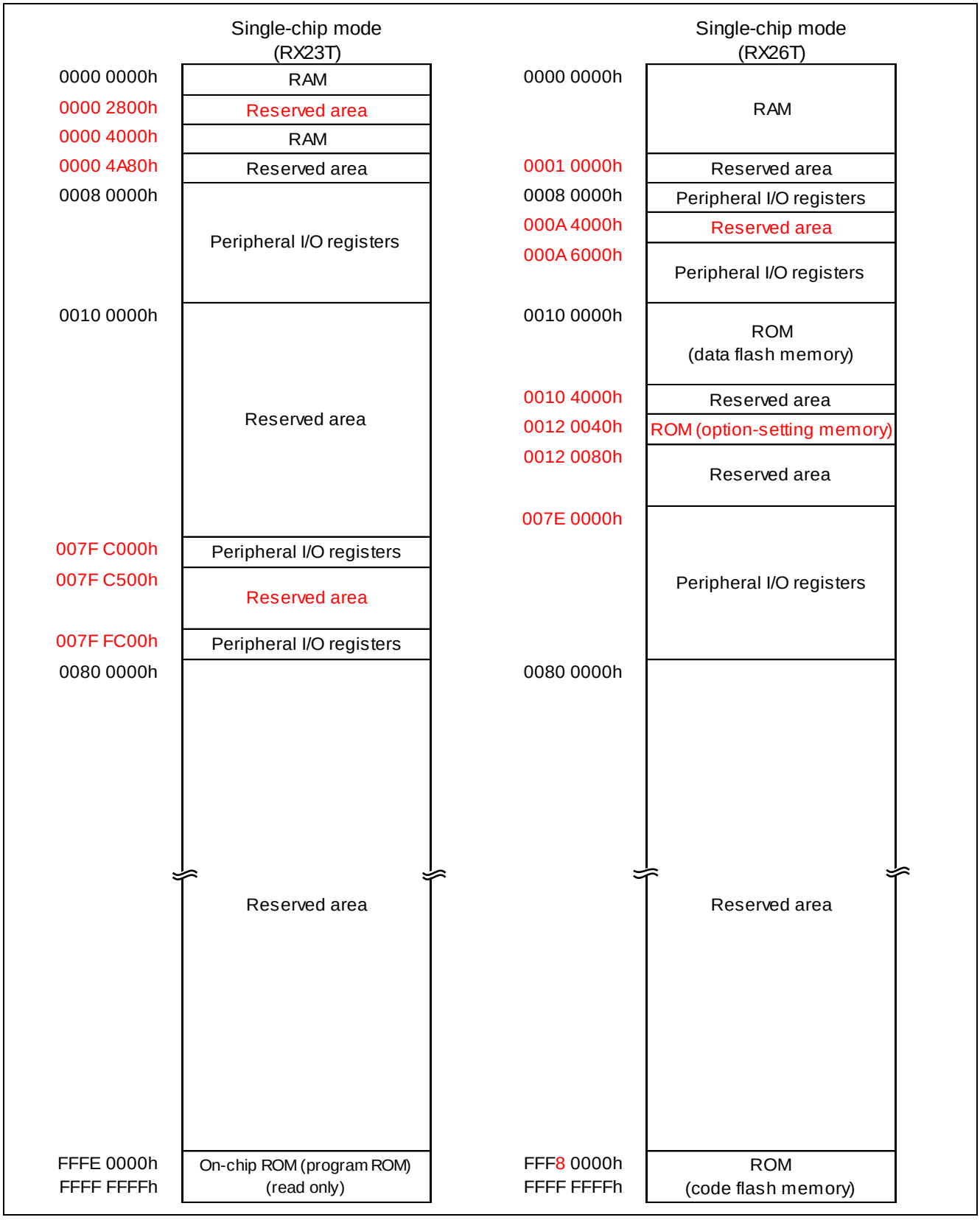

Figure 2.1 Comparative Memory Map in Single-Chip Mode

2.4 Resets

Table 2.3 is Comparative Overview of Resets, and Table 2.4 is Comparison of Reset-Related Registers.

Table 2.3 Comparative Overview of Resets

Item	RX23T	RX26T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage monitored: Vdet2)
Independent Watchdog Timer Reset	Independent watchdog timer underflow, or refresh error	Independent watchdog timer underflow or refresh error
Watchdog timer Reset	—	Watchdog timer underflow or refresh error
Software reset	Register setting	Register setting

Table 2.4 Comparison of Reset-Related Registers

Register	Bit	RX23T	RX26T
RSTSR2	WDTRF	—	Watchdog timer reset Detection flag

2.5 Option-Setting Memory

Figure 2.2 is Comparison of Option-Setting Memory Areas, and Table 2.5 is Comparison of Option-Setting Memory Registers.

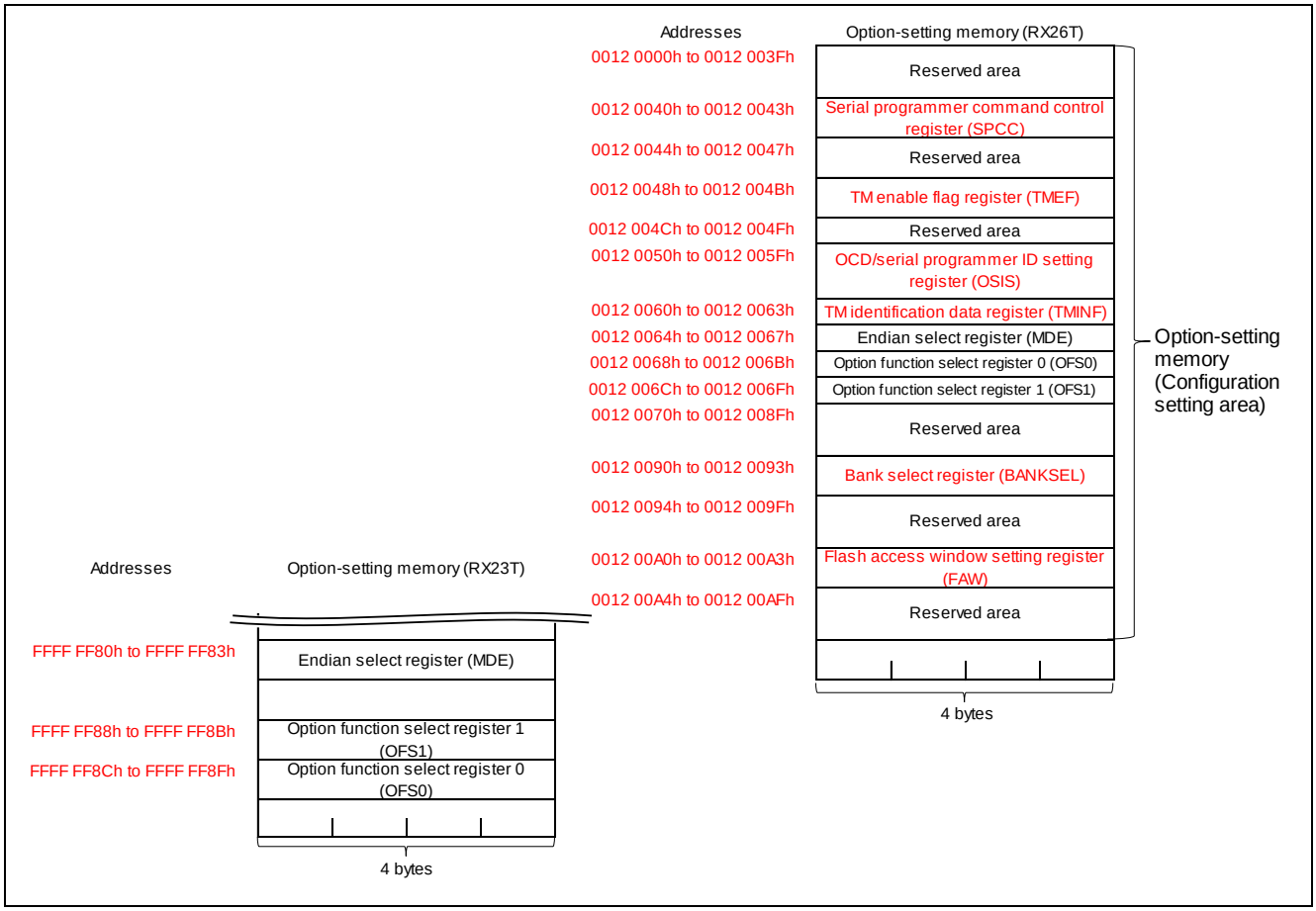

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.5 Comparison of Option-Setting Memory Registers

Register	Bit	RX23T	RX26T (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial programmer ID setting register
OFS0	IWDTTOPS [1:0]	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode.
	WDTSTRT	—	WDT start mode select bit
	WDTTOPS[1:0]	—	WDT timeout period select bits
	WDTCKS[3:0]	—	WDT clock frequency division ratio select bits
	WDTRPES[1:0]	—	WDT window end position select bits
	WDTRPSS[1:0]	—	WDT window start position select bits
	WDTRSTIRQS	—	WDT reset interrupt request select bit
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Settings other than above are prohibited when the voltage detection 0 circuit is used.	Voltage detection 0 level select bits b1 b0 0 0: Reserved 0 1: Reserved 1 0: 2.83 V is selected 1 1: 4.22 V is selected
MDE	BANKMD[2:0]	—	Bank mode select bits
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
BANKSEL	—	—	Bank select register
FAW	—	—	Flash Access Window Setting Register

2.6 Voltage Detection Circuit

Table 2.6 is Comparative Overview of Voltage Detection Circuits, and Table 2.7 is Comparison of Voltage Detection Circuit Registers.

In addition, Table 2.8 is Comparison of Setting Procedures for Monitoring Vdet1, Table 2.9 is Comparison of Setting Procedures for Monitoring Vdet2, and Table 2.10 to Table 2.13 are comparative listings of the setting procedures for bits related to the voltage monitoring 1 and 2 interrupts and the voltage monitoring 1 and 2 resets.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX23T (LVDAb)			RX26T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
	Detection voltage	Selectable from 2 levels using the OFS1 register	Selectable from 9 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 4 levels using LVDLVLR. LVD2LVL[1:0] bits	Selectable from 2 levels using OFS1. VDSEL[1:0] bits	Selectable from 5 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 5 levels using LVDLVLR. LVD2LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	Not available	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection		LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage Monitoring 0 reset	Voltage Monitoring 1 reset	Voltage Monitoring 2 reset	Voltage Monitoring 0 reset	Voltage Monitoring 1 reset	Voltage Monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	Not available	Voltage Monitoring 1 interrupt	Voltage Monitoring 2 interrupt	Not available	Voltage Monitoring 1 interrupt	Voltage Monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either

Item		RX23T (LVDAb)			RX26T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Digital filter	Enable/ disable switching	—	—	—	Digital filter function not available	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	Not available	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX23T (LVDAb)	RX26T (LVDA)
LVDLVLR	—	Voltage detection level select register	Voltage detection level select register
		Initial value after a reset differs.	
	LVD1LVL [3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.
	LVD2LVL [1:0] (RX23T) LVD2LVL [3:0] (RX26T)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	—	Voltage monitoring 1 circuit control register 0	Voltage monitoring 1 circuit control register 0
		Initial value after a reset differs.	
	LVD1DFDIS	—	Voltage monitoring 1 digital filter disable mode select bit
	LVD1FSAMP [1:0]	—	Sampling clock select bits
LVD2CR0	—	Voltage monitoring 2 circuit control register 0	Voltage monitoring 2 circuit control register 0
		Initial value after a reset differs.	
	LVD2DFDIS	—	Voltage monitoring 2 digital filter disable mode select bit
	LVD2FSAMP [1:0]	—	Sampling clock select bits

Table 2.8 Comparison of Setting Procedures for Monitoring Vdet1

Item		RX23T (LVDAb)	RX26T (LVDA)
Setting procedure for monitoring Vdet1	1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Wait for at least td(E-A).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 1).	LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1)

Table 2.9 Comparison of Setting Procedures for Monitoring Vdet2

Item		RX23T (LVDAb)	RX26T (LVDA)
Setting procedure for monitoring Vdet2	1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 level select).	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Wait for at least td(E-A).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 2).	LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2)

Table 2.10 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	Set LVD1CR0.LVD1RI = 0 (voltage monitoring 1 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.
	9	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 1).	—
	10	Set the LVD1SR.LVD1DET bit to 0.	Set LVD1SR.LVD1DET = 0.
	11	Set the LVD1CR0.LVD1RIE bit to 1 (enabling voltage monitoring 1 interrupts/resets).	Set LVD1CR0.LVD1RIE = 1 (enabling voltage monitoring 1 interrupts/resets).
	12	—	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 reset	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	• Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Set the LVD1CR0.LVD1RIE bit to 1 (enabling voltage monitoring 1 interrupts/resets).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	• Set the LVD1CR0.LVD1RI = 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.
	8	Wait for at least td(E-A).	Set LVD1SR.LVD1DET = 0.
	9	—	Set LVD1CR0.LVD1RIE = 1 (enabling voltage monitoring 1 interrupts/resets).
	10	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.11 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 interrupt	1	Set the LVD1CR0.LVD1RIE bit to 0 (disabling voltage monitoring 1 interrupts/resets).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD1CR0.LVD1CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1RIE = 0 (disabling voltage monitoring 1 interrupts/resets).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVCMPCR.LVD1E bit to 0 (disabling the voltage detection 1 circuit).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	—
Operation-disable setting procedure for bits related to voltage monitoring 1 reset	1	Set the LVD1CR0.LVD1CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD1E bit to 0 (disabling the voltage detection 1 circuit).	Set LVD1CR0.LVD1RIE = 0 (disabling voltage monitoring 1 interrupts/resets).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVD1CR0.LVD1RIE bit to 0 (disabling voltage monitoring 1 interrupts/resets).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 reset	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	—

Table 2.12 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 interrupt	1	Set the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	Set LVD2CR0.LVD2RI = 0 (voltage monitoring 2 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	9	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 2).	—
	10	Set the LVD2SR.LVD2DET bit to 0.	Set LVD2SR.LVD2DET = 0.
	11	Set the LVD2CR0.LVD2RIE bit to 1 (enabling voltage monitoring 2 interrupts/resets).	Set LVD2CR0.LVD2RIE = 1 (enabling voltage monitoring 2 interrupts/resets).
	12	—	LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2)

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 reset	1	Set the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	• Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Set the LVD2CR0.LVD2RIE bit to 1 (enabling voltage monitoring 2 interrupts/resets).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	• Set the LVD2CR0.LVD2RI = 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.
	8	Wait for at least td(E-A).	Set LVD2SR.LVD2DET = 0.
	9	—	Set LVD2CR0.LVD2RIE = 1 (enabling voltage monitoring 2 interrupts/resets).
	10	Set the LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).	LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2)

Table 2.13 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 2 interrupt	1	Set the LVD2CR0.LVD2RIE bit to 0 (disabling voltage monitoring 2 interrupts/resets).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD2CR0.LVD2CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 2).	Set LVD2CR0.LVD2RIE = 0 (disabling voltage monitoring 2 interrupts/resets).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVCMPCR.LVD2E bit to 0 (disabling the voltage detection 2 circuit).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—
Operation-disable setting procedure for bits related to voltage monitoring 2 reset	1	Set the LVD2CR0.LVD2CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 2).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	(No procedure because there is no digital filter) —	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD2E bit to 0 (disabling the voltage detection 2 circuit).	Set LVD2CR0.LVD2RIE = 0 (disabling voltage monitoring 2 interrupts/resets).
	4	(No procedure because there is no digital filter) —	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is not in use — (No procedure)
	5	Set the LVD2CR0.LVD2RIE bit to 0 (disabling voltage monitoring 2 interrupts/resets).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).

Item		RX23T (LVDAb)	RX26T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 2 reset	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—

2.7 Clock Generation Circuit

Table 2.14 is Comparative Overview of Clock Generation Circuits, and Table 2.15 is Comparison of Clock Generation Circuit Registers.

Table 2.14 Comparative Overview of Clock Generation Circuits

Item	RX23T	RX26T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules: The peripheral module clock PCLKA is the operating clock for MTU3, the peripheral module clock PCLKD is for the S12AD, and peripheral module clock PCLKB is for modules other than MTU3 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, RSCI, RI3C, CANFD, MTU (internal peripheral bus), GPTW (internal peripheral bus), and HRPWM (internal peripheral bus). • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the counter reference clock for peripheral modules and the HRPWM reference clock (PCLKC) to be supplied to the MTU and GPTW. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX23T	RX26T
Operating frequency	• ICLK: 40 MHz (max.) • PCLKA: 40 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same as the clock from respective oscillators • IWDTCLK: 15 kHz	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 120 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with the 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • CACCLK: Same as the clock from respective oscillators • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU pin is driven to high-impedance state. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU and GPTW pins are driven to high-impedance state.
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 10 (increments of 0.5) • Oscillation frequency: 24 MHz to 40 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz

Item	RX23T	RX26T
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.15 Comparison of Clock Generation Circuit Registers

Register	Bit	RX23T	RX26T
SCKCR	—	System clock control register	System clock control register
		Initial value after a reset differs.	
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
SCKCR2	—	—	System clock control register 2
PLLCR	—	PLL control register	PLL control register
		Initial value after a reset differs.	
	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: Divided by 1 0 1: Divided by 2 1 0: Divided by 4 1 1: Setting prohibited	PLL input frequency division ratio select bits b1 b0 0 0: Divided by 1 0 1: Divided by 2 1 0: Divided by 3 1 1: Setting prohibited
	PLLSRCSEL	—	PLL clock source selection bit (b4)
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 : : 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
HOCOWTCR	—	High-speed on-chip oscillator wait Control register	—

Register	Bit	RX23T	RX26T
OSCOVFSR	—	Oscillation stabilization flag register	Oscillation stabilization flag register
		Initial value after a reset differs.	
	ILCOVF	—	IWDT-dedicated clock oscillation stabilization flag
OSTDCR	OSTDIE	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled, and oscillation stop detection is not reported to the POE. 1: The oscillation stop detection interrupt is enabled, and oscillation stop detection is reported to the POE.	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled, and oscillation stop detection is not reported to the POE or POEG. 1: The oscillation stop detection interrupt is enabled, and oscillation stop detection is reported to the POE or POEG.
MOSCWTCR	—	Main clock oscillator wait control register	Main clock oscillator wait control register
		Initial value after a reset differs.	
	MSTS[4:0] (RX23T) MSTS[7:0] (RX26T)	Main clock oscillator wait time setting bits (b4 to b0) b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	Waiting time until output from the main clock oscillator to the internal circuits starts (b7 to b0) MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: main clock oscillation stabilization time; fLOCO_max: maximum fLOCO frequency)
MOFCR	MODRV21 (RX23T) MODRV2 [1:0] (RX26T)	Main clock oscillator drive capability switch bits 0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz	Main clock oscillator drive capability 2 switch bits b5 b4 0 0: 20.1 to 24 MHz 0 1: 16.1 to 20 MHz 1 0: 8.1 to 16 MHz 1 1: 8 MHz
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register
MEMWAIT	—	Memory wait cycle setting register	—

2.8 Low Power Consumption

Table 2.16 is Comparative Overview of Low Power Consumption Functions, Table 2.17 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.18 is Comparison of Low Power Consumption Registers.

Table 2.16 Comparative Overview of Low Power Consumption Functions

Item	RX23T	RX26T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), and flash interface clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available: High-speed operating mode Middle-speed operating mode	—

Table 2.17 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23T	RX26T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	—
	Flash memory	Operation possible	Operation possible
	Watchdog timer	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	Comparator C	Operation possible	—
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	—
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	—	Stopped (retained)
	8-bit timer (unit 0, unit1) (TMR)	—	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX23T	RX26T
Software standby mode	I/O ports	Retained	Retained
	Comparator C	Operation possible	—
Deep sleep mode	Transition method	Control register + instruction	—
	Method of cancellation other than reset	Interrupt	—
	State after cancellation	Program execution state (interrupt processing)	—
	Main clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	—
	Low-speed on-chip oscillator	Operation possible	—
	IWDT-dedicated on-chip oscillator	Operation possible	—
	PLL	Operation possible	—
	CPU	Stopped (retained)	—
	RAM	Stopped (retained)	—
	DTC	Stopped (retained)	—
	Flash memory	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	—
	Power-on reset circuit	Operation	—
	Peripheral modules	Operation possible	—
	I/O ports	Operation	—
	Comparator C	Operation possible	—
All-module clock stop mode	Transition method	—	Control register + instruction
	Method of cancellation other than reset	—	Interrupt
	State after cancellation	—	Program execution state (interrupt processing)
	Main clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	—	Stopped (retained)
	RAM	—	Stopped (retained)
	Flash memory	—	Stopped (retained)
	Watchdog timer	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Port output enable (POE)	—	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Stopped (retained)
	I/O ports	—	Retained

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

Table 2.18 Comparison of Low Power Consumption Registers

Register	Bit	RX23T	RX26T
SBYCR	SSBY	Software standby bit 0: Transition to sleep mode or deep sleep mode after the execution of the WAIT instruction 1: Transition to software standby mode after the execution of the WAIT instruction	Software standby bit 0: Transition to sleep mode or all module clock stop mode after the execution of the WAIT instruction 1: Transition to software standby mode after the execution of the WAIT instruction
MSTPCRA	—	Module stop control register A	Module stop control register A
		Initial value after a reset differs.	
	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA2	—	8-bit timer 7/6 (unit 3) module stop bit
	MSTPA3	—	8-bit timer 5/4 (unit 2) module stop bit
	MSTPA7	—	General purpose PWM timer/high resolution PWM/GPTW-dedicated port output enable module stop bit
	MSTPA16	—	12-bit A/D converter (unit 1) module stop bit
	MSTPA19	Comparator C reference voltage generation D/A converter module stop bit Target module: DA 0: Release from module-stop state 1: Transition to module-stop state	12-bit D/A converter module stop bit Target module: 12-bit DA 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA23	—	12-bit A/D converter (unit 2) module stop bit
	MSTPA24	—	Module stop A24 setting bit
	MSTPA27	—	Module stop A27 setting bit
	MSTPA28	Data transfer controller module stop bit Target module: DTC 0: Release from module-stop state 1: Transition to module-stop state	DMA controller/data transfer controller module stop bit Target module: DMAC/DTC 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA29	—	Module stop A29 setting bit
	ACSE	—	All-module clock stop mode enable bit
MSTPCRB	MSTPB4	—	Serial communications interface 12 module stop bit
	MSTPB9	—	Event link controller module stop bit
	MSTPB25	—	Serial communications interface 6 module stop bit

Register	Bit	RX23T	RX26T
MSTPCRC	MSTPC24	—	Serial communications interface 11 module stop bit
	MSTPC26	—	Serial communications interface 9 module stop bit
	MSTPC27	—	Serial communications interface 8 module stop bit
	DSLPE	Deep sleep mode enable bit	—
MSTPCRD	—	—	Module stop control register D
RSTCKCR	—	—	Sleep mode return clock source switching register
OPCCR	—	Operating power control register	—

2.9 Register Write Protection Function

Table 2.19 is Comparative Overview of Register Write Protection Functions, and Table 2.20 is Comparison of Register Write Protection Function Registers.

Table 2.19 Comparative Overview of Register Write Protection Functions

Item	RX23T	RX26T
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, MEMWAIT	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2,OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR • Registers related to the clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	• Registers related to the clock generation circuit: HOCOWTCR	—
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.20 Comparison of Register Write Protection Function Registers

Register	Bit	RX23T	RX26T
PRCR	PRC2	Protect bit 2	—

2.10 Interrupt Controller

Table 2.21 is Comparative Overview of Interrupt Controllers, and Table 2.22 is Comparison of Interrupt Controller Registers.

Table 2.21 Comparative Overview of Interrupt Controllers

Item		RX23T (ICUb)	RX26T (ICUG)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ5 • Number of sources: 6 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • Digital filter function: Supported	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.

Item		RX23T (ICUb)	RX26T (ICUG)
Interrupts	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority level	Specified by registers.	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Interrupt from voltage detection 1 circuit (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Interrupt from voltage detection 2 circuit (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in RAM.
Return from low power consumption state	Sleep mode	Exit sleep mode by a non-maskable interrupt or any other interrupt source.	Exit sleep mode by any interrupt source.
	Deep sleep mode	Exit deep sleep mode by a non-maskable interrupt or any other interrupt source.	—
	All-module clock stop mode	—	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, IWDT, or TMR0 to TMR3).

Item		RX23T (ICUb)	RX26T (ICUG)
Return from low power consumption state	Software standby mode	Exit software standby mode by a non-maskable interrupt or IRQ0 to IRQ5 interrupt.	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, or IWDT).

Table 2.22 Comparison of Interrupt Controller Registers

Register	Bit	RX23T (ICUb)	RX26T (ICUG)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register r (r = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC transfer request enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 026 to 255)
	DTCE	DTC transfer request enable bit 0: DTC initiation disabled 1: DTC initiation enabled	DTC transfer request enable bit 0: Set to an interrupt source to the CPU, or DMAC activation source. 1: Set to the DTC activation source.
DMRSRm	—	—	DMAC activation source select register m (m = 0 to 7)
IRQCRi	—	IRQ control register i (i = 0 to 5)	IRQ control register i (i = 0 to 15)
IRQFLTE0	FLTEN6	—	IRQ6 digital filter enable bit
	FLTEN7	—	IRQ7 digital filter enable bit
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC0	FCLKSEL6	—	IRQ6 digital filter sampling clock setting bit
	FCLKSEL7	—	IRQ7 digital filter sampling clock setting bit
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	WDTST	—	WDT underflow/refresh error status flag
	RAMST	—	RAM error interrupt status flag
NMIER	WDTEN	—	WDT underflow/refresh error enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit
GRPBL0/ GRPBL1/ GRPBL2	—	—	Group BL0/BL1/BL2 interrupt request register
GRPAL0/ GRPAL1	—	—	Group AL0/ AL1 interrupt request register
GENBL0/ GENBL1/ GENBL2	—	—	Group BL0/BL1/BL2 interrupt request enable register
GENAL0/ GENAL1	—	—	Group AL0/ AL1 interrupt request enable register
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to Fh, 12h to 14)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register Write protection register

Note 1. On the RX23T Group, n = 250 to 255 correspond to a reserved area.

2.11 Buses

Table 2.23 is Comparative Overview of Buses, and Table 2.24 is Comparison of Bus Registers.

Table 2.23 Comparative Overview of Buses

Item		RX23T	RX26T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral module (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (DOC, RSCI, CANFD, and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, GPTW, HRPWM, and RSPI) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX23T	RX26T
Internal peripheral buses	Internal peripheral bus 5	—	• Connected to peripheral modules (RSCI, RSPIA, RI3C, and CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to the flash control module • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.24 Comparison of Bus Registers

Register	Bit	RX23T	RX26T
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPHB[1:0]	Internal peripheral bus 4 priority control bits b9 b8 0 0: Fixed priority 0 1: Toggled priority 1 0: Setting prohibited 1 1: Setting prohibited	Priority control bits for internal peripheral buses 4 and 5 b9 b8 0 0: Fixed priority 0 1: Toggled priority 1 0: Setting prohibited 1 1: Setting prohibited

2.12 Data Transfer Controller

Table 2.25 is Comparative Overview of Data Transfer Controllers, and Table 2.26 is Comparison of Data Transfer Controller Registers.

Table 2.25 Comparative Overview of Data Transfer Controllers

Item	RX23T (DTCa)	RX26T (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. (transferred by a DTC transfer request from ICU) • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX23T (DTCa)	RX26T (DTCb)
Transfer space	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	—	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Read skip of transferred information can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back skip can be executed when the transfer source address or transfer destination address is fixed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.26 Comparison of Data Transfer Controller Registers

Register	Bit	RX23T (DTCa)	RX26T (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.13 I/O ports

Table 2.27 is Comparative Overview of I/O Ports on 64-Pin Products, Table 2.28 is Comparative Overview of I/O Ports on 48-Pin Products, Table 2.29 is Comparison of I/O Port Functions, and Table 2.31 is Comparison of I/O Port Registers.

Table 2.27 Comparative Overview of I/O Ports on 64-Pin Products

Item	RX23T (64-Pin)	RX26T (64-Pin)
PORT0	P00 to P02	P00, P01
PORT1	P10, P11	P11
PORT2	P22 to P24	P20 to P22
PORT3	P30 to P33, P36, P37	P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	—	P52 to P54
PORT6	—	P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P94	P90 to P96
PORTA	PA2 to PA5	—
PORTB	PB0 to PB7	PB0 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTN	—	PN6, PN7

Table 2.28 Comparative Overview of I/O Ports on 48-Pin Products

Item	RX23T (48-Pin)	RX26T (48-Pin)
PORT0	—	P00
PORT1	P10, P11	P10, P11
PORT2	P22 to P24	P20, P21
PORT3	P36, P37	P36, P37
PORT4	P40 to P47	P40 to P44
PORT5	—	P52, P53
PORT6	—	P62
PORT7	P70 to P76	P71 to P76
PORT9	P93, P94	P91 to P95
PORTA	PA2, PA3	—
PORTB	PB0 to PB6	PB0 to PB6
PORTD	PD3 to PD6	PD3, PD5, PD7
PORTE	PE2	PE2
PORTN	—	PN6

Table 2.29 Comparison of I/O Port Functions

Item	Port Symbol	RX23T	RX26T
Input pull-up function	PORT0	P00 to P02	P00, P01
	PORT1	P10, P11	P10, P11
	PORT2	P22 to P24	P20 to P24, P27
	PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	P70 to P76	P70 to P76
	PORT8	—	P80 to P82
	PORT9	P91 to P94	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA5
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	—	—
	PORTD	PD3 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5
	PORTN	—	PN6, PN7
Open-drain output function	PORT0	P00 to P02	P00, P01
	PORT1	P10, P11	P10, P11
	PORT2	P22 to P24	P20 to P24, P27
	PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	P70 to P76	P70 to P76
	PORT8	—	P80 to P82
	PORT9	P91 to P94	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA5
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	—	—
	PORTD	PD3 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5
	PORTN	—	PN6
5 V tolerant	PORTB	PB1, PB2	PB1, PB2

Table 2.30 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX23T	RX26T
PORT0	Fixed to normal output	—	—
	Normal/high	P00 to P02	P00, P01
PORT1	Fixed to normal output	—	—
	Normal/high	P10, P11	P10, P11
PORT2	Fixed to normal output	—	—
	Normal/high	P22 to P24	P20 to P24, P27
PORT3	Fixed to normal output	P30 to P33, P36, P37	P36, P37
	Normal/high	—	P30 to P33
PORT4	Fixed to normal output	P40 to P47	P40 to P47
	Normal/high	—	—
PORT5	Fixed to normal output	—	P50 to P55
	Normal/high	—	—
PORT6	Fixed to normal output	—	P60 to P65
	Normal/high	—	—
PORT7	Fixed to normal output	—	—
	Fixed to high drive output	P71 to P76	—
	Normal/high	P70	P70
	Normal/high/large current output	—	P71 to P76
PORT8	Fixed to normal output	—	—
	Fixed to high drive output	—	—
	Normal/high	—	P80, P82
	Normal/high/large current output	—	P81
PORT9	Fixed to normal output	—	—
	Fixed to high drive output	—	—
	Normal/high	P91 to P94	P96
	Normal/high/large current output	—	P90 to P95
PORTA	Fixed to normal output	—	—
	Normal/high	PA2 to PA5	PA0 to PA5
PORTB	Fixed to normal output	—	PB1, PB2
	Fixed to high drive output	PB1, PB2, PB5	—
	Normal/high	PB0, PB3, PB4, PB6, PB7	PB0, PB3, PB4, PB6, PB7
	Normal/high/large current output	—	PB5
PORTD	Fixed to normal output	—	—
	Fixed to high drive output	PD3	—
	Normal/high	PD4 to PD7	PD0 to PD2, PD4 to PD7
	Normal/high/large current output	—	PD3
PORTE	Fixed to normal output	—	—
	Normal/high	—	PE0, PE1, PE3 to PE5
PORTN	Normal/high	—	PN6, PN7

Table 2.31 Comparison of I/O Port Registers

Register	Bit	RX23T	RX26T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 4, 7, 9, A, B, D, E)	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E, N)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7, 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A, B, D, E, N)
ODR0	B0, B2, B4, B6	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 3, 7, 9, A, B, D)	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 9, A, B, D, E)
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 2, 3, 7, 9, A, B, D)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 2 to 7, 9, A, B, D, E, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E, N)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7, 9, A, B, D)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A, B, D, E, N)
DSCR2	—	—	Drive capacity control register 2
POHSR1	—	—	Port output retention setting register 1
POHSR2	—	—	Port output retention setting register 2
POHCR	—	—	Port output retention control register
GPSEXT	—	—	General I/O pin select extended register

2.14 Multi-Function Pin Controller

Table 2.32 is Comparison of Multiplexed Pin Assignments, and Table 2.33 to Table 2.47 show a comparison of the multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX26T Group only, **orange text** pins that exist on the RX23T Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.32 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	PE2	○	○	○	○
	IRQ0 (input)	P10	○	○	×	○
		P52	×	×	○	○
		P93	○	○	×	×
		PE2	×	×	○	○
	IRQ1 (input)	P11	○	○	○	○
		P53	×	×	○	○
		P94	○	○	×	×
		P95	×	×	○	○
	IRQ2 (input)	P00	○	×	○	○
		P22	○	○	×	×
		P54	×	×	○	×
		PB1	○	○	×	×
		PB6	×	×	○	○
		PD4	○	○	○	×
	IRQ3 (input)	P24	○	○	×	×
		PB4	○	○	○	○
		PD5	○	○	×	×
	IRQ4 (input)	P01	○	×	○	×
		P23	○	○	×	×
		P96	×	×	○	×
		PA2	○	○	×	×
		PB1	×	×	○	○
	IRQ5 (input)	P02	○	×	×	×
		P70	○	○	○	×
		PB6	○	○	×	×
		PD6	○	○	○	×
		PN7	×	×	○	×
	IRQ6 (input)	P21			○	○
		P62			×	○
		PD5			○	○
	IRQ7 (input)	P20			○	○
	IRQ8 (input)	P64			○	×
		PB0			○	○
		PD7			○	○
	IRQ9 (input)	P65			○	×
		PB3			○	○
	IRQ10 (input)	P22			○	×
	IRQ14 (input)	P93			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	×	×	×
		P70	×	×	○	×
		PB3	○	○	○	○
	MTIOC0B(input/output)/ MTIOC0B# (input/output)	P30	○	×	×	×
		P93	○	○	×	×
		PB2	○	○	○	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	P94	○	○	×	×
		PB1	○	○	○	○
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	○	○	○
	MTIOC1A (input/output)/ MTIOC1A# (input/output)	P95	×	×	○	○
		PA5	○	×	×	×
	MTIOC1B (input/output)/ MTIOC1B# (input/output)	PA4	○	×	×	×
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	P94	×	×	○	○
		PA3	○	○	×	×
	MTIOC2B (input/output)/ MTIOC2B# (input/output)	PA2	○	○	×	×
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○	○	○
		P33	○	×	×	×
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○	○	○
	MTIOC3C (input/output)/ MTIOC3C# (input/output)	P32	○	×	×	×
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○	○	○
	MTIC5U (input)/ MTIC5U# (input)	P24	○	○	×	×
	MTIC5V (input)/ MTIC5V# (input)	P23	○	○	×	×
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○	○	×
	MTIOC6A (input/output)/ MTIOC6A# (input/output)	P93			○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95			○	○
	MTIOC6C (input/output)/ MTIOC6C# (input/output)	P92			○	○
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92			○	○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94			○	○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91			○	○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90			○	×
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P00			○	○
		P21			○	○
		PD7			○	○
	MTIOC9B (input/output)	P22			○	×
	MTIOC9B (input/output)/ MTIOC9B# (input/output)	P10			×	○
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P01			○	×
		P20			○	○
		PD6			○	×
	MTIOC9D (input/output)	P11			○	○
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	PN7			○	×
	MTCLKA (input)/ MTCLKA# (input)	P21	×	×	○	○
		P33	○	×	×	×
	MTCLKB (input)/ MTCLKB# (input)	P20	×	×	○	○
		P32	○	×	×	×
	MTCLKC (input)/ MTCLKC# (input)	P11	○	○	○	○
		P31	○	×	×	×
		P70	×	×	○	×
	MTCLKD (input)/ MTCLKD# (input)	P10	○	○	×	○
		P22	×	×	○	×
		P30	○	×	×	×
	ADSM0 (output)	PB2	○	○	○	○
	ADSM1 (output)	PB1			○	○
8-bit timer	TMO0 (output)	PB0	×	×	○	○
		PD3	○	○	○	○
	TMCI0 (input)	PB1	×	×	○	○
		PD4	○	○	○	×
	TMRI0 (input)	PB2	×	×	○	○
		PD5	○	○	○	○
	TMO1 (output)	P94	○	○	×	×
		PD6	○	○	○	×
	TMCI1 (input)	P92	○	×	×	×
	TMRI1 (input)	P93	○	○	×	×
		PD7	○	×	○	○
	TMO2 (output)	P20	×	×	○	○
		P23	○	○	×	×
		P92	×	×	○	○
	TMCI2 (input)	P24	○	○	×	×
	TMRI2 (input)	P22	○	○	○	×
	TMO3 (output)	P11	○	○	○	○
	TMCI3 (input)	P95	×	×	○	○
		PA5	○	×	×	×
	TMRI3 (input)	P10	○	○	×	○
	TMO4 (output)	P22			○	×
		P93			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
8-bit timer	TMCI4 (input)	P21			○	○
	TMRI4 (input)	P20			○	○
	TMRI5 (input)	PD7			○	○
	TMO6 (output)	P21			○	○
	TMCI6 (input)	PD4			○	×
	TMRI6 (input)	P70			○	×
		PD5			○	○
	TMRI7 (input)	P94			○	○
Port output enable 3	POE0# (input)	P70	○	○	○	×
	POE4# (input)	P96			○	×
	POE8# (input)	PB4	○	○	○	○
	POE9# (input)	P11			○	○
	POE10# (input)	PE2	○	○	○	○
	POE12# (input)	P01			○	×
		P10			×	○
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○	○	○
	SCK1 (input/output)	PD4	○	○	○	×
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P02	○	×	×	×
		PD6	○	○	○	×
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	P37	×	×	○	○
		P91	×	×	○	○
		PB1	○	○	×	×
		PB6	○	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	P36	×	×	○	○
		P90	×	×	○	×
		PB2	○	○	×	×
		PB5	○	○	○	○
		PD7	×	×	○	○
	SCK5 (input/output)	P70	×	×	○	×
		P93	○	○	×	×
		PB3	○	○	×	×
		PB7	○	×	×	×
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA2	○	○	×	×
		PB4	×	×	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P95			○	○
		PB1			○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	PB0			○	○
		PB2			○	○
	SCK6 (input/output)	PB3			○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P10			×	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Serial communications interface	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00			○	○
		P22			○	×
		PB4			○	○
		PB6			○	○
		PD6			○	×
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01			○	×
		P21			○	○
		PB3			○	○
		PB5			○	○
		PD4			○	×
	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	P20			○	○
		P22			○	×
		P95			○	○
	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	P21			○	○
		PB0			○	○
		PD7			○	○
	SCK008 (input/output)	P11			○	○
		P22			○	×
		P94			○	○
	TXDB008 (output)	P22			○	×
		P94			○	○
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	P20			○	○
		P96			○	×
	DE008 (output)	P20			○	○
		P96			○	×
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	P00			○	○
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	P01			○	×
		P10			×	○
		P93			○	○
		P94			○	○
	SCK009 (input/output)	P11			○	○
		P92			○	○
		PD7			○	○
	TXDB009 (output)	P11			○	○
		P92			○	○
		PD7			○	○
	CTS009# (input)/ RTS009# (output)/ SS009# (input)	P70			○	×
		PB3			○	○
	DE009 (output)	P70			○	×
		PB3			○	○
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P93			○	○
		PB6			○	○
		PD5			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Serial communications interface	TXD011 (output)/ TXDA011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P92			○	○
		PB5			○	○
		PD3			○	○
	SCK011 (input/output)	PB4			○	○
		PD4			○	×
	TXDB011 (output)	PB4			○	○
		PD4			○	×
	CTS011# (input)/ RTS011# (output)/ SS011# (input)	PB0			○	○
		PB4			○	○
		PD6			○	×
	DE011 (output)	PB0			○	○
		PD6			○	×
I²C bus interface	SCL0 (input/output)	PB1	○	○	○	○
	SDA0 (input/output)	PB2	○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	P20	×	×	○	○
		P24	○	○	×	×
		P93	○	○	×	×
		PA4	○	×	×	×
		PB3	○	○	○	○
	MOSIA (input/output)	P21	×	×	○	○
		P23	○	○	×	×
		PB0	○	○	○	○
	MISOA (input/output)	P22	○	○	○	×
		P94	○	○	×	×
		P95	×	×	○	○
		PA5	○	×	×	×
		PB4	×	×	○	○
	SSLA0 (input/output)	P30	○	×	×	×
		P70	×	×	○	×
		P94	×	×	○	○
		PA3	○	○	×	×
		PD6	○	○	○	×
	SSLA1 (output)	P31	○	×	×	×
		PA2	○	○	×	×
		PD7	○	×	○	○
	SSLA2 (output)	P32	○	×	×	×
		P92	○	×	×	×
		P93	×	×	○	○
	SSLA3 (output)	P33	○	×	×	×
		P91	○	×	×	×
		P92	×	×	○	○
	RSPCK0 (input/output)	P20			○	○
		P70			○	×
		P91			○	○
		P96			○	×
		PB5			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Serial peripheral interface	MOSI0 (input/output)	P21			○	○
		P72			○	○
		P93			○	○
		PB0			○	○
		PD3			○	○
	MISO0 (input/output)	P22			○	×
		P71			○	○
		P92			○	○
		P95			○	○
		PB6			○	○
	SSL00 (input/output)	P73			○	○
		P94			○	○
		PD5			○	○
		PD6			○	×
	SSL01 (output)	P74			○	○
	SSL01 (output)	P90			○	×
		PB4			○	○
		PD7			○	○
		P75			○	○
		P93			○	○
		P95			○	○
		PD4			○	×
	SSL03 (output)	P76			○	○
		P92			○	○
		P96			○	×
12-bit A/D converter	AN000 (input)	P40	○	○	○	○
	AN001 (input)	P41	○	○	○	○
	AN002 (input)	P42	○	○	○	○
	AN003 (input)	P43	○	○	○	○
	AN004 (input)	P44	○	○		
	AN005 (input)	P45	○	○		
	AN006 (input)	P46	○	○		
	AN007 (input)	P47	○	○		
	AN016 (input)	P11	○	○		
	AN017 (input)	P10	○	○		
	ADTRG0# (input)	PA4	○	×	×	×
		P20	×	×	○	○
		P93	×	×	○	○
	ADST0 (output)	P02	○	×	×	×
		PD6	○	○	○	×
		PN7	×	×	○	×
	AN100 (input)	P44			○	○
	AN101 (input)	P45			○	×
	AN102 (input)	P46			○	×
	AN103 (input)	P47			○	×
	ADTRG1# (input)	P21			○	○
		P95			○	○
	ADST1 (output)	P00			○	○
	AN200 (input)	P52			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
12-bit A/D converter	AN201 (input)	P53			○	○
	AN202 (input)	P54			○	×
	AN208 (input)	P62			×	○
	AN210 (input)	P64			○	×
	AN211 (input)	P65			○	×
	AN216 (input)	P20			○	○
	AN217 (input)	P21			○	○
	ADTRG2# (input)	P22			○	×
		PB0			○	○
	ADST2 (output)	P01			○	×
12-bit D/A converter	DA0 (output)	P64			○	×
	DA1 (output)	P65			○	×
Clock frequency accuracy measurement circuit	CACREF (input)	P00	×	×	○	○
		P01	○	×	×	×
		P23	○	○	×	×
		PB3	○	○	○	○
Comparator	CMPC00 (input)	P40	○	○	○	○
	CMPC01 (input)	P43	○	○	×	×
		P40	×	×	○	○
	CMPC02 (input)	P46	○	○	×	×
		P52	×	×	○	○
	CMPC10 (input)	P41	○	○	○	○
	CMPC11 (input)	P44	○	○	×	×
		P41	×	×	○	○
	CMPC12 (input)	P47	○	○	×	×
		P53	×	×	○	○
	CMPC20 (input)	P42	○	○	○	○
	CMPC21 (input)	P45	○	○	×	×
		P42	×	×	○	○
	CMPC22 (input)	P47	○	○	×	×
		P54	×	×	○	×
	CMPC30 (input)	P44			○	○
	CMPC31 (input)	P44			○	○
	CMPC33 (input)	P64			○	×
	CMPC40 (input)	P45			○	×
	CMPC41 (input)	P45			○	×
	CMPC43 (input)	P62			×	○
	CMPC50 (input)	P46			○	×
	CMPC51 (input)	P46			○	×
	CMPC53 (input)	P65			○	×
	COMP0 (output)	P24	○	○	×	×
		P00	×	×	○	○
	COMP1 (output)	P23	○	○	×	×
		P01	×	×	○	×
	COMP2 (output)	P22	○	○	○	×
	COMP4 (output)	P20			○	○
		P81			×	×
	COMP5 (output)	P21			○	○
		P82			×	×

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Comparator	CVREFC0 (input)	P11	○	○	×	×
		P53	×	×	○	○
	CVREFC1 (input)	P10	○	○	×	×
		P54	×	×	○	×
General purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P71			○	○
		PD7			○	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P74			○	○
		PD6			○	×
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P72			○	○
		PD5			○	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P75			○	○
		PD4			○	×
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P73			○	○
		PB6			○	○
		PD3			○	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P76			○	○
		PB5			○	○
		PD2			×	×
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P10			×	○
		PB6			○	○
		PD7			○	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P11			○	○
		PB5			○	○
		PD6			○	×
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71			○	○
		P95			○	○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74			○	○
		P92			○	○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72			○	○
		P94			○	○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75			○	○
		P91			○	○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73			○	○
		P93			○	○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76			○	○
		P90			○	×
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P95			○	○
		PB2			○	○
	GTIOC7A (input/output)	PD5			○	○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P92			○	○
		PB1			○	○
	GTIOC7B (input/output)	PD3			○	○
	GTETRGA (input)	P01			○	×
		P11			○	○
		P70			○	×
		P96			○	×
		PB4			○	○
		PD5			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
General purpose PWM timer	GTETRGB (input)	P01			○	×
		P10			×	○
		P70			○	×
		P96			○	×
		PB4			○	○
		PD4			○	×
	GTETRGC (input)	P01			○	×
		P11			○	○
		P70			○	×
		P96			○	×
		PB4			○	○
		PD3			○	○
	GTETRGD (input)	P01			○	×
		P10			×	○
		P70			○	×
		P96			○	×
		PB4			○	○
	GTADSM0 (output)	P94			○	○
		PB2			○	○
	GTADSM1 (output)	PB1			○	○
	GTCPPO0 (output)	P11			○	○
		P70			○	×
		PB4			○	○
	GTCPPO4 (output)	P96			○	×
	GTIU (input)	P00			○	○
		P21			○	○
		PB3			○	○
		PD7			○	○
	GTIV (input)	P10			×	○
		P22			○	×
		PB2			○	○
	GTIW (input)	P01			○	×
		P20			○	○
		PB1			○	○
		PD6			○	×
	GTOULO (output)	P74			○	○
		P92			○	○
	GTOUUP (output)	P71			○	○
		P95			○	○
	GTOVLO (output)	P75			○	○
		P91			○	○
	GTOVUP (output)	P72			○	○
		P94			○	○
	GTOWLO (output)	P76			○	○
		P90			○	×
	GTOWUP (output)	P73			○	○
		P93			○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)		RX26T (MPC)	
			64-Pin	48-Pin	64-Pin	48-Pin
Compare match timer W	TOC0 (output)	PB6			○	○
	TIC0 (input)	PB5			○	○
	TOC1 (output)	PB3			○	○
	TIC1 (input)	PB2			○	○
	TOC2 (output)	PB1			○	○
	TIC2 (input)	PB0			○	○
	TOC3 (output)	P11			○	○
	TIC3 (input)	P00			○	○
		P10			×	○
I^3C bus interface	SCL00 (input/output)	PB1			○	○
	SDA00 (input/output)	PB2			○	○
CAN FD module	CRX0 (input)	P22			○	×
		P93			○	○
		PB4			○	○
		PB6			○	○
	CTX0 (output)	P92			○	○
		PB3			○	○
		PB5			○	○
		PD7			○	○

Table 2.33 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX23T (n = 0 to 2)	RX26T (n = 0, 1)
P00PFS	PSEL[5:0]	—	P00 Pin function select bits
P01PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: CACREF	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTIW 011110b: COMP1 101100b: XD009/TXDA009/ SMOSI009/SSDA009
P02PFS	—	P02 pin function control register	—
P0nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (64-pin) P01: IRQ4 (64-pin) P02: IRQ5 (64/52-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ2 (48/64/80/100-pin) P01: IRQ4 (64/80/100-pin)

Table 2.34 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX23T (n = 0, 1)	RX26T (n = 0, 1)
P10PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKD 00101b: TMRI3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000010b: MTCLKD 000011b: MTIOC9B# 000100b: MTCLKD# 000101b: TMRI3 000111b: POE12# 001010b: CTS6#/RTS6#/SS6# 010100b: GTIOC3A 010101b: GTETRGB 010110b: GTIOC3A# 010111b: GTETRGD 011000b: GTIV 011101b: TIC3 101100b: TXD009/TXDA009/ SMOSI009/SSDA009
P11PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00101b: TMO3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKC 000011b: MTIOC3A# 000100b: MTCLKC# 000101b: TMO3 000111b: POE9# 001000b: MTIOC9D 010100b: GTIOC3B 010101b: GTETRGA 010110b: GTIOC3B# 010111b: GTETRGC 011000b: GTCPPO0 011101b: TOC3 101100b: SCK009 101101b: SCK008 101110b: TXDB009
P1nPFS	ASEL	Analog input function select bit	—

Table 2.35 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX23T (n = 2 to 4)	RX26T (n = 0 to 4, 7)
P20PFS	—	—	P20 pin function select register
P21PFS	—	—	P21 pin function select register
P22PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00101b: TMRI2 01101b: MISOA 11110b: COMP2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: MISOA 001110b: MISO0 010000b: CRX0 011000b: GTIV 011110b: COMP2 101100b: RXD008/SMISO008/ SSCL008 101101b: SCK008 101110b: TXDB008
P23PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: MOSIA 001110b: MOSI0 010000b: CTX0 011110b: COMP1 101100b: TXD008/TXDA008/ SMOSI008/SSDA008

Register	Bit	RX23T (n = 2 to 4)	RX26T (n = 0 to 4, 7)
P24PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI2 01101b: RSPCKA 11110b: COMP0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001101b: RSPCKA 001110b: RSPCK0 011110b: COMP0 101100b: CTS008#/RTS008#/ SS008# 101101b: SCK008 101110b: DE008
P27PFS	—	—	P27 pin function control register
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P22: IRQ2 (64/52/48 pin) P23: IRQ4 (64/52/48 pin) P24: IRQ3 (64/52/48 pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (48/64/80/100-pin) P21: IRQ6 (48/64/80/100-pin) P22: IRQ10 (64/80/100-pin) P23: IRQ11 (100-pin) P24: IRQ4 (100-pin) P27: IRQ15 (80/100-pin)
	ASEL	—	Analog function select bit

Table 2.36 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX23T (n = 0 to 3)	RX26T (n = 0 to 3, 6, 7)
P30PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 01101b: SSLA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001101b: SSLA0 001110b: SSL00 011000b: GTIV 011110b: COMP3 101100b: SCK008 101101b: CTS008#/RTS008# SS008# 101110b: DE008
P31PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1 001110b: SSL01 011000b: GTIU
P32PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 01101b: SSLA2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 001110b: SSL02 010100b: GTIOC3A 010101b: GTIOC7A 010110b: GTIOC3A# 010111b: GTIOC7A#

Register	Bit	RX23T (n = 0 to 3)	RX26T (n = 0 to 3, 6, 7)
P33PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 01101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 001110b: SSL03 010100b: GTIOC3B 010101b: GTIOC7B 010110b: GTIOC3B# 010111b: GTIOC7B# 011000b: GTCPPO0
P36PFS	—	—	P36 pin function control register
P37PFS	—	—	P37 pin function control register
P3nPFS	ISEL	—	Interrupt input function select bit

Table 2.37 Comparison of P4n Pin Function Control Registers (P4nPFS)

Register	Bit	RX23T	RX26T (n = 0 to 7)
P4nPFS	—	—	P4n pin function control register

Table 2.38 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX23T	RX26T (n = 0 to 5)
P5nPFS	—	—	P5n pin function control register

Table 2.39 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX23T	RX26T (n = 0 to 5)
P6nPFS	—	—	P6n pin function control register

Table 2.40 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX23T (n = 0 to 6)	RX26T (n = 0 to 6)
P70PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 000111b: POE0# 001010b: SCK5 001101b: SSLA0 001110b: RSPCK0 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO0 101100b: CTS009#/RTS009#/ SS009# 101110b: DE009
P71PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 001110b: MISO0 010100b: GTIOC0A 010101b: GTIOC4A 010110b: GTIOC0A# 010111b: GTIOC4A# 011000b: GTOUUP
P72PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 001110b: MOSI0 010100b: GTIOC1A 010101b: GTIOC5A 010110b: GTIOC1A# 010111b: GTIOC5A# 011000b: GTOVUP

Register	Bit	RX23T (n = 0 to 6)	RX26T (n = 0 to 6)
P73PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 001110b: SSL00 010100b: GTIOC2A 010101b: GTIOC6A 010110b: GTIOC2A# 010111b: GTIOC6A# 011000b: GTOWUP
P74PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 001110b: SSL01 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B# 011000b: GTOULO
P75PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 001110b: SSL02 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B# 011000b: GTOVLO
P76PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 001110b: SSL03 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B# 011000b: GTOWLO

Table 2.41 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX23T	RX26T (n = 0 to 2)
P8nPFS	—	—	P8n pin function control register

Table 2.42 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX23T (n = 1 to 4)	RX26T (n = 0 to 6)
P90PFS	PSEL[5:0]	—	P90 Pin function select bits
P91PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 001010b: RXD5/SMISO5/SSCL5 001110b: RSPCK0 010100b: GTIOC5B 010110b: GTIOC5B# 011000b: GTOVLO
P92PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 01101b: SSLA2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6D 000010b: MTIOC6C 000011b: MTIOC6D# 000100b: MTIOC6C# 000101b: TMO2 001101b: SSLA3 001110b: MISO0 010000b: CTX0 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B# 011000b: GTOULO 101100b: SCK009 101101b: TXD011/TXDA011/ SMOSI011/SSDA011 101110b: TXDB009 110011b: SSL03

Register	Bit	RX23T (n = 1 to 4)	RX26T (n = 0 to 6)
P93PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMRI1 01010b: SCK5 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7B 000010b: MTIOC6A 000011b: MTIOC7B# 000100b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001101b: SSLA2 001110b: MOSI0 010000b: CRX0 010100b: GTIOC6A 010110b: GTIOC6A# 011000b: GTOWUP 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: RXD011/SMISO011/ SSCL011 110011b: SSL02
P94PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO1 01101b: MISOA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7A 000010b: MTIOC2A 000011b: MTIOC7A# 000100b: MTIOC2A# 000101b: TMRI7 001101b: SSLA0 001110b: SSL00 010100b: GTIOC5A 010101b: GTADSM0 010110b: GTIOC5A# 011000b: GTOVUP 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: SCK008 101110b: TXDB008 110011b: SSL00
P95PFS	PSEL[5:0]	—	P95 pin function select register
P96PFS	PSEL[5:0]	—	P96 pin function select register
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ0 (64/52/48-pin) P94: IRQ1 (64/52/48 pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ14 (48/64/80/100 pin) P95: IRQ1 (48/64/80/100-pin) P96: IRQ4 (64/80/100-pin)

Table 2.43 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX23T (n = 2 to 5)	RX26T (n = 0 to 5)
PA0PFS	—	—	PA0 pin function select register
PA1PFS	—	—	PA1 pin function select register
PA2PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 01010b: CTS5#/RTS5#/SS5# 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/RTS6#/SS6# 001101b: SSLA1 001110b: SSL01 010100b: GTADSM1 101101b: RXD009/SMISO009/ SSCL009
PA3PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 01101b: SSLA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001101b: SSLA0 001110b: SSL00 010100b: GTADSM0 101100b: TXD009/TXDA009/ SMOSI009/SSDA009 101101b: SCK008 101110b: TXDB008
PA4PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 01001b: ADTRG0# 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001101b: RSPCKA 001110b: RSPCK0 101101b: TXD008/TXDA008/ SMOSI008/SSDA008

Register	Bit	RX23T (n = 2 to 5)	RX26T (n = 0 to 5)
PA5PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMCI3 01101b: MISOA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/SSCL6 001101b: MISOA 001110b: MISO0 101101b: RXD008/SMISO008/ SSCL008
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA2: IRQ4 (64/52/48 pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14 (100-pin) PA5: IRQ1 (80/100-pin)

Table 2.44 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX23T (n = 0 to 7)	RX26T (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 01101b: MOSIA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/SSDA6 001101b: MOSIA 001110b: MOSI0 011101b: TIC2 101100b: TXD008/TXDA008/ SMOSI008/SSDA008 101101b: CTS011#/RTS011#/ SS011# 101110b: DE011
PB1PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD5/SMISO5/SSCL5 01111b: SCL0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/SSCL6 001111b: SCL0 010100b: GTADSM1 010101b: GTIOC7B 010111b: GTIOC7B# 011000b: GTIW 011101b: TOC2 110010b: SCL00
PB2PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 01001b: ADSM0 01010b: TXD5/SMOSI5/SSDA5 01111b: SDA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/SSDA6 001111b: SDA0 010100b: GTADSM0 010101b: GTIOC7A 010111b: GTIOC7A# 011000b: GTIV 011101b: TIC1 110010b: SDA00

Register	Bit	RX23T (n = 0 to 7)	RX26T (n = 0 to 7)
PB3PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: RSPCKA 010000b: CTX0 011000b: GTIU 011101b: TOC1 101100b: CTS009#/RTS009#/ SS009# 101110b: DE009
PB4PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8#	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/SS5# 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: MISOA 001110b: SSL01 010000b: CRX0 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO0 101100b: CTS011#/RTS011#/ SS011# 101101b: SCK011 101110b: TXDB011
PB5PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5	Pin function select bits b5 b0 000000b: Hi-Z 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001110b: RSPCK0 010000b: CTX0 010100b: GTIOC2B 010101b: GTIOC3B 010110b: GTIOC2B# 010111b: GTIOC3B# 011101b: TIC0 101101b: TXD011/TXDA011/ SMOSI011/SSDA011

Register	Bit	RX23T (n = 0 to 7)	RX26T (n = 0 to 7)
PB6PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5	Pin function select bits b5 b0 000000b: Hi-Z 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001110b: MISO0 010000b: CRX0 010100b: GTIOC2A 010101b: GTIOC3A 010110b: GTIOC2A# 010111b: GTIOC3A# 011101b: TOC0 101101b: RXD011/SMISO011/ SSCL011
PB7PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5	Pin function select bits b5 b0 000000b: Hi-Z 001010b: SCK5 001100b: SCK12 001110b: SSL03 010100b: GTIOC1B 010110b: GTIOC1B# 101101b: SCK011 101110b: TXDB011
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (64/52/48-pin) PB4: IRQ3 (64/52/48-pin) PB6: IRQ5 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (48/64/80/100-pin) PB1: IRQ4 (48/64/80/100 pin) PB3: IRQ9 (48/64/80/100-pin) PB4: IRQ3 (48/64/80/100-pin) PB6: IRQ2 (48/64/80/100 pin)

Table 2.45 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX23T (n = 3 to 7)	RX26T (n = 0 to 7)
PD0PFS	—	—	PD0 pin function select register
PD1PFS	—	—	PD1 pin function select register
PD2PFS	—	—	PD2 pin function select register
PD3PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/SSDA1	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/SMOSI1/SSDA1 001110b: MOSI0 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A# 010111b: GTIOC7B 101101b: TXD011/TXDA011/ SMOSI011/SSDA011
PD4PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 01010b: SCK1	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001110b: SSL02 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B# 101101b: SCK011 101110b: TXDB011
PD5PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 01010b: RXD1/SMISO1/SSCL1	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/SMISO1/SSCL1 001110b: SSL00 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A# 010111b: GTIOC7A 101101b: RXD011/SMISO011/ SSCL011

Register	Bit	RX23T (n = 3 to 7)	RX26T (n = 0 to 7)
PD6PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/SS1# 01101b: SSLA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/RTS1#/SS1# 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: SSLA0 001110b: SSL00 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B# 011000b: GTIW 101101b: CTS011#/RTS011#/ SS011# 101110b: DE011
PD7PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI1 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA1 001110b: SSL01 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A# 011000b: GTIU 101100b: SCK009 101101b: TXD008/TXDA008/ SMOSI008/SSDA008 101110b: TXDB009
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (64/52/48 pin) PD5: IRQ3 (64/52/48 pin) PD6: IRQ5 (64/52/48 pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (64/80/100-pin) PD5: IRQ6 (48/64/80/100 pin) PD6: IRQ5 (64/80/100-pin) PD7: IRQ8 (48/64/80/100-pin)

Table 2.46 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX23T (n = 2)	RX26T (n = 0 to 5)
PE0PFS	—	—	PE0 pin function control register
PE1PFS	—	—	PE1 pin function control register
PE2PFS	PSEL[4:0] (RX23T) PSEL[5:0] (RX26T)	Interrupt input function select bit b4 b0 00000b: Hi-Z 00111b: POE10#	Interrupt input function select bit b5 b0 000000b: Hi-Z 000111b: POE10#
PE3PFS	—		PE3 pin function control register
PE4PFS	—		PE4 pin function control register
PE5PFS	—	—	PE5 pin function control register
PEnPFS	ISEL	—	Interrupt input function select bit

Table 2.47 Comparison of PN7 Pin Function Control Registers (PN7PFS)

Register	Bit	RX23T	RX26T
PN7PFS	—	—	PN7 pin function control register

2.15 Multi-Function Timer Pulse Unit 3

Table 2.48 is Comparative Overview of Multi-Function Timer Pulse Unit 3, and Table 2.49 is Comparison of Multi-Function Timer Pulse Unit 3 Registers.

Table 2.48 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX23T (MTU3c)	RX26T (MTU3d)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	11 clocks for each channel (14 for MTU0, 12 for MTU2, 10 for MTU5, and 4 for MTU1 and MTU2 (when LWA = 1))	11 clocks for each channel (14 for MTU0 and MTU9, 12 for MTU2, 10 for MTU5, and 4 for MTU1 and MTU2 (when LWA = 1))
Operating frequency	Up to 40 MHz	Up to 120 MHz
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4] • Ability to specify buffer operation	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation
	[MTU3, MTU4] • Ability to produce waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode

Item	RX23T (MTU3c)	RX26T (MTU3d)
Available operations	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[MTU5] • Can be used as a dead time compensation counter.	[MTU5] • Can be used as a dead time compensation counter.
	—	[MTU6, MTU7] • Through linked operation with MTU9, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
Interrupt skipping function	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D converter start request delay function Ability to synchronize operation with PWM output	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D converter start request delay function Ability to synchronize operation with PWM output
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.49 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX23T(MTU3c)	RX26T (MTU3d)
TMDR1	BFE	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF make normal operation 1: MTU0.TGRE and MTU0.TGRF make buffer operation	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF make normal operation 1: MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF make buffer operation
TMDR2B	—	—	Timer mode register 2B
TBTM	TTSE	Timing select E bits 0: Transfer from MTU0.TGRF to MTU0.TGRE is made at compare match E of MTU0 1: Transfer to MTU0.TGRF to MTU0.TGRE is made when MTU0.TCNT is cleared	Timing select E bits 0: Transfer from MTU0.TGRF to MTU0.TGRE, or from MTU9.TGRF to MTU9.TGRE is made at compare match E of MTU0 or MTU9 1: Transfer from MTU0.TGRF to MTU0.TGRE, or from MTU9.TGRF to MTU9.TGRE is made when MTU0.TCNT or MTU9.TCNT is cleared
TSYCR	—	—	Timer synchronization clear register
TSTRA/ TSTR (RX23T) TSTRA/ TSTRB/ TSTR (RX26T)	CST9	—	Counter start 9 bit
TSYRA (RX23T) TSYRA/ TSYRB (RX26T)	SYNC9	—	Timer synchronization 9 bit
TCSYSTR	SCH7	—	Synchronization start 7 bit
	SCH6	—	Synchronization start 6 bit
	SCH9	—	Synchronization start 9 bit
TRWERB	—	—	Timer read/write enable register B
TOERB	—	—	Timer output master enable register B
TOCR1B	—	—	Timer output control register 1B
TOCR2B	—	—	Timer output control register 2B
TOLBRB	—	—	Timer output level buffer register B
TGCRB	—	—	Timer gate control register B
TCNTSB	—	—	Timer sub-counter B
TCDRB	—	—	Timer period data register B
TCBRB	—	—	Timer period buffer register B
TDDRB	—	—	Timer dead time data register B
TDERB	—	—	Timer dead time enable register B

Register	Bit	RX23T(MTU3c)	RX26T (MTU3d)
TBTERB	—	—	Timer buffer transfer setting register B
TWCRB	—	—	Timer waveform control register B
NFCRn	—	Noise filter control register n (n = 0 to 4, C)	Noise filter control register n (n = 0 to 4, 6, 7, 9, C)
TITMRB	—	—	Timer interrupt skipping mode register B
TITCR1B	—	—	Timer interrupt skipping setting register 1B
TITCNT1B	—	—	Timer interrupt skipping counter 1B
TITCR2B	—	—	Timer interrupt skipping setting register 2B
TITCNT2B	—	—	Timer interrupt skipping counter 2B
TADSTRGR0	TADSMEN0	—	ADSM0 pin output enable bit
TADSTRGR1	—	—	A/D conversion start request select register 1

2.16 Port Output Enable 3

Table 2.50 is Comparative Overview of Port Output Enable 3, and Table 2.51 is Comparison of Port Output Enable 3 Registers.

Table 2.50 Comparative Overview of Port Output Enable 3

Item	RX23T (POE3b)	RX26T (POE3D)
Pin status while output is disabled	• High-impedance • General I/O port	• High-impedance • General I/O port
Output stop control target pins	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B)
Conditions for generating an output stop request	• Input pin changes: When signal input occurs on pin POE0#, POE8#, or POE10# • Register settings are specified. • Detection of stopped oscillation on clock oscillator • Detection of comparator C (CMPC) output	• Input pin changes: When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# • SPOER register settings are specified. • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output

Item	RX23T (POE3b)	RX26T (POE3D)
Conditions for generating an output stop request	• Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D	• Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B
Functions	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE8#, and POE10# input pins.	• Falling-edge detection or low level detection can be set for each of the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, and POE9# pins. For low level detection, the sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the sampling count can be selected from 4 times, 8 times, and 16 times.
	• Pins for complementary PWM output from the MTU and the MTU0 pin can be driven to the high impedance state on the detection of falling edges or sampling of the low level on the POE0#, POE8#, or POE10# pin.	• Output on all control target pins can be stopped on detection of the falling edge of input or low level on the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# pin.
	• Pins for complementary PWM output from the MTU and the MTU0 pin can be driven to the high-impedance state when oscillation stop is detected in the clock generation circuit.	• Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit.
	• When output levels on pins for complementary PWM output from the MTU are compared and simultaneous output of the active level continues for one or more cycles, output on the pins can be driven to the high-impedance state.	• It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be stopped.

Item	RX23T (POE3b)	RX26T (POE3D)
Functions		• It is possible to compare levels output on GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 pins), and when simultaneous output of the active level continues for at least one cycle, output on the pins can be stopped.
	• Pins for complementary PWM output from the MTU and the MTU0 pin can be driven to the high-impedance state by comparator detection of the comparator (CMPC).	• Output on all control target pins can be stopped on detection of output of comparator C (CMPC).
	• Pins for complementary PWM output from the MTU and the MTU0 pin can be driven to the high-impedance state by the setting of POE register.	• Output on all control target pins can be stopped by modifying settings of POE registers.
	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.
		• Signals output from the MTU output pins (MTU0 to MTU4, MTU6, MTU7, MTU9) and GPTW output pins (GPTW0 to GPTW7) can be used to mask output stop requests by the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, POE9# pins and COMP0 to COMP5 level detection signal.

Table 2.51 Comparison of Port Output Enable 3 Registers

Register	Bit	RX23T (POE3b)	RX26T (POE3D)
ICSR1	POE0M[1:0] (RX23T) POE0M[3:0] (RX26T)	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Samples the low level of the POE0# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE0# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE0# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE0# pin input. 0 0 0 1: Samples the input from the POE0# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE0# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE0# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE0# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE0# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE0# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	POE0 sampling count select bit
	INV	—	POE0# pin input invert bit
ICSR2	—	—	Input level control/status register 2

Register	Bit	RX23T (POE3b)	RX26T (POE3D)
ICSR3	POE8M[1:0] (RX23T) POE8M[3:0] (RX26T)	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Samples the low level of the POE8# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE8# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE8# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE8# pin input. 0 0 0 1: Samples the input from the POE8# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE8# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE8# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE8# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE8# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE8# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	POE8 sampling count select bit
	INV	—	POE8# pin input invert bit

Register	Bit	RX23T (POE3b)	RX26T (POE3D)
ICSR4	POE10M[1:0] (RX23T) POE10M[3:0] (RX26T)	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Samples the low level of the POE10# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE10# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE10# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE10# pin input. 0 0 0 1: Samples the input from the POE10# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE10# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE10# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE10# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE10# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE10# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	POE10 sampling count select bit
	INV	—	POE10# pin input invert bit
ICSR5	—	—	Input level control/status register 5
ICSR7	—	—	Input level control/status register 7
ICSR8	—	—	Input level control/status register 8
OCSR2	—	—	Output level control/status register 2
OCSR3	—	—	Output level control/status register 3
OCSR4	—	—	Output level control/status register 4

Register	Bit	RX23T (POE3b)	RX26T (POE3D)
OCSR5	—	—	Output level control/status register 5
ALR2	—	—	Active level register 2
ALR3	—	—	Active level register 3
ALR4	—	—	Active level register 4
ALR5	—	—	Active level register 5
SPOER	—	Software port output enable register SPOER is an 8-bit register.	Software port output enable register SPOER is a 16-bit register.
	MTUCH67HIZ	—	MTU6 and MTU7 pin output stop enable bit
	GPT01HIZ	—	GPTW0 and GPTW1 pin output stop enable bit
	GPT23HIZ	—	GPTW2 and GPTW3 pin output stop enable bit
	MTUCH9HIZ	—	MTU9 pin output stop enable bit
	GPT02HIZ	—	GPTW0 to GPTW2 pin output stop enable bit
	GPT46HIZ	—	GPTW4 to GPTW6 pin output stop enable bit
	GPT79HIZ	—	GPTW7 pin output stop enable bit
POECR1	MTU0A1ZE	MTIOC0A P31 pin high-impedance enable bit	—
	MTU0B1ZE	MTIOC0B P30 pin high-impedance enable bit	—
	MTU0B2ZE	MTIOC0B P93 pin high-impedance enable bit	—
	MTU0C1ZE	MTIOC0C P94 pin high-impedance enable bit	—
POECR2	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
POECR3	—	—	Port output enable control register 3
POECR4	IC1ADDMT34ZE	—	Bit for adding POE0F to the MTU3 and MTU4 output stop conditions
	IC2ADDMT34ZE	—	Bit for adding POE4F to the MTU3 and MTU4 output stop conditions
	IC5ADDMT34ZE	—	Bit for adding POE11F to the MTU3 and MTU4 output stop conditions
	IC6ADDMT34ZE	—	Bit for adding POE12F to the MTU3 and MTU4 output stop conditions
	IC8ADDMT34ZE	—	Bit for adding POE9F to the MTU3 and MTU4 output stop conditions
POECR4B	—	—	Port output enable control register 4B
POECR5	IC2ADDMT0ZE	—	Bit for adding POE4F to the MTU0 output stop conditions
	IC3ADDMT0ZE	—	Bit for adding POE8F to the MTU0 output stop conditions
	IC5ADDMT0ZE	—	Bit for adding POE11F to the MTU0 output stop conditions
	IC6ADDMT0ZE	—	Bit for adding POE12F to the MTU0 output stop conditions
	IC8ADDMT0ZE	—	Bit for adding POE9F to the MTU0 output stop conditions
POECR6	—	—	Port output enable control register 6

Register	Bit	RX23T (POE3b)	RX26T (POE3D)
POECR6B	—	—	Port output enable control register 6B
POECR7	—	—	Port output enable control register 7
POECR8	—	—	Port output enable control register 8
POECR9	—	—	Port output enable control register 9
POECR10	—	—	Port output enable control register 10
POECR11	—	—	Port output enable control register 11
PMMCR0	—	—	Port mode mask control register 0
PMMCR1	—	—	Port mode mask control register 1
PMMCR2	—	—	Port mode mask control register 2
POECMPFR	C3FLAG	—	Comparator channel 3 output detection flag
	C4FLAG	—	Comparator channel 4 output detection flag
	C5FLAG	—	Comparator channel 5 output detection flag
POECMPSEL	POEREQ3	—	Comparator channel 3 output stop enable bit
	POEREQ4	—	Comparator channel 4 output stop enable bit
	POEREQ5	—	Comparator channel 5 output stop enable bit
POECMPEXm	—	—	Port output enable comparator request extension select register m (m = 0 to 8)
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2
M6SELR	—	—	MTU6 pin select register
M7SELR1	—	—	MTU7 pin select register 1
M7SELR2	—	—	MTU7 pin select register 2
M9SELR1	—	—	MTU9 pin select register 1
M9SELR2	—	—	MTU9 pin select register 2
G0SELR	—	—	GPTW0 pin select register
G1SELR	—	—	GPTW1 pin select register
G2SELR	—	—	GPTW2 pin select register
G3SELR	—	—	GPTW3 pin select register
G4SELR	—	—	GPTW4 pin select register
G5SELR	—	—	GPTW5 pin select register
G6SELR	—	—	GPTW6 pin select register
G7SELR	—	—	GPTW7 pin select register
IMCR0	—	—	Input signal mask control register 0
IMCR1	—	—	Input signal mask control register 1
IMCR2	—	—	Input signal mask control register 2
IMCR3	—	—	Input signal mask control register 3
IMCR4	—	—	Input signal mask control register 4
IMCR5	—	—	Input signal mask control register 5
IMCR6	—	—	Input signal mask control register 6
IMCR9	—	—	Input signal mask control register 9
IMCR10	—	—	Input signal mask control register 10
IMCR11	—	—	Input signal mask control register 11
IMCR12	—	—	Input signal mask control register 12
IMCR13	—	—	Input signal mask control register 13
IMCR14	—	—	Input signal mask control register 14

2.17 8-bit Timer

Table 2.52 is Comparative Overview of 8-Bit Timers, and Table 2.53 is Comparison of 8-Bit Timer Registers.

Table 2.52 Comparative Overview of 8-Bit Timers

Item	RX23T (TMR)	RX26T (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal	Selectable among compare match A or B, or an external counter reset signal
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, and TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, and TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0, TMR2, TMR4, or TMR6
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of SCI basic clock

Item	RX23T (TMR)	RX26T (TMRb)
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

Table 2.53 Comparison of 8-Bit Timer Registers

Register	Bit	RX23T (TMR)	RX26T (TMRb)
TCSTR	—	—	Timer counter start register

2.18 Compare Match Timer

Table 2.54 is Comparative Overview of Compare Match Timers.

Table 2.54 Comparative Overview of Compare Match Timers

Item	RX23T (CMT)	RX26T (CMT)
Count clocks	• Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	• Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output upon a CMT1 compare match.
Event link function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

2.19 Independent Watchdog Timer

Table 2.55 is Comparative Overview of Independent Watchdog Timers, and Table 2.56 is Comparison of Independent Watchdog Timer Registers.

Table 2.55 Comparative Overview of Independent Watchdog Timers

Item	RX23T (IWDTa)	RX26T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error occurs — Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX23T (IWDTa)	RX26T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.56 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX23T (IWDTa)	RX26T (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request output is enabled. 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled when entering sleep, software standby, and deep sleep mode.	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, and all-module clock stop mode.

2.20 Serial Communications Interface

Table 2.57 is Comparative Overview of Serial Communications Interfaces, Table 2.58 is Comparison of Serial Communications Interface Channel Specifications, and Table 2.59 is Comparison of Serial Communications Interface Registers.

Table 2.57 Comparative Overview of Serial Communications Interfaces

Item		RX23T (SCIg)	RX26T (SCIk, SCIh)
Number of channels		• SCIg: 2 channels	• SCIk: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1, SCI5, SCI6).
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	• Transmit end, transmit data empty, receive data full, receive error, and data coincidence (SCI1, SCI5, SCI6) • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Data match detection	—	Compares receive data and comparison data register, and generates interrupt when they match (SCI1, SCI5, SCI6).
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1, SCI5, SCI6).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI1, SCI5, SCI6).

Item		RX23T (SCIg)	RX26T (SCIk, SCIh)
Asynchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag (SCI5, SCI6).
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, SCI12).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection

Item		RX23T (SCIg)	RX26T (SCIk, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame reception	—	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	—	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	—	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.58 Comparison of Serial Communications Interface Channel Specifications

Item	RX23T (SCIg)	RX26T (SCIk, SCIh)
Asynchronous mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI1, SCI5	SCI1, SCI5, SCI6, SCI12
Data match detection	—	SCI1, SCI5, SCI6
Extended serial mode	—	SCI12
TMR clock input	SCI5	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5	PCLKB: SCI1, SCI5, SCI6, SCI12

Table 2.59 Comparison of Serial Communications Interface Registers

Register	Bit	RX23T (SCIg)	RX26T (SCIk, SCIh)
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 only) Available compare match output varies per SCI channel.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) Available compare match output varies per SCI channel.
	ITE	—	Immediate transmission enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
SPMR	MSS	Master/slave select bit 0: TXDn pin: Transmit, RXDn pin: Receive (master mode) 1: TXDn pin: Receive, RXDn pin: Transmit (slave mode)	Master/slave select bit 0: SMOSIn pin: Transmit, SMISOn pin: Receive (master mode) 1: SMOSIn pin: Receive, SMISOn pin: Transmit (slave mode)
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control Field 0 data register
CF0CR	—	—	Control Field 0 compare enable register
CF0RR	—	—	Control Field 0 receive data register
PCF1DR	—	—	Primary Control Field 1 data register
SCF1DR	—	—	Secondary Control Field 1 data register
CF1CR	—	—	Control Field 1 compare enable register
CF1RR	—	—	Control Field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register
PRDFR0	—	—	Product function select register 0

2.21 I²C Bus Interface

Table 2.60 is Comparative Overview of I2C Bus Interfaces.

Table 2.60 Comparative Overview of I²C Bus Interfaces

Item	RX23T (RIICa)	RX26T (RIICa)
Communication format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode is supported (up to 400 kbps)	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX23T (RIICa)	RX26T (RIICa)
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	• Four sources: — Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end	• Four sources: — Error in transfer or occurrence of events Detection of arbitration lost, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Item	RX23T (RIICa)	RX26T (RIICa)
RIIC operating modes	• 4 modes: — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode	• 4 modes: — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode
Event link function (output)	—	• Four sources (RIIC0): — Error in transfer or occurrence of events Detection of arbitration lost, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end

2.22 Serial Peripheral Interface

Table 2.61 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.62 is Comparison of Serial Peripheral Interface Registers.

Table 2.61 Comparative Overview of Serial Peripheral Interfaces

Item	RX23T (RSPIa)	RX26T (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). — Width at high level: 4 cycles of PCLK — Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX23T (RSPIa)	RX26T (RSPId)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — RSPI error interrupt (mode fault, overrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt

Item	RX23T (RSPIa)	RX26T (RSPId)
Event link function (output)	—	• The following events can be output to the event link controller. (RSPI0) — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle events — Communication completion events
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.62 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX23T (RSPIa)	RX26T (RSPId)
SPSR	UDRF	—	Underrun error flag
	SPCF	—	Communication completion flag
SPDR	—	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Word access (SPDCR.SPLW = 0, SPDCR.SPBYT = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

2.23 CRC Calculator

Table 2.63 is Comparative Overview of CRC Calculators, and Table 2.64 is Comparison of CRC Calculator Registers.

Table 2.63 Comparative Overview of CRC Calculators

Item	RX23T (CRC)	RX26T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: $X^{16} + X^{15} + X2 + 1$ $X^{16} + X^{12} + X5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X9 + X^8 + X^6 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state	

Table 2.64 Comparison of CRC Calculator Registers

Register	Bit	RX23T (CRC)	RX26T (CRCA)
CRCCR	GPS[1:0] (RX23T) GPS[2:0] (RX26T)	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Supported access sizes • Byte access	CRC data input register Supported access sizes • Longword access (32-bit CRC selected) • Byte access (16-bit or 8-bit CRC selected)
CRCDOR	—	CRC data output register Supported access sizes • Word access The lower byte (b7 to b0) is used when generating 8-bit CRC.	CRC data output register Supported access sizes • Longword access (32-bit CRC selected) • Word access (16-bit CRC selected) • Byte access (8-bit CRC selected)

2.24 12-Bit A/D Converter

Table 2.65 is Comparative Overview of 12-Bit A/D Converters, and Table 2.66 is Comparison of 12-Bit A/D Converter Registers.

Table 2.65 Comparative Overview of 12-Bit A/D Converters

Item	RX23T (S12ADE)	RX26T (S12ADHa)
Number of units	1 unit	Three units (S12AD, S12AD1, and S12AD2) (For products with a RAM capacity of 64 KB) Two units (S12AD and S12AD2) (For products with a RAM capacity of 48 KB)
Input channels	10 channels	S12AD: 4 channels S12AD1: 4 channels S12AD2: 14 channels (For products with a RAM capacity of 64 KB) S12AD: 7 channels S12AD2: 8 channels (For products with a RAM capacity of 48 KB)
Extended analog function	Internal reference voltage	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1 µs per channel (when A/D conversion clock (ADCLK) = 40 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLK to ADCLK frequency division ratio = 1:1, 1:2, 2:1, 4:1, 8:1 • ADCLK is set by using the clock generation circuit.	• Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 2:1, 4:1, 1:2 • ADCLK is set by using the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.

Item	RX23T (S12ADE)	RX26T (S12ADHa)
Data registers	• 10 registers for analog input, one register for A/D-converted data duplication in double trigger mode, and two registers for A/D-converted data duplication during extended operation in double trigger mode	• 22 registers for analog input (S12AD: 4 registers, S12AD1: 4 registers, S12AD2: 14 registers), one register for A/D-converted data duplication in double trigger mode for each unit, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD2)
	• One register for internal reference	• One register for internal reference (S12AD2)
	• One register for self-diagnosis	• One register for self-diagnosis for each unit
	• The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion	• The results of A/D conversion are stored in 12-bit A/D data registers.
	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode
	• Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.
	• Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX23T (S12ADE)	RX26T (S12ADHa)
Operating modes	• Single scan mode: — A/D conversion is performed only once on a maximum of 10 arbitrarily selected analog inputs. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on a maximum of 10 arbitrarily selected analog inputs. • Group scan mode: — A maximum of 10 analog inputs arbitrarily selected are divided into two groups (group A and group B), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A and B (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group A priority control selected) — When there is a trigger input of group A during A/D conversion of group B, A/D conversion of group B is suspended and A/D conversion of group A is performed. — A setting is possible for restarting (re-scanning) A/D conversion of group B at the completion of A/D conversion of group A.	The operating mode can be set individually for each of three units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Arbitrarily selected analog input channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) — If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. — The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.

Item	RX23T (S12ADE)	RX26T (S12ADHa)
Conditions for A/D conversion start	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU) or 8-bit timer (TMR) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) pin.	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), general purpose PWM timer (GPTW), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of three units).
Functions	• Channel-dedicated sample-and-hold function (three channels) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set.) • Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Order of channel conversion can be specified for each unit. • Input signal amplification function using the programmable gain amplifier (each unit has 3 channels) (Only for products with a RAM capacity of 64 KB)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan . • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan.	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each unit). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each unit).

Item	RX23T (S12ADE)	RX26T (S12ADHa)
Interrupt sources	• In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, and an A/D scan end interrupt request (GBADI) for group B is generated on completion of group B scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a double scan of group A, and an A/D scan end interrupt request (GBADI) for group B is generated on completion of group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function. • S12ADI / S12ADI1 / S12ADI2, S12GBADI / S12GBADI1 / S12GBADI2, S12GCADI / S12GCADI1 / S12GCADI2 The above interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).
Event link function	—	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.66 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX23T(S12ADE)	RX26T(S12ADHa)
ADDRy	—	A/D data register y (y = 0 to 7, 16, 17)	A/D data register y (y = 0 to 3: S12AD, y = 0 to 3: S12AD1, y = 0 to 11, 16, 17: S12AD2)
ADTSDR	—	—	A/D temperature sensor data register
ADCSR	DBLANS[4:0] (S12AD)	Double trigger target channel select bits b0 b4 00000: AN000 00001: AN001 00010: AN002 00011: AN003 00100: AN004 00101: AN005 00110: AN006 00111: AN007 10000: AN016 10001: AN017	Double trigger target channel select bits b0 b4 00000: AN000 00001: AN001 00010: AN002 00011: AN003 00100: AN004 00101: AN005 00110: AN006
	DBLANS[4:0] (S12AD1)	—	Double trigger target channel select bits
	DBLANS[4:0] (S12AD2)	—	Double trigger target channel select bits
ADANSA0	—	A/D channel select register A0	—
S12AD. ADANSA0	—	—	A/D channel select register A0
S12AD1. ADANSA0	—	—	A/D channel select register A0
S12A2. ADANSA0	—	—	A/D channel select register A0
ADANSA1	ANSA100/ ANSA101	A/D conversion channel select bit 0: Exclude AN016 and AN017 from conversion targets 1: Include AN016 and AN017 in conversion targets	A/D conversion channel select bit Set whether to include AN216 and AN217 in conversion targets. 0: Exclude from conversion targets 1: Include in conversion targets
ADANSB0	—	A/D channel select register B0	—
S12AD. ADANSB0	—	—	A/D channel select register B0
S12AD1. ADANSB0	—	—	A/D channel select register B0
S12A2. ADANSB0	—	—	A/D channel select register B0
ADANSB1	ANSB100/ ANSB101	A/D conversion channel select bit 0: Exclude AN016 and AN017 from conversion targets 1: Include AN016 and AN017 in conversion targets	A/D conversion channel select bit Set whether to include AN216 and AN217 in conversion targets. 0: Exclude from conversion targets 1: Include in conversion targets

Register	Bit	RX23T(S12ADE)	RX26T(S12ADHa)
S12AD. ADANSC0	—	—	A/D channel select register C0
S12AD1. ADANSC0	—	—	A/D channel select register C0
S12A2. ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 13)
ADADS0	—	A/D-converted value addition/average channel select register 0	—
S12AD. ADADS0	—	—	A/D-converted value addition/average channel select register 0
S12AD1. ADADS0	—	—	A/D-converted value addition/average channel select register 0
S12AD2. ADADS0	—	—	A/D-converted value addition/average channel select register 0
ADADS1	ADS100/ ADS101	A/D-converted value addition/average channel select bit 0: Not selectable between A/D-converted value addition mode and average mode for AN016 and AN017 1: Selectable between A/D-converted value addition mode and average mode for AN016 and AN017	A/D-converted value addition/average channel select bit Set A/D-converted value addition mode or average mode for AN216 and AN217 0: Disable A/D-converted value addition mode and average mode 1: Enable A/D-converted value addition mode and average mode
ADCER	ASE	—	A/D data register automatic setting enable bit
ADSTRGR	TRSB[5:0] (RX23T) TRSB[6:0] (RX26T)	A/D conversion start trigger select bits for Group B	A/D conversion start trigger select bits for Group B
	TRSA[5:0] (RX23T) TRSA[6:0] (RX26T)	A/D conversion start trigger select bits	A/D conversion start trigger select bits
ADEXICR	TSSAD	—	Temperature sensor output A/D-converted value addition/average mode select bit
	TSSA	—	Temperature sensor output A/D conversion select bit
	TSSB	—	Group B temperature sensor output A/D conversion select bit
	OCSB	—	Group B internal reference voltage A/D conversion select bit

Register	Bit	RX23T(S12ADE)	RX26T(S12ADHa)
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADGCTRGR2	—	—	A/D group C trigger select register 2
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, O)	A/D sampling state register n (n = 0 to 11, L, T, O)
		Initial value after a reset differs.	
ADSHCR	—	A/D sample and hold circuit control register	A/D sample and hold circuit control register
		Initial value after a reset differs.	
	SSTSH[7:0]	These bits set a sampling time in the range from 4 to 255 state cycles.	These bits set a sampling time between 12 and 252 clock cycles.
ADSHCR	SHANS[2:0] (RX23T) SHANS[0] SHANS[1] SHANS[2] (RX26T)	Channel-dedicated sample and hold circuit bypass select bits Whether to use the channel-dedicated sample & hold circuit for AN000 to AN002 or bypass it without using it can be selected. 0: The channel-dedicated sample and hold circuit is bypassed. 1: The channel-dedicated sample and hold circuit is used.	Channel-dedicated sample and hold circuit bypass select bits Whether to use the channel-dedicated sample & hold circuit for AN000 or AN100 channel/AN001 or AN101 channel/AN002 or AN102 channel can be selected. 0: The channel-dedicated sample and hold circuit is disabled. 1: The channel-dedicated sample and hold circuit is enabled.
ADSHMSR	—	—	A/D sample and hold operating mode select register

Register	Bit	RX23T(S12ADE)	RX26T(S12ADHa)
ADDISCR	—	Disconnection detection assist setting bits ADNDIS[4]: Discharge or precharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0]: Discharge or precharge period b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 0 to 1 1 1 1: Number of states in precharge/discharge period Settings other than the above are prohibited.	Disconnection detection assist setting bits ADNDIS[4] Discharge or precharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0] The discharge/precharge period is specified by the number of ADCLK clock cycles. b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 1: Charge period of 3 clock cycles 0 1 1 0: Charge period of 6 clock cycles 1 0 0 1: Charge period of 9 clock cycles 1 1 0 0: Charge period of 12 clock cycles 1 1 1 1: Charge period of 15 clock cycles Settings other than the above are prohibited.
ADELCCR	—	—	A/D event link control register
ADGSPCR	LGRRS	—	Restart channel select bit
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A compare condition setting register 0
ADCMPLR1	—	—	A/D compare function window A compare condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input compare condition setting register
ADCMPDR0	—	—	A/D compare function window A lower level setting register
ADCMPDR1	—	—	A/D compare function window A upper level setting register

Register	Bit	RX23T(S12ADE)	RX26T(S12ADHa)
ADCMPSR0	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADWINMON	—	—	A/D compare function window A/B status monitoring register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower level setting register
ADWINULB	—	—	A/D compare function window B upper level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
S12AD. ADPGACR	—	—	A/D programmable gain amplifier control register
S12AD1. ADPGACR	—	—	A/D programmable gain amplifier control register
S12AD. ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0
S12AD1. ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register

2.25 D/A Converter and 12-Bit D/A Converter

Table 2.67 is Comparative Overview of D/A Converters, and Table 2.68 is Comparison of D/A Converter Registers.

Table 2.67 Comparative Overview of D/A Converters

Item	RX23T (DA)	RX26T (R12DAb)
Resolution	8 bits	12 bits
Output channels	1 channel	2 channels
Measure against interference between analog modules	—	• Measure against interference between D/A and A/D converters: — D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	—	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	—	Output to external pins and to comparator C can be controlled independently.

Table 2.68 Comparison of D/A Converter Registers

Register	Bit	RX23T (DA)	RX26T (R12DAb)
DADR1	—	—	D/A data register 1
DACR	DAE	—	D/A enable bit
	DAOE1	—	D/A output enable 1 bit
DAADSCR	—	—	D/A A/D synchronization start control register
DADSELR	—	—	D/A destination select register

2.26 Comparator C

Table 2.69 is Comparative Overview of Comparator C Modules, and Table 2.70 is Comparison of Comparator C Registers.

Table 2.69 Comparative Overview of Comparator C Modules

Item	RX23T (CMPC)	RX26T (CMPCa)
Number of channels	3 channels (comparator C0 to comparator C2)	6 channels (comparator C0 to comparator C5)
Analog input voltage	• Input voltage to CMPCnm pin (n = channel number, m = 0 to 2) • Internal reference voltage	• Input voltage on CMPCnm pin (n = channel number, m = 0 to 3)
Reference input voltage	• Input voltage on CVREFC0/CVREFC1 pin or output voltage from on-chip D/A converter	• Input voltage from CVREFC0/CVREFC1 pin, output voltage from on-chip D/A converter 0, or output voltage from on-chip D/A converter 1
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output and POE source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, event output to the ELC, and POE source output*1, and comparison results can be read from registers.
Interrupt request signal	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Note 1. The POE only uses the level detection signal, and the POEG uses the level detection and edge detection signals

Table 2.70 Comparison of Comparator C Registers

Register	Bit	RX23T (CMPC)	RX26T (CMPCa)
CMPSEL0	CMPSEL [3:0]	Comparator input select bits • For Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. 0 0 1 0: CMPC01 is selected. 0 1 0 0: CMPC02 is selected. 1 0 0 0: CMPC03 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. 0 0 1 0: CMPC11 is selected. 0 1 0 0: CMPC12 is selected. 1 0 0 0: CMPC13 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. 0 0 1 0: CMPC21 is selected. 0 1 0 0: CMPC22 is selected. 1 0 0 0: CMPC23 is selected. Settings other than the above are prohibited.	Comparator input select bits • For Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. 0 0 1 0: CMPC01 is selected. 0 1 0 0: CMPC02 is selected. 1 0 0 0: CMPC03 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. 0 0 1 0: CMPC11 is selected. 0 1 0 0: CMPC12 is selected. 1 0 0 0: CMPC13 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. 0 0 1 0: CMPC21 is selected. 0 1 0 0: CMPC22 is selected. 1 0 0 0: CMPC23 is selected. Settings other than the above are prohibited. • For Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 is selected. 0 0 1 0: CMPC31 is selected. 0 1 0 0: CMPC32 is selected. 1 0 0 0: CMPC33 is selected. Settings other than the above are prohibited. • For Comparator C4 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC40 is selected. 0 0 1 0: CMPC41 is selected. 0 1 0 0: CMPC42 is selected. 1 0 0 0: CMPC43 is selected. Settings other than the above are prohibited.

Register	Bit	RX23T (CMPC)	RX26T (CMPCa)
CMPSEL0	CMPSEL [3:0]		• For Comparator C5 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC50 is selected. 0 0 1 0: CMPC51 is selected. 0 1 0 0: CMPC52 is selected. 1 0 0 0: CMPC53 is selected. Settings other than the above are prohibited.
CMPSEL1	CVRS[1:0] (RX23T) CVRS[3:0] (RX26T)	Reference input voltage select bits [For Comparators C0 and C1] b1 b0 0 0: No input 0 1: CVREFC1 input is selected for the reference input voltage. 1 0: Output of on-chip D/A converter is selected for the reference input voltage. Settings other than the above are prohibited. [For Comparator C2] b1 b0 0 0: No input 0 1: CVREFC0 input is selected for the reference input voltage. 1 0: Output of on-chip D/A converter is selected for the reference input voltage. Settings other than the above are prohibited.	Reference input voltage select bits b3 b0 0 0 0 0: No input 0 0 0 1: Output of on-chip D/A converter 1 is selected for the reference input voltage. 0 0 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. 0 1 0 0: CVREFC1 input is selected for the reference input voltage. 1 0 0 0: CVREFC0 input is selected for the reference input voltage. Settings other than the above are prohibited.
CMPIOC	VREFEN	Internal reference voltage ON/OFF control bit	—
CMPCTL2	—	—	Comparator control register 2

2.27 Data Operation Circuit

Table 2.71 is Comparative Overview of Data Operation Circuits, and Table 2.72 is Comparison of Data Operation Circuit Registers.

Table 2.71 Comparative Overview of Data Operation Circuits

Item	RX23T (DOC)	RX26T (DOCA)
Data operation functions	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32-bit data
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event link function (output)	—	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.72 Comparison of Data Operation Circuit Registers

Register	Bit	RX23T (DOC)	RX26T (DOCA)
DOCR	DCSEL (RX23T) DCSEL[2:0] (RX26T)	Detection condition select bit b2 0: Data mismatches are detected. 1: Data matches are detected.	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPSZ	—	Data operation size select bit
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register DODIR is a 16-bit register.	DOC data input register DODIR is a 32-bit register.
DODSR	—	DOC data setting register	—
DODSR0	—	—	DOC data setting register 0
DODSR1	—	—	DOC data setting register 1

2.28 RAM

Table 2.73 is Comparative Overview of RAMs, and Table 2.74 is Comparison of RAM Registers.

Table 2.73 Comparative Overview of RAMs

Item	RX23T	RX26T
RAM capacity	12 KB (RAM0: 12 KB)	64 KB
RAM Addresses	RAM0: 0000 0000h to 0000 27FFh 0000 4000h to 0000 4A7Fh	0000 0000h to 0000 FFFFh
Memory buses	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Low power consumption function	The module stop state is selectable for RAM0.	Ability to transition to module stop state
Error checking	—	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Table 2.74 Comparison of RAM Registers

Register	Bit	RX23T	RX26T
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.29 Flash Memory

Table 2.75 is Comparative Overview of Flash Memories, and Table 2.76 is Comparison of Flash Memory Registers.

Table 2.75 Comparative Overview of Flash Memories

Item	RX23T ROM	RX26T Code flash memory	 Data flash memory
Memory space	• User area: Max. 128 KB • Extra area: Storage for startup area information, access window information, and unique IDs	Max. 512 KB	16 KB
Address	• Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB: — FFFF 0000h to FFFF FFFFh	• Products with capacity of 512 KB: [Linear mode] — FFF8 0000h to FFFF FFFFh [Dual mode] Bank 1 — FFF8 0000h to FFFB FFFFh Bank 2 — FFFC 0000h to FFFF FFFFh • Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh	• Products with capacity of 16 KB: — 0010 0000h to 0010 3FFFh
Read cycle	No ROM wait cycles when ICLK ≤ 32 MHz ROM wait cycle when ICLK > 32 MHz	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	ROM: FFh	FFh	Undefined

Item	RX23T ROM	RX26T Code flash memory	 Data flash memory
Programming/ erasing method	Rewrite by software command • The following software commands are implemented: — Program, blank check, block erase, all-block erase • The following commands are implemented for programs in the extra area: — Start-up area information program — Access window information program	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	
Security function	Protects against illicit tampering with or reading of data in flash memory.	Protects against illicit tampering with or reading of data in flash memory.	
Protection function	Protects against erroneous programming of the flash memory.	Protects against erroneous programming of the flash memory.	
Dual bank function	—	The dual bank configuration allows safe updating even upon interruption during a rewrite operation. • Linear mode: In this mode, code flash memory is used as a single area. • Dual mode: In this mode, code flash memory is used as two separate areas.	—
Trusted Memory (TM) function	—	Protects against illicit reading in code flash memory. • Linear mode: Blocks 8 and 9 • Dual mode: Blocks 8, 9, 30, and 31	—
BGO (Background Operation) function	—	• Code flash memory can be read while it is being programmed or erased. • Data flash memory can be read while code flash memory is being programmed or erased. • Code flash memory can be read while data flash memory is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Programming: 128 bytes • Erasure: Block units	• Programming: 4-byte units • Erasure: block units
Other functions	—	Interrupts can be accepted during self-programming.	

Item	RX23T ROM	RX26T Code flash memory	 Data flash memory
On-board programming (serial programming and self-programming)	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area is programmable. • Boot mode (FINE interface) — FINE is used. — The user area is programmable. • Self-programming in single-chip mode — The user area is programmable using a flash programming routine in a user program.	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing by code flash memory or data flash memory is possible.	
Off-board programming (programming and erasure using a parallel programmer)	The user area is rewritable using a flash programmer compatible with this MCU.	—	—
Unique ID	A unique 16-byte ID code is provided for each MCU.	A unique 12-byte ID code is provided for each MCU.	

Table 2.76 Comparison of Flash Memory Registers

Register	Bit	RX23T	RX26T
FWEPROR	—	—	Flash P/E protect register
FASTAT	—	—	Flash access status register
FAEINT	—	—	Flash access error interrupt enable register
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSTATR	—	—	Flash status register
FENTRYR	—	—	Flash P/E mode entry register
FSUINITR	—	—	Flash sequencer set-up initialization register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FAWMON	—	—	Flash access window monitor register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock notification register
FSUACR	—	—	Start-up area control register
FENTRYR	—	Flash P/E mode entry register	—
FPR	—	Protection unlock register	—
FPSR	—	Protection unlock status register	—
FPMCR	—	Flash P/E mode control register	—
FISR	—	Flash initial setting register	—
FRESETR	—	Flash reset register	—
FASR	—	Flash area select register	—
FCR	—	Flash control register	—
FEXCR	—	Flash extra area control register	—
FSARH	—	Flash processing start address register H	—
FSARL	—	Flash processing start address register L	—
FEARH	—	Flash processing end address register H	—
FEARL	—	Flash processing end address register L	—
FWBn	—	Flash write buffer n register (n = 0 to 3)	—
FSTATR0	—	Flash status register 0	—
FSTATR1	—	Flash status register 1	—
FEAMH	—	Flash error address monitor register H	—

Register	Bit	RX23T	RX26T
FEAML	—	Flash error address monitor register L	—
FSCMR	—	Flash start-up setting monitor register	—
FAWSMR	—	Flash access window start address monitor register	—
FAWEMR	—	Flash access window end address monitor register	—
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)

2.30 Packages

As indicated in Table 2.77, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.77 Packages

Package Type	RENESAS Code	
	RX23T	RX26T
100-pin LFQFP	×	○
80-pin LFQFP	×	○
64-pin HWQFN	×	○
52-pin LQFP	○	×
48-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. Black text indicates there is no differences in the item's specifications between groups.

3.1 64-Pin Package

Table 3.1 is Comparative Listing of 64-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX23T (64-pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
1	P02/CTS1#/RTS1#/SS1#/ADST0/IRQ5	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
2	P00/IRQ2	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009/SMISO009/SSCL009/IRQ2/ADST1/ COMP0
3	VCL	VCL
4	P01/CACREF/IRQ4	MD/FINED/PN6
5	MD/NMI	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/TXDA009/ SMOSI009/SSDA009/IRQ4/ADST2/COMP1
6	RES#	RES#
7	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
10	VCC	VCC
11	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
12	PD7/TMRI1/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8
13	PD6/TMO1/SSLA0/CTS1#/RTS1#/SS1#/ ADST0/IRQ5	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
14	PD5/TMRI0/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
15	PD4/TMCI0/SCK1/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2

64-Pin	RX23T (64-pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
16	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/TMO0/GTIOC2A/GTETRGC/GTIOC2A#/GTIOC7B/TXD1/SMOSI1/SSDA1/TXD011/TXDA011/SMOSI011/SSDA011/MOSI0
17	PB7/SCK5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/RXD12/SMISO12/SSCL12/RXDX12/RXD011/SMISO011/SSCL011/MISO0/CRX0/IRQ2
18	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD011/TXDA011/SMOSI011/SSDA011/RSPCK0/CTX0
19	PB5/TXD5/SMOSI5/SSDA5	PB4/POE8#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO0/CTS5#/RTS5#/SS5#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/SCK011/TXDB011/MISOA/SSL01/CRX0/IRQ3
20	VCC	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/TOC1/SCK6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTS009#/RTS009#/SS009#/DE009/RSPCKA/CTX0/IRQ9
21	PB4/POE8#/IRQ3	PB2/MTIOC0B/MTIOC0B#/TMRI0/GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
22	VSS	PB1/MTIOC0C/MTIOC0C#/TMCI0/GTADSM1/GTIOC7B/GTIOC7B#/GTIW/TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/IRQ4/ADSM1
23	PB3/MTIOC0A/CACREF/SCK5/RSPCKA	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/TXD6/SMOSI6/SSDA6/TXD008/TXDA008/SMOSI008/SSDA008/CTS011#/RTS011#/SS011#/DE011/MOSIA/MOSI0/IRQ8/ADTRG2#
24	PB2/MTIOC0B/ADSM0/TXD5/SMOSI5/SSDA5/SDA0	VCC
25	PB1/MTIOC0C/RXD5/SMISO5/SSCL5/SCL0/IRQ2	P96/POE4#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO4/CTS008#/RTS008#/SS008#/DE008/SSL03/RSPCK0/IRQ4
26	PB0/MTIOC0D/MOSIA	VSS
27	PA3/MTIOC2A/SSLA0	P95/MTIOC6B/MTIOC1A/MTIOC6B#/MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/SMISO6/SSCL6/RXD008/SMISO008/SSCL008/MISOA/SSL02/MISO0/IRQ1/ADTRG1#
28	PA2/MTIOC2B/CTS5#/RTS5#/SS5#/SSLA1/IRQ4	P94/MTIOC7A/MTIOC2A/MTIOC7A#/MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/GTIOC5A#/GTOVUP/TXD009/TXDA009/SMOSI009/SSDA009/SCK008/TXDB008/SSLA0/SSL00

64-Pin	RX23T (64-pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
29	P94/MTIOC0C/TMO1/MISOA/IRQ1	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
30	P93/MTIOC0B/TMRI1/SCK5/RSPCKA/IRQ0	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
31	P92/TMCI1/SSLA2	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
32	P91/SSLA3	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
33	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
34	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
35	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
36	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
37	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
38	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
39	P70/POE0#/IRQ5	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
40	P33/MTIOC3A/MTCLKA/SSLA3	VCC
41	P32/MTIOC3C/MTCLKB/SSLA2	VSS
42	VCC	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
43	P31/MTIOC0A/MTCLKC/SSLA1	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5

64-Pin	RX23T (64-pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
44	VSS	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
45	P30/MTIOC0B/MTCLKD/SSLA0	P65/IRQ9/AN211/CMPC53/DA1
46	P24/MTIC5U/TMCI2/RSPCKA/COMP0/IRQ3	P64/IRQ8/AN210/CMPC33/DA0
47	P23/MTIC5V/CACREF/TMO2/MOSIA/ COMP1/IRQ4	AVCC2
48	P22/MTIC5W/TMRI2/MISOA/COMP2/IRQ2	AVSS2
49	P47/AN007/CMPC12/CMPC22	P54/IRQ2/AN202/CMPC22/CVREFC1
50	P46/AN006/CMPC02	P53/IRQ1/AN201/CMPC12/CVREFC0
51	P45/AN005/CMPC21	P52/IRQ0/AN200/CMPC02
52	P44/AN004/CMPC11	P47/AN103
53	P43/AN003/CMPC01	P46/AN102/CMPC50/CMPC51
54	P42/AN002/CMPC20	P45/AN101/CMPC40/CMPC41
55	P41/AN001/CMPC10	P44/AN100/CMPC30/CMPC31
56	P40/AN000/CMPC00	P43/AN003
57	AVCC0	P42/AN002/CMPC20/CMPC21
58	VREFH0	P41/AN001/CMPC10/CMPC11
59	VREFL0	P40/AN000/CMPC00/CMPC01
60	AVSS0	AVCC1
61	P11/MTIOC3A/MTCLKC/TMO3/IRQ1/AN016/ CVREFC0	AVCC0
62	P10/MTCLKD/TMRI3/IRQ0/AN017/ CVREFC1	AVSS0
63	PA5/MTIOC1A/TMCI3/MISOA	AVSS1
64	PA4/MTIOC1B/RSPCKA/ADTRG0#	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1

3.2 48-Pin Package

Table 3.2 is Comparative Listing of 48-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 48-Pin Package Pin Functions

48-Pin	RX23T (48-pin LFQFP)	RX26T (48-Pin LFQFP, 48-Pin HWQFN)
1	VCL	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/TIC3/RXD12/SMISO12/SSCL12/RXDX12/RXD009/SMISO009/SSCL009/IRQ2/ADST1/COMP0
2	MD/FINED	VCL
3	RES#	MD/FINED/PN6
4	XTAL/P37	RES#
5	VSS	XTAL/P37/RXD5/SMISO5/SSCL5
6	EXTAL/P36	VSS
7	VCC	EXTAL/P36/TXD5/SMOSI5/SSDA5
8	PE2/POE10#/NMI	VCC
9	PD6/TMO1/SSLA0/CTS1#/RTS1#/SS1#/ADST0/IRQ5	PE2/POE10#/NMI/IRQ0
10	PD5/TMRI0/RXD1/SMISO1/SSCL1/IRQ3	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/SCK009/TXD008/TXDA008/SMOSI008/SSDA008/TXDB009/SSLA1/SSL01/CTX0/IRQ8
11	PD4/TMCI0/SCK1/IRQ2	TDI/PD5/TMRI0/TMRI6/GTIOC1A/GTETRGA/GTIOC1A#/GTIOC7A/RXD1/SMISO1/SSCL1/RXD011/SMISO011/SSCL011/SSL00/IRQ6
12	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/TMO0/GTIOC2A/GTETRGC/GTIOC2A#/GTIOC7B/TXD1/SMOSI1/SSDA1/TXD011/TXDA011/SMOSI011/SSDA011/MOSI0
13	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/RXD12/SMISO12/SSCL12/RXDX12/RXD011/SMISO011/SSCL011/MISO0/CRX0/IRQ2
14	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD011/TXDA011/SMOSI011/SSDA011/RSPCK0/CTX0
15	VCC	PB4/POE8#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO0/CTS5#/RTS5#/SS5#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/SCK011/TXDB011/MISOA/SSL01/CRX0/IRQ3
16	PB4/POE8#/IRQ3	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/TOC1/SCK6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/CTS009#/RTS009#/SS009#/DE009/RSPCKA/CTX0/IRQ9

48-Pin	RX23T (48-pin LFQFP)	RX26T (48-Pin LFQFP, 48-Pin HWQFN)
17	PB3/MTIOC0A/CACREF/SCK5/RSPCKA	PB2/MTIOC0B/MTIOC0B#/TMRI0/GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
18	PB2/MTIOC0B/ADSM0/TXD5/SMOSI5/SSDA5/SDA0	PB1/MTIOC0C/MTIOC0C#/TMCI0/GTADSM1/GTIOC7B/GTIOC7B#/GTIW/TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/IRQ4/ADSM1
19	PB1/MTIOC0C/RXD5/SMISO5/SSCL5/SCL0/IRQ2	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/TXD6/SMOSI6/SSDA6/TXD008/TXDA008/SMOSI008/SSDA008/CTS011#/RTS011#/SS011#/DE011/MOSIA/MOSI0/IRQ8/ADTRG2#
20	PB0/MTIOC0D/MOSIA	P95/MTIOC6B/MTIOC1A/MTIOC6B#/MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/SMISO6/SSCL6/RXD008/SMISO008/SSCL008/MISOA/SSL02/MISO0/IRQ1/ADTRG1#
21	PA3/MTIOC2A/SSLA0	P94/MTIOC7A/MTIOC2A/MTIOC7A#/MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/GTIOC5A#/GTOVUP/TXD009/TXDA009/SMOSI009/SSDA009/SCK008/TXDB008/SSLA0/SSL00
22	PA2/MTIOC2B/CTS5#/RTS5#/SS5#/SSLA1/IRQ4	P93/MTIOC7B/MTIOC6A/MTIOC7B#/MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/GTOWUP/TXD009/TXDA009/SMOSI009/SSDA009/RXD011/SMISO011/SSCL011/SSLA2/SSL02/MOSI0/CRX0/IRQ14/ADTRG0#
23	P94/MTIOC0C/TMO1/MISOA/IRQ1	P92/MTIOC6D/MTIOC6C/MTIOC6D#/MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#/GTOULO/SCK009/TXD011/TXDA011/SMOSI011/SSDA011/TXDB009/SSLA3/SSL03/MISO0/CTX0
24	P93/MTIOC0B/TMRI1/SCK5/RSPCKA/IRQ0	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/RSPCK0
25	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/SSL03
26	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/SSL02
27	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/SSL01
28	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/SSL00
29	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/MOSI0
30	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/MISO0

48-Pin	RX23T (48-pin LFQFP)	RX26T (48-Pin LFQFP, 48-Pin HWQFN)
31	P70/POE0#/IRQ5	VCC
32	VCC	VSS
33	VSS	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
34	P24/MTIC5U/TMCI2/RSPCKA/COMP0/IRQ3	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
35	P23/MTIC5V/CACREF/TMO2/MOSIA/ COMP1/IRQ4	AVCC2
36	P22/MTIC5W/TMRI2/MISOA/COMP2/IRQ2	AVSS2
37	P47/AN007/CMPC12/CMPC22	P62/IRQ6/AN208/CMPC43
38	P46/AN006/CMPC02	P53/IRQ1/AN201/CMPC12/CVREFC0
39	P45/AN005/CMPC21	P52/IRQ0/AN200/CMPC02
40	P44/AN004/CMPC11	P44/AN100/CMPC30/CMPC31
41	P43/AN003/CMPC01	P43/AN003
42	P42/AN002/CMPC20	P42/AN002/CMPC20/CMPC21
43	P41/AN001/CMPC10	P41/AN001/CMPC10/CMPC11
44	P40/AN000/CMPC00	P40/AN000/CMPC00/CMPC01
45	AVCC0	AVCC0/AVCC1
46	AVSS0	AVSS0/AVSS1
47	P11/MTIOC3A/MTCLKC/TMO3/IRQ1/AN016/ CVREFC0	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
48	P10/MTCLKD/TMRI3/IRQ0/AN017/ CVREFC1	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

4. Important Information When Migrating Between MCUs

This section describes important information on differences between the RX26T Group and the RX23T Group.

For notes regarding hardware, see section 4.1, Notes on Pin Design. For notes regarding software, see section 4.2, Notes on Functional Design.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

When connecting a smoothing capacitor to the VCL pin to stabilize the internal power supply, select a capacitor rated at 4.7 µF for the RX23T Group, and 0.47 µF on the RX26T Group.

4.1.2 Main Clock Oscillator

When connecting an oscillator to the EXTAL or XTAL pin of the RX26T Group, use an oscillator whose resonator frequency is 8 MHz to 24 MHz.

4.1.3 Connecting Capacitors to Analog Power Supply Pins

When using an A/D conversion clock frequency higher than 40 MHz on the RX26T Group, add a 0.01 µF-capacitor between the 0.1 µF capacitor and the power supply pin.

4.2 Notes on Functional Design

Software operating on the RX23T Group is compatible with some software written for the RX26T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

This section describes software-related considerations regarding function settings that differ between the RX26T Group and RX23T Group.

For differences between modules and functions, see section 2, Comparative Overview of Specifications. For further information, refer to the *User's Manual: Hardware* of each MCU group, listed in section 5, Reference Documents.

4.2.1 Changing the Option-Setting Memory Though Self-Programming

In the RX26T Group, when changing the option setting memory through self-programming, use the configuration setting command to program the option setting memory to the configuration setting area.

For details on the configuration setting command, refer to the *RX26T Group Flash Memory User's Manual: Hardware* listed in section 5, Reference Documents.

4.2.2 Software Configurable Interrupt

On the RX23T Group, the interrupt sources have fixed vector numbers, but on the RX26T Group, the MTU and GPTW interrupt sources are classified as software configurable interrupt A and set in software configurable interrupt A source select register n (SLIARn), allowing interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.3 Using Flash Memory Commands

On the RX23T Group, programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for ROM programming and erasing and then issuing software commands. On the RX26T Group, programming and erasing of the flash memory is accomplished by setting FACI commands in the FACI command-issuing area to control the FCU.

Table 4.1 is Comparison of Specifications of Software Commands and FACI Commands.

Table 4.1 Comparison of Specifications of Software Commands and FACI Commands

Item	Software Command (RX23T)	FACI command (RX26T)
Command-issuing area	—	FACI command issuing area (007E 0000h)
Usable commands	• Programming • Block erase • All-block erase • Blank check • Start-up area information program • Access window information program	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration setting

4.2.4 Flash Access Window Setting Register

In the RX26T Group, the access window protect bit (FSPR) in the flash access window setting register (FAW) cannot be set back to 1 once it is set to 0.

For details, refer to the *RX26T Group User's Manual: Hardware* listed in section 5, Reference Documents.

4.2.5 Clock Frequency Settings

The clock frequency setting restrictions differ between the RX23T Group and RX26T Group.

For details, see Table 4.2.

Table 4.2 Comparison of Clock Frequency Setting Restrictions

Item	RX23T	RX26T
Clock frequency setting restrictions	ICLK ≥ PCLK	PCLKC ≥ PCLKA ≥ PCLKB
Clock frequency setting restrictions when using CANFD	—	PCLKA:PCLKB = 2:1 PCLKB ≥ CANFDCLK PCLKB ≥ CANFDMCLK
Clock frequency ratio restrictions	ICLK:FCLK = N:1 ICLK:PCLKA = N:1 ICLK:PCLKB = N:1 ICLK:PCLKD = N:1	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKC = 1:1 or 1:2 PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2

4.2.6 RIIC Operating Voltage Setting

When using the RIIC on the RX26T Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC.

For details, refer to the description of the VOLSR.RICVLS bit in *RX26T Group User's Manual: Hardware*.

4.2.7 Voltage Level Setting

On the RX26T Group, the operating mode setting in the voltage level setting register (VOLSR), the voltage detection circuit setting in the voltage detection level select register (LVDLVLR), and the option-setting memory setting in the option function select register 1 (OFS1) need to be changed as appropriate to match the operating voltage. Use a program to set these values.

4.2.8 Option-Setting Memory

On the RX23T Group, the ID code protection codes and ID code protection codes for the on-chip debugger are located in the ROM, but on the RX26T Group, they are located in the option-setting memory. Note that the setting configuration procedures are different.

4.2.9 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to 4 to 10 (in 0.5 increments) on the RX23T Group and to 10 to 30 (in 0.5 increments) on the RX26T Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value. Also, on the RX26T Group, use a program to switch the PLL clock.

4.2.10 All-Module Clock Stop Mode

The RX23T Group does not have an all-module clock stop mode.

On the RX26T Group, it is necessary to write 1 to the MSTPA24, MSTPA27, MSTPA29 bits to transition to the all-module clock stop mode.

4.2.11 MTU/GPTW Operating Frequency

On the RX26T Group, the PCLKC is used as the MTU/GPTW count clock, and PCLKA is used as the bus clock. Note that limitations apply regarding the usable frequency combinations.

4.2.12 DMAC Activation by MTU

When the DMAC is activated by the MTU on the RX26T Group, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may delay the start of a DMAC transfer, even if the activation source has been cleared.

4.2.13 Performing RAM Self-Diagnostics on Save Register Banks

On the RX26T Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.

(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.

(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.2.14 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX26T Group is subject to the following restrictions.

(1) The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)

(2) It is necessary to specify single scan mode when using match or mismatch event outputs.

(3) When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.

(4) When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.

(5) It is not possible to set the same channel for window A and window B.

(6) It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.2.15 Eliminating I^2C Bus Interface Noise

The RX23T Group has integrated analog noise filters on the SCL and SDA lines, but the RX26T Group has no integrated analog noise filters.

4.2.16 Control When a Port Output Enable 3 Output Stop Request Is Generated

On the RX26T Group, when an output stop request occurs, the pins with the corresponding bits of the POECR1 to POECR3 and POECR7 registers set to 1 are put in a high-impedance state and the pins with the corresponding bits of the PMMCR0 to PMMCR2 registers set to 1 are switched to the general I/O ports.

When both bits are set to 1 for the same pin, the POECR1 to POECR3 and POECR7 register settings take precedence and the pin is placed in a high-impedance state. After switching to the general I/O port, the state of the pins is determined by the PDR and PODR register settings.

The corresponding bits in the POECRn registers (n = 0 to 3) should be cleared to 0 beforehand.

4.2.17 Comparator C Operation with 12-Bit A/D Converter in Module Stop Mode

On the RX26T Group, the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal, so it is not possible to compare the following PGA outputs when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

It is not possible to compare the following analog pins when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

4.2.18 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX23T Group and RX26T Group, even on products with the same pin count.

4.2.19 Pulse Width of Count Clock Source

The pulse width of the MTU's count clock source differs between the RX23T Group and RX26T Group. For details, see Table 4.2. Correct operation cannot be achieved if the pulse width is less than the appropriate value listed below.

Table 4.3 Comparison of Count Clock Source Pulse Widths

Item		RX23T	RX26T
Single edge		3 or more PCLKA cycles	1.5 or more PCLKC cycles
Both edges		5 or more PCLKA cycles	2.5 or more PCLKC cycles
Phase counting mode	Phase difference and overlap	3 or more PCLKA cycles	1.5 or more PCLKC cycles
	Pulse width	5 or more PCLKA cycles	2.5 or more PCLKC cycles

4.2.20 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX26T Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.21 Active Level Setting for MTU/GPTW Inverted Output

On the RX26T Group, either normal output or inverted output can be selected for MTU and GPTW outputs by making settings in the MPC.PmnPFS registers.

When MTU inverted output is selected, the active level specified in the MTU.TOCR1j and MTU.TOCR2j registers (j = A or B) and the active level of the signals output to the pins are inverted. To use output short detection in this case, specify active levels in the ALR1 and ALR2 registers based on the signals actually output to the pins.

When GPTW inverted output is selected, the active level of the signals output to the pins is inverted. To use output short detection in this case, specify active levels in the ALR3 to ALR5 registers based on the signals actually output to the pins.

4.2.22 Note on Using Both POE and POEG

When using the POE and POEG together on the RX26T Group, do not use both the POE and POEG to control output disabling for the same GPTW output pins.

4.2.23 Reading Pins in High-Impedance State

When pins are put into the high-impedance state by the POE on the RX26T Group, the level of those pins cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state.

This restriction does not apply when port switching control is selected instead of high-impedance control.

5. Reference Documents

User's Manual: Hardware

RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX26T Group User's Manual: Hardware Rev.1.01 (R01UH0979EJ0101)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A151A/E

TN-RX*-A163A/E

TN-RX*-A173A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A200A/E

TN-RX*-A0206A/E

TN-RX*-A0213A/E

TN-RX*-A0216A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 22.23	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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