

ChipWhisperer CW310 "Bergen Board" - Xilinx Kintex 7 Target Board

NewAE Technology Inc.

Suggested Layer Stack

Bergen
Towel
Mat
Bed 1
Bed 2



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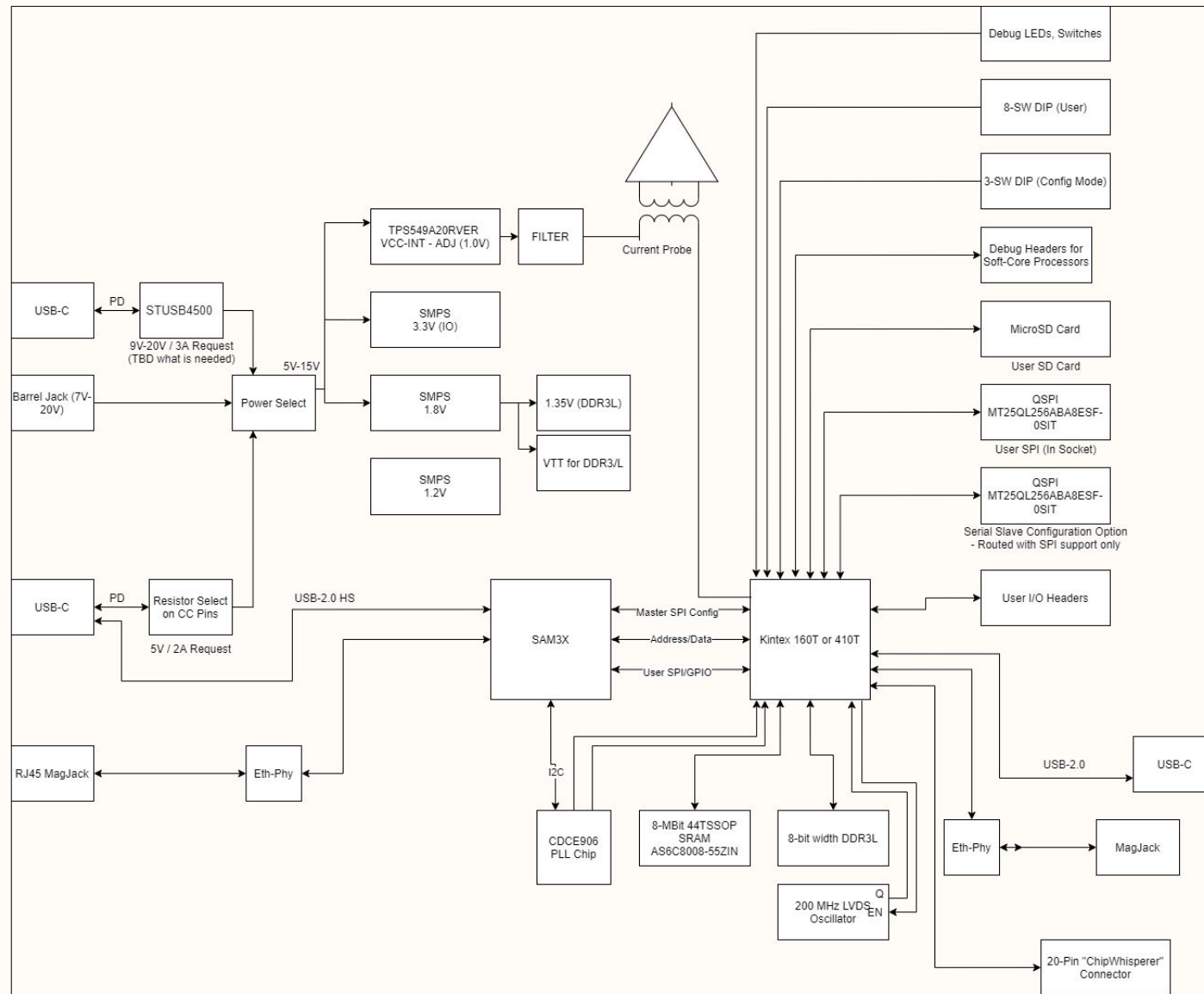
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Revision Summary

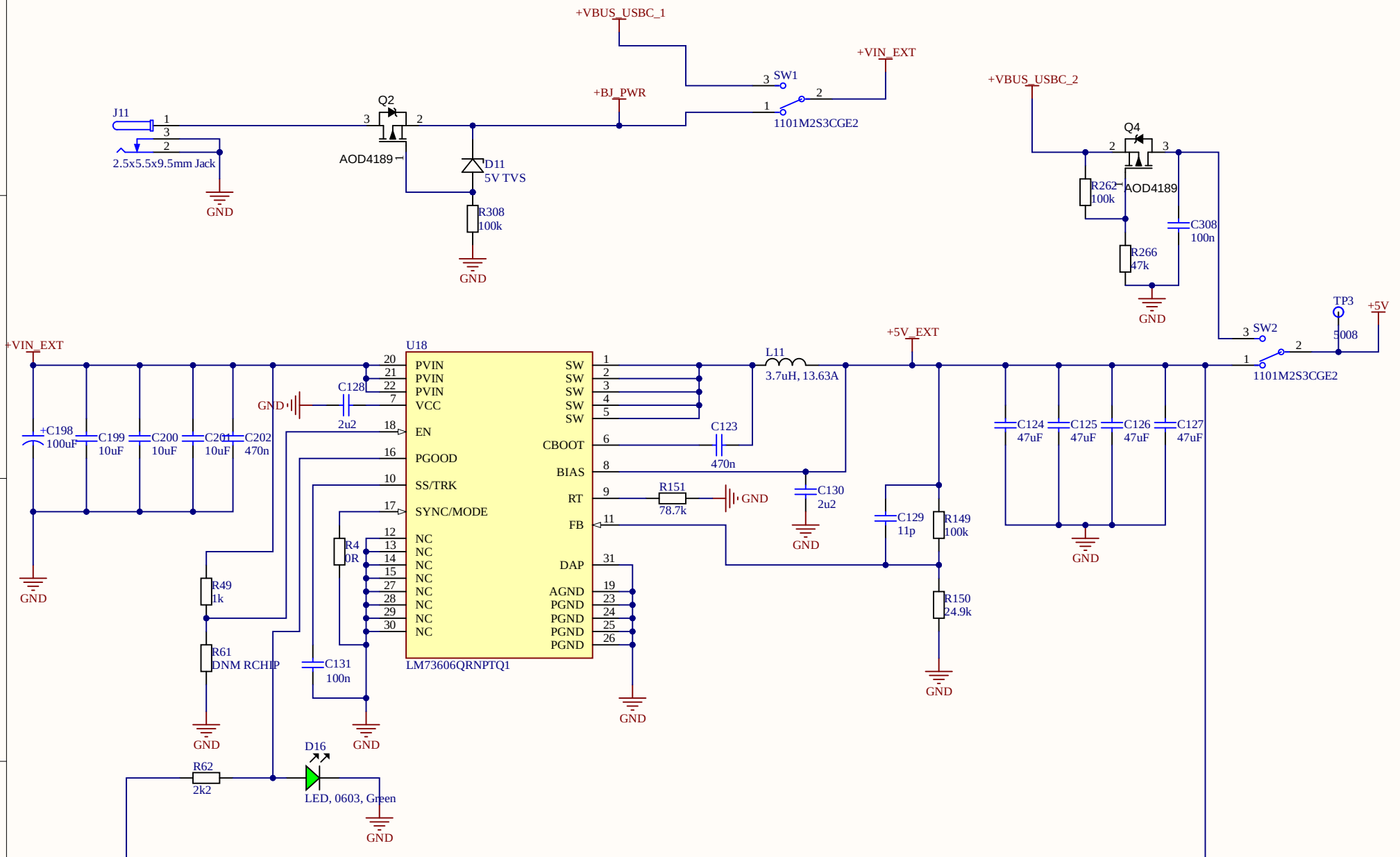
- 00: Ultra-alpha.
- 01: Super-alpha.
- 02: March 10/2021
Feature complete.
- 03: March 13/2021
Internal release.
- 04: March 15/2021
Add brown-out on 5V,
silkscreen updates
- 05: March 22/2021
Change FPGA routing
for HP/HR banks.
- 06: March 30/2021
Mark DNP parts, fix a few
missing resistors.

Title: Bergen Board - The Cover Sheet			 Approved: Yes	
Rev: 06	Project: BERGENBOARD		License: NewAE	
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Block Diagram



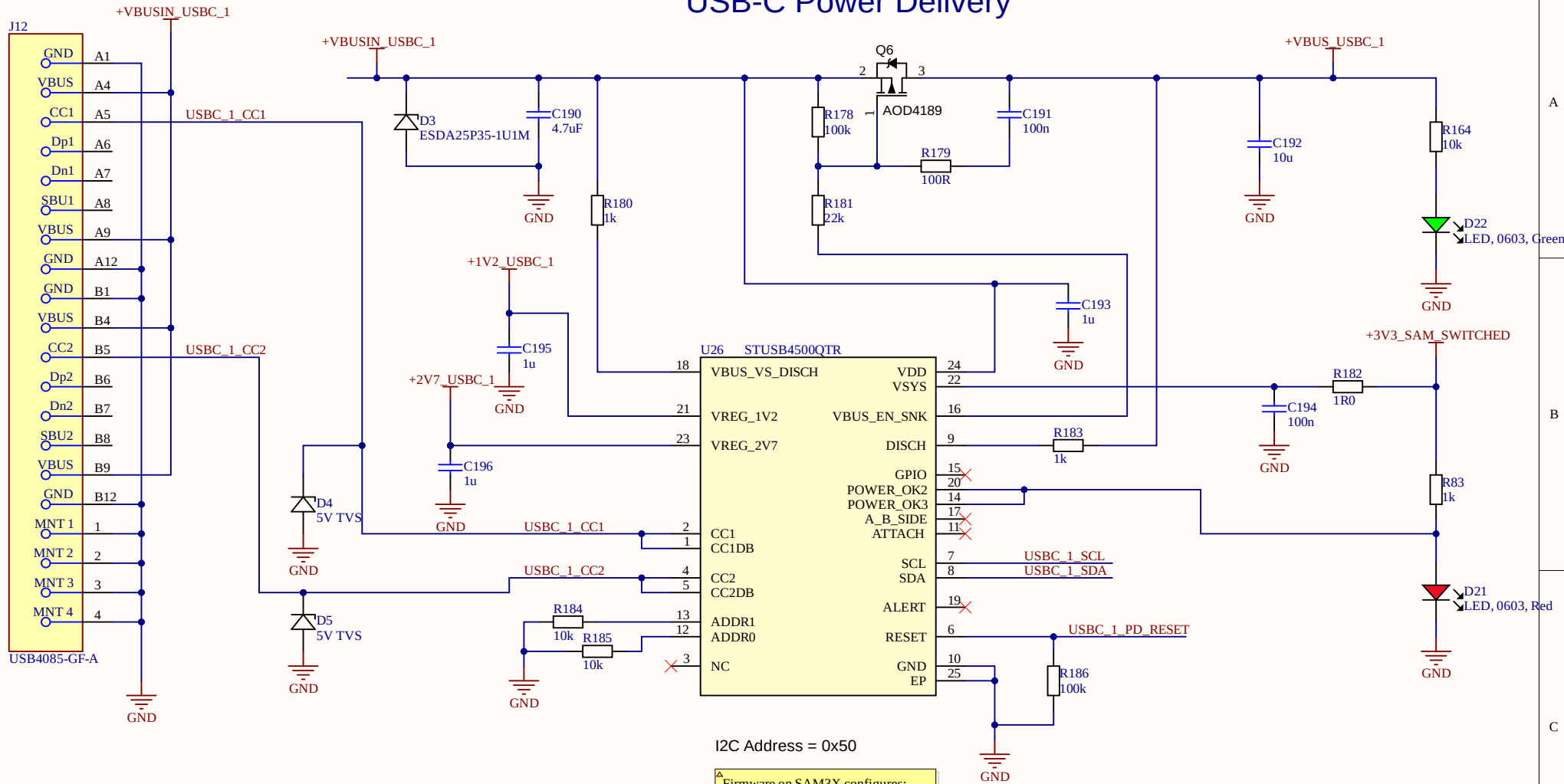
INPUT POWER



Based on design from
<https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=9C49F428E2C4FF82>

Title: 5V Regulator			 Approved: Yes		
Rev: 06	Project: BERGENBOARD		License: NewAE		
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File: CW310_INPUT_POWER.SchDoc					

USB-C Power Delivery



Title: **USB-C PD Controller**

Approved: Yes

Rev: 06

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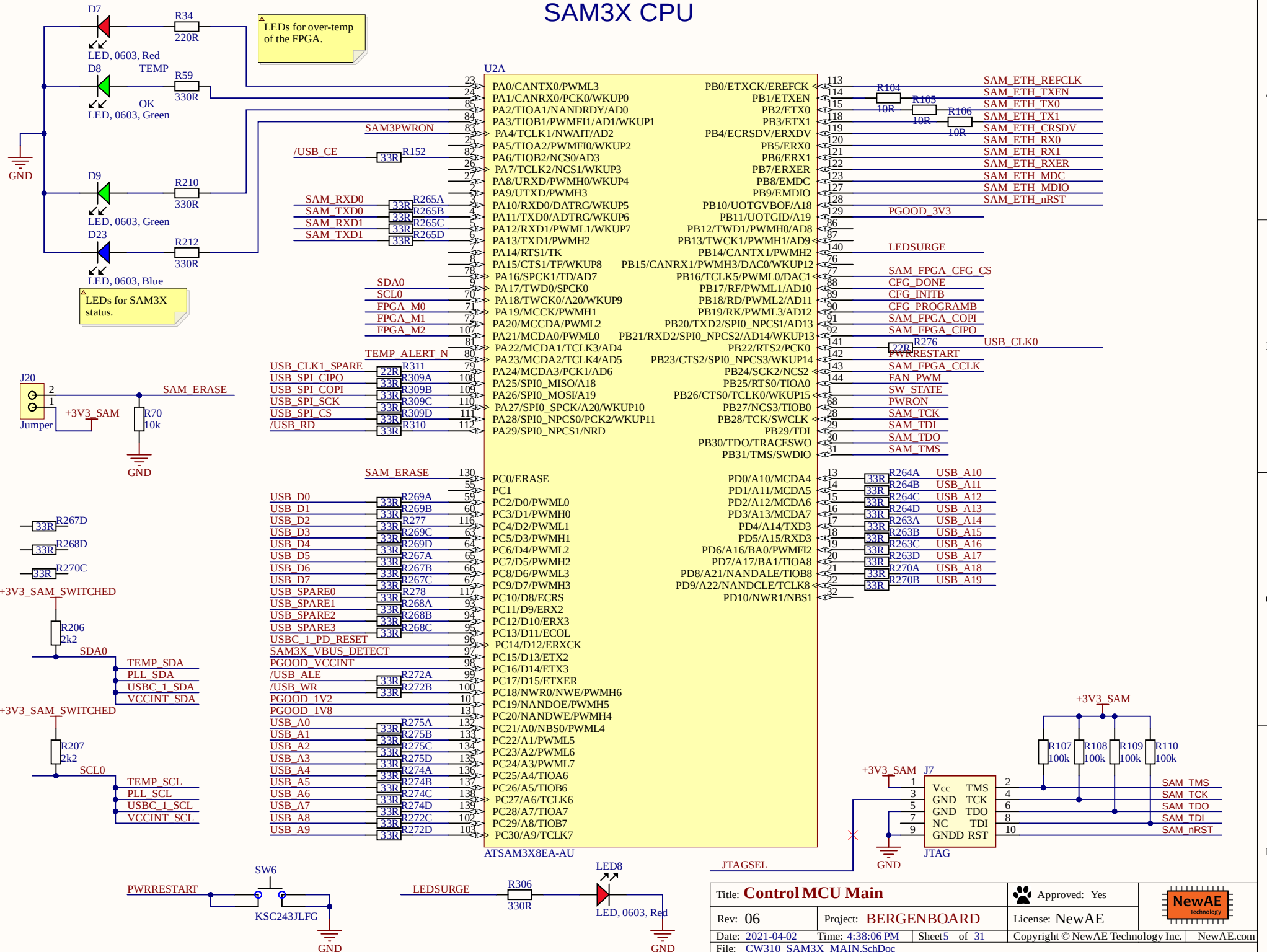
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File: CW310_USB_POWER.SchDoc



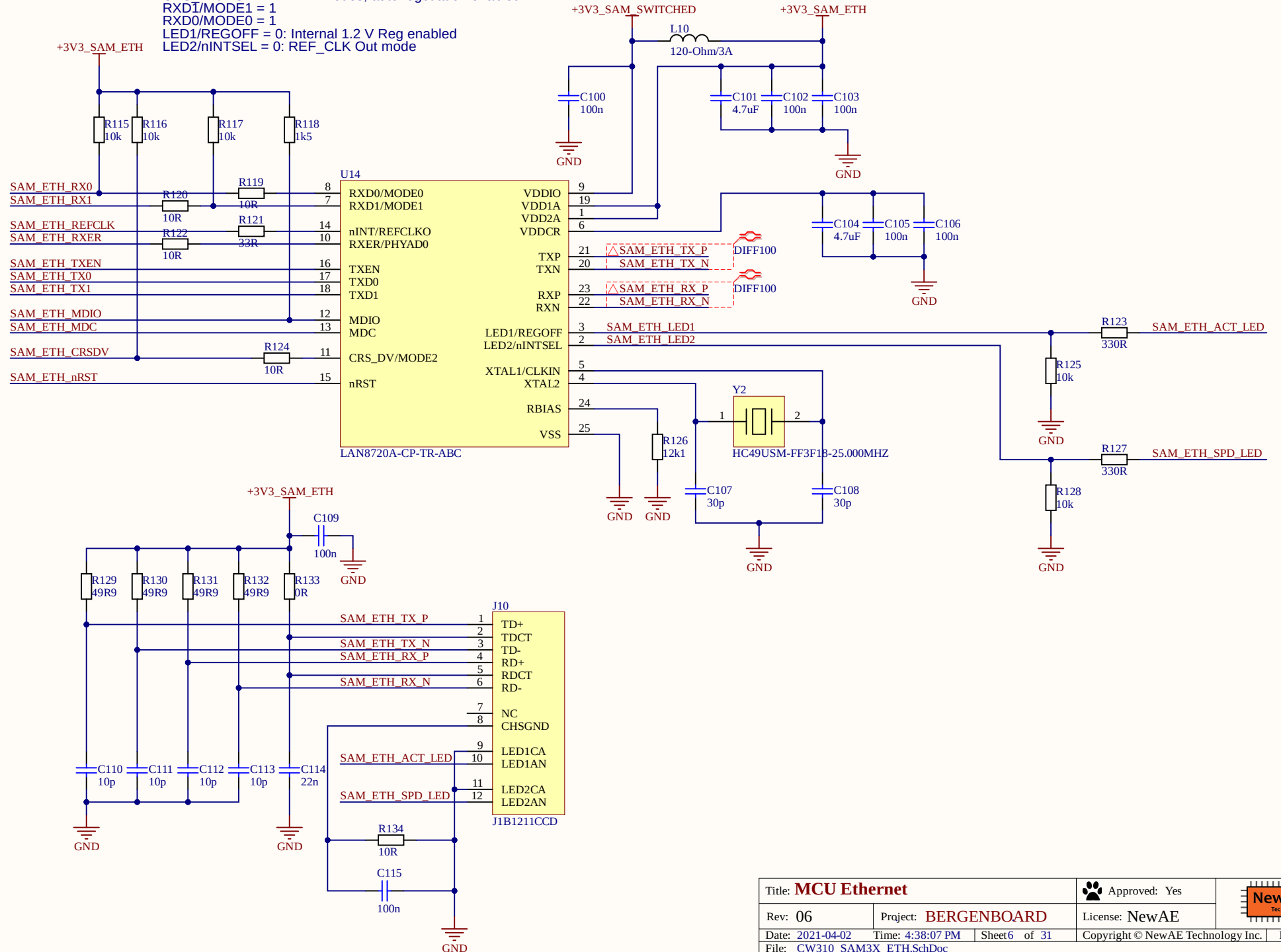
SAM3X CPU



SAM3X Ethernet

LAN8720 PHY Configuration

PHYAD0 = 0: Phy Address 0
CRS_DV/MODE2 = 1: All modes, autonegotiation enabled
RXD1/MODE1 = 1
RXD0/MODE0 = 1
LED1/REGOFF = 0: Internal 1.2 V Reg enabled
LED2/nINTSEL = 0: REF_CLK Out mode



Title: **MCU Ethernet**

Approved: Yes

Rev: 06

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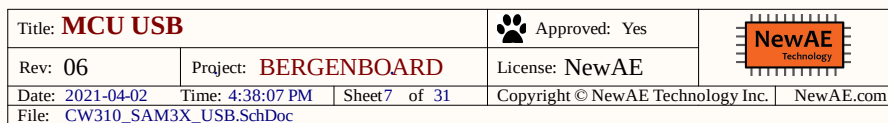
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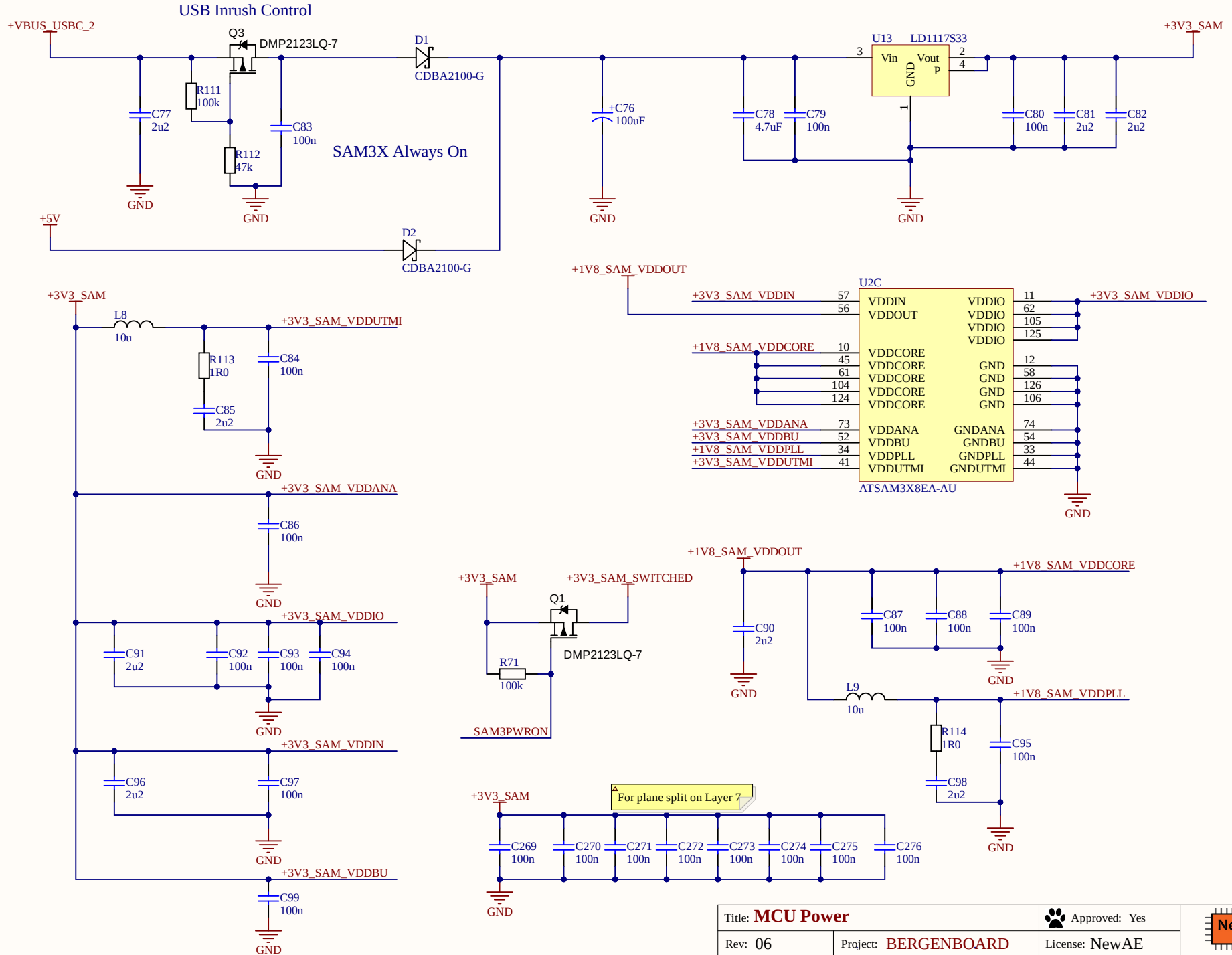
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File: CW310_SAM3X_ETH.SchDoc





SAM3X Power



Title: **MCU Power**

Approved: Yes



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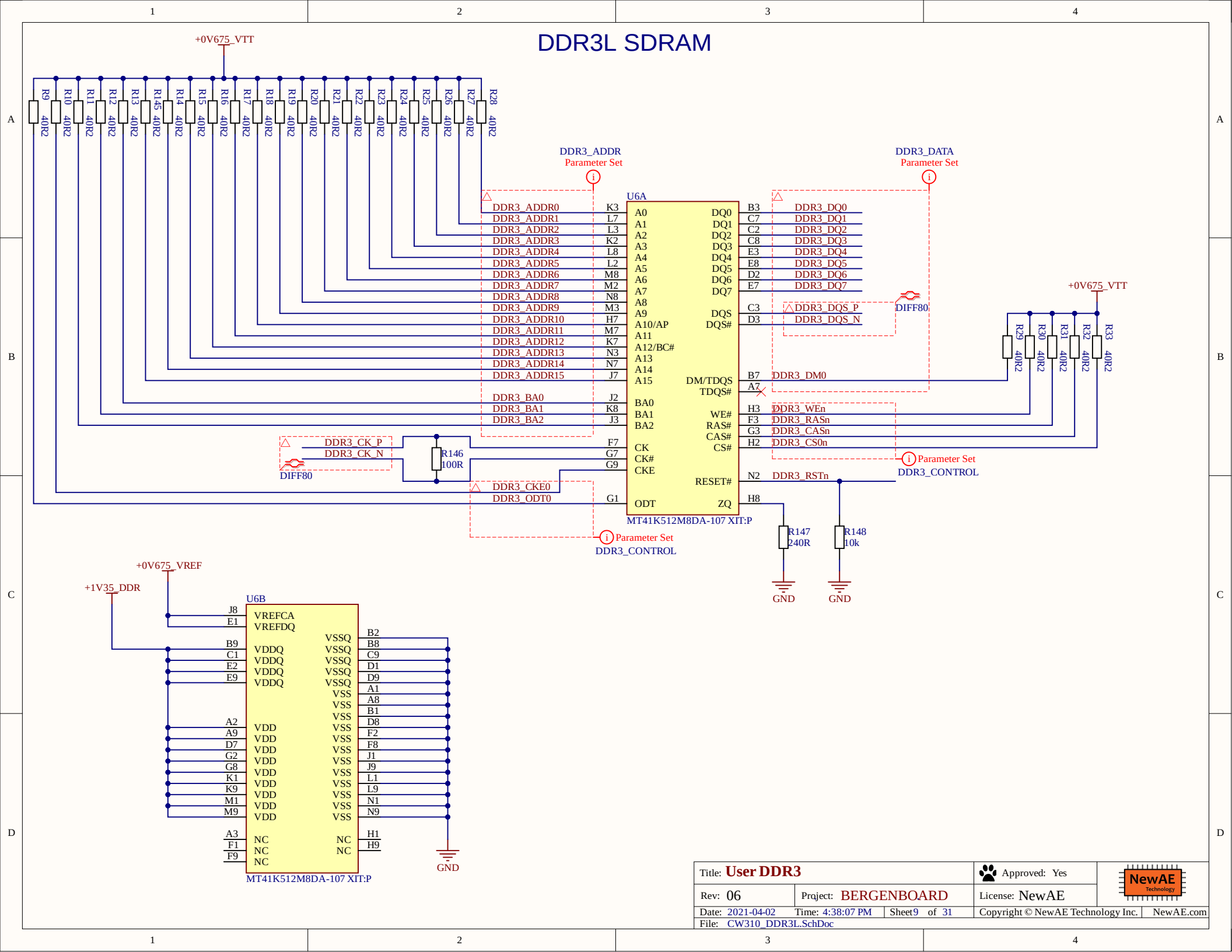
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DDR3L SDRAM



Title: **User DDR3**

Approved: Yes



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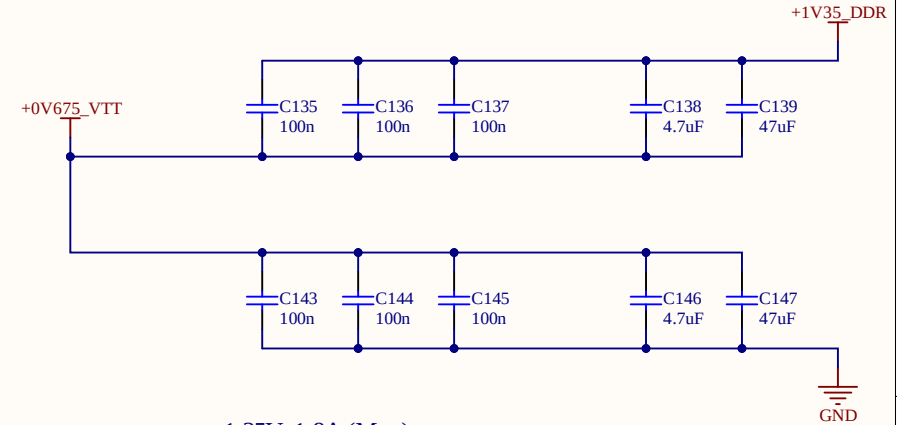
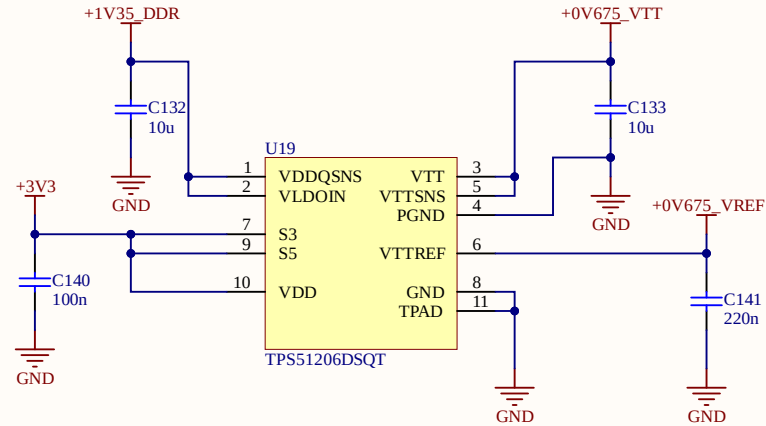
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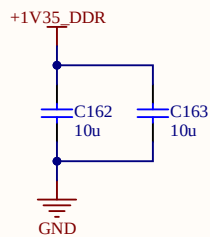
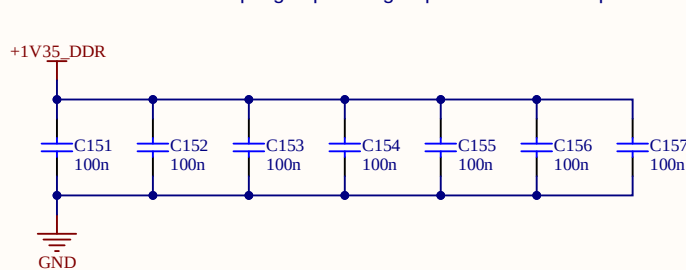
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DDR3L VTT & DECOUPLING

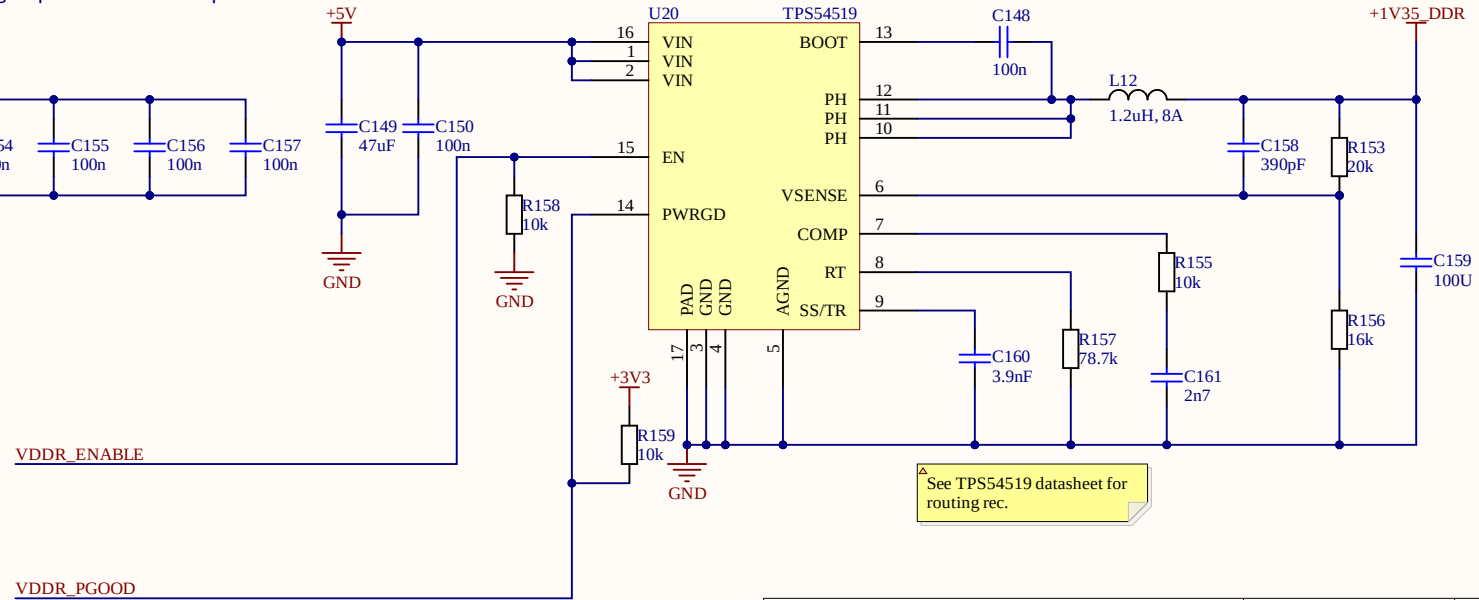
Place VTT decoupling capacitor groups by VTT island, near terminations of DRAM Address & Control lines



Place DRAM decoupling capacitor group near DRAM component



1.35V, 1.8A (Max)

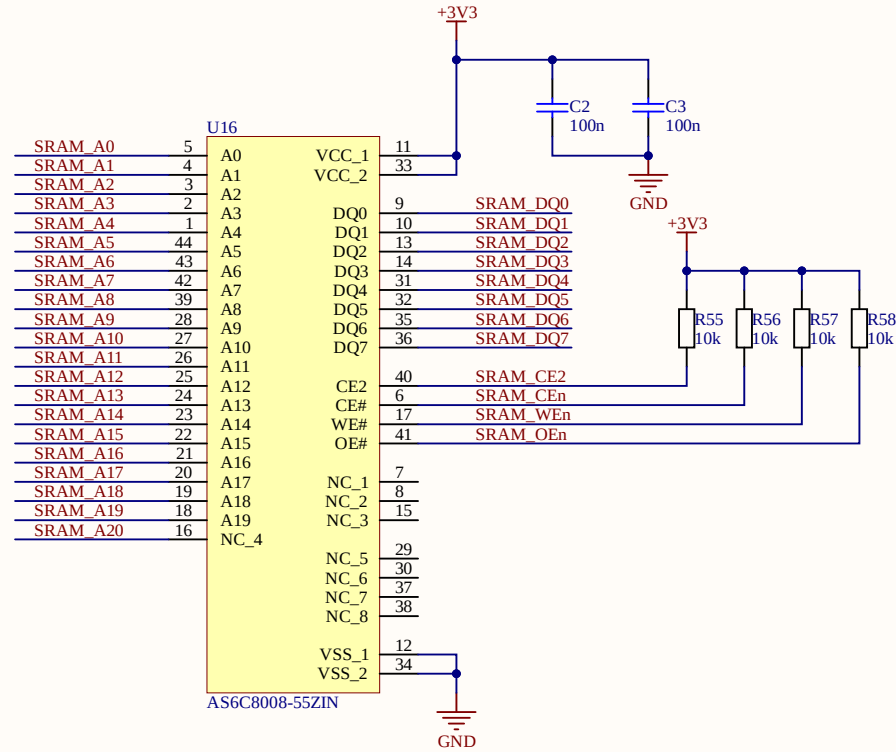


See TPS54519 datasheet for routing rec.

Title: DDR3L Power Supply			 Approved: Yes	
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SRAM

SRAM should be footprint compatible with:
AS6C8008-55ZIN
CY62158EV30LL-45ZSXIT
IS62WV10248DBLL-55TLI



FPGA Bank: 3.3V
U1A

BANK 12

IO_L21N_T3_DQS_12	AE26	USB_A3
IO_L23P_T3_12	AD25	USB_A2
IO_L21P_T3_DQS_12	AD26	USB_A1
IO_L16N_T2_12	AD24	USB_A6
IO_L11N_T1_SRCC_12	AB24	USB_A4
IO_L10P_T1_12	Y25	/USB_ALE
IO_L9P_T1_DQS_12	AB26	USB_A8
IO_L24N_T3_12	AF22	CWIO_MOSI
IO_L14N_T2_SRCC_12	AC24	USB_A5
IO_L2P_T0_12	U24	USB_A13
IO_L18P_T2_12	AB21	CWIO_HSI
IO_L1P_T0_12	U22	USB_A14
IO_L16P_T2_12	AD23	USB_A7
IO_L17N_T2_12	AC22	
IO_L7N_T1_12	AB25	USB_A9
IO_L4P_T0_12	U26	USB_D1
IO_L2N_T0_12	U25	USB_D0
IO_L15P_T2_DQS_12	W20	USB_A19
IO_L8P_T1_12	W23	USB_A10
IO_L3P_T0_DQS_12	V23	USB_A11
IO_L1N_T0_12	V22	USB_A15
IO_0_12	U21	USB_A16
IO_L6P_T0_12	V21	USB_A17
IO_L11P_T1_SRCC_12	AA23	/USB_CE
IO_L19N_T3_VREF_12	AE21	CWIO_MISO
IO_L6N_T0_VREF_12	W21	USB_A18
IO_L14P_T2_SRCC_12	AC23	/USB_RD
IO_L5N_T0_12	W26	USB_D5
IO_L15N_T2_DQS_12	Y21	USB_A12
IO_L5P_T0_12	W25	USB_D6
IO_L10N_T1_12	Y26	USB_D7
IO_L9N_T1_DQS_12	AC26	USB_A0
IO_L18N_T2_12	AC21	USB_D2
IO_L17P_T2_12	AB22	SAM_RXD0
IO_L12N_T1_MRCC_12	AA24	SAM_TXD0
IO_L13N_T2_MRCC_12	AA22	SAM_RXD1
IO_L8N_T1_12	W24	SAM_TXD1
IO_L20P_T3_12	AF24	CWIO_IO4
IO_L7P_T1_12	AA25	/USB_WR
IO_L3N_T0_DQS_12	V24	USB_D3
IO_L4N_T0_12	V26	USB_D4
IO_L23N_T3_12	AE25	CWIO_IO1
IO_L20N_T3_12	AF25	CWIO_IO2
IO_L22N_T3_12	AF23	CWIO_IO3
IO_L12P_T1_MRCC_12	Y23	USB_CLK0
IO_L24P_T3_12	AE22	CWIO_TSCK
IO_L19P_T3_12	AD21	CWIO_TPDIC
IO_L22P_T3_12	AE23	CWIO_TPDID
IO_L13P_T2_MRCC_12	Y22	CWIO_HS2
IO_25_12	Y20	CWIO_RST

XC7K160T-1FBG676C

FPGA Bank: 3.3V
U1B

BANK 13

IO_25_13	U16	
IO_L19N_T3_VREF_13	T19	USR_DBG_VCCDETECT
IO_L17N_T2_13	T23	PMOD1_IO8
IO_L4P_T0_13	P24	PMOD1_IO6
IO_L20N_T3_13	N17	PMOD1_IO1
IO_L2P_T0_13	R26	PMOD1_IO2
IO_L14N_T2_SRCC_13	R23	PMOD1_IO3
IO_L17P_T2_13	T22	PMOD1_IO4
IO_L6P_T0_13	R25	PMOD1_IO5
IO_L11P_T1_SRCC_13	P23	PMOD1_IO7
IO_L10N_T1_13	M22	PMOD2_IO1
IO_L10P_T1_13	M21	PMOD2_IO2
IO_L7P_T1_13	N19	PMOD2_IO3
IO_L1P_T0_13	K25	USRLED7
IO_L8N_T1_13	L24	USRLED6
IO_L1N_T0_13	K26	USRLED5
IO_L3N_T0_DQS_13	L25	USRLED4
IO_L22N_T3_13	M19	USRLED3
IO_L8P_T1_13	M24	USRLED2
IO_L3P_T0_DQS_13	M25	USRLED1
IO_L5N_T0_13	M26	USRLED0
IO_L15P_T2_DQS_13	T24	
IO_L2N_T0_13	P26	PMOD2_IO4
IO_L12P_T1_MRCC_13	N21	PLL_CLK2
IO_L11N_T1_SRCC_13	N23	PMOD2_IO5
IO_L5P_T0_13	N26	PMOD2_IO6
IO_L7N_T1_13	M20	PMOD2_IO7
IO_L14P_T2_SRCC_13	R22	PLL_CLK1
IO_L15N_T2_DQS_13	T25	USB_SPARE0
IO_L12N_T1_MRCC_13	N22	
IO_0_13	N16	USR_DBG_TMS
IO_L9N_T1_DQS_13	P20	
IO_L9P_T1_DQS_13	P19	USRUSB_PWREN
IO_L6N_T0_VREF_13	P25	PMOD2_IO8
IO_L23P_T3_13	U17	
IO_L18P_T2_13	U19	USR_DBG_TDAT1
IO_L18N_T2_13	U20	USR_DBG_TDAT2
IO_L16P_T2_13	T20	USR_DBG_TDAT3
IO_L16N_T2_13	R20	USR_DBG_NC0
IO_L13N_T2_MRCC_13	P21	USR_DBG_TDAT0
IO_L19P_T3_13	T18	
IO_L13P_T2_MRCC_13	R21	USR_DBG_TRACECLK
IO_L22P_T3_13	N18	USR_DBG_TCK
IO_L20P_T3_13	P16	USR_DBG_TDO
IO_L21P_T3_DQS_13	R16	USR_DBG_TDI
IO_L23N_T3_13	T17	USR_DBG_nRST
IO_L4N_T0_13	N24	VDDR_ENABLE
IO_L24P_T3_13	R18	VDDR_PGOOD
IO_L24N_T3_13	P18	USRUSB_VBUS_DETECT
IO_L21N_T3_DQS_13	R17	

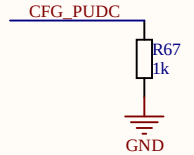
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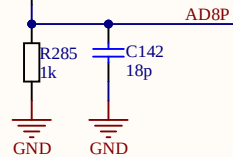
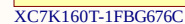
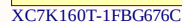
FPGA Bank: 3.3V, Configuration, SRAM
U1C

BANK 14

IO_0_14	K21	
IO_L1P_T0_D00_MOSI_14	B24	CFG_SPI_MOSI
IO_L1N_T0_D01_DIN_14	A25	CFG_SER_DIN
IO_L2P_T0_D02_14	B22	USB_CLK1_SPARE
IO_L2N_T0_D03_14	A22	USB_SPI_CIPO
IO_L3P_T0_DQS_PUDC_B_14	B25	CFG_PUDC
IO_L3N_T0_DQS_EMCCCLK_14	B26	CFG_EMCCCLK
IO_L4P_T0_D04_14	A23	USB_SPARE3
IO_L4N_T0_D05_14	A24	USB_SPI_COPI
IO_L5P_T0_D06_14	D26	USB_SPI_SCK
IO_L5N_T0_D07_14	C26	USB_SPI_CS
IO_L6P_T0_FCS_B_14	C23	CFG_SPI_CS
IO_L19P_T3_A10_D26_14	H21	SRAM_A12
IO_L12N_T1_MRCC_14	E23	SRAM_A13
IO_L21N_T3_DQS_A06_D22_14	H22	SRAM_A14
IO_L9N_T1_DQS_D13_14	E22	SRAM_A15
IO_L20P_T3_A08_D24_14	H23	SRAM_A16
IO_L20N_T3_A07_D23_14	H24	SRAM_A17
IO_L18P_T2_A12_D28_14	I26	SRAM_A18
IO_L18N_T2_A11_D27_14	H26	SRAM_A19
IO_25_14	L23	SRAM_A20
IO_L22P_T3_A05_D21_14	I24	SRAM_DQ0
IO_L17N_T2_A13_D29_14	E26	SRAM_DQ1
IO_L24P_T3_A01_D17_14	K23	SRAM_DQ2
IO_L7P_T1_D09_14	D21	SRAM_DQ3
IO_L6N_T0_D08_VREF_14	C24	SRAM_DQ4
IO_L11N_T1_SRCC_14	D24	SRAM_DQ5
IO_L11P_T1_SRCC_14	D23	SRAM_DQ6
IO_L7N_T1_D10_14	C22	SRAM_DQ7
IO_L15P_T2_DQS_RDWR_B_14	E25	USB_SPARE2
IO_L15N_T2_DQS_DOUT_CSO_B_14	D25	CFG_SER_DOUT
IO_L16P_T2_CSI_B_14	G25	USB_SPARE1
IO_L13N_T2_MRCC_14	F23	SRAM_A0
IO_L17P_T2_A14_D30_14	F25	SRAM_A1
IO_L14P_T2_SRCC_14	G24	SRAM_A2
IO_L12P_T1_MRCC_14	F22	SRAM_A3
IO_L19N_T3_A09_D25_VREF_14	G21	SRAM_A4
IO_L8P_T1_D11_14	B20	SRAM_A5
IO_L8N_T1_D12_14	A20	SRAM_A6
IO_L23N_T3_A02_D18_14	K22	SRAM_A7
IO_L10N_T1_D15_14	B21	SRAM_A8
IO_L9P_T1_DQS_14	E21	SRAM_A9
IO_L13P_T2_MRCC_14	G22	SRAM_A10
IO_L14N_T2_SRCC_14	F24	SRAM_A11
IO_L22N_T3_A04_D20_14	I25	
IO_L23P_T3_A03_D19_14	L22	
IO_L21P_T3_DQS_14	I21	SRAM_CE2
IO_L16N_T2_A15_D31_14	G26	SRAM_CEn
IO_L24N_T3_A00_D16_14	I23	SRAM_WEn
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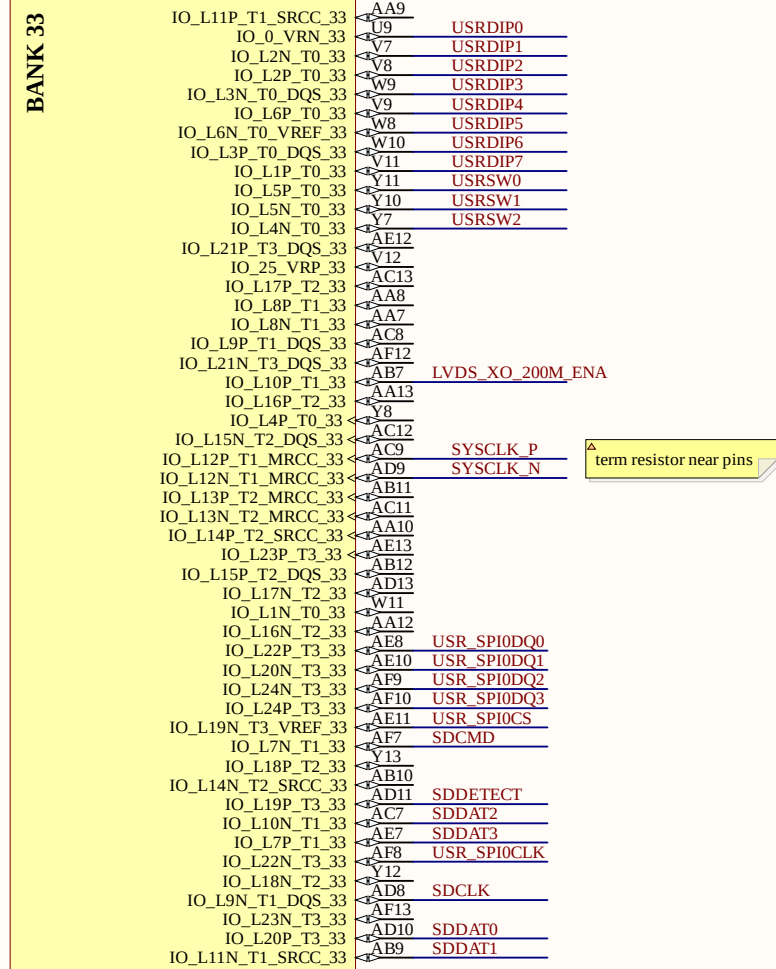




Title: Kintex IO Banks			 Approved: Yes		
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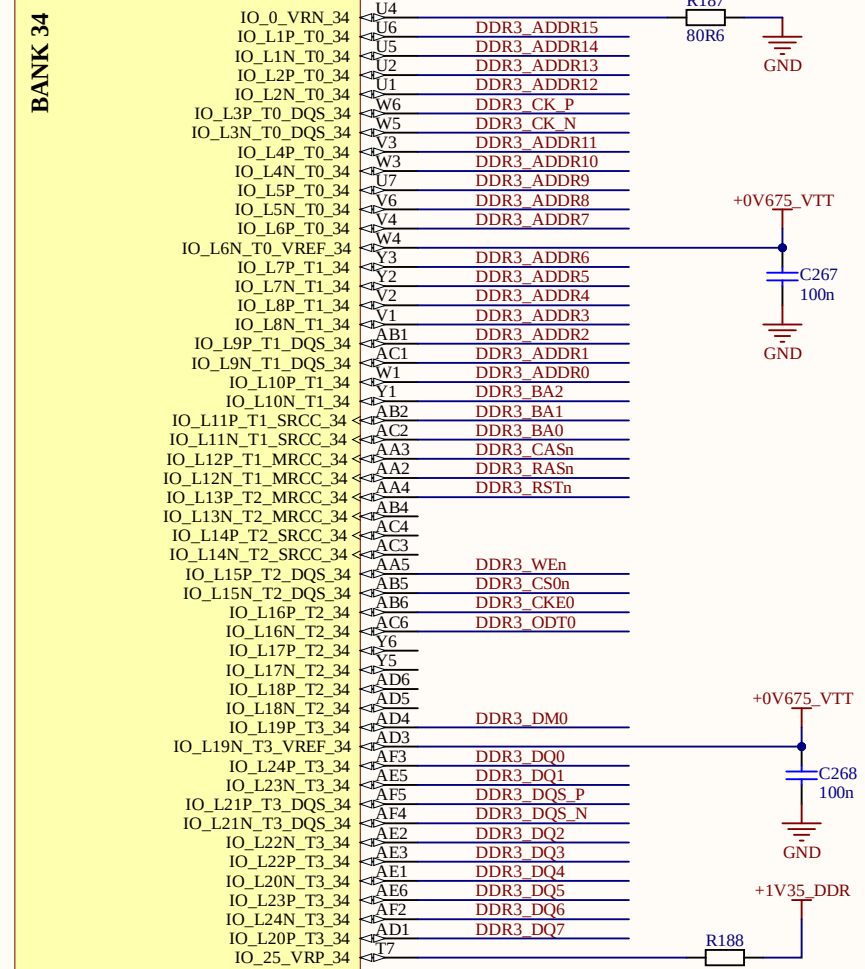
FPGA Bank: 1.8V (HP Bank)

U1G



FPGA Bank: DDR3, 1.35V (HP Bank)

U1H



Title: **Kintex IO Banks**

Approved: Yes



Rev: 06

Project: **BERGENBOARD**

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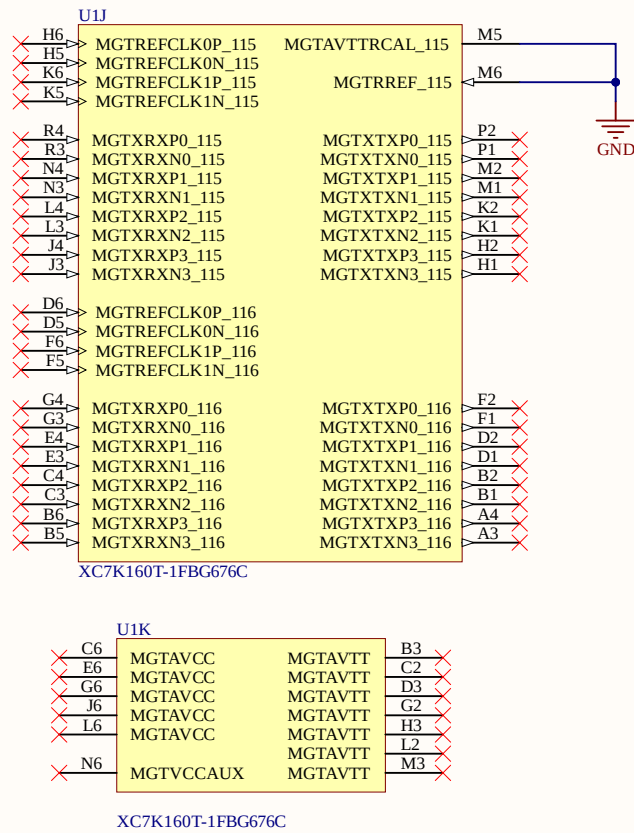
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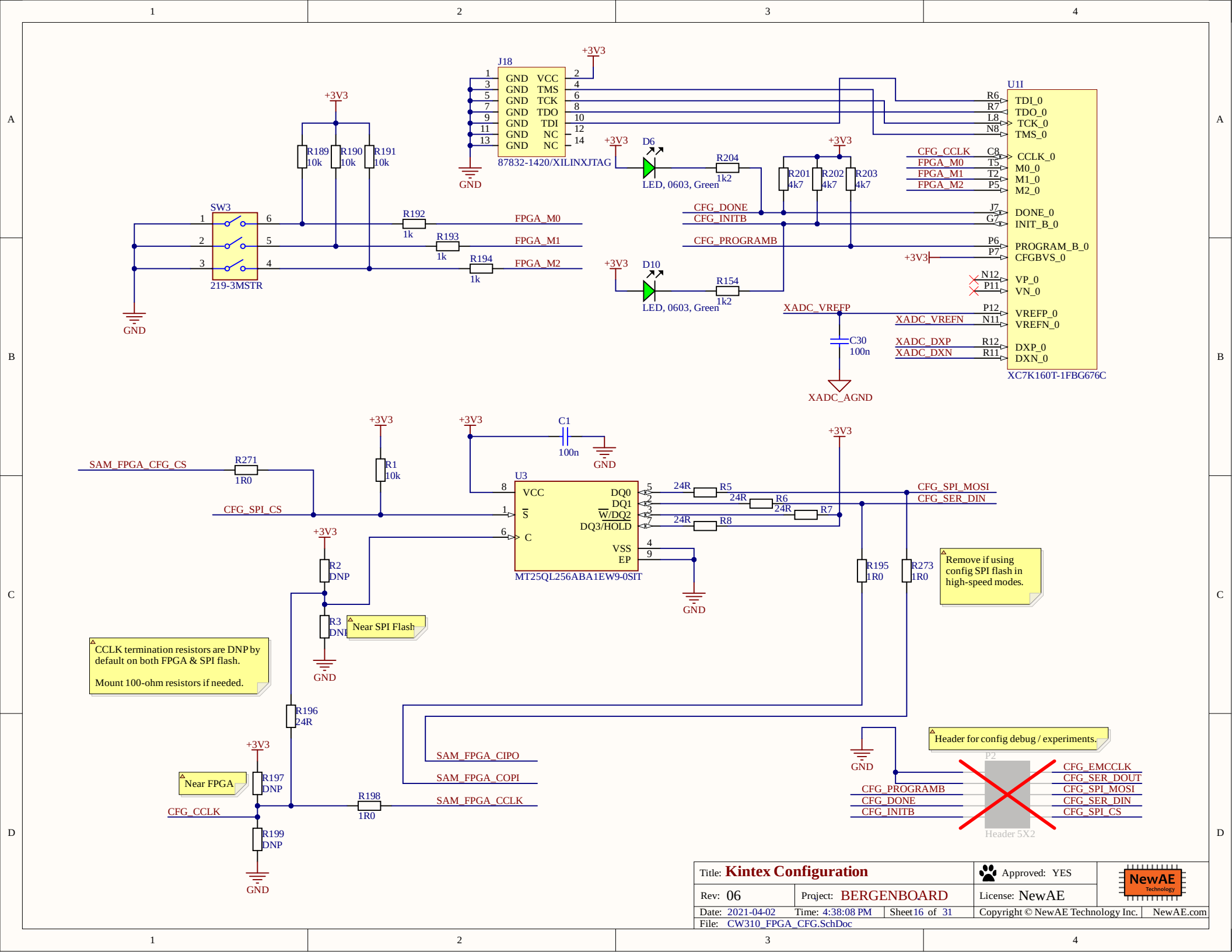
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FPGA MGT Interface



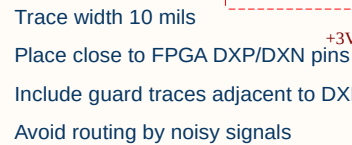


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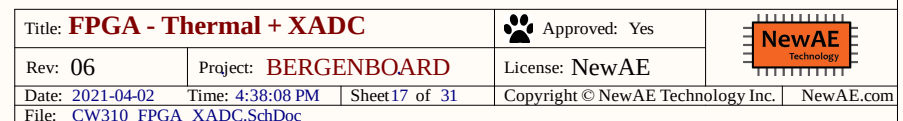


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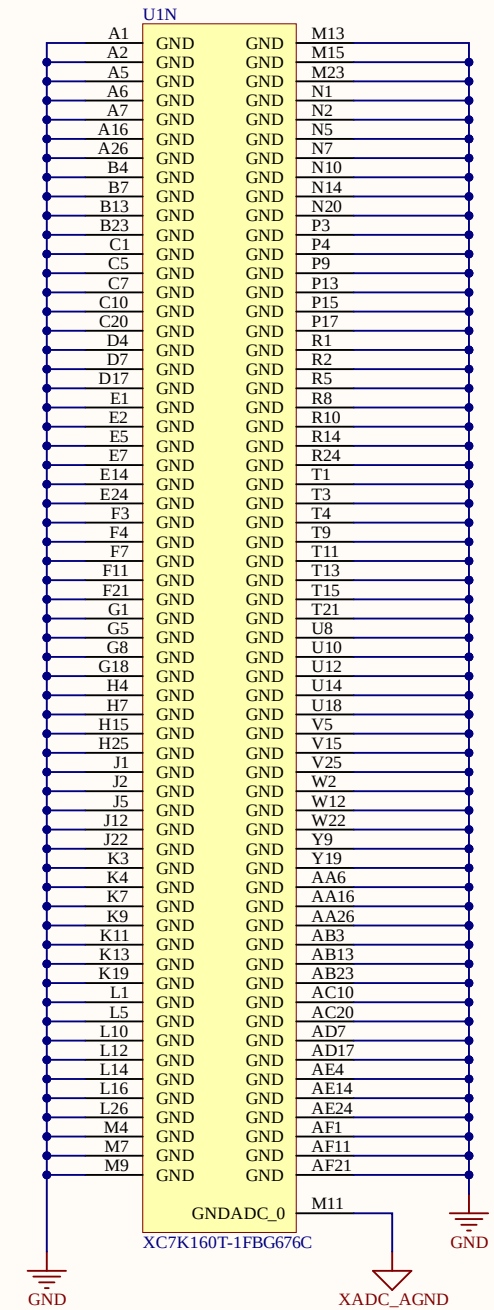
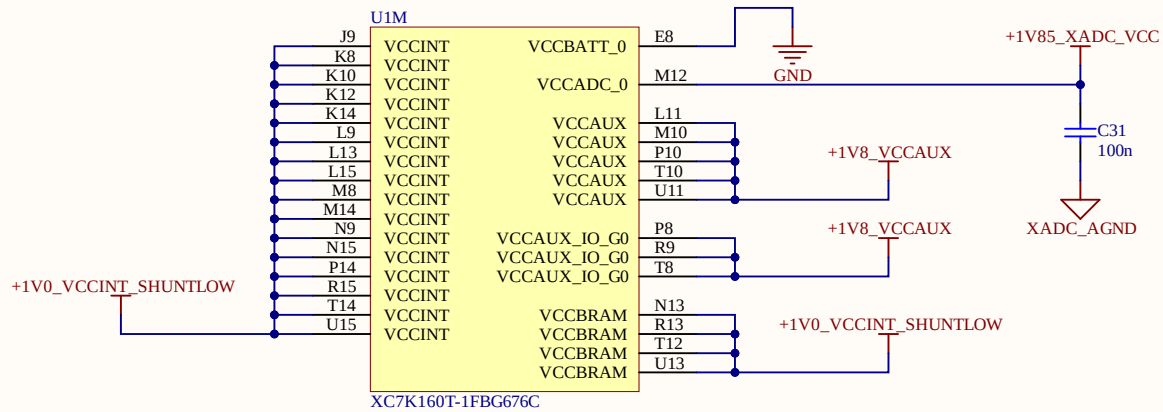
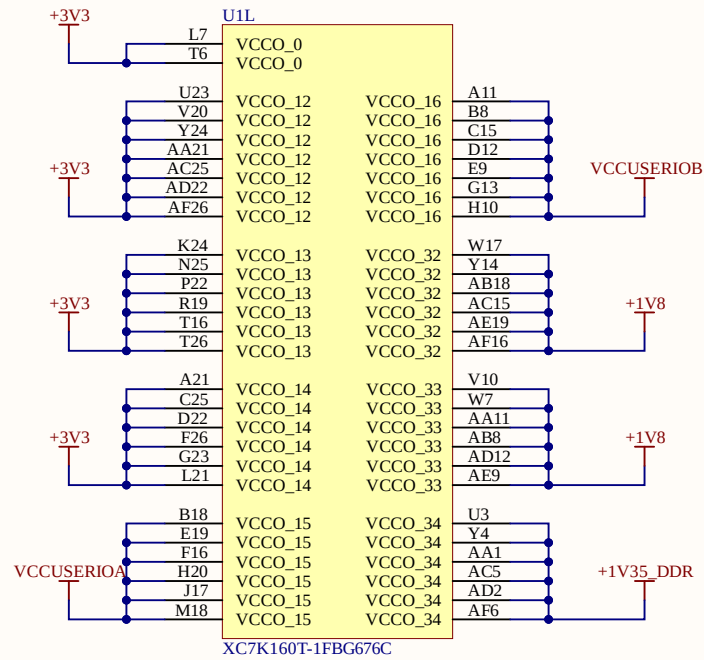


Temperature diode series resistance = 2

D



FPGA POWER



Title: **Kintex Power Connections**

Approved: YES

Rev: 06

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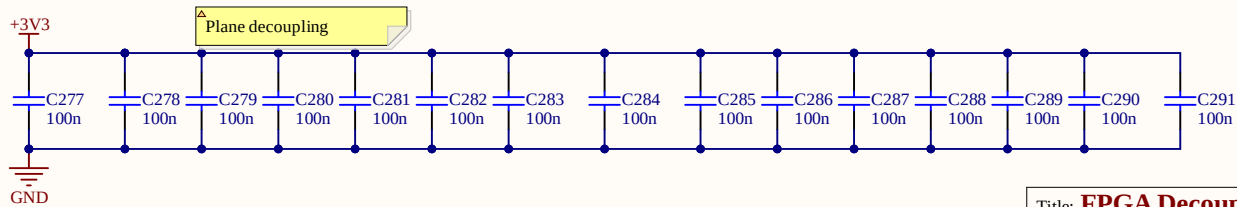
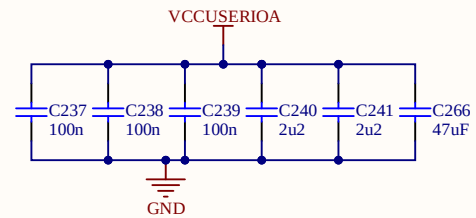
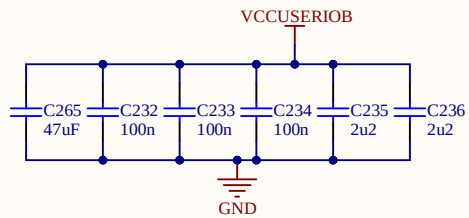
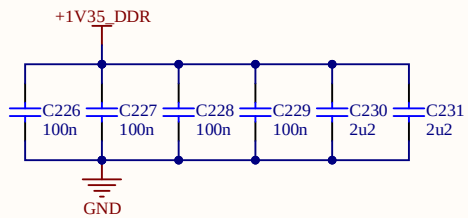
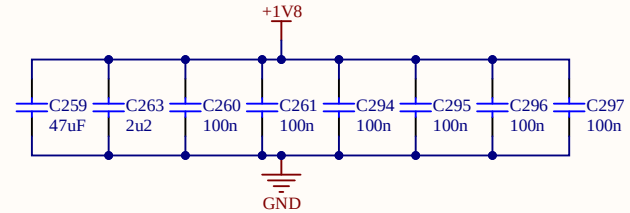
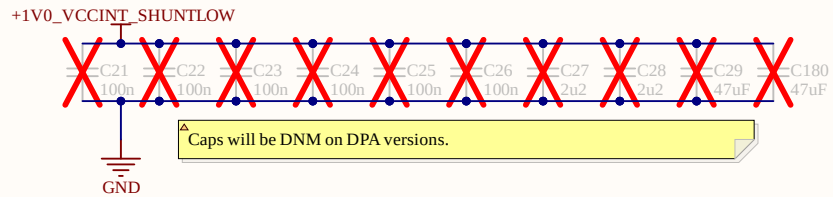
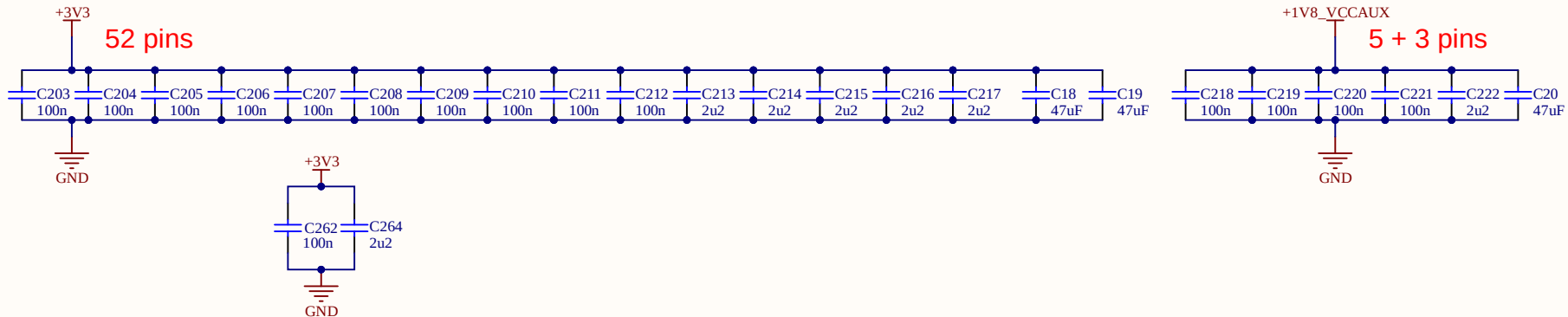
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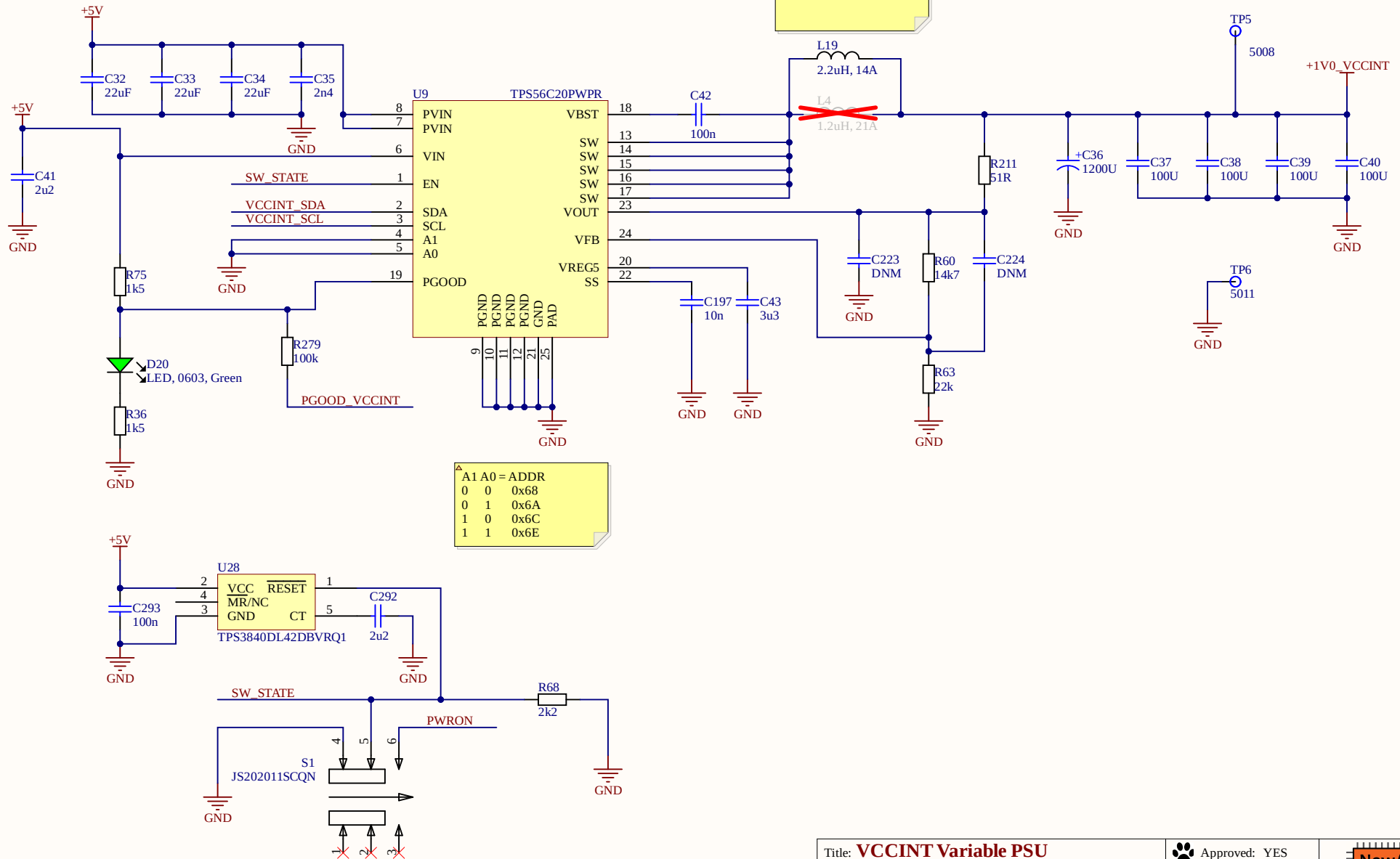


FPGA Decoupling



Title: FPGA Decoupling			 Approved: Yes		
Rev: 06	Project: BERGENBOARD		License: NewAE		
Date: 2021-04-02	Time: 4:38:08 PM	Sheet 19 of 31	Copyright © NewAE Technology Inc.		NewAE.com
File: CW310_FPGA_DECOUP.SchDoc					

FPGA VCCINT Power Generation / Control



Title: **VCCINT Variable PSU**

Approved: YES

Rev: 06

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Date: 2021-04-02

Time: 4:38:08 PM

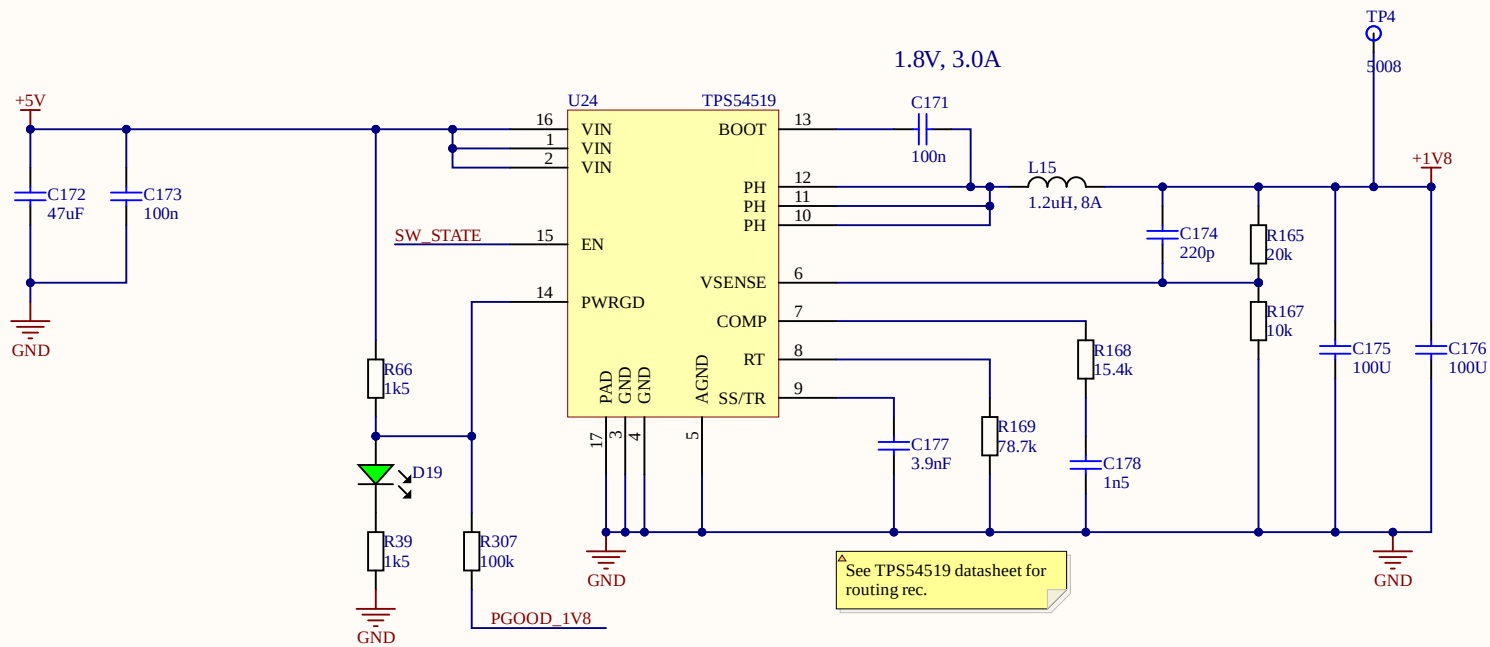
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File: CW310_PSU_VCCINT.SchDoc





Title: **VCC-AUX SMPS**

Approved: YES

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Date: 2021-04-02

Time: 4:38:08 PM

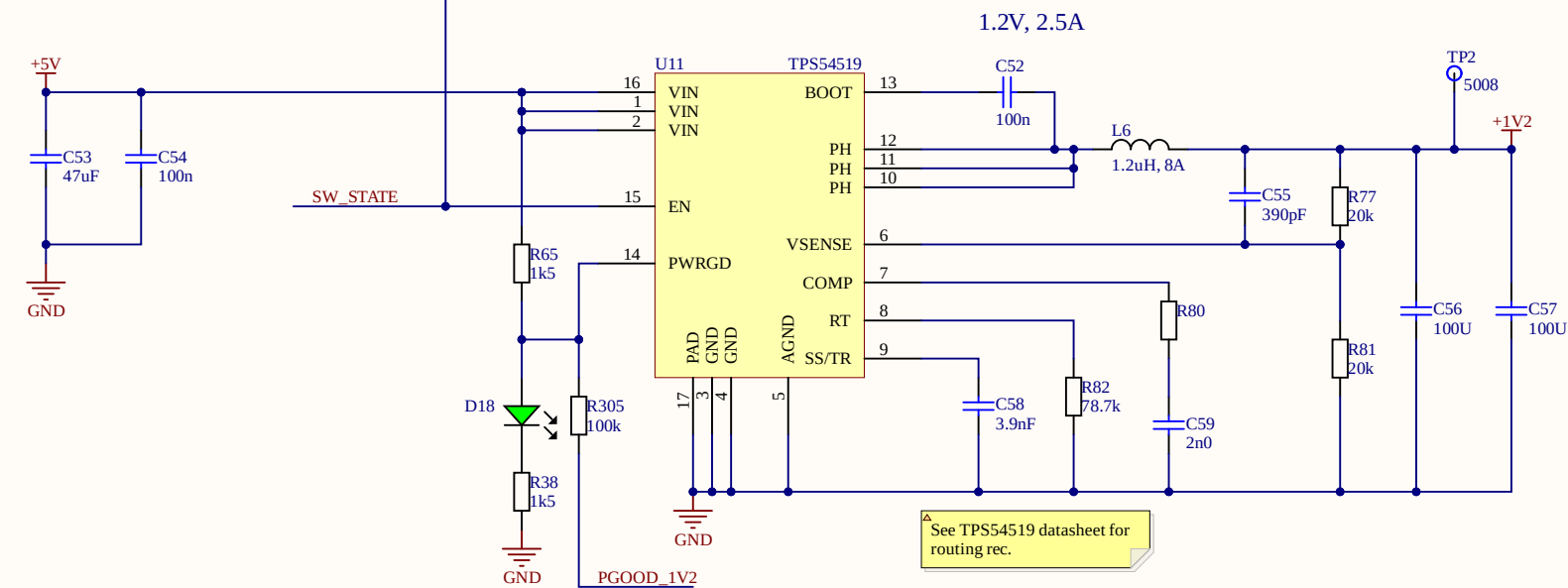
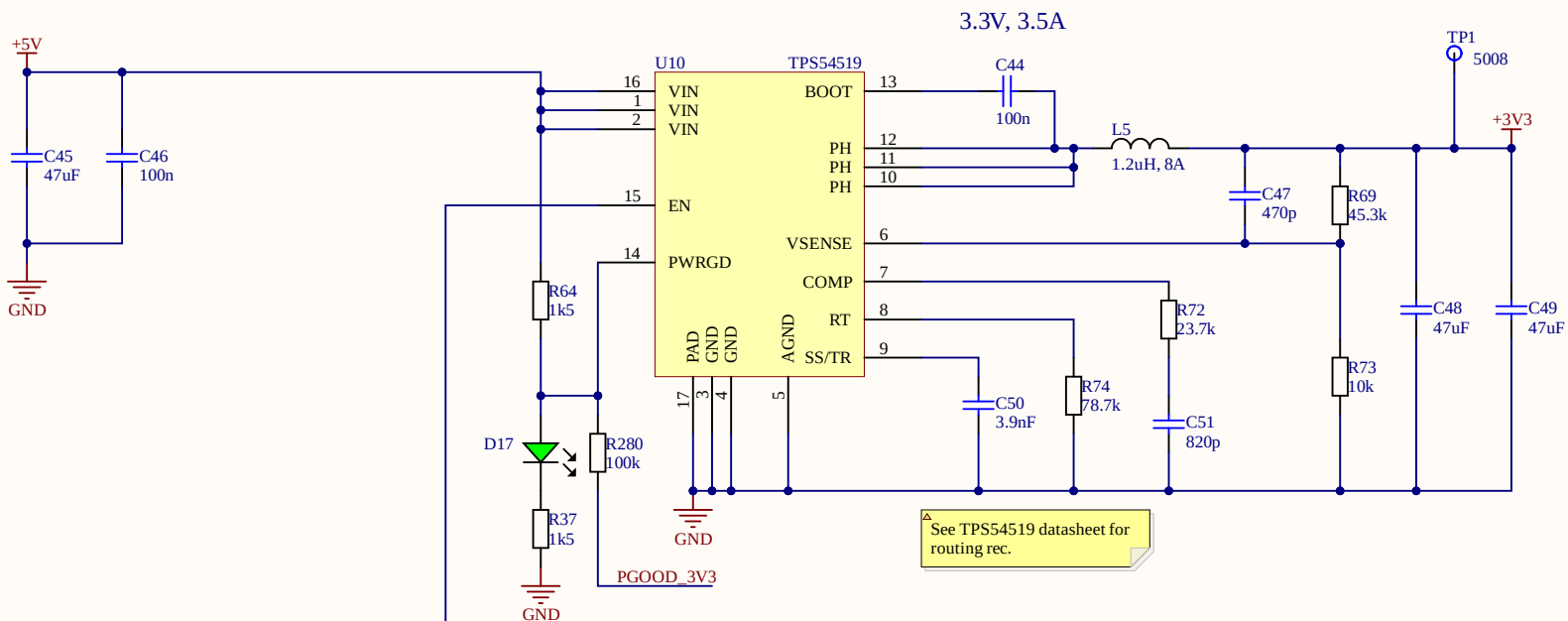
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Title: **VCCIO Fixed Supplies**

Approved: Yes

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File: **CW310_PSU_VCCIO.SchDoc**



FPGA Ethernet

Title: **User Ethernet**

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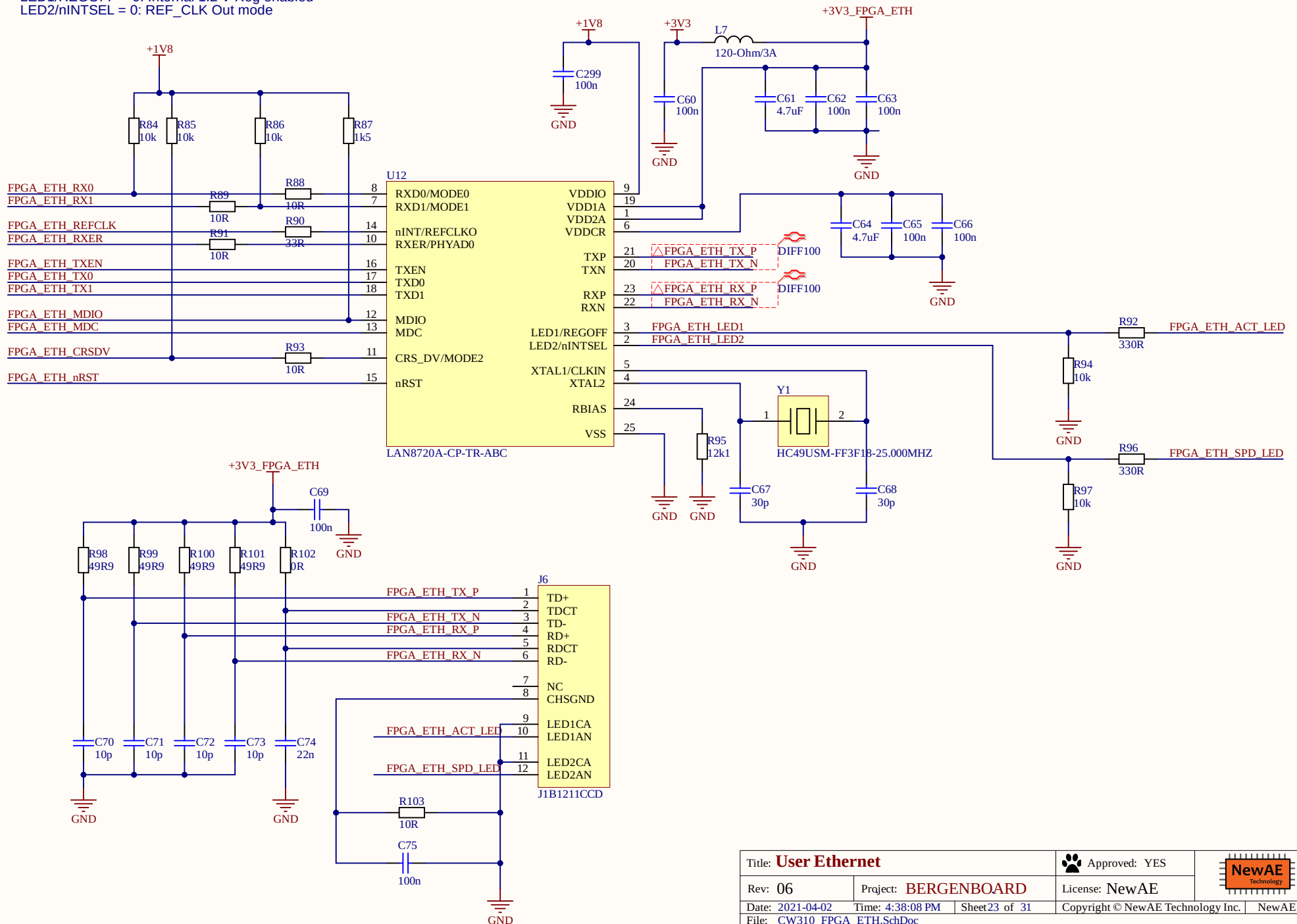
Project: **BERGENBOARD**

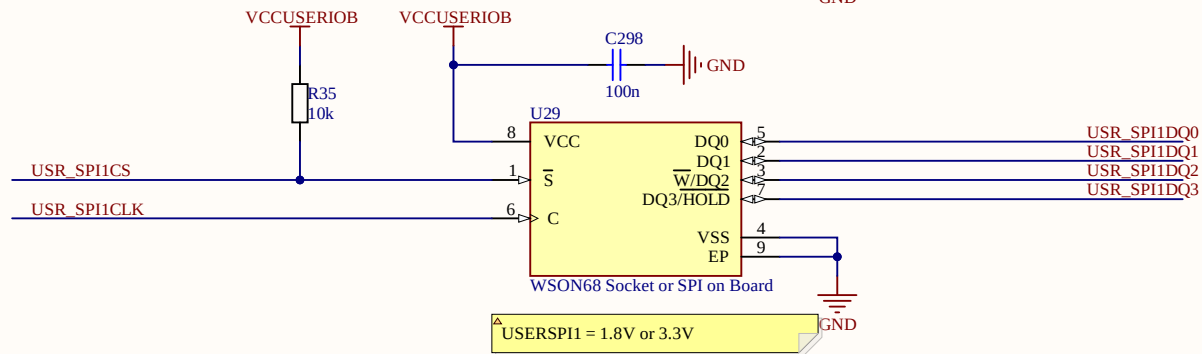
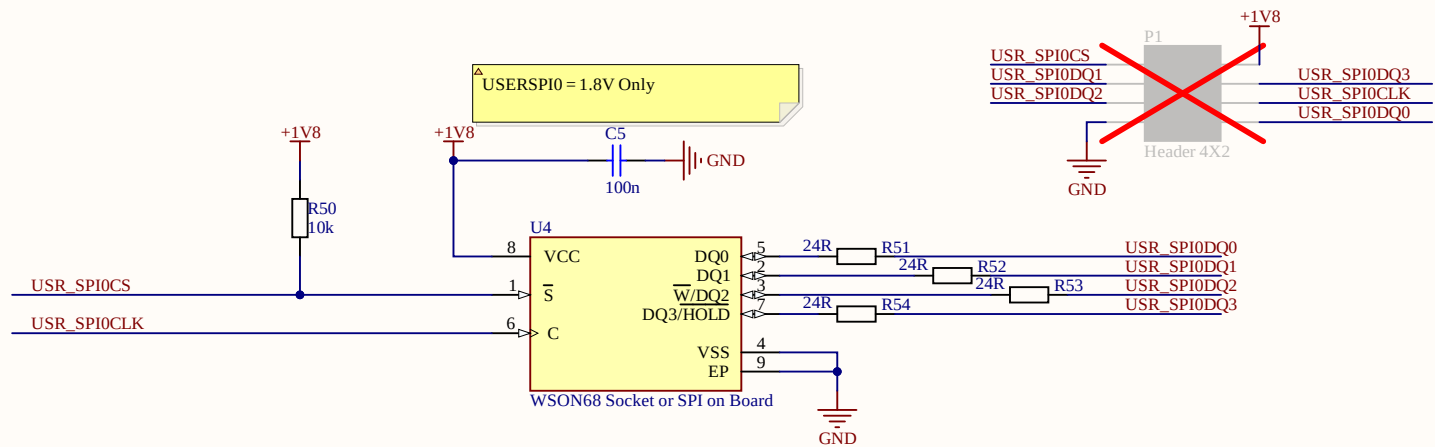
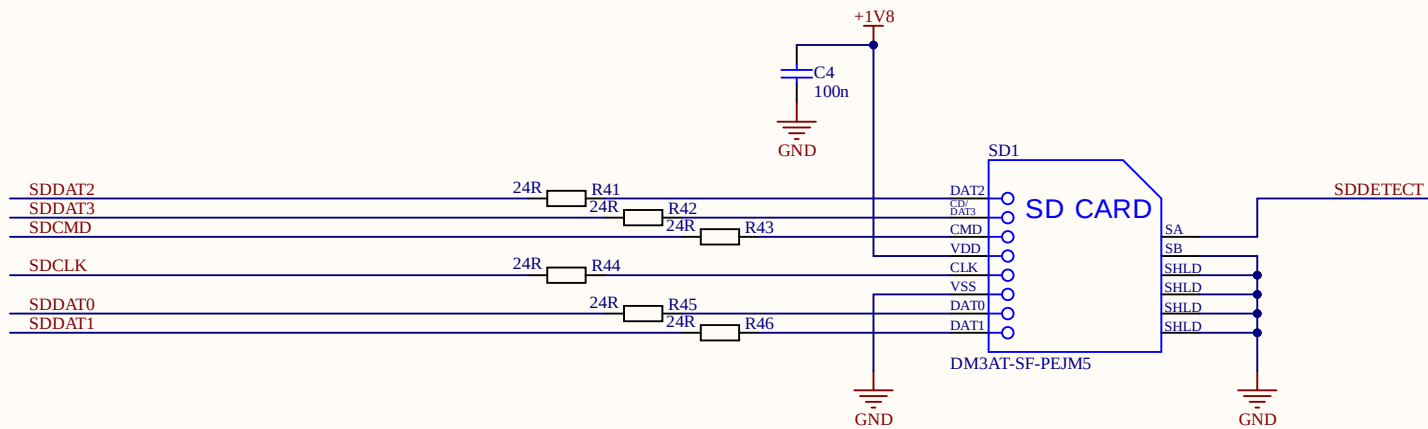
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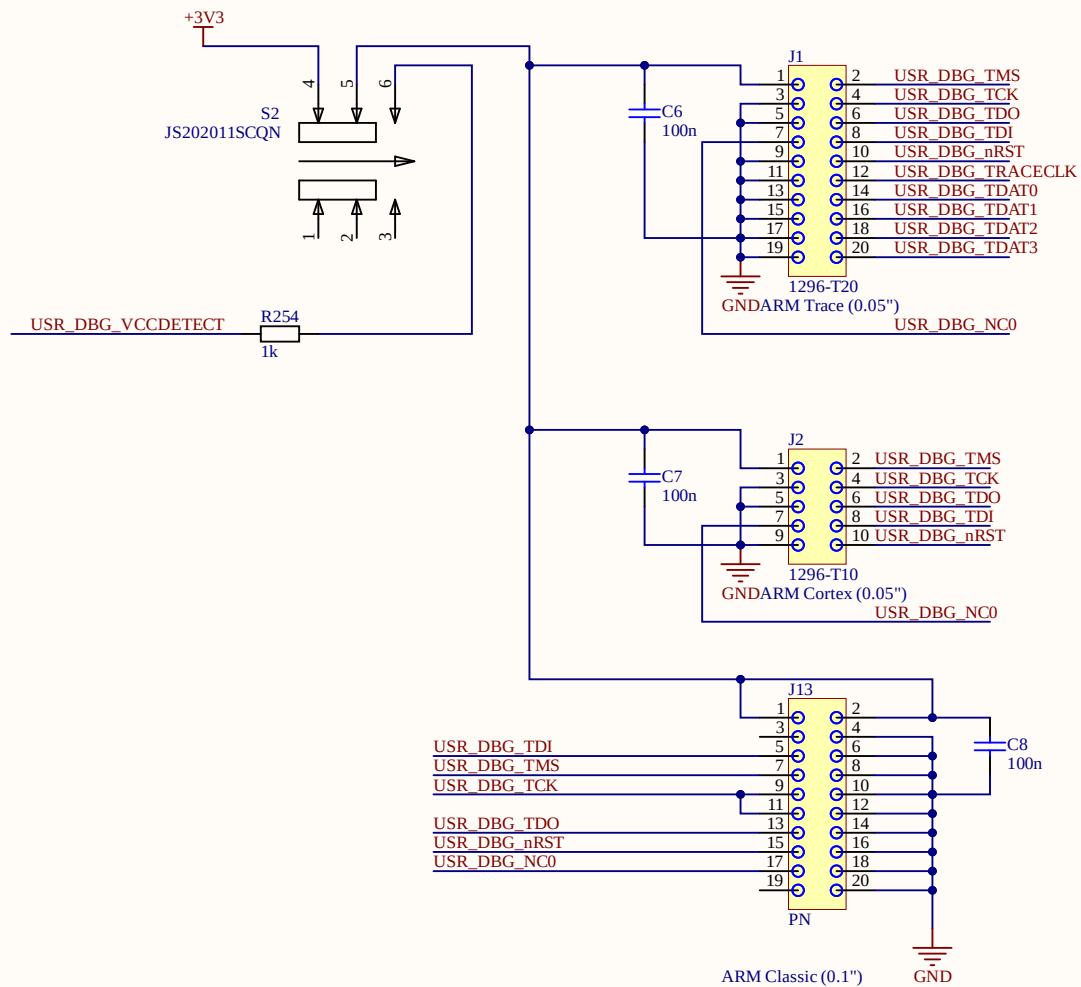
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File: CW310_FPGA_ETH.SchDoc

[illegible]



Title: **User Debug Headers**

Approved: Yes

Rev: 06

Project: **BERGENBOARD**License: **NewAE**

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File: CW310_USERIO_debug.SchDoc



A

A

B

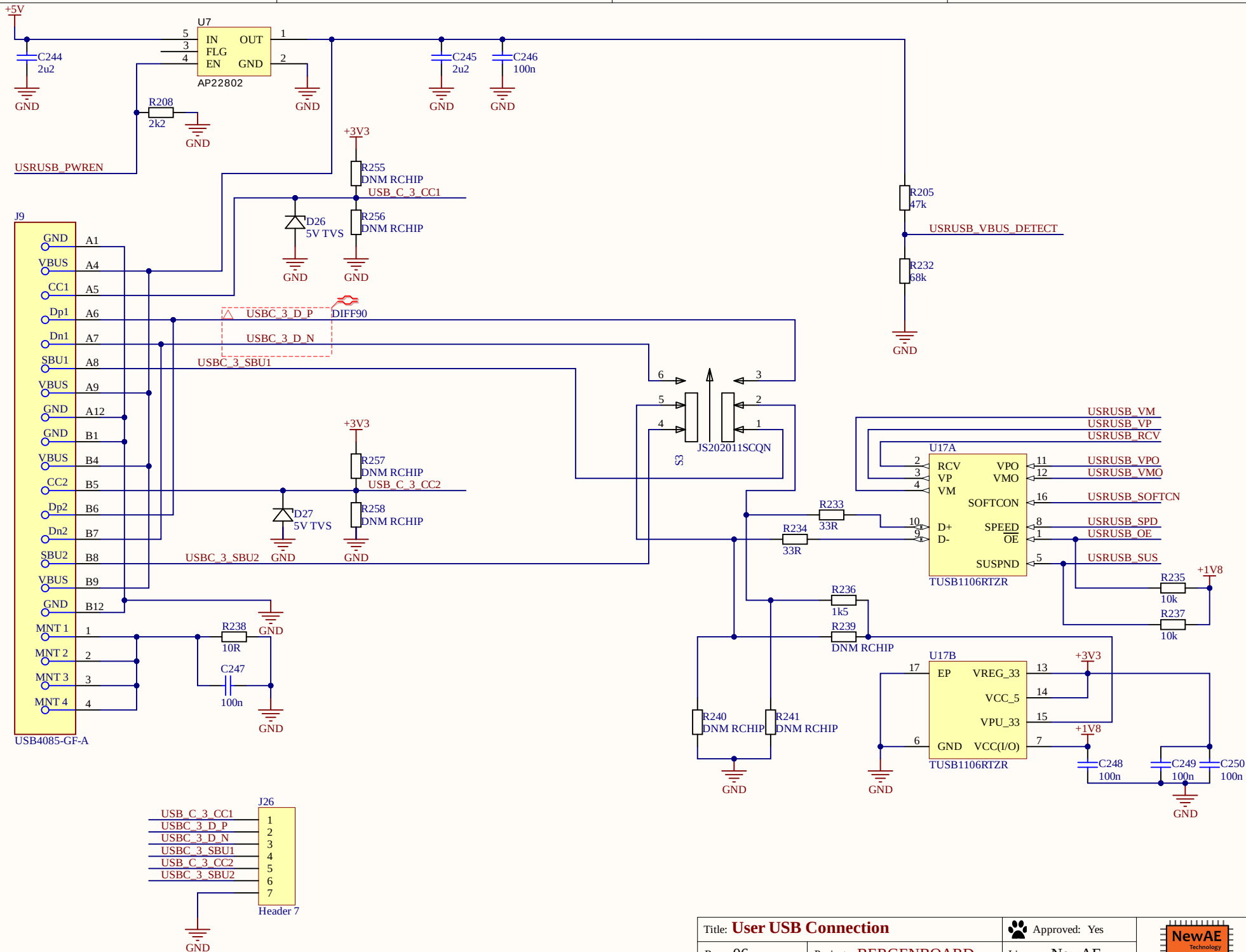
B

C

C

D

D

Title: **User USB Connection**
 Approved: Yes

Rev: 06

Project: **BERGENBOARD**

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Date: 2021-04-02

Time: 4:38:09 PM

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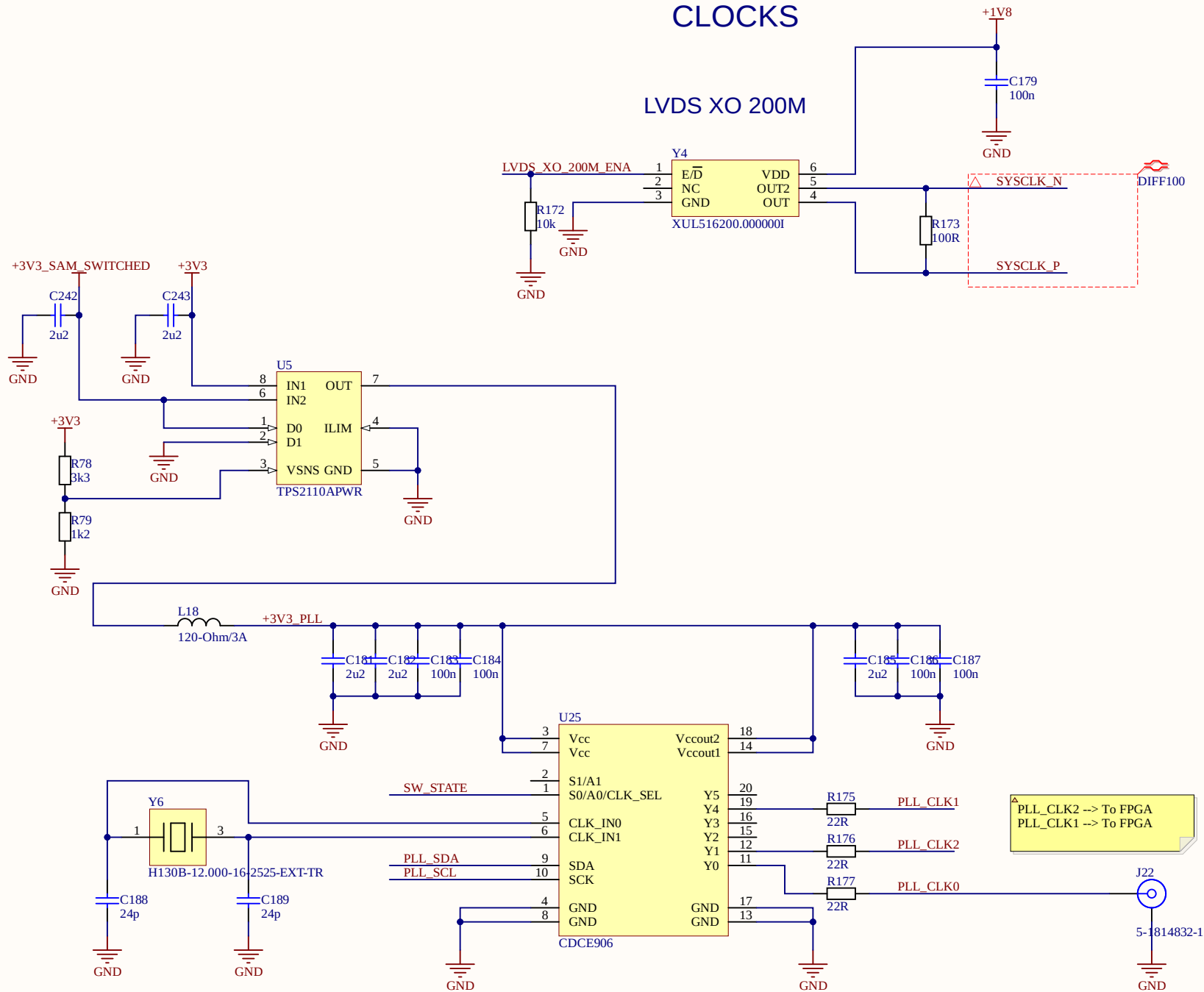
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File: CW310_USERIO_USB.SchDoc



CLOCKS

LVDS XO 200M



Title: **PLL, Clocks for FPGA**

Approved: Yes

Rev: 06

Project: **BERGENBOARD**

License: NewAE

Date: 2021-04-02

Time: 4:38:09 PM

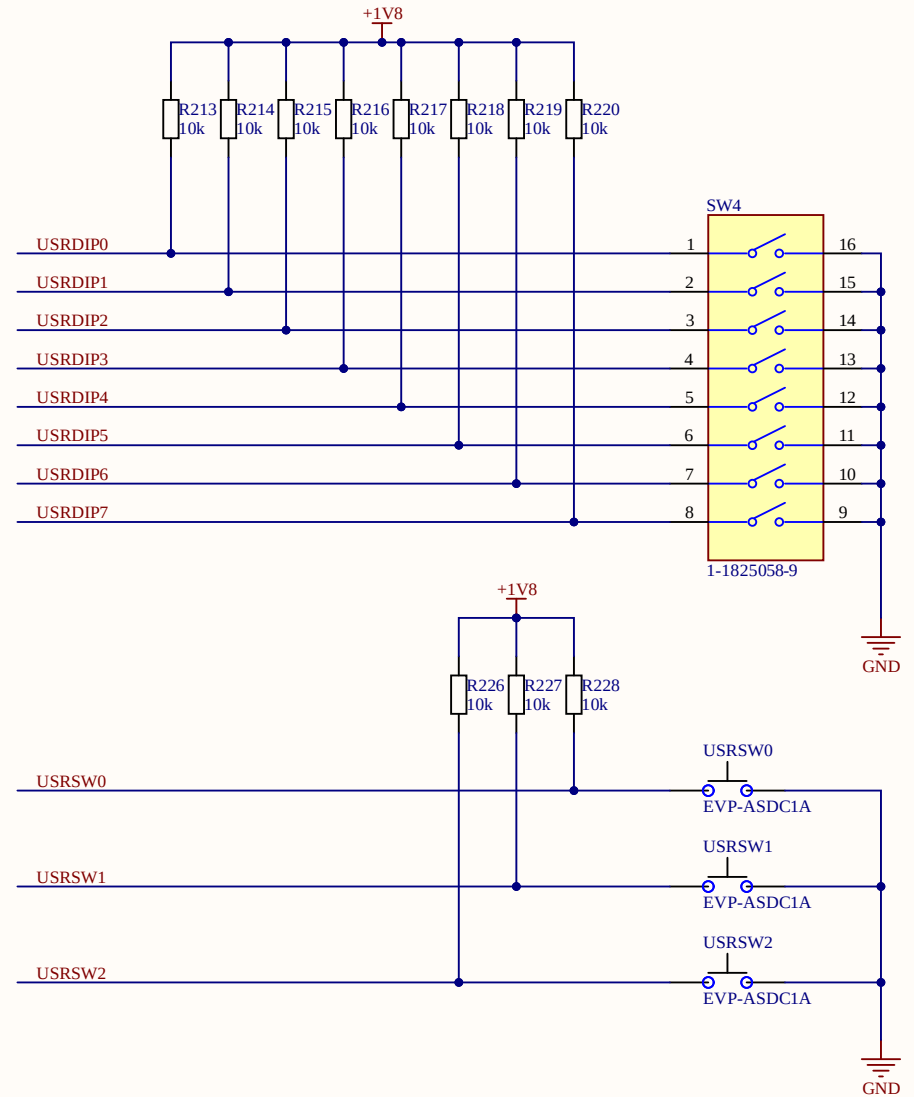
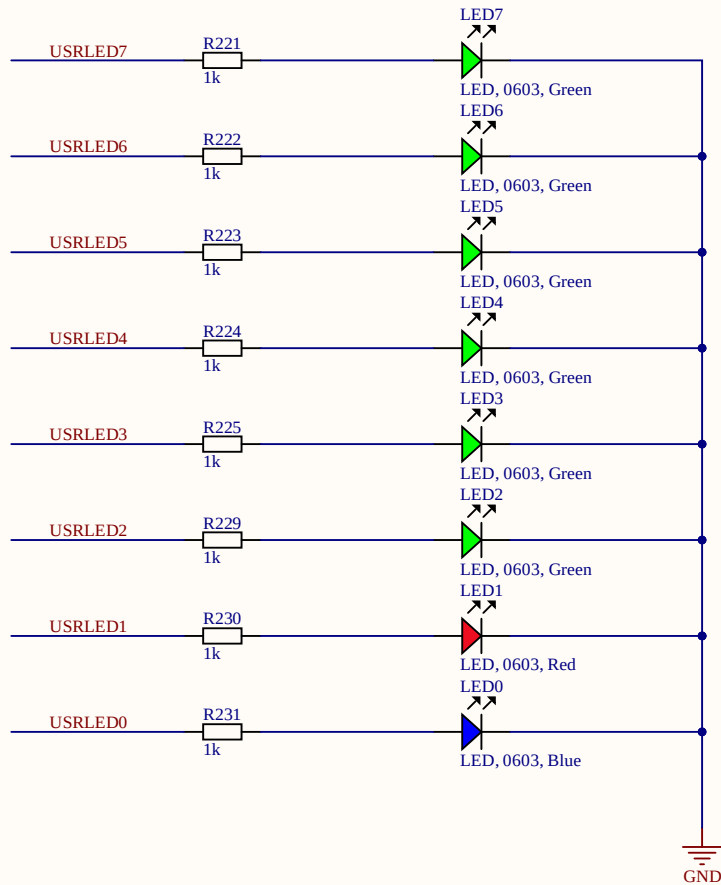
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File: CW310_Clocks.SchDoc





Title: **User LED / Switches**

Approved: Yes

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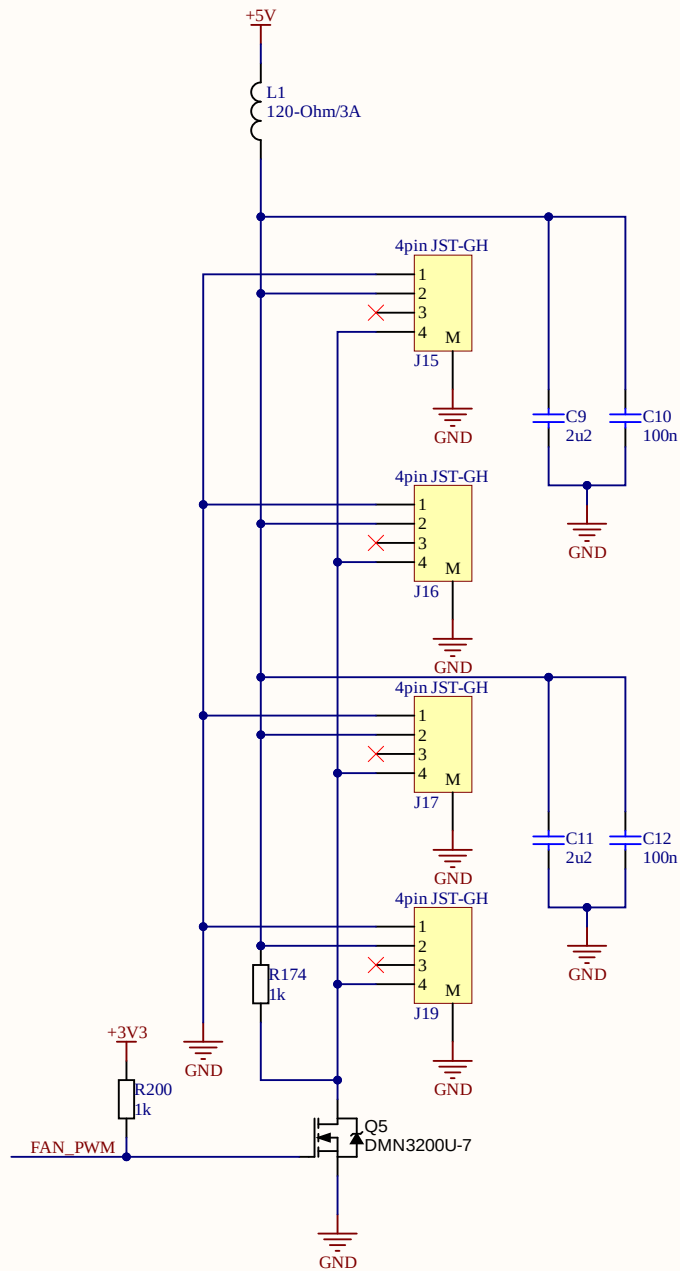
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File: **CW310_STATUS_LEDs.SchDoc**





2x connectors top & bottom. One for blower fan, one for heatsink-mounted fan.

2-pin fan, or 3-pin fan with tach output:
 * Connect pin 2 (VCC), pin 4 (GND).
 4-pin fan, or 3-pin fan with control input:
 * Connect pin 1 (GND), pin 2 (VCC), pin 4 (CTRL).
 If fan has tach output, connect to pin 3 (NC) to terminate header.

Mating connector:
 * Housing GHR-04V-S
 * Contacts SSL-002T-P0.2
 * Crimp tool YRS-1590

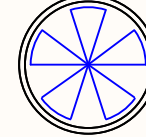


HS1
960-29-18-D-AB-0



HS2
960-29-18-D-AB-0

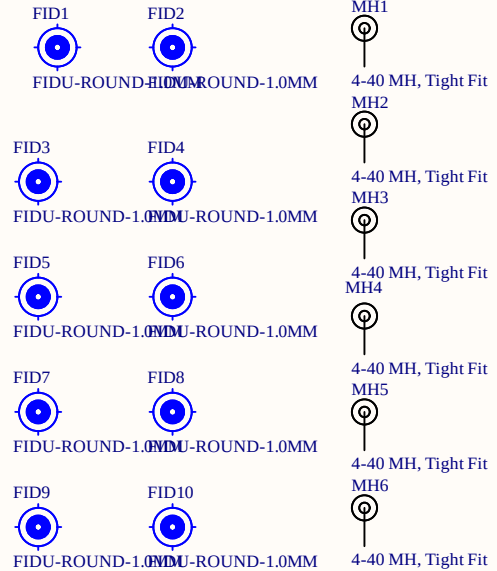
FAN1



Blower Fan, 5V, 35x35mm

Fan mounted top or bottom side of board. Blower style to pass over "open die top".

Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.



Title: **FAN Headers**

Approved: Yes

Rev: 06

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