ChipWhisperer CW310 "Bergen Board" - Xilinx Kintex 7 Target Board

NewAE Technology Inc.

Suggested Layer Stack

Bergen Towel Mat

Bed 1

Bed 2

Table of Contents

Revision Summary

-00:
Ultra-alpha.

-01:
Super-alpha.

-02: March 10/2021
Feature complete.

-03: March 13/2021
Internal release.

-04: March 15/2021
Add brown-out on 5V, silkscreen updates

-05: March 22/2021
Change FPGA routing for HP/HR banks.

-06: March 30/2021
Mark DNP parts, fix a few missing resistors.

Title: **Bergen Board - The Cover Sheet**		Approved: Yes	NewAE Technology
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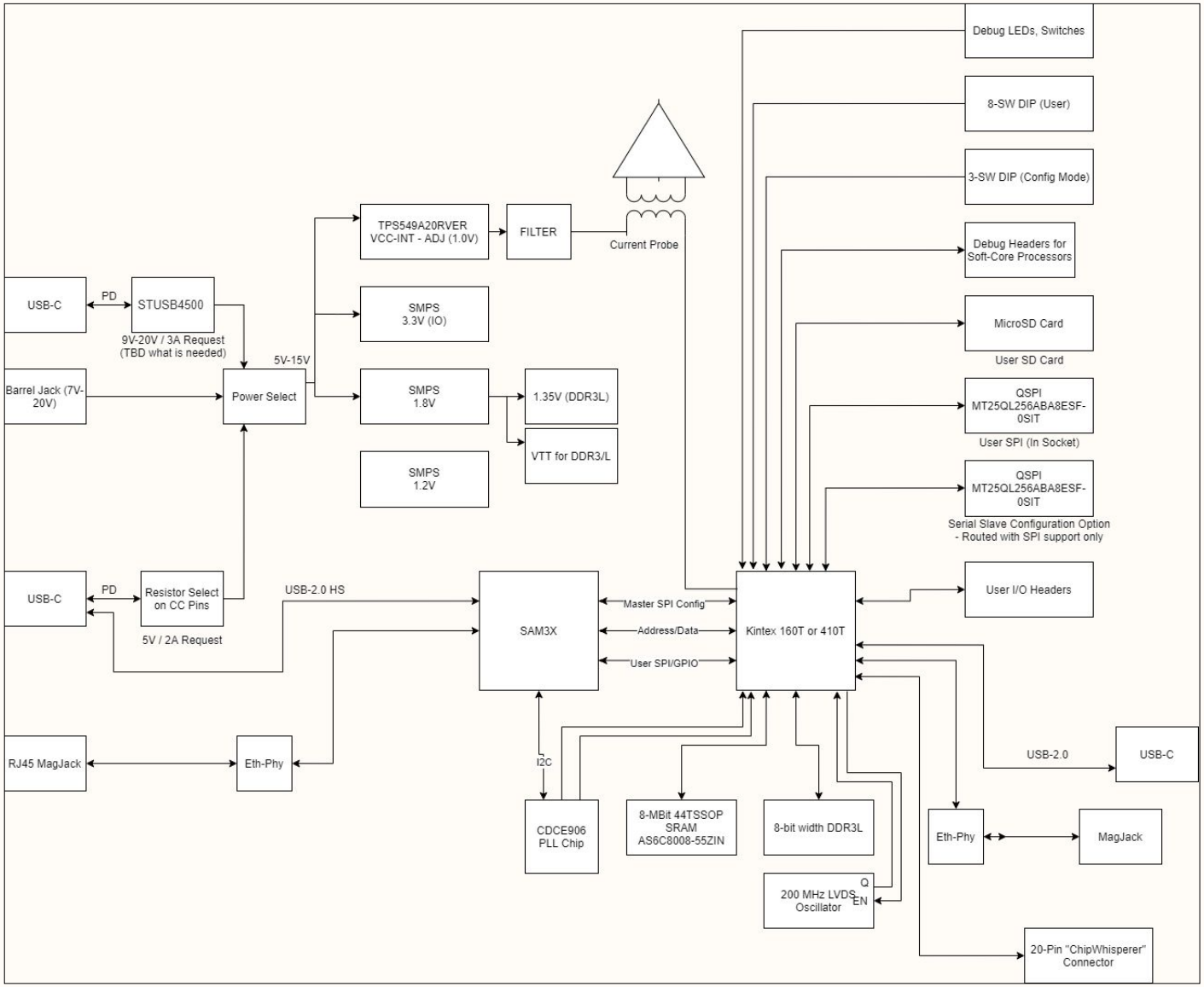
Block Diagram



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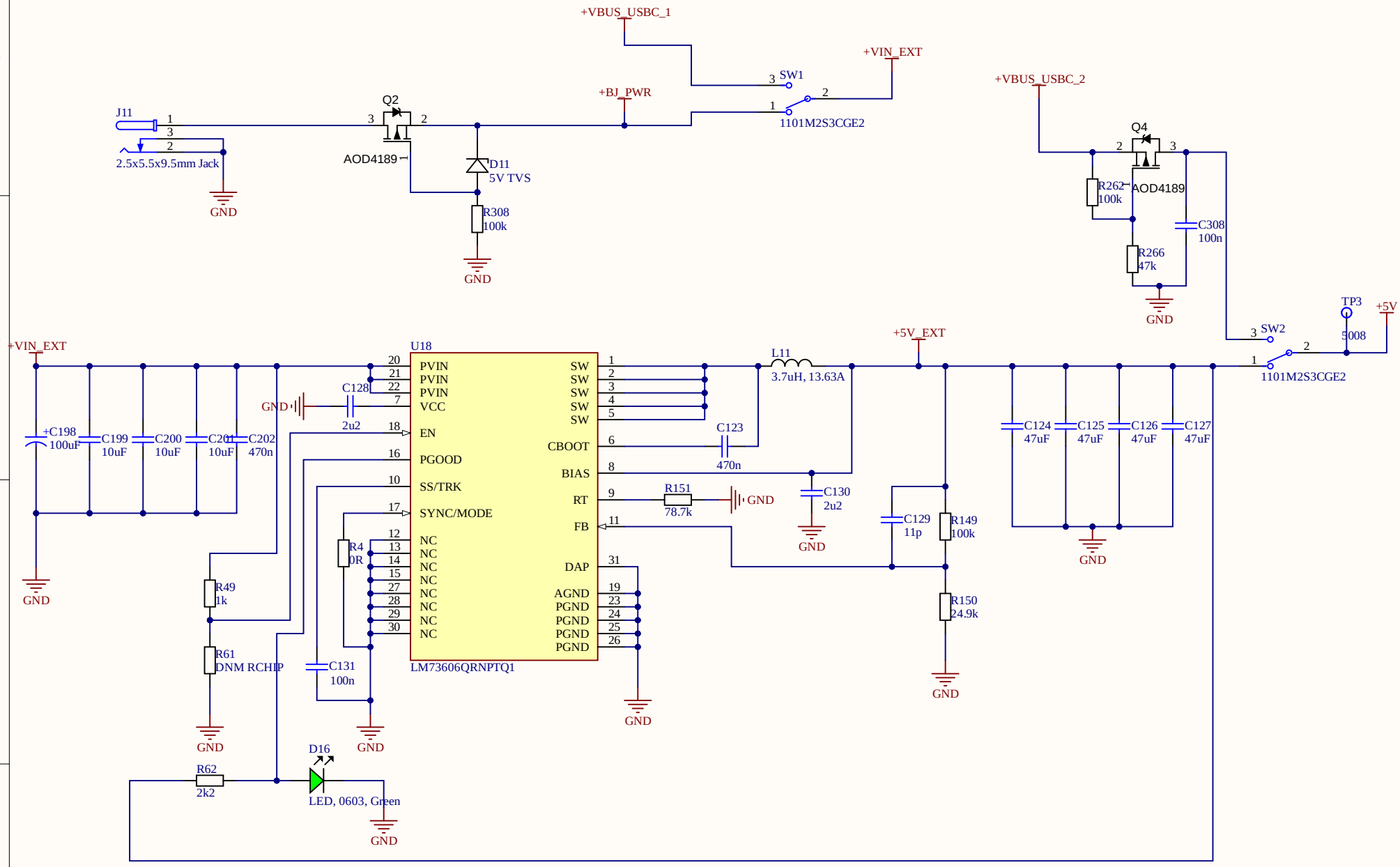
INPUT POWER



Based on design from
https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=9C49F428E2C4FF82

Title: **5V Regulator**		Approved: Yes	NewAE Technology
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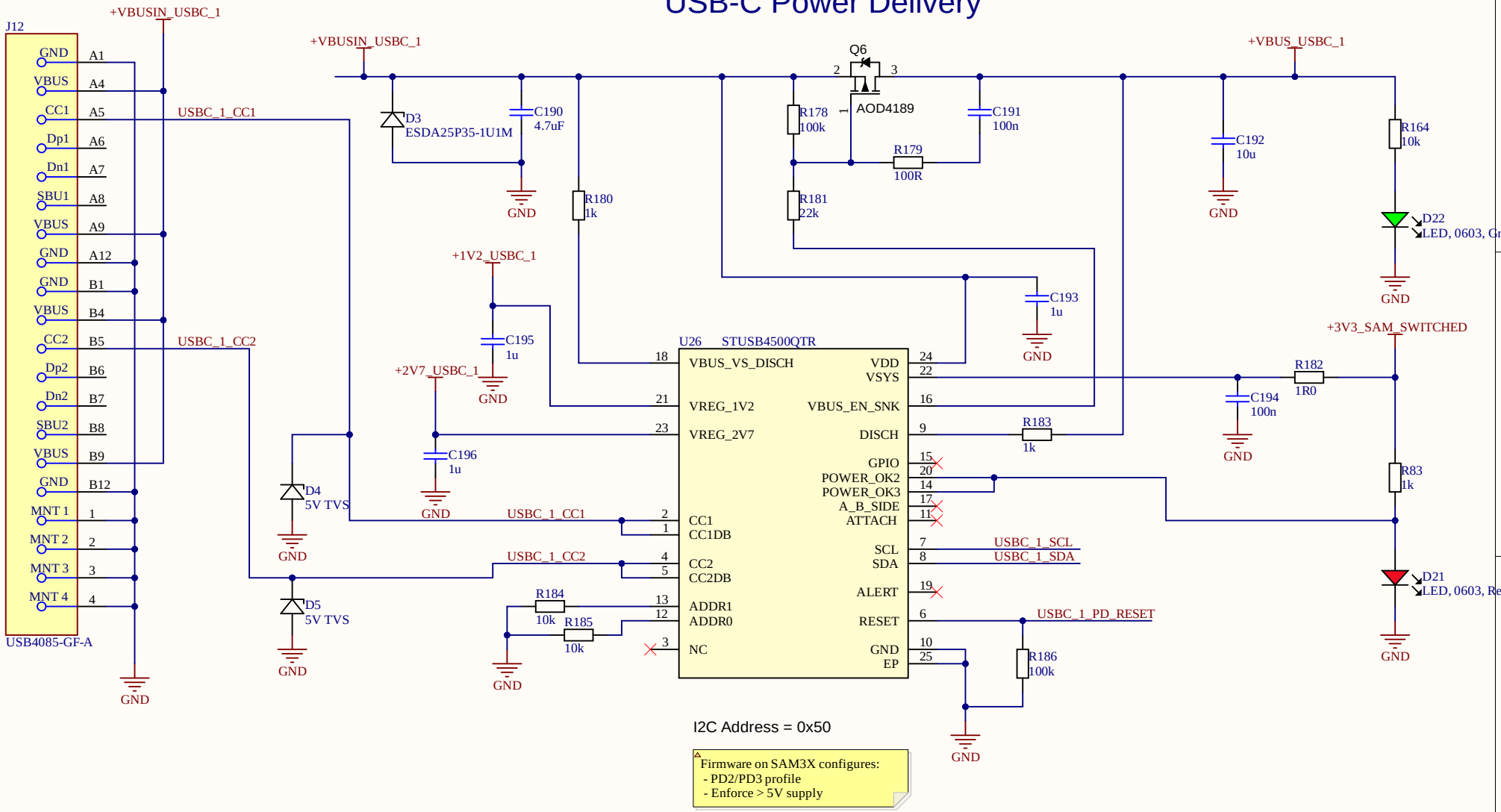
USB-C Power Delivery



Title: **USB-C PD Controller**		Approved: Yes	
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File: CW310_USB_POWER.SchDoc			

SAM3X CPU

LEDs for over-temp of the FPGA.

LEDs for SAM3X status.

U2A

ATSAM3X8EA-AU

Title: Control MCU Main		Approved: Yes	
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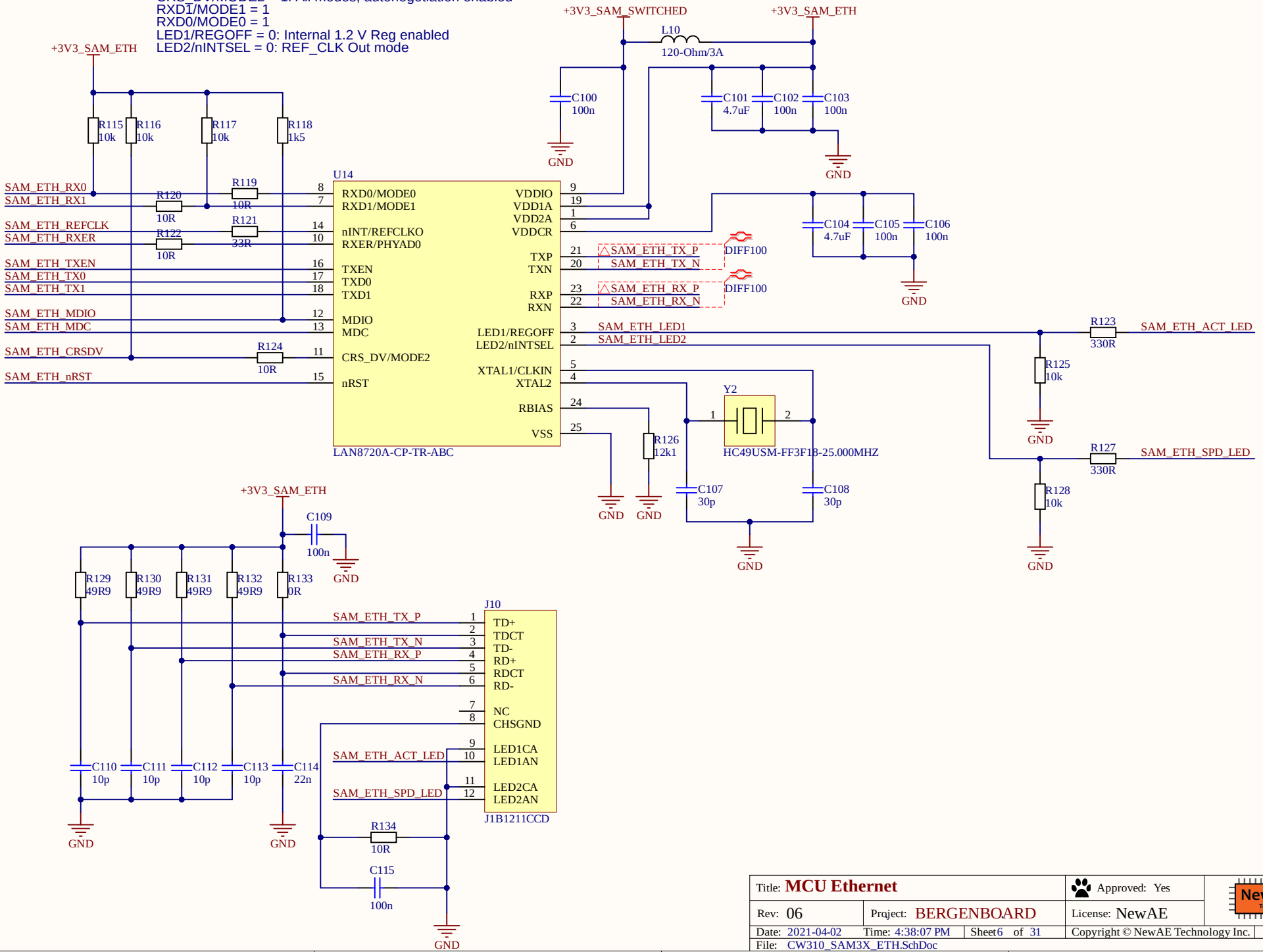
File: CW310_SAM3X_MAIN.SchDoc			

SAM3X Ethernet

LAN8720 PHY Configuration
PHYAD0 = 0: Phy Address 0
CRS_DV/MODE2 = 1: All modes, autonegotiation enabled
RXD1/MODE1 = 1
RXD0/MODE0 = 1
LED1/REGOFF = 0: Internal 1.2 V Reg enabled
LED2/nINTSEL = 0: REF_CLK Out mode



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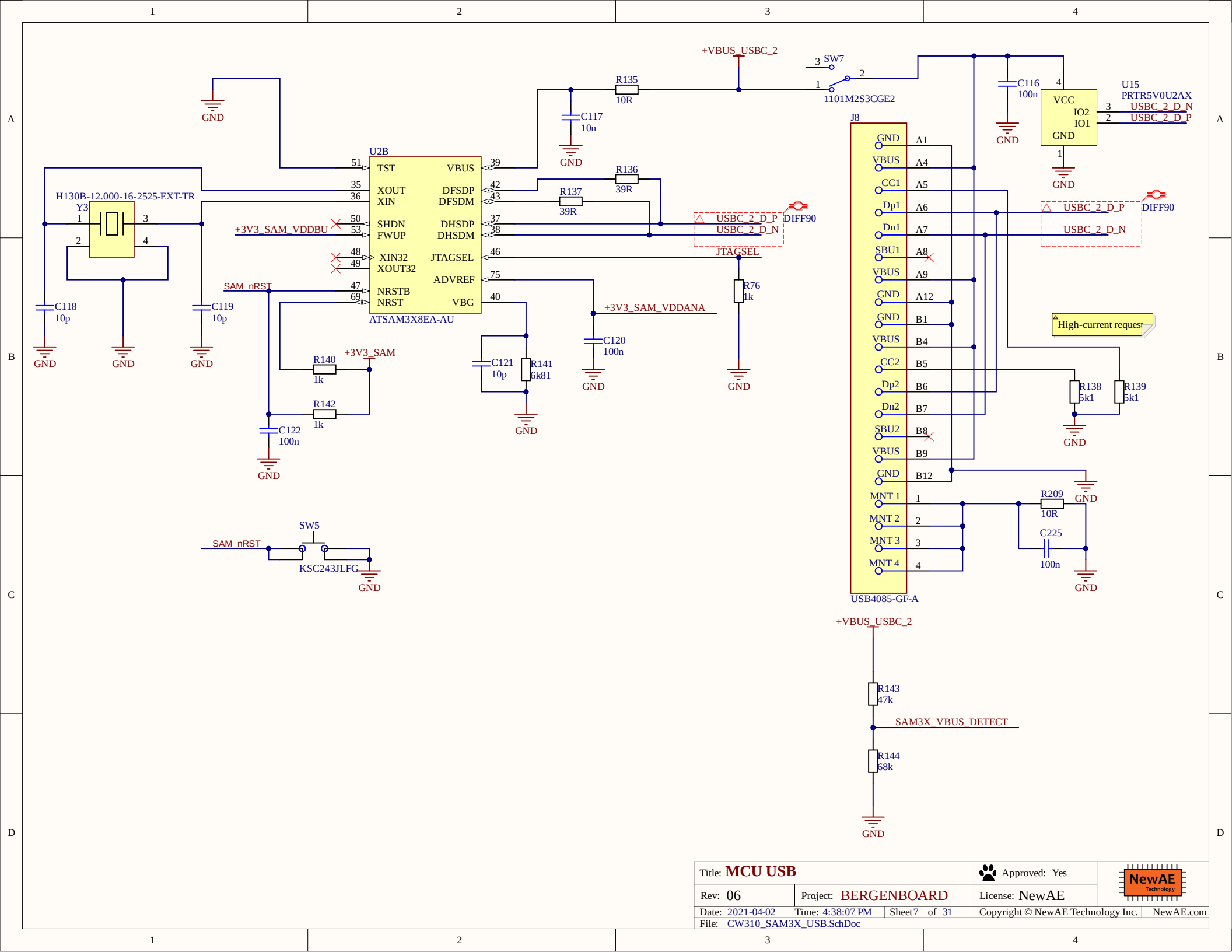

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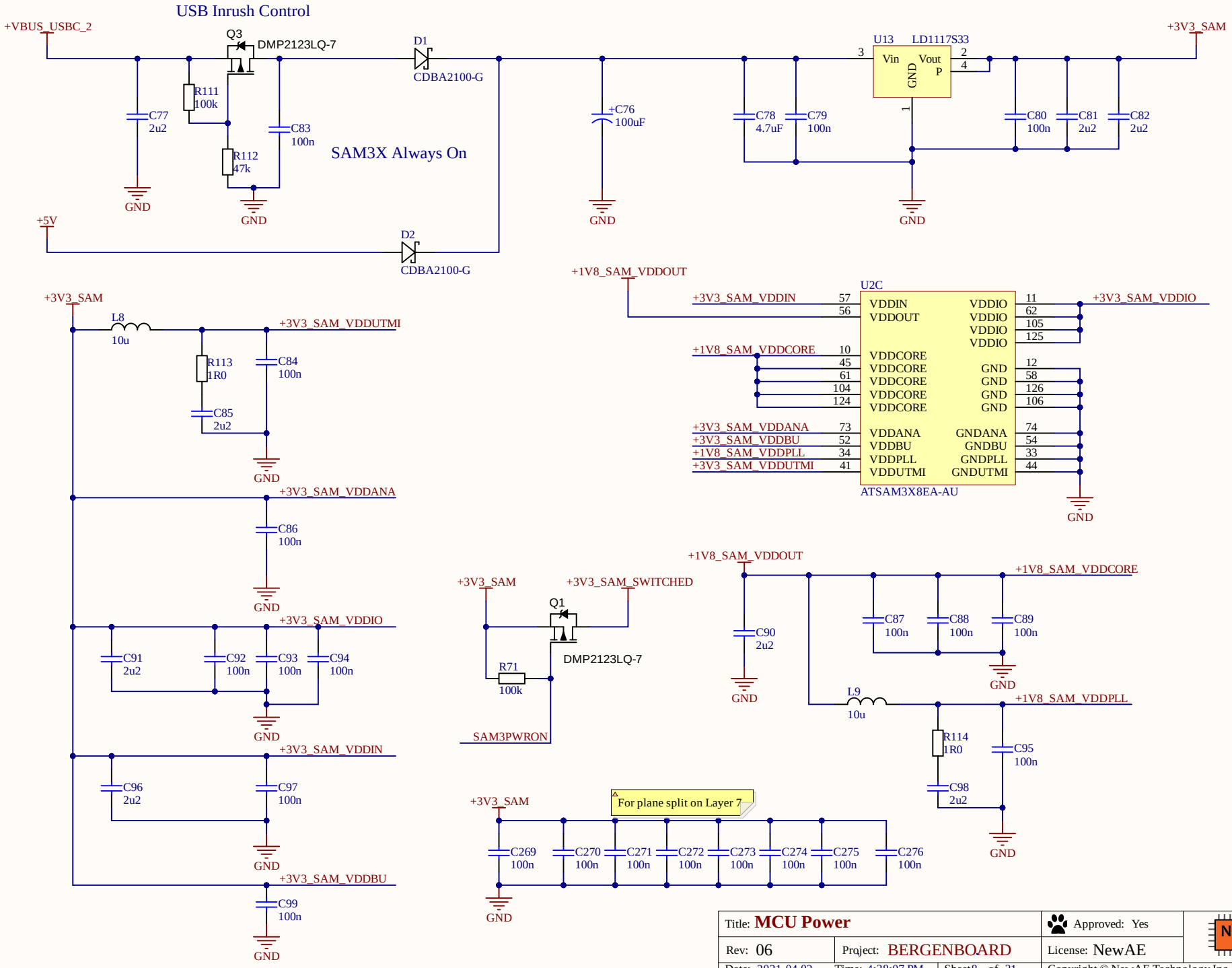
SAM3X Power



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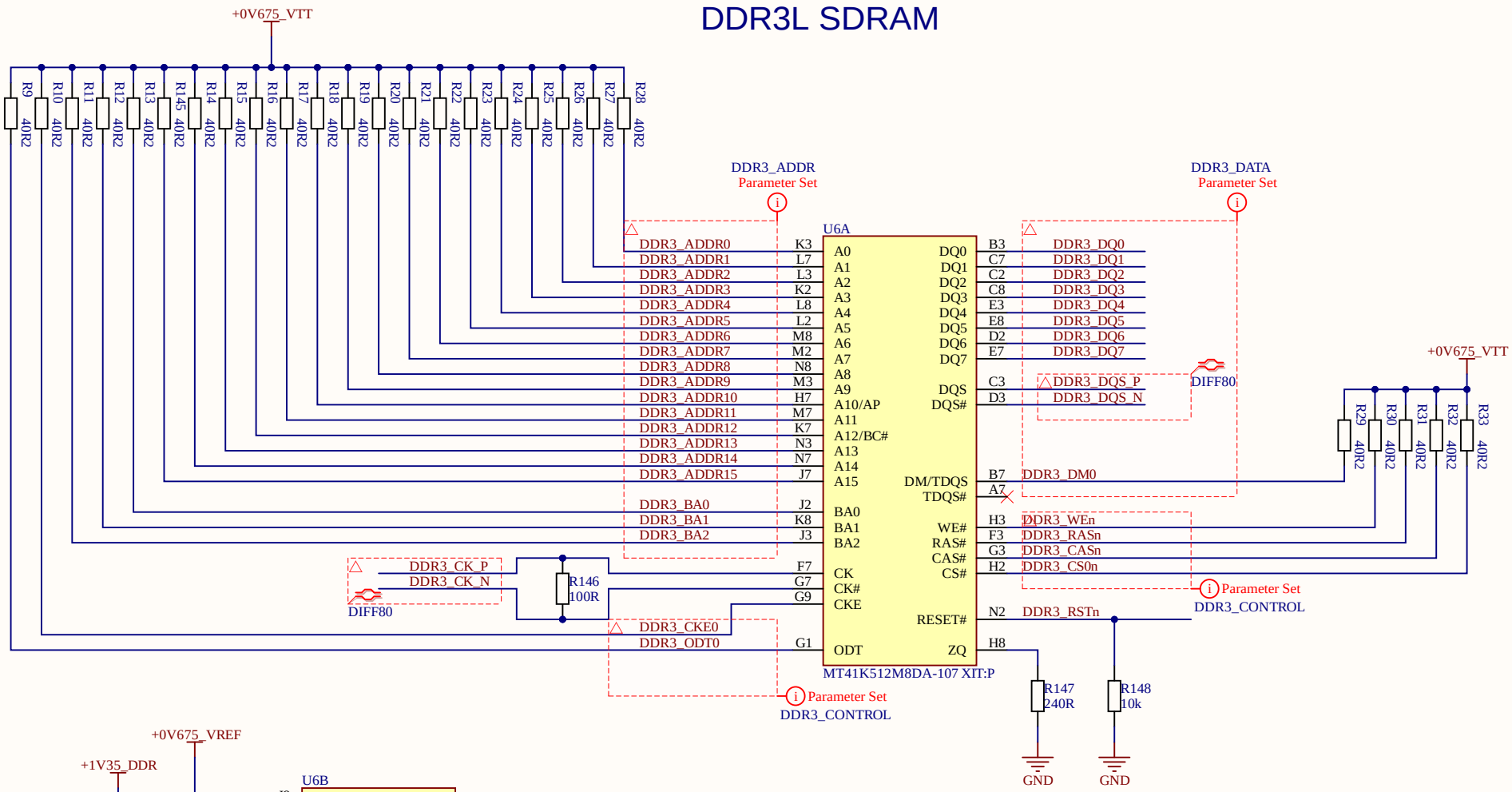
DDR3L SDRAM



Title: **User DDR3**		Approved: Yes	NewAE Technology
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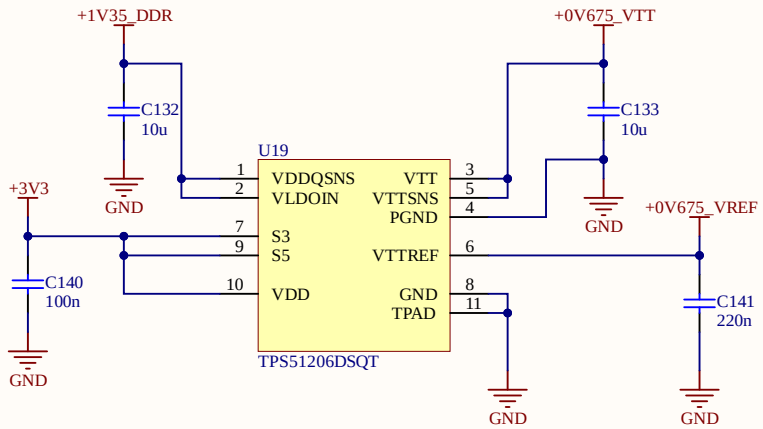
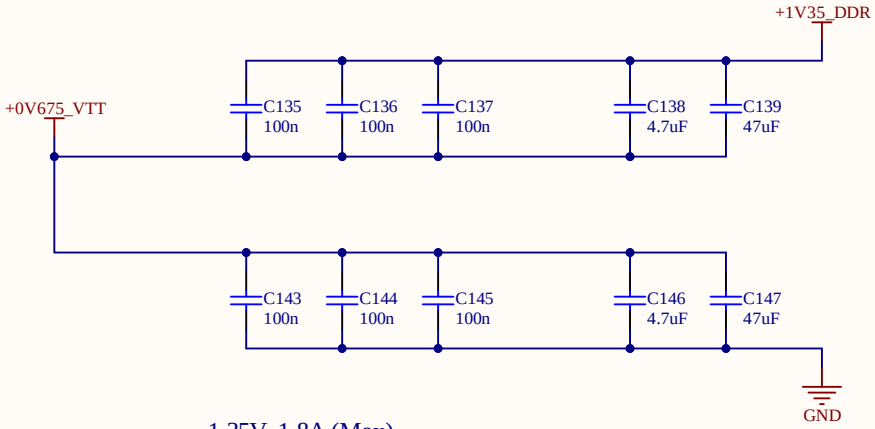
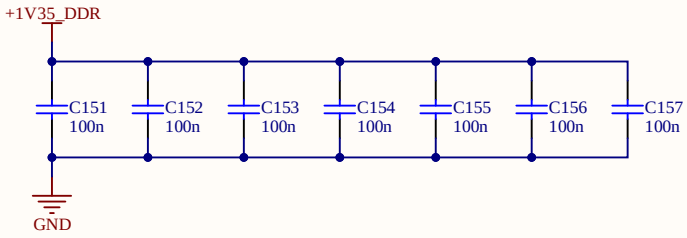
DDR3L VTT & DECOUPLING



Place VTT decoupling capacitor groups by VTT island,
near terminations of DRAM Address & Control lines



Place DRAM decoupling capacitor group near DRAM component



1.35V, 1.8A (Max)

Title: **DDR3L Power Supply**		Approved: Yes	NewAE Technology
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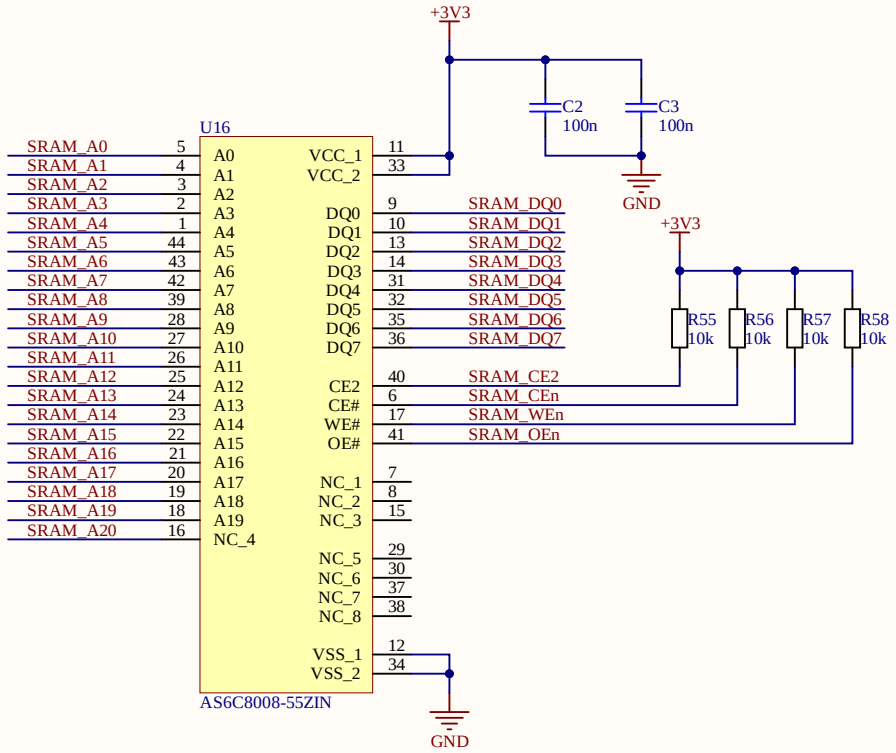
SRAM

SRAM should be footprint compatible with:
AS6C8008-55ZIN
CY62158EV30LL-45ZSXIT
IS62WV10248DBLL-55TLI



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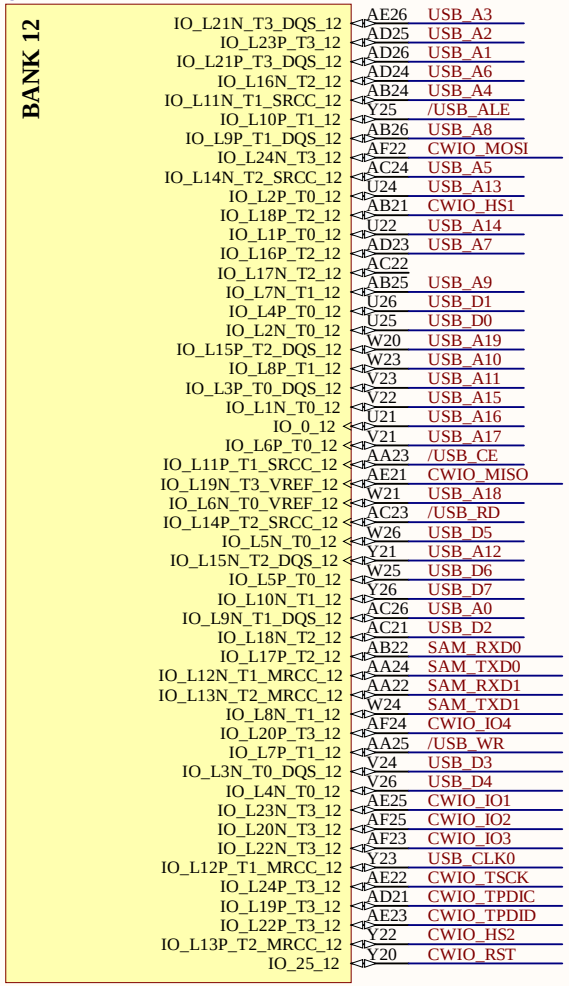
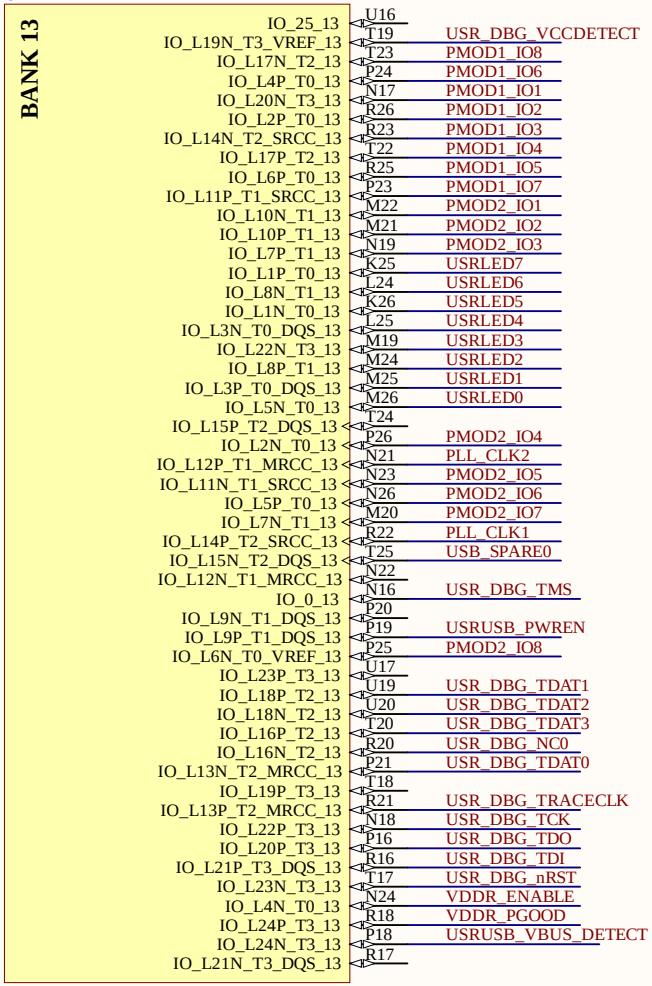
FPGA Bank: 3.3V
U1A



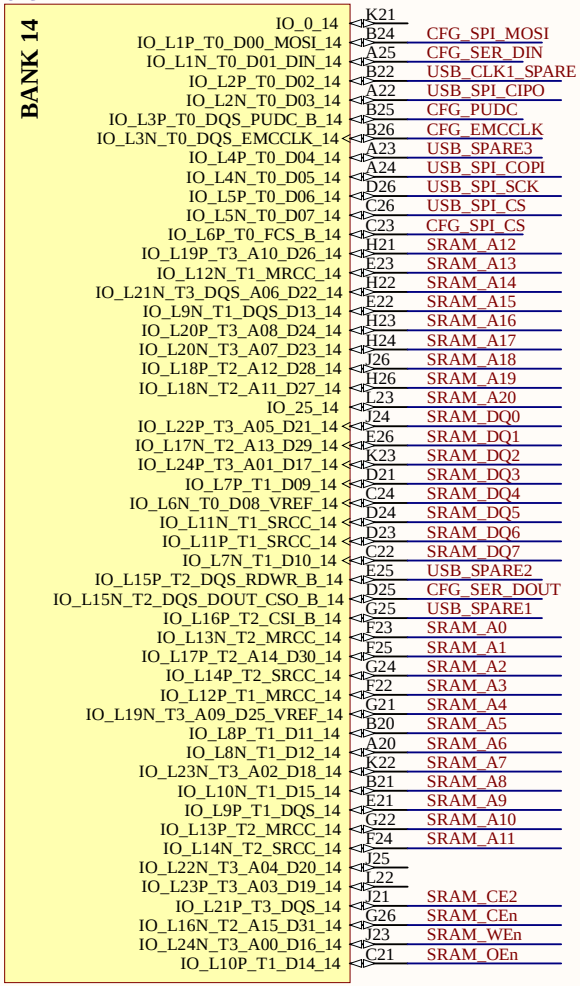
XC7K160T-1FBG676C

FPGA Bank: 3.3V
U1B



XC7K160T-1FBG676C

FPGA Bank: 3.3V, Configuration, SRAM
U1C



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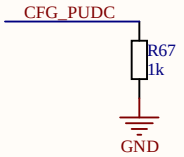

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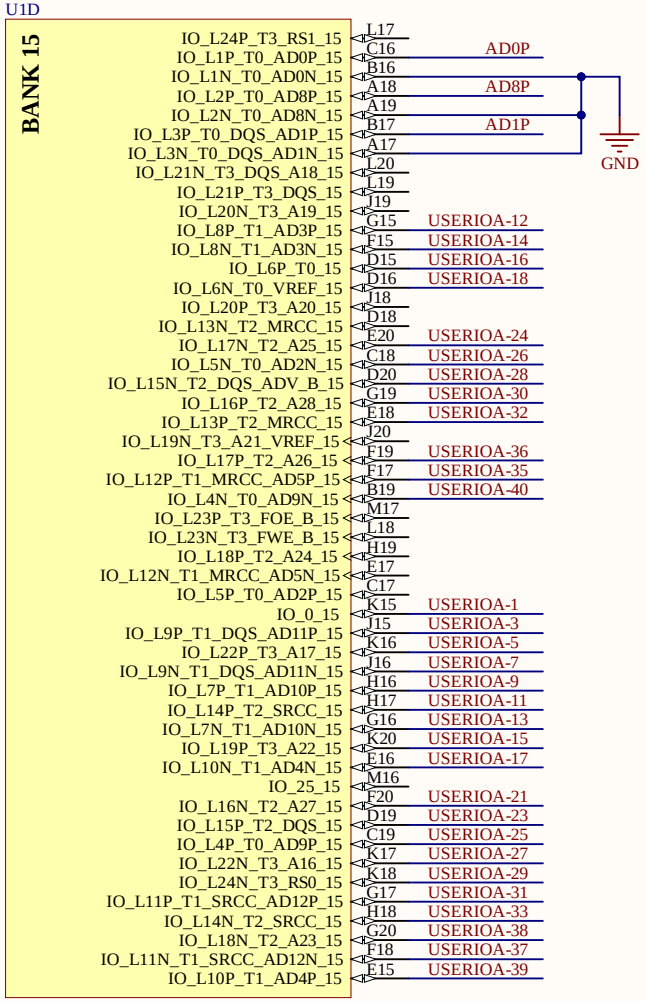
FPGA Bank: VCCIOA
U1D



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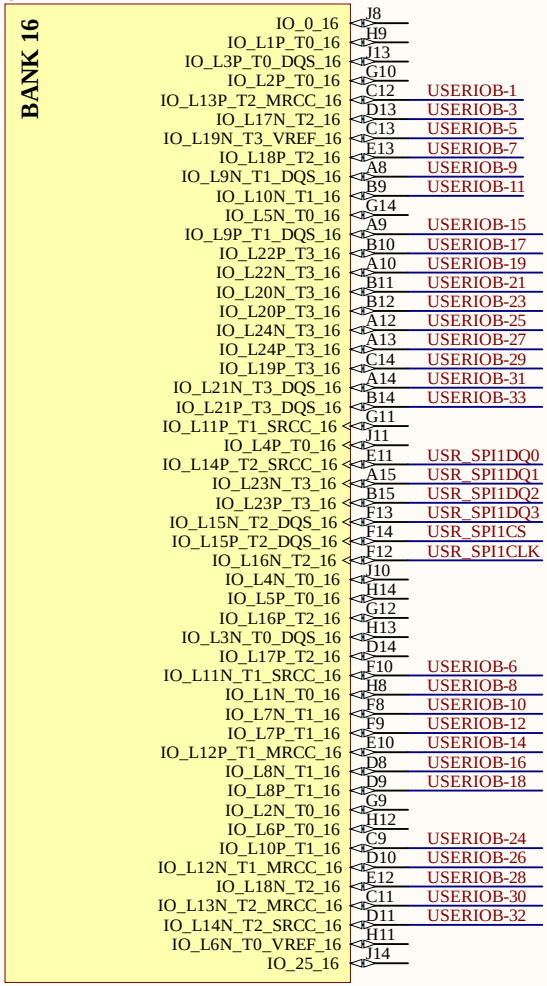
FPGA Bank: VCCIOB
U1E



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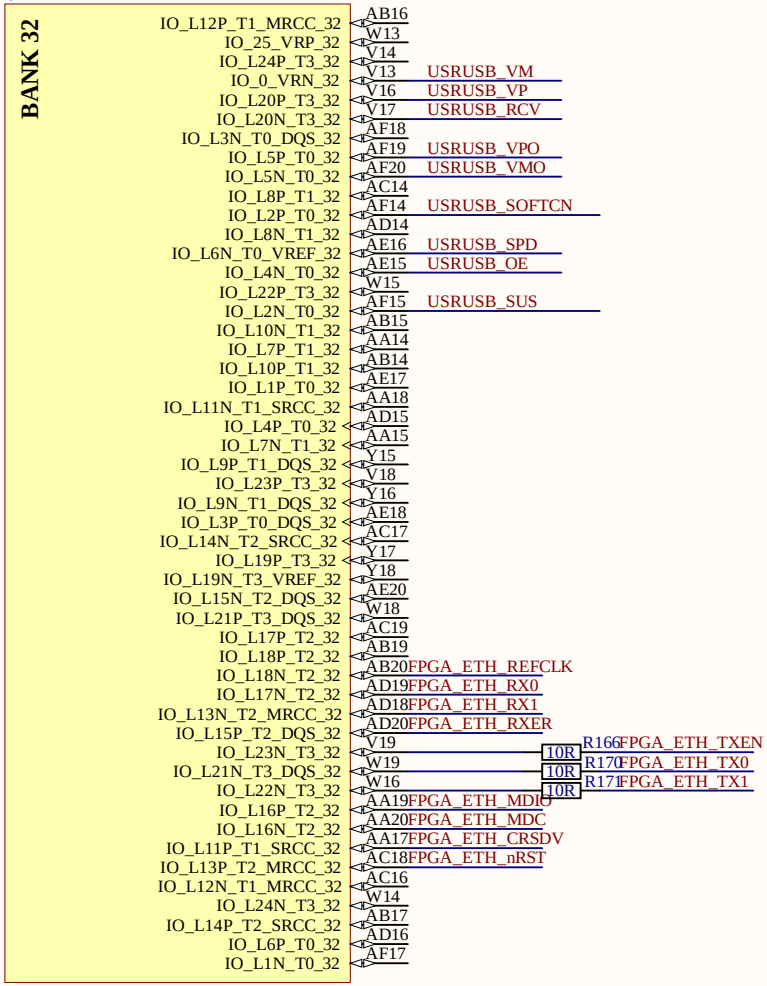
FPGA Bank: 1.8V (HP Bank)
U1F



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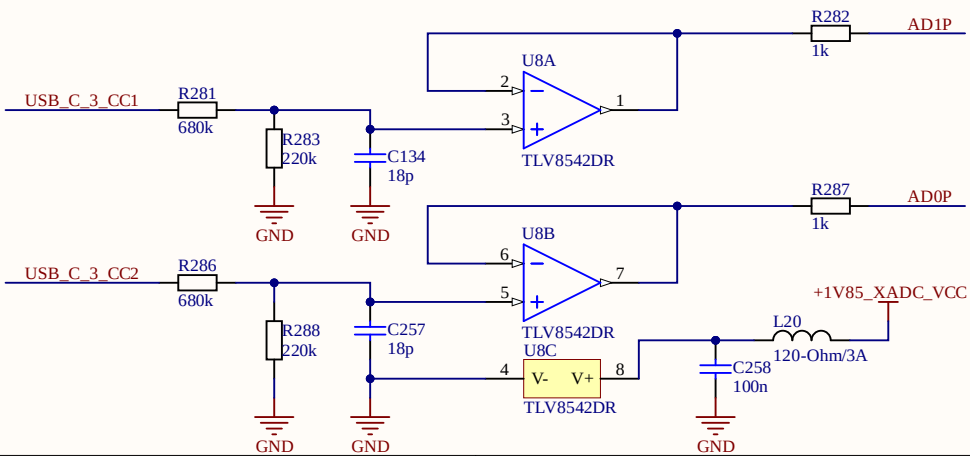

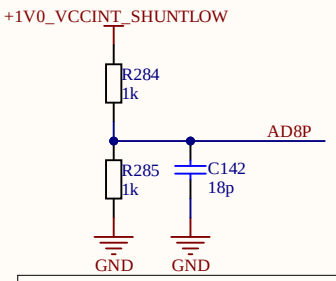

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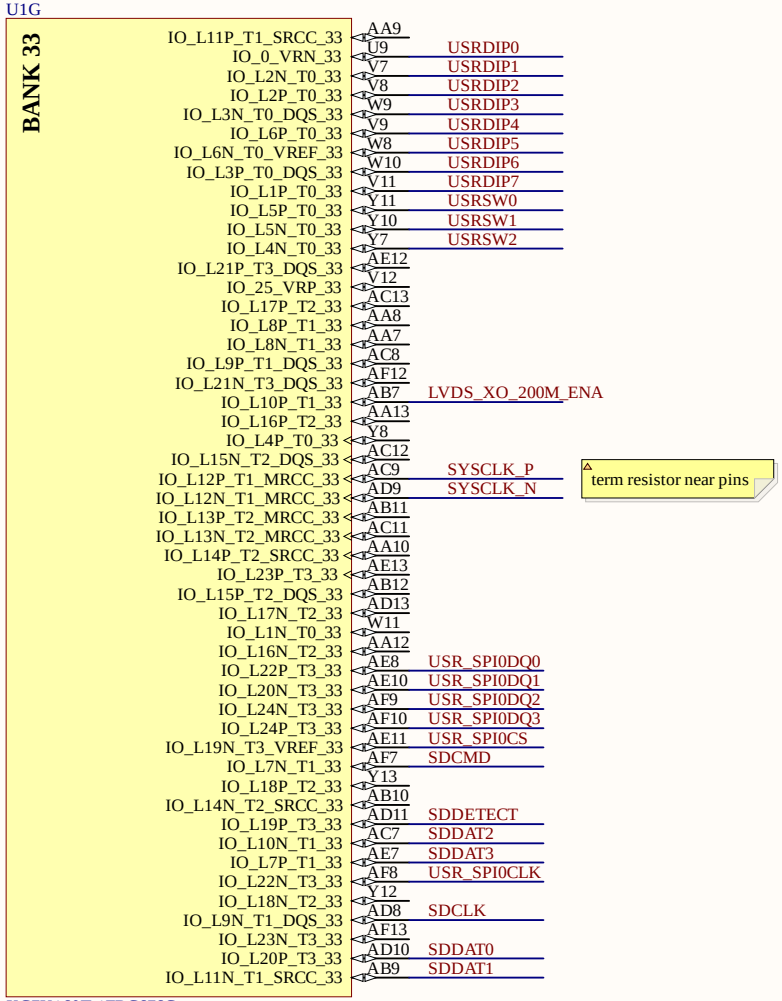
FPGA Bank: 1.8V (HP Bank)

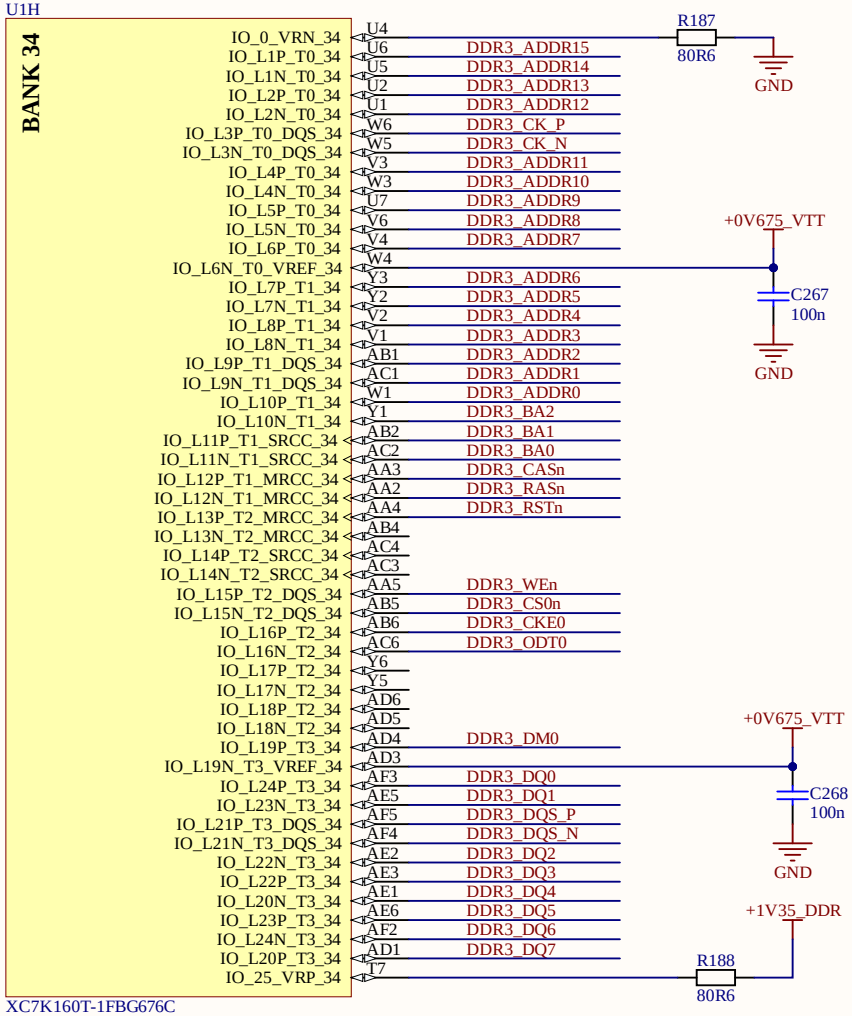
U1G



XC7K160T-1FBG676C

FPGA Bank: DDR3, 1.35V (HP Bank)

U1H



XC7K160T-1FBG676C

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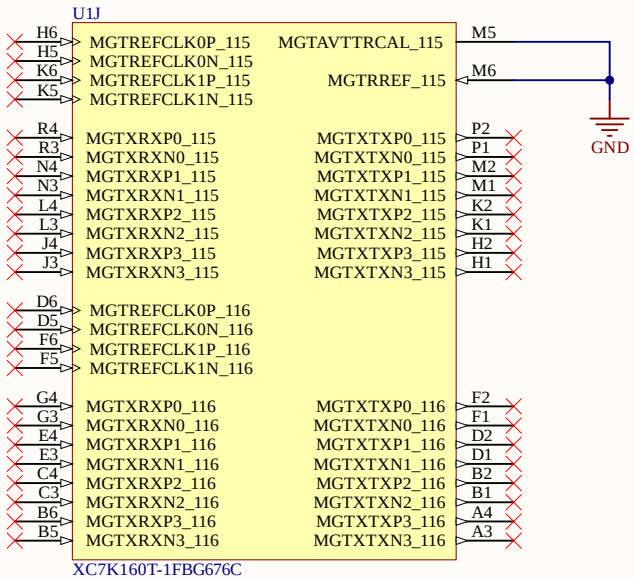
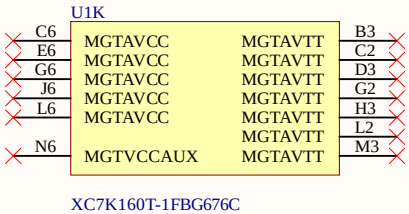
FPGA MGT Interface





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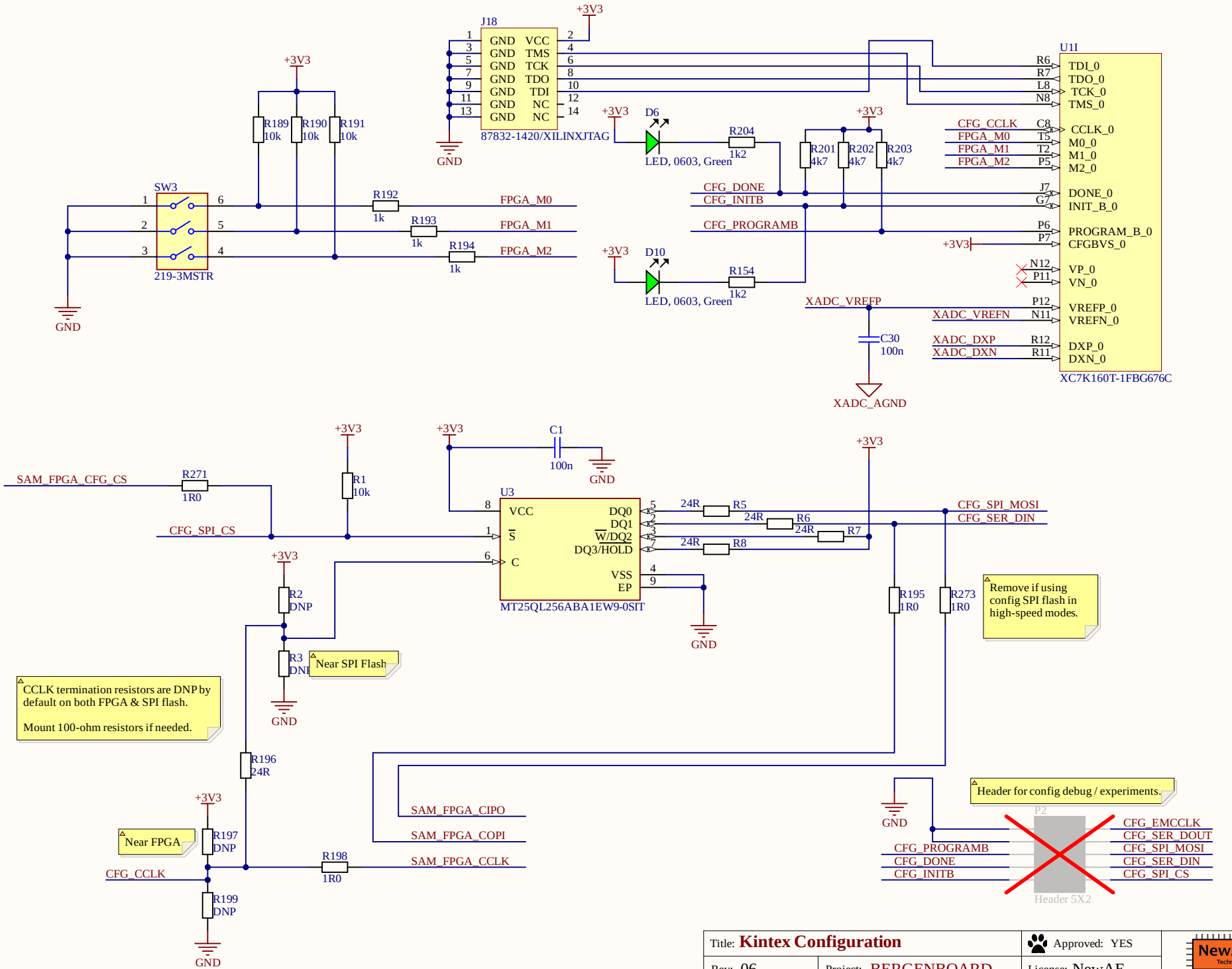

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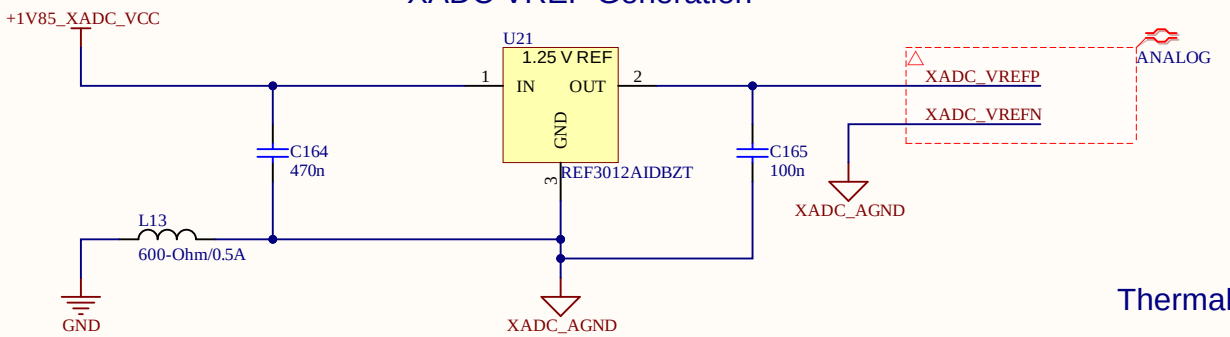
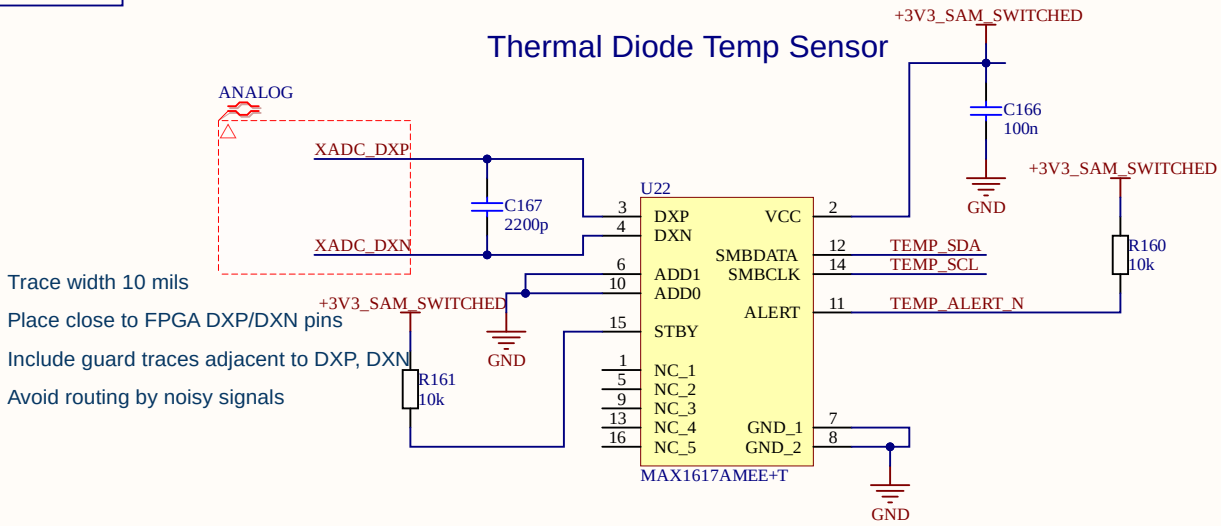
FPGA XADC POWER

XADC VREF Generation



Thermal Diode Temp Sensor



Trace width 10 mils

Place close to FPGA DXP/DXN pins

Include guard traces adjacent to DXP, DXN

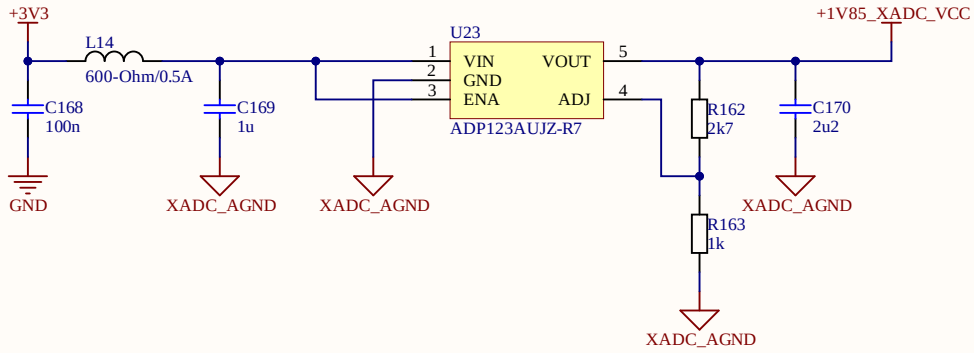
Avoid routing by noisy signals

I2C Address = 0x18

Temperature diode ideality factor = 1.010

Temperature diode series resistance = 2

XADC VCC Generation



Title: **FPGA - Thermal + XADC**		Approved: Yes	NewAE Technology
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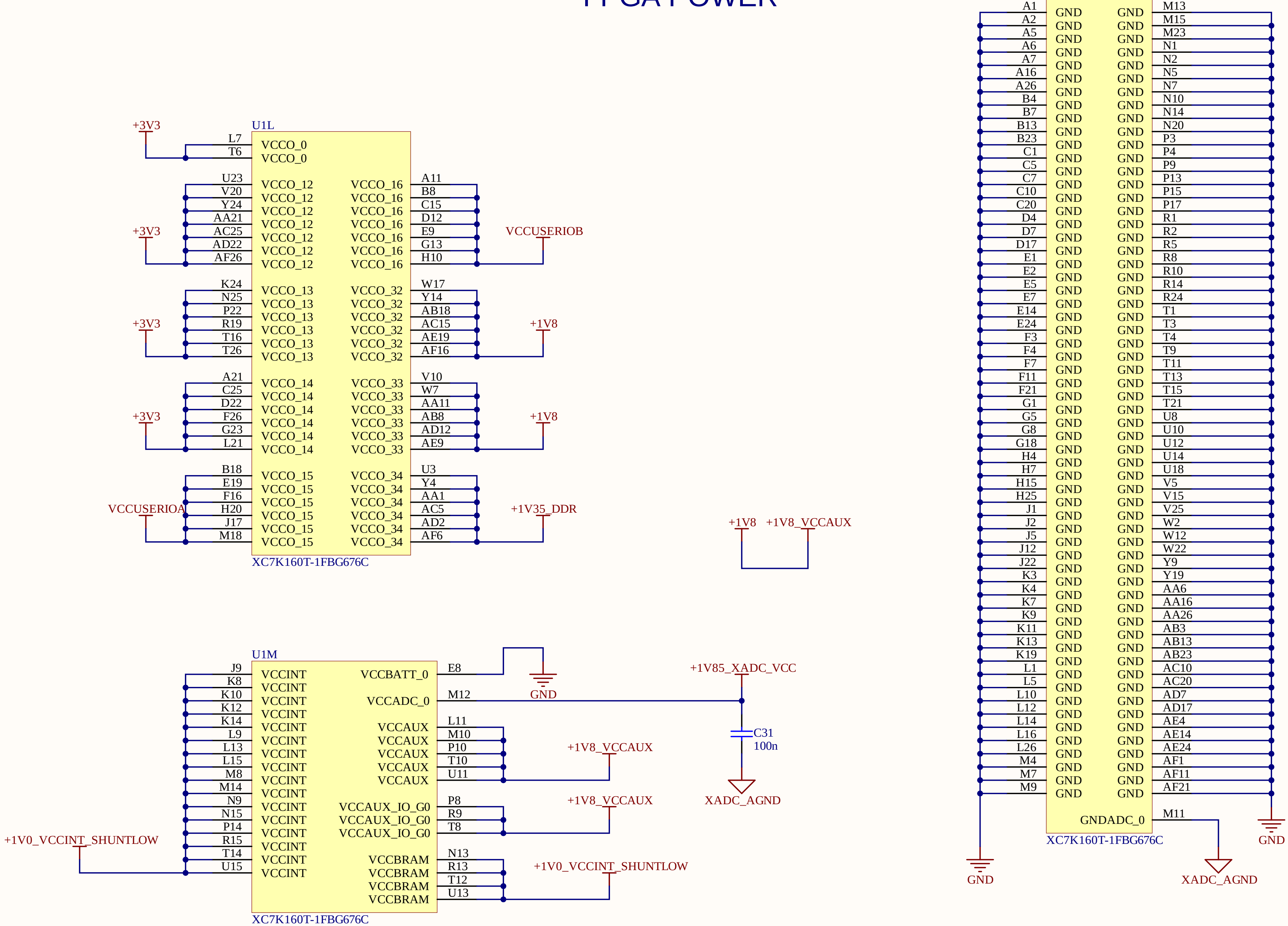
FPGA POWER



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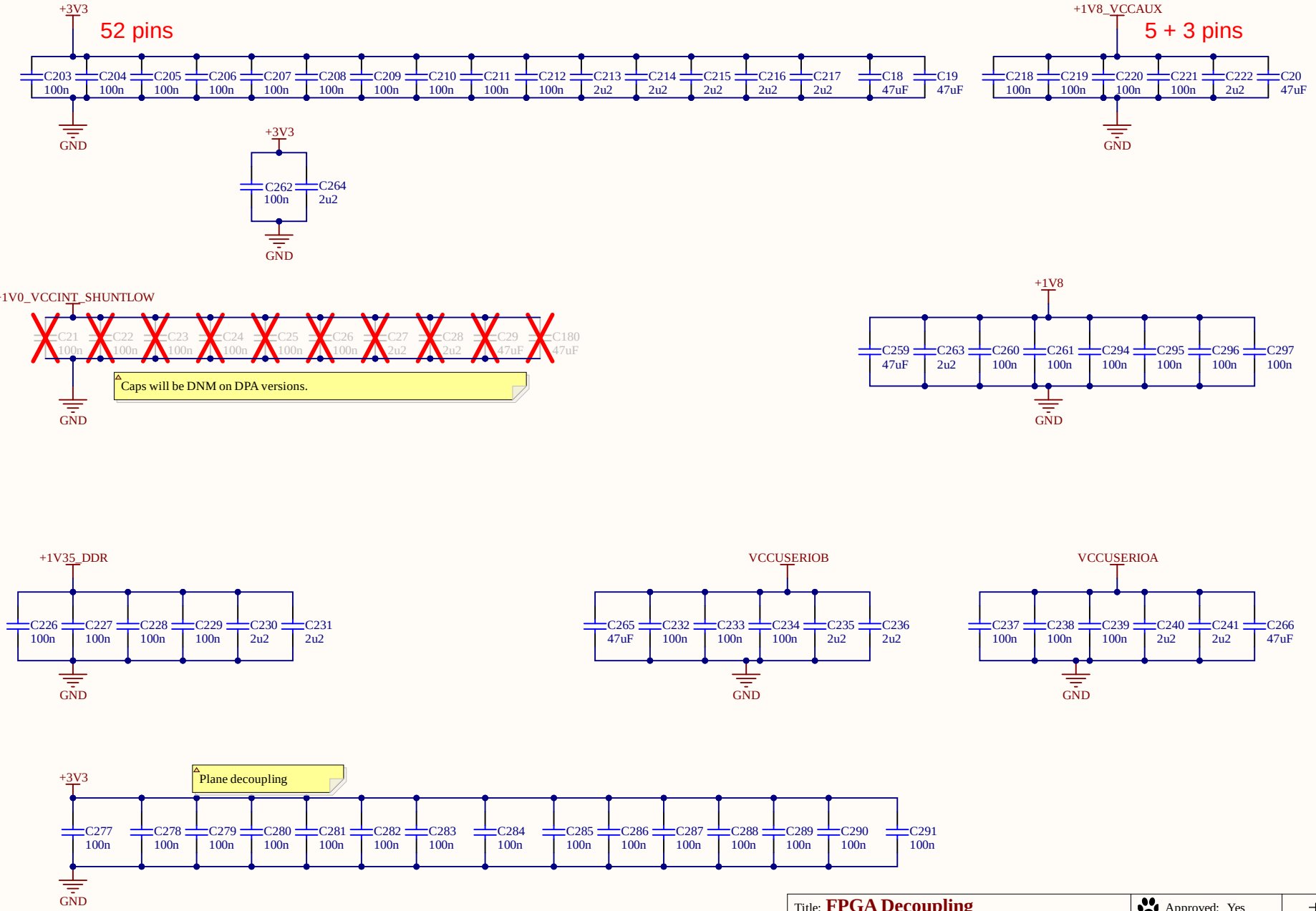
FPGA Decoupling



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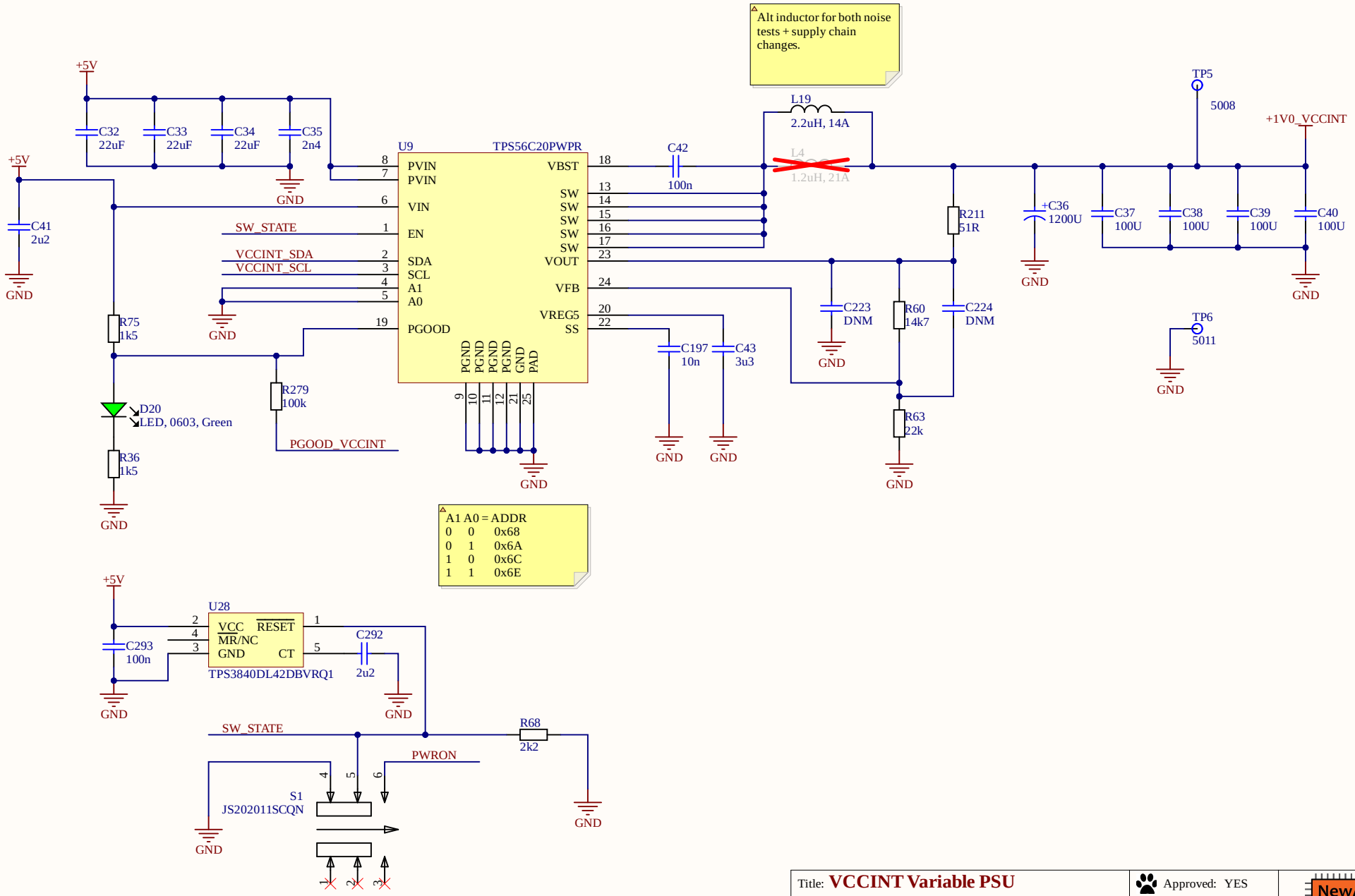
FPGA VCCINT Power Generation / Control



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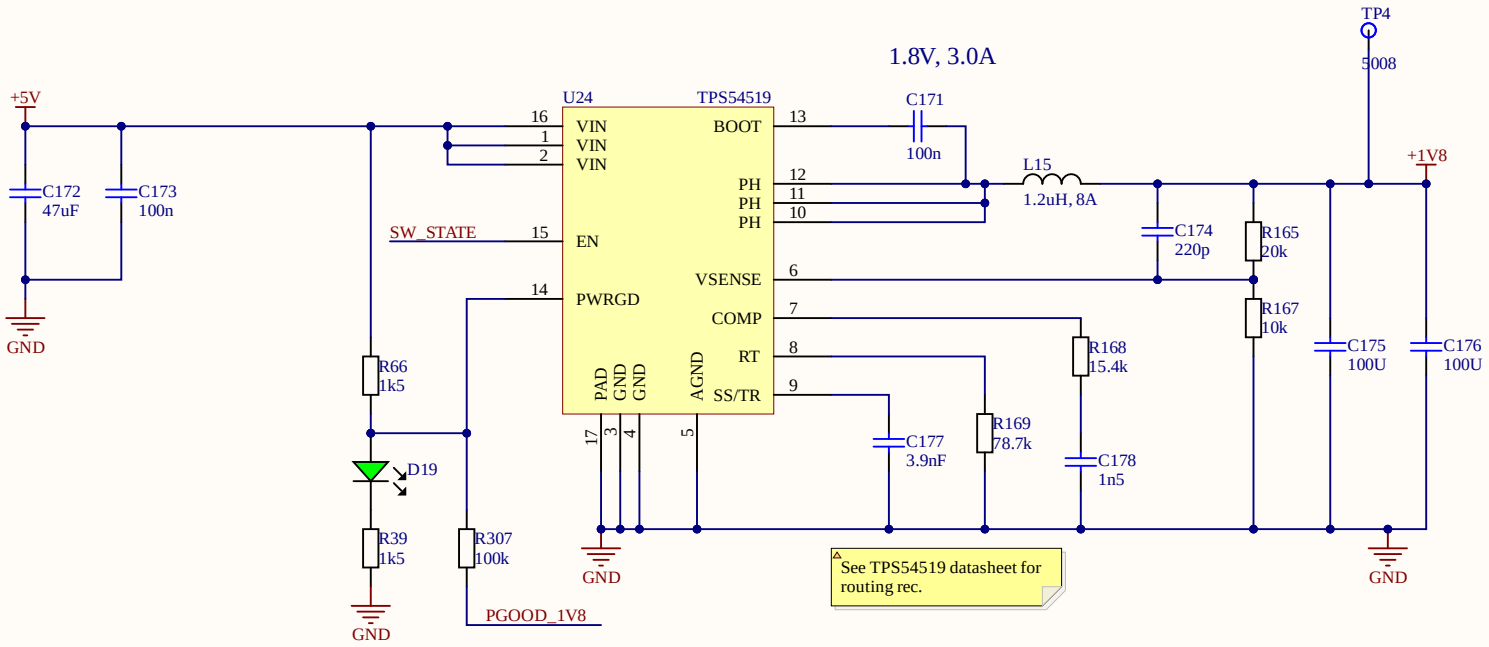

Title: **VCC-AUX SMPS**		Approved: YES	NewAE Technology
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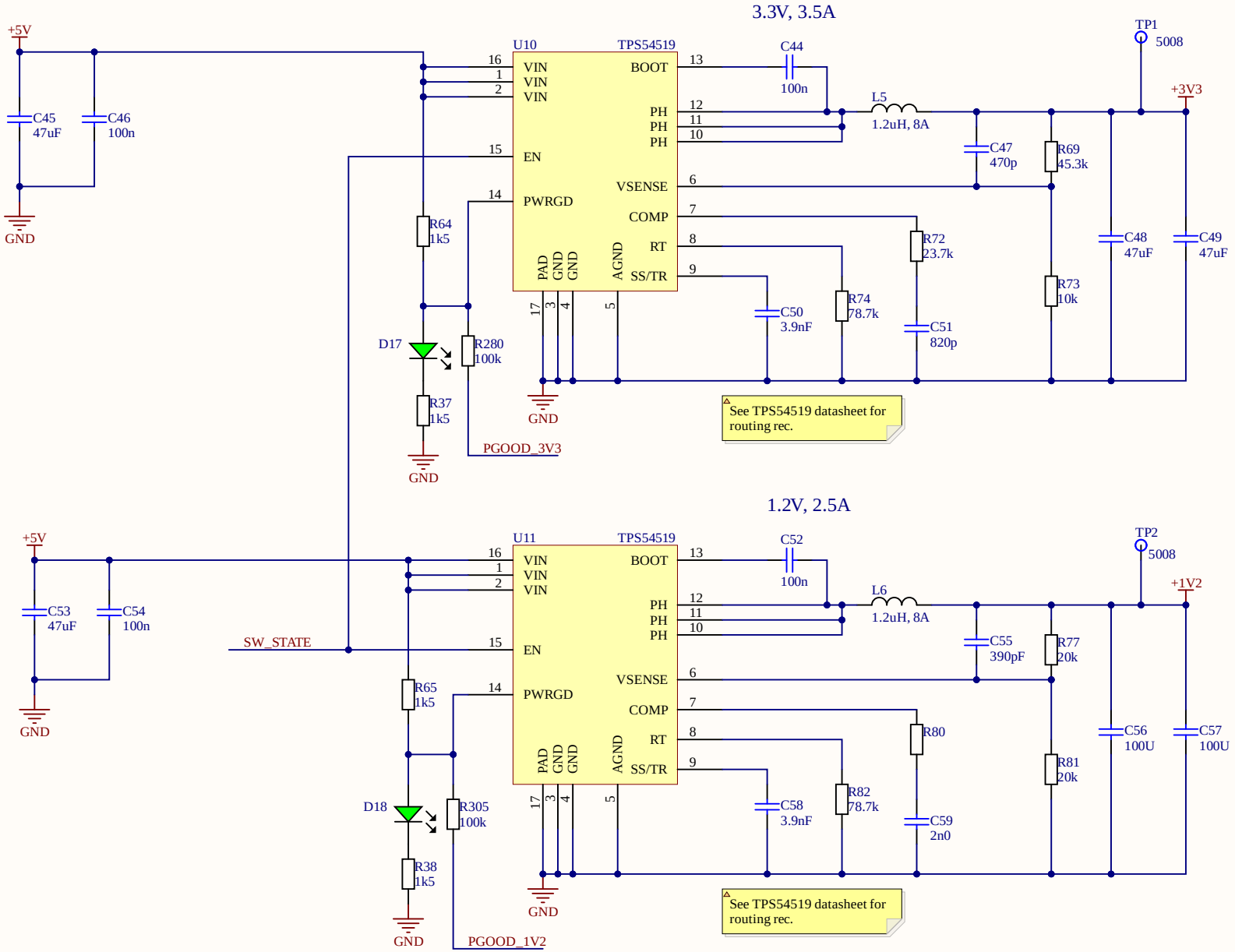

Title: **VCCIO Fixed Supplies**		Approved: Yes	NewAE Technology
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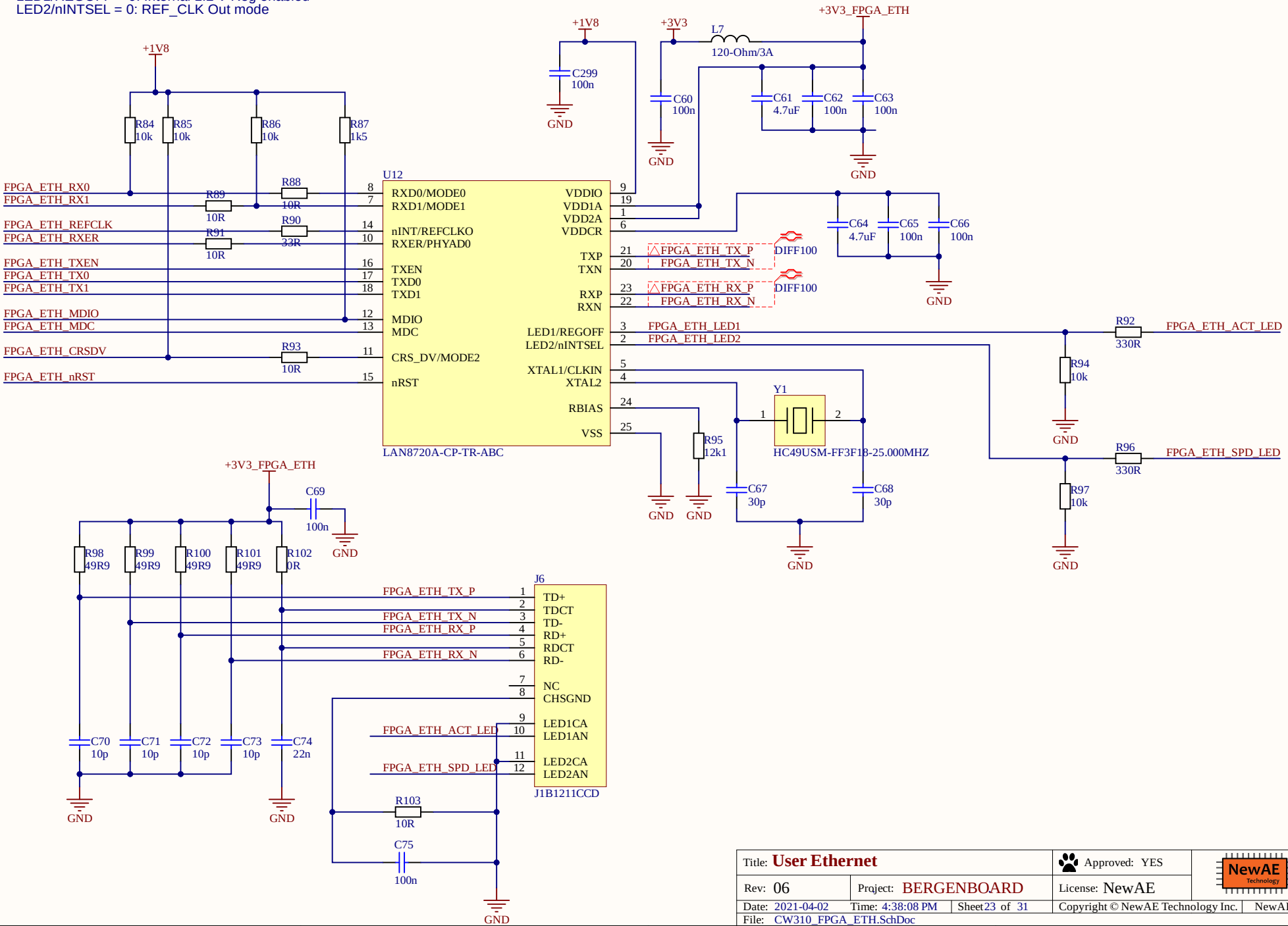
FPGA Ethernet

LAN8720 PHY Configuration

PHYAD0 = 0: Phy Address 0
CRS_DV/MODE2 = 1: All modes, autonegotiation enabled
RXD1/MODE1 = 1
RXD0/MODE0 = 1
LED1/REGOFF = 0: Internal 1.2 V Reg enabled
LED2/nINTSEL = 0: REF_CLK Out mode



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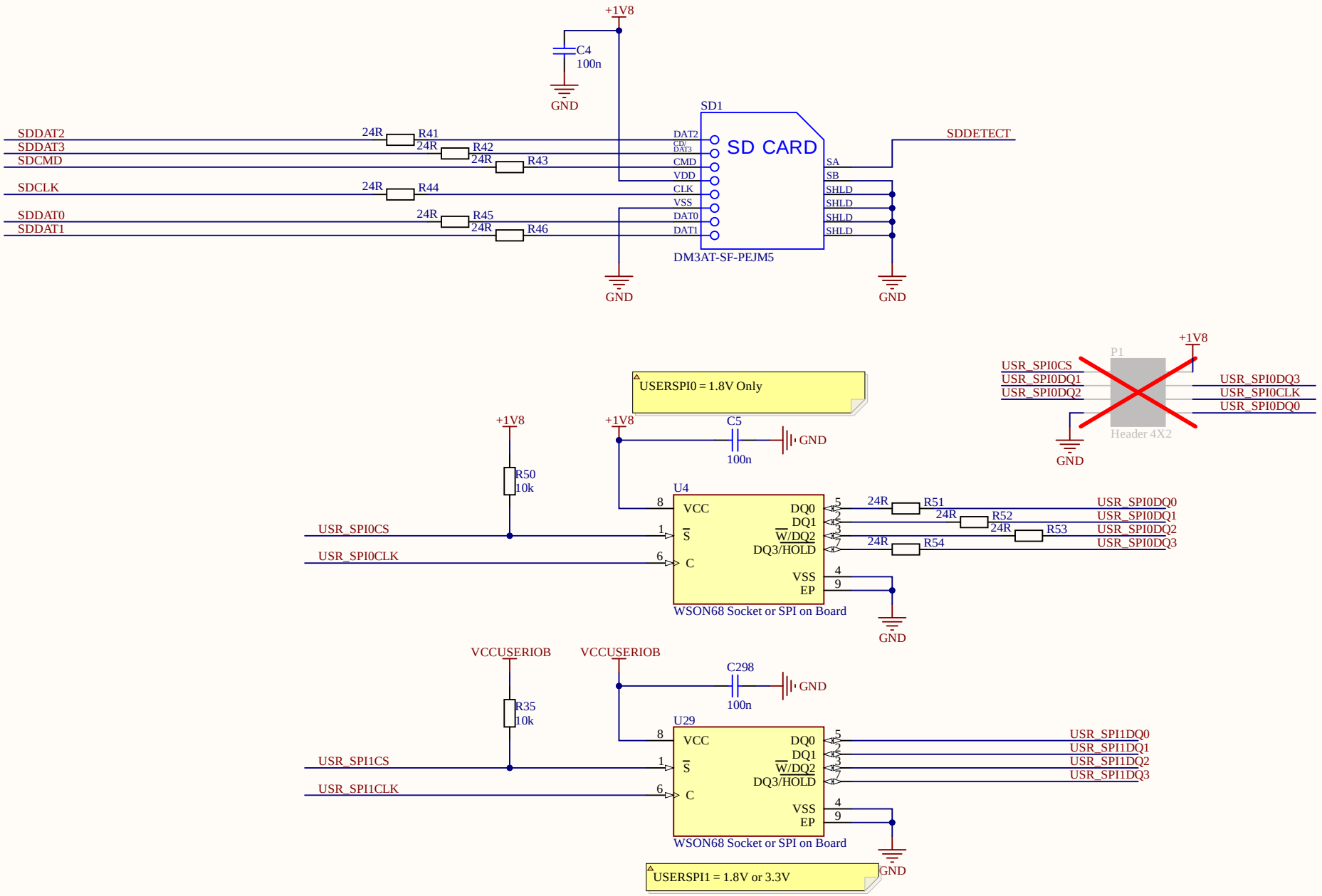

Title: **User SPI Flash + SD Card**		Approved: Yes	NewAE Technology
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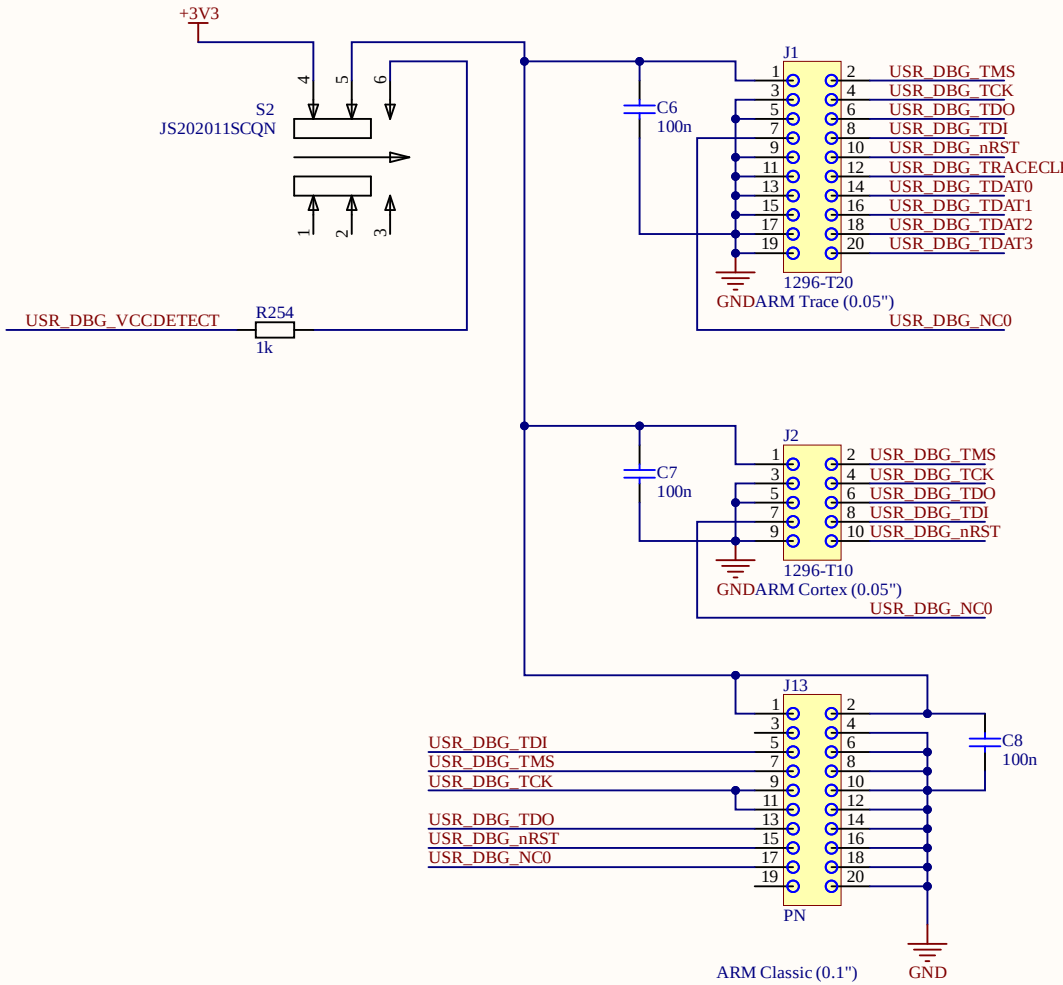

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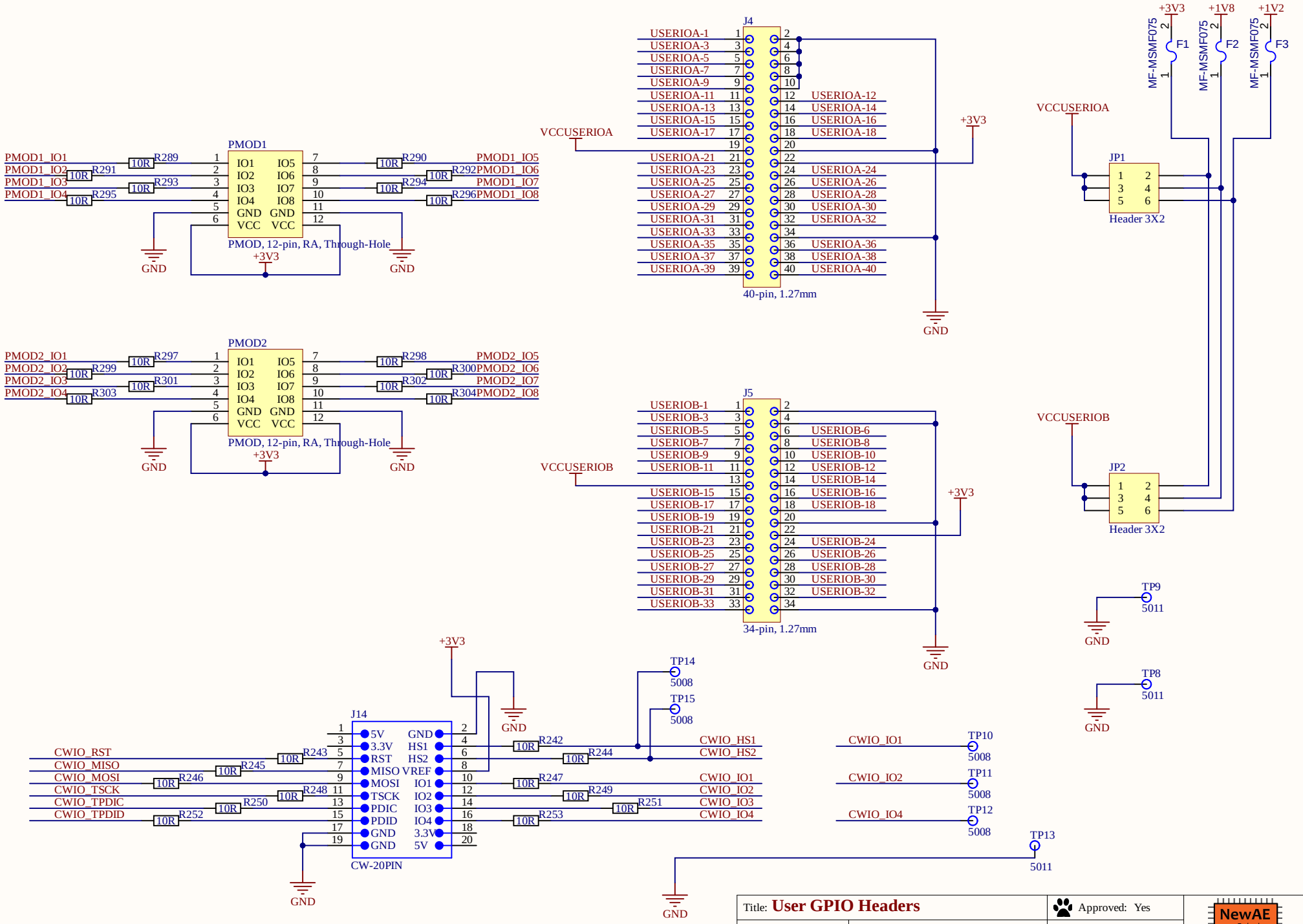
PMOD1
PMOD1_IO1
PMOD1_IO2
PMOD1_IO3
PMOD1_IO4
R289
R291
R293
R295
10R
IO1
IO2
IO3
IO4
GND
VCC
IO5
IO6
IO7
IO8
R290
R292
R294
R296
PMOD1_IO5
PMOD1_IO6
PMOD1_IO7
PMOD1_IO8
PMOD, 12-pin, RA, Through-Hole
+3V3
GND
PMOD2
PMOD2_IO1
PMOD2_IO2
PMOD2_IO3
PMOD2_IO4
R297
R299
R301
R303
R298
R300
R302
R304
PMOD2_IO5
PMOD2_IO6
PMOD2_IO7
PMOD2_IO8
J4
USERIOA-1
USERIOA-3
USERIOA-5
USERIOA-7
USERIOA-9
USERIOA-11
USERIOA-13
USERIOA-15
USERIOA-17
USERIOA-21
USERIOA-23
USERIOA-25
USERIOA-27
USERIOA-29
USERIOA-31
USERIOA-33
USERIOA-35
USERIOA-37
USERIOA-39
USERIOA-12
USERIOA-14
USERIOA-16
USERIOA-18
USERIOA-24
USERIOA-26
USERIOA-28
USERIOA-30
USERIOA-32
USERIOA-36
USERIOA-38
USERIOA-40
40-pin, 1.27mm
VCCUSERIOA
J5
USERIOB-1
USERIOB-3
USERIOB-5
USERIOB-7
USERIOB-9
USERIOB-11
USERIOB-15
USERIOB-17
USERIOB-19
USERIOB-21
USERIOB-23
USERIOB-25
USERIOB-27
USERIOB-29
USERIOB-31
USERIOB-33
USERIOB-6
USERIOB-8
USERIOB-10
USERIOB-12
USERIOB-14
USERIOB-16
USERIOB-18
USERIOB-24
USERIOB-26
USERIOB-28
USERIOB-30
USERIOB-32
34-pin, 1.27mm
VCCUSERIOB
+1V8
+1V2
MF-MSMF075
F1
F2
F3
JP1
JP2
Header 3X2
TP9
TP8
5011
J14
5V
3.3V
RST
MISO
MOSI
TSCK
PDIC
PDID
GND
VREF
HS1
HS2
IO1
IO2
IO3
IO4
CW-20PIN
CWIO_RST
CWIO_MISO
CWIO_MOSI
CWIO_TSCK
CWIO_TPDIC
CWIO_TPDID
R242
R243
R244
R245
R246
R247
R248
R249
R250
R251
R252
R253
CWIO_HS1
CWIO_HS2
CWIO_IO1
CWIO_IO2
CWIO_IO3
CWIO_IO4
TP14
TP15
TP10
TP11
TP12
TP13
5008
Title: User GPIO Headers
Approved: Yes
Rev: 06
Project: BERGENBOARD
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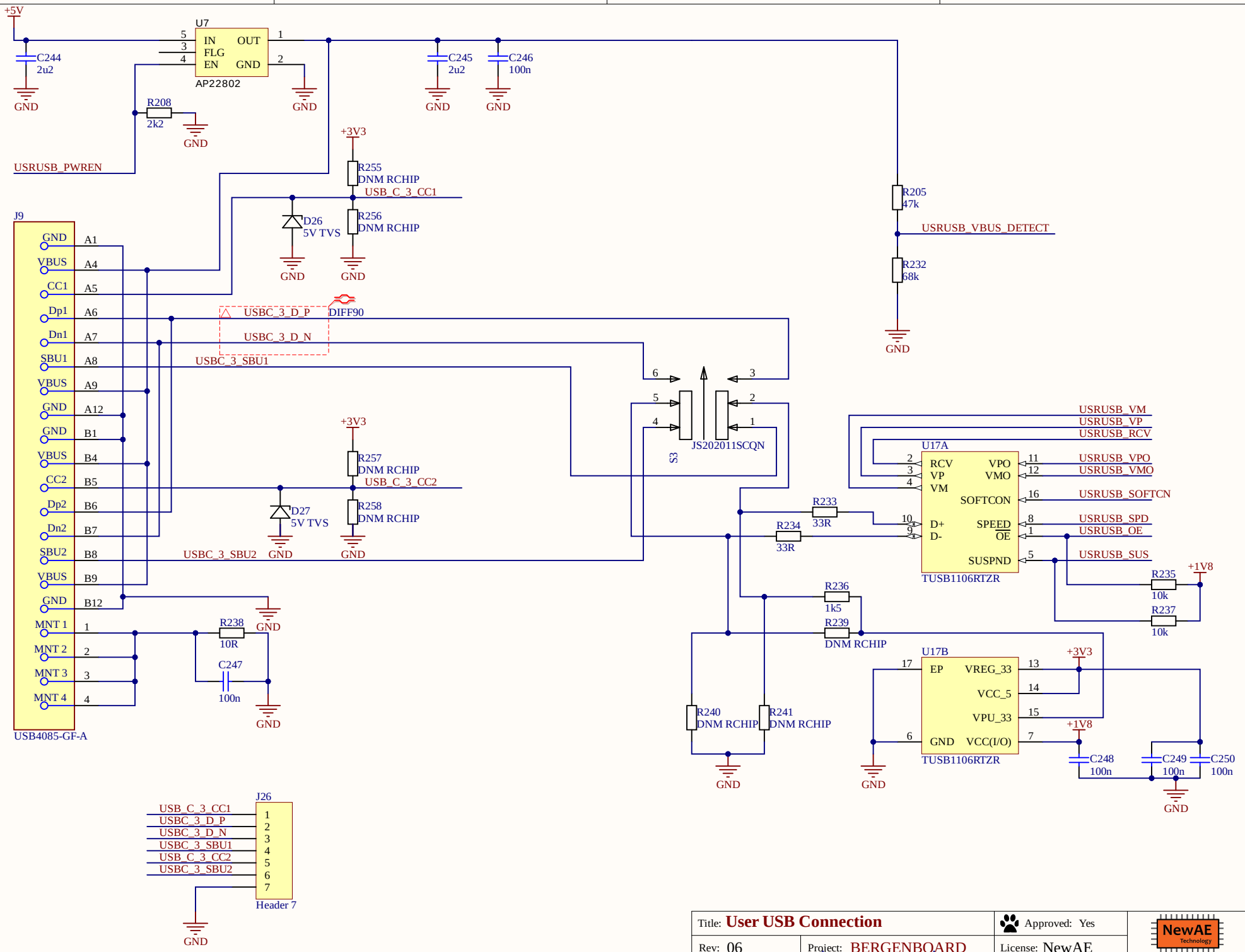

Title: **User USB Connection**		Approved: Yes	NewAE Technology
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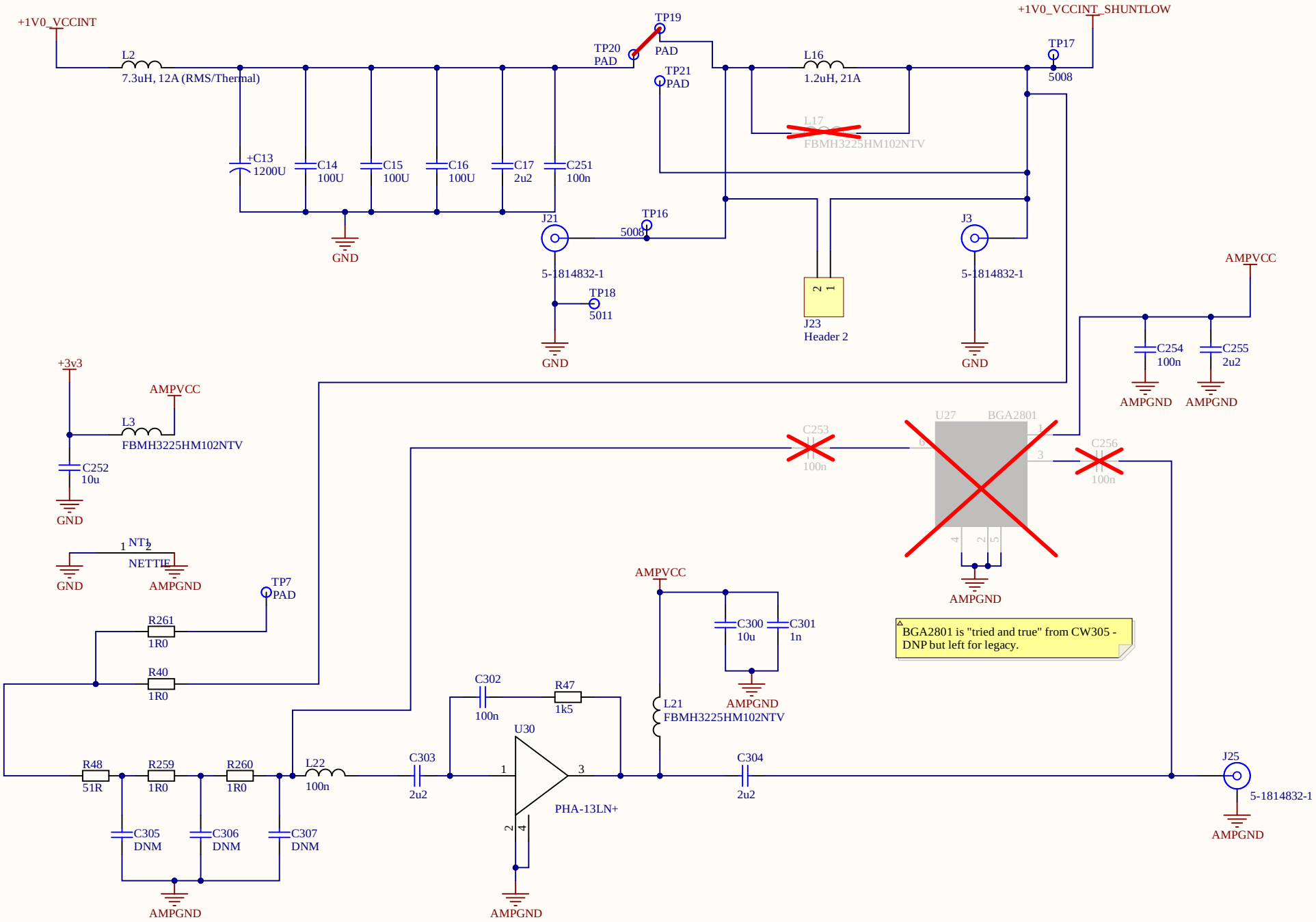

Title: **Power Measurements**		Approved: Yes	NewAE Technology
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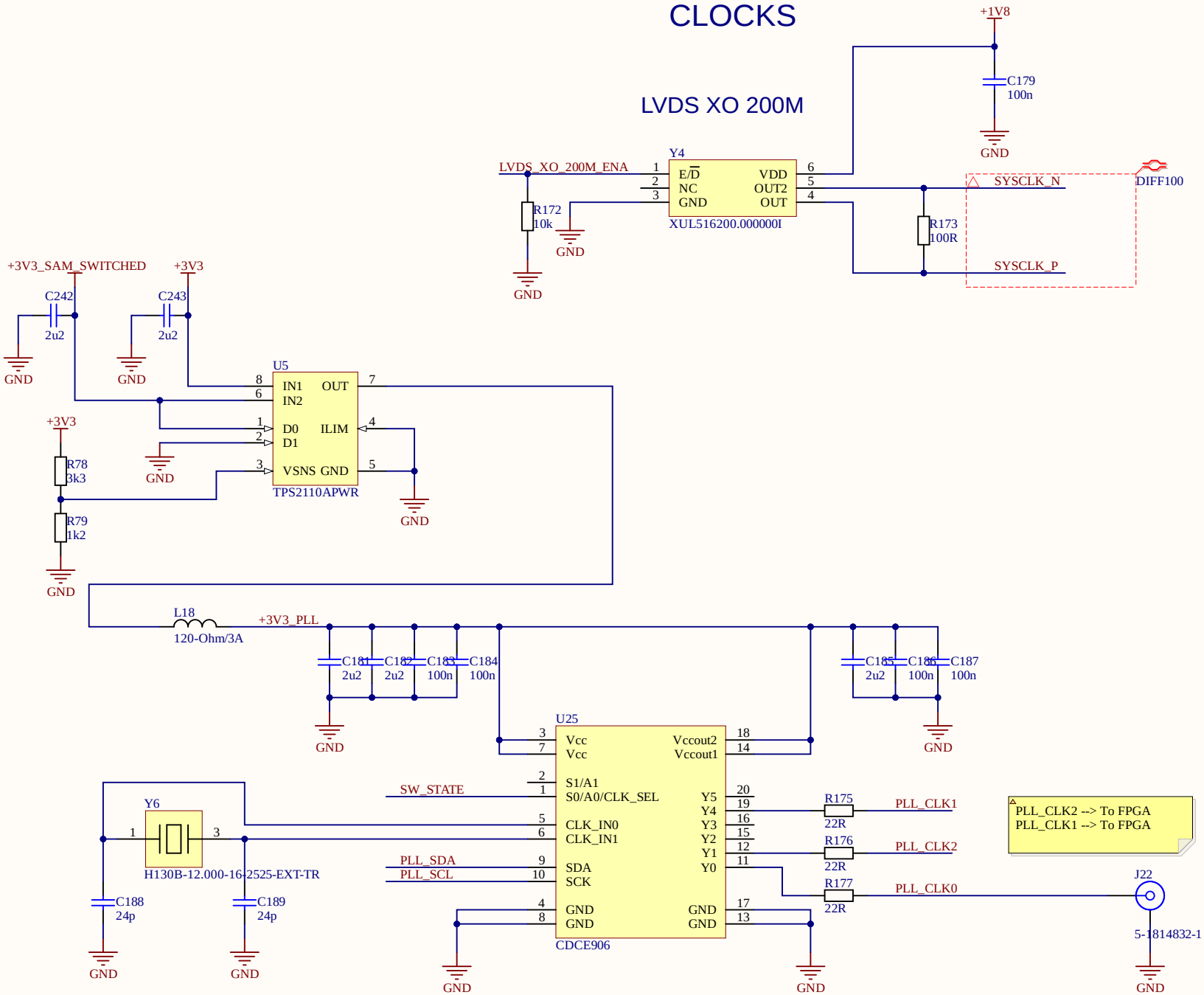
File: CW310_POWERMEASURE.SchDoc			

CLOCKS

LVDS XO 200M



Title: **PLL, Clocks for FPGA**		Approved: Yes	NewAE Technology
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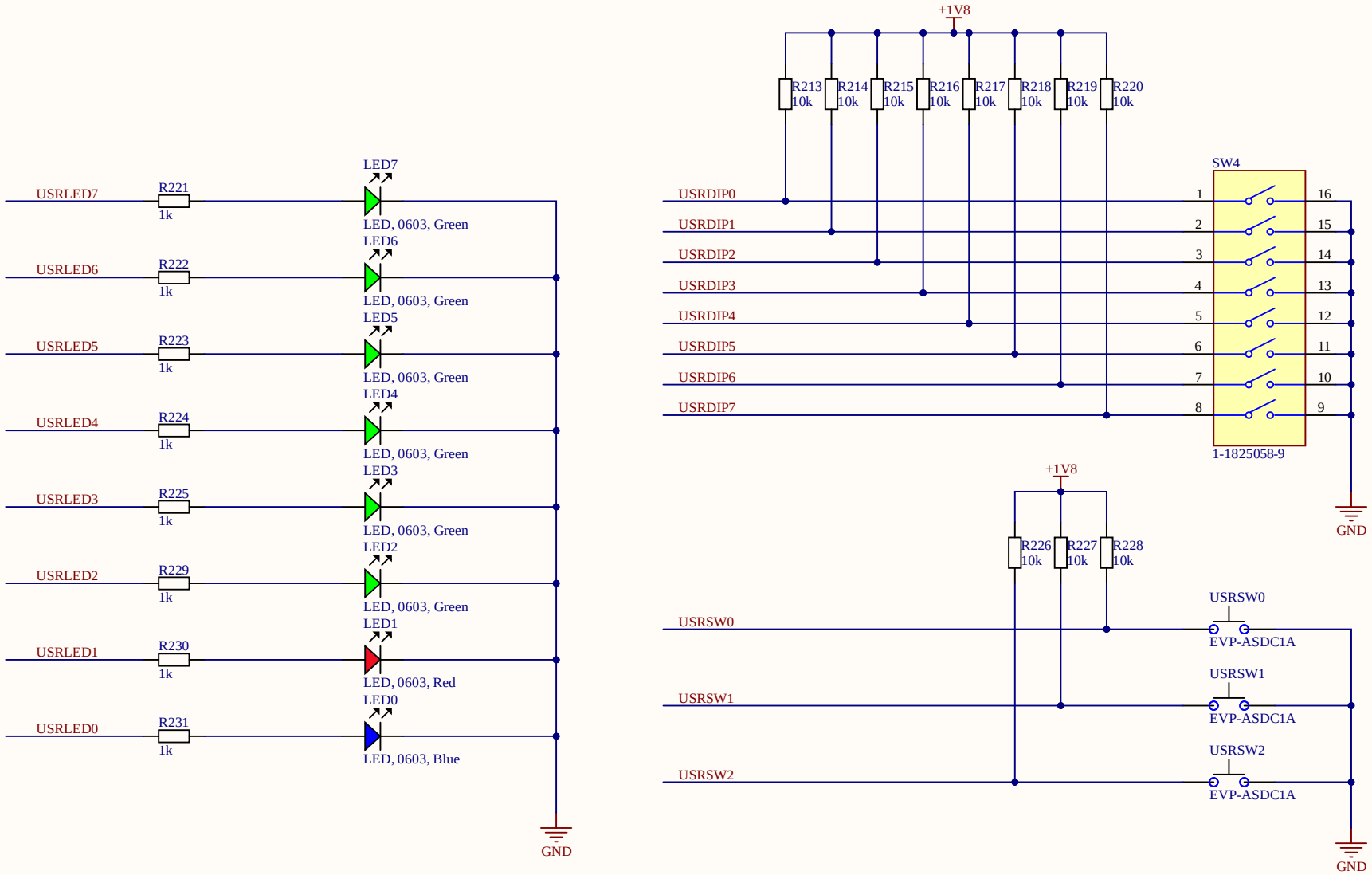

Title: **User LED / Switches**		Approved: Yes	NewAE Technology
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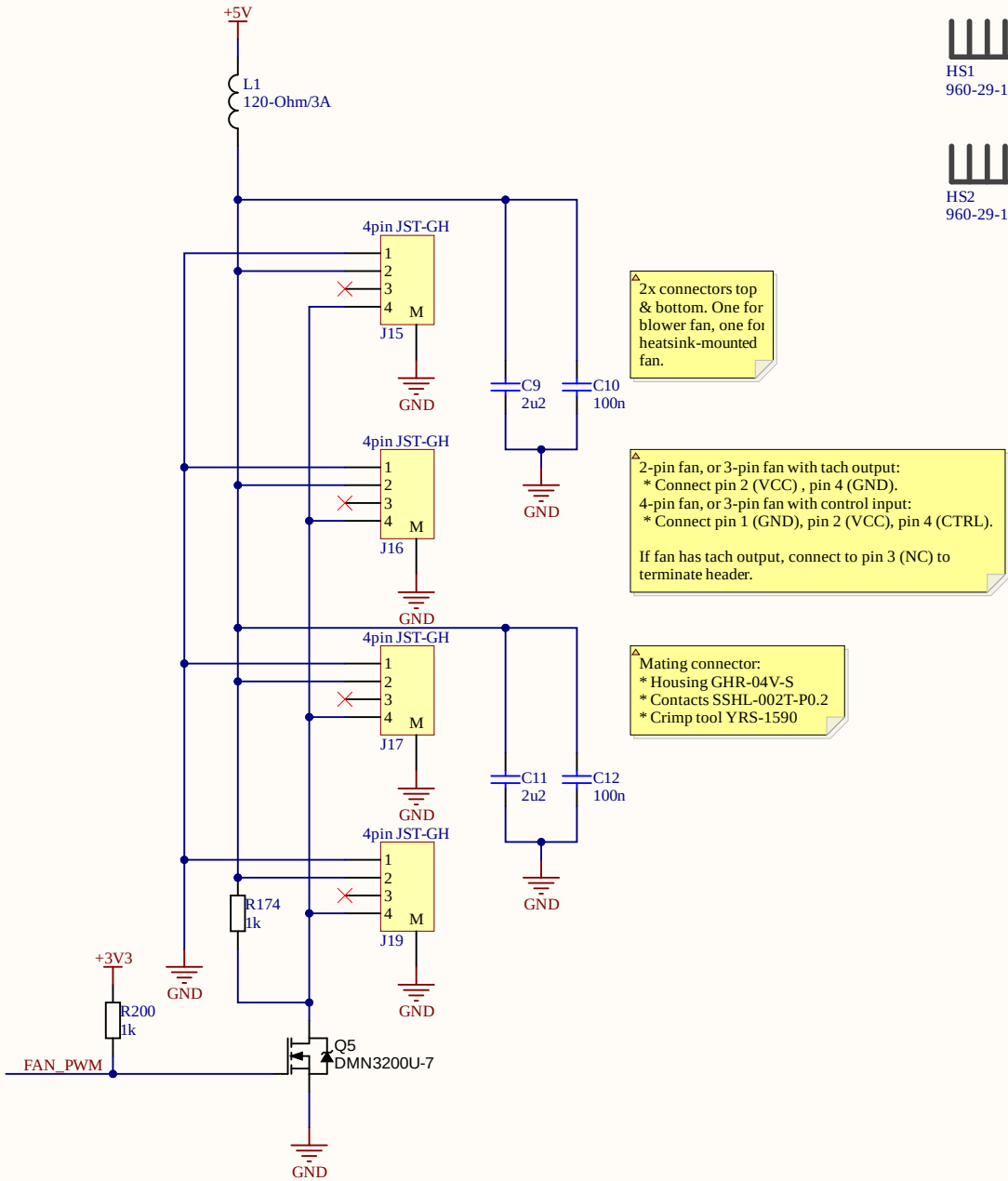
File: CW310_STATUS_LEDs.SchDoc			



2x connectors top & bottom. One for blower fan, one for heatsink-mounted fan.

2-pin fan, or 3-pin fan with tach output:
* Connect pin 2 (VCC) , pin 4 (GND).
4-pin fan, or 3-pin fan with control input:
* Connect pin 1 (GND), pin 2 (VCC), pin 4 (CTRL).

If fan has tach output, connect to pin 3 (NC) to terminate header.

Mating connector:
* Housing GHR-04V-S
* Contacts SSHL-002T-P0.2
* Crimp tool YRS-1590

HS1
960-29-18-D-AB-0

HS2
960-29-18-D-AB-0

FAN1
Blower Fan, 5V, 35x35mm

Fan mounted top or bottom side of board. Blower style to pass over "open die top".

Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.

FID1 FID2 FID3 FID4 FID5 FID6 FID7 FID8 FID9 FID10
FIDU-ROUND-1.0MM

MH1 MH2 MH3 MH4 MH5 MH6
4-40 MH, Tight Fit

Title: **FAN Headers**		Approved: Yes	NewAE Technology
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