User Manual

Reference Manual for Allegro APEK85110 Demonstration Board Using AHV85110

Description

The Allegro APEK85110 Half-Bridge Driver Switch Board (Part number APEK85110KNH-01-T-MH) is a demonstration board containing two AHV85110 GaN FET drivers and two GaN FETs in a half-bridge configuration.

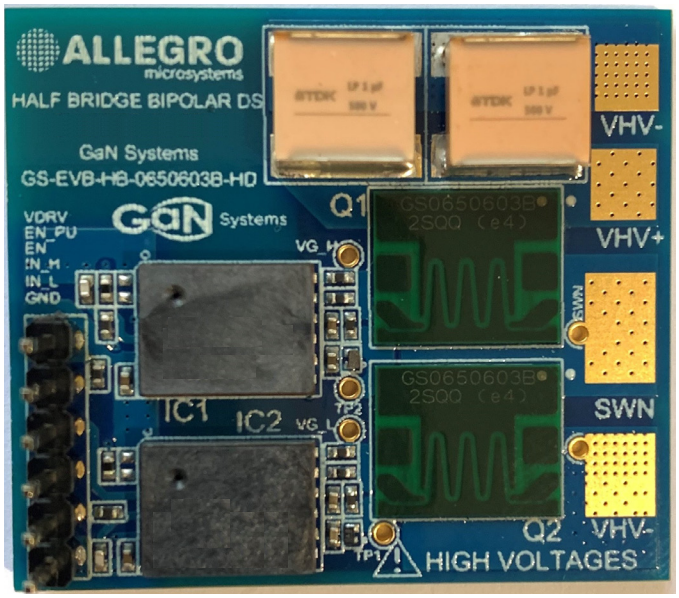

Figure 1: APEK85110 Demonstration Board

The APEK85110 can be used to perform double pulse tests (see Double Pulse Test section) or to interface the half bridge to an existing LC power section, as shown below.

The isolated AHV85110 driver does not require secondary-side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary-side supply voltage, V_{DRV}. The amplitude of the gate drive can be varied by varying V_{DRV} between 10.5 V and 13.2 V.

DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Ensure that appropriate safety procedures are followed. This demonstration board is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. There is NO built-in electrical or thermal protection on this demonstration board. The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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Quick Start Guide

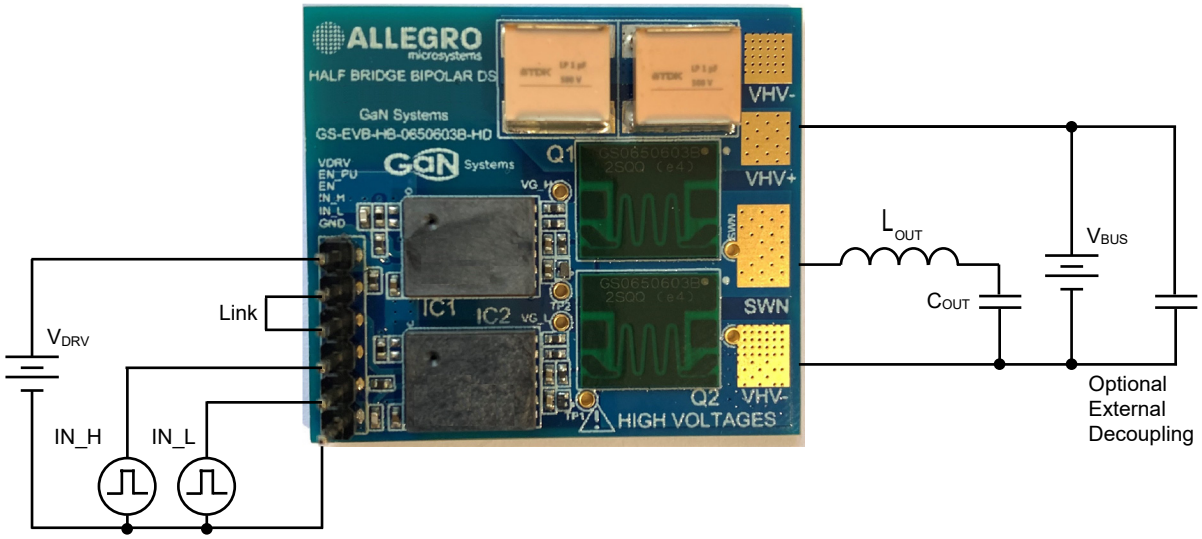

Figure 2: APEK85110 Quick Start

1. Apply V_{DRV} = 12 V
2. Link pins EN_PU and EN (if not using external Enable control)
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points are located on the test board as shown above. A suitable differential oscilloscope should be used to monitor the high-side gate signal from V_{GH} to V_{SW}.

Gate Pull-Up and Pull-Down Resistors

The AHV85110 gate driver has independent outputs for the gate pull-up and gate pull-down allowing control of the on and off rise and fall times.

The default values for these resistors are:

- OUTPU: R1 and R5 = 10 Ω
- OUTPD: R3 and R7 = 1 Ω

These values can be modified to suit the application.

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Enable and Start Sequence

The AHV85110 has an open-drain enable pin (EN) to facilitate a system level wired-AND startup.

When the enable pin is externally pulled low, the driver is forced into a low-power mode. The driver output is pulled low in this mode. In the event of an internal fault condition, such as UVLO, this pin is actively pulled low internally by the driver. During normal operation, the pin is released by the driver, and must be pulled high with an external pull-up resistor. This functionality can be used by the PWM controller to indicate that it can start sending IN pulses to the driver. It is typically wired-AND with the controller enable pin as shown in Figure 3.

The APEK85110 demonstration board provides direct access to the EN pin on connector CONN1. Internally the board contains a 100 kΩ pull-up resistor connected from VDRV to the EN_PU pin on connector CONN1—see schematic in Figure 12. If external control of the enable function is not required, pins EN and EN_PU must be linked together on CONN1 to make use of the internal 100 kΩ pull-up resistor to enable the driver. If the EN pin is left floating, the drivers will not respond to INL or INH input signals.

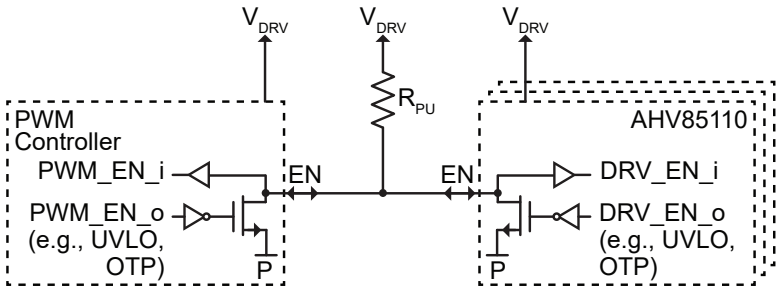

Figure 3: AHV85110 Wired-AND Enable

The start up sequence of the AHV85110 is shown in Figure 4. Time t_{START} is defined as the time after which VDRV reaches the UVLO rising level to the AHV85110 releasing the EN internal pull down.

IMPORTANT: the IN signal must not be applied before the EN pin has been released.

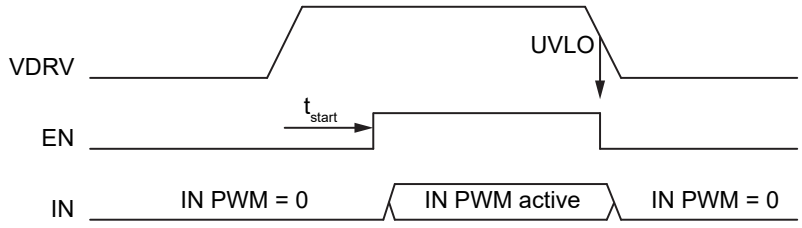

Figure 4: AHV85110 Start-Up Sequence

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Measurement Points

The APEK85110 demonstration board contains convenient test points for monitoring the high- and low-side gate drives as well as the switch node as shown in Figure 5.

When measuring V_{GS_H}, use a differential probe with suitable ratings for the applied bus voltage. The APEK85110 demonstration board uses a bipolar gate drive arrangement as shown in Figure 6. When measuring V_{GS}, both gate drives are measured relative to the source of their associated GaN FET. Therefore, the off-state voltage will be negative.

It is important to use a low-inductance scope probe ground lead as shown to avoid pickup of spurious switching noise.

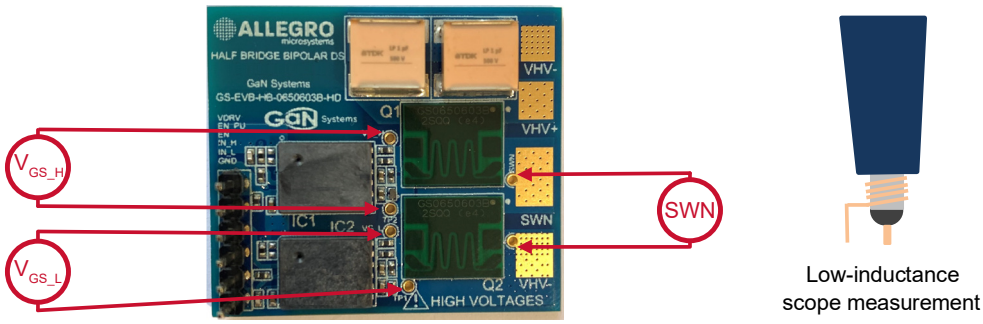

Figure 5: Measurements Points

Bipolar Gate Drive

Due to the high rate of change of voltages and currents in power switching circuits, unwanted inductor currents and capacitor voltage drops can be created.

One such example is the false turn on of a FET due to a dv/dt event. In a half-bridge circuit, after the low-side FET has been turned off and a suitable dead-time has elapsed, the high-side FET is turned on. This produces a rapidly changing switch node voltage at the drain of the low-side FET. This voltage will produce a capacitor current,

$$i_{C_{GD}} = C_{GD} \times (dV_{DS\_L} / dt)$$

flowing in the gate-drain capacitance, C_{GD}, and driver output. It will cause the voltage on the gate of the low-side FET to rise. If this voltage spike peaks beyond the threshold voltage, V_{TH}, the FET will conduct. Considering that the high-side FET is also conducting, this can result in a potentially destructive shoot-through event.

The APEK85110 demonstration board uses a bipolar gate drive arrangement which is useful to mitigate against the effects of gate-drain capacitor currents. The secondary supply voltage, V_{SEC}, is a function of the primary supply voltage, V_{DRV}. The Zener diode, CR1, will regulate the positive turn-on voltage of the GaN FET. During the turn-off period, the gate voltage will be negative with a value of:

$V_{GS\_OFF} = V_{SEC} - V_{ZENER}$. V_{SEC} is typically 9 V.

This negative V_{GS_OFF} voltage allows more margin before the threshold voltage can be reached.

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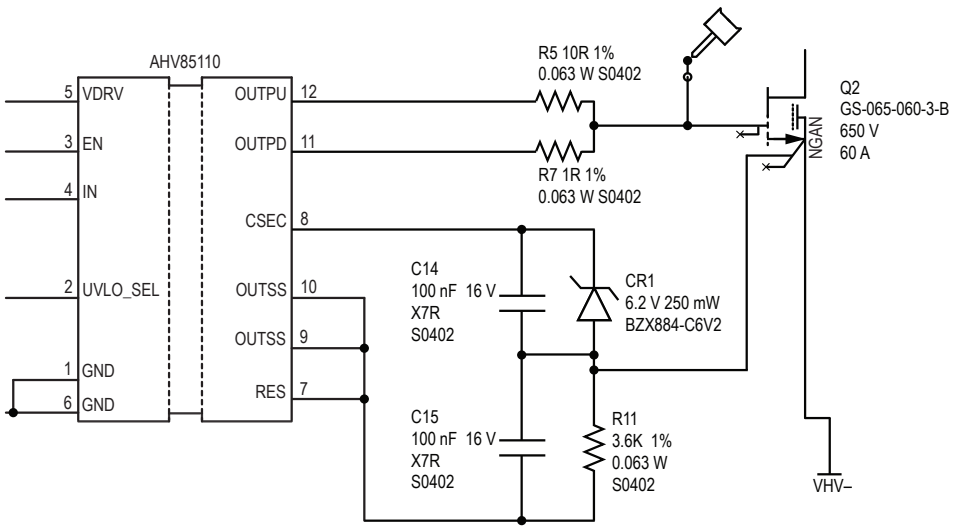
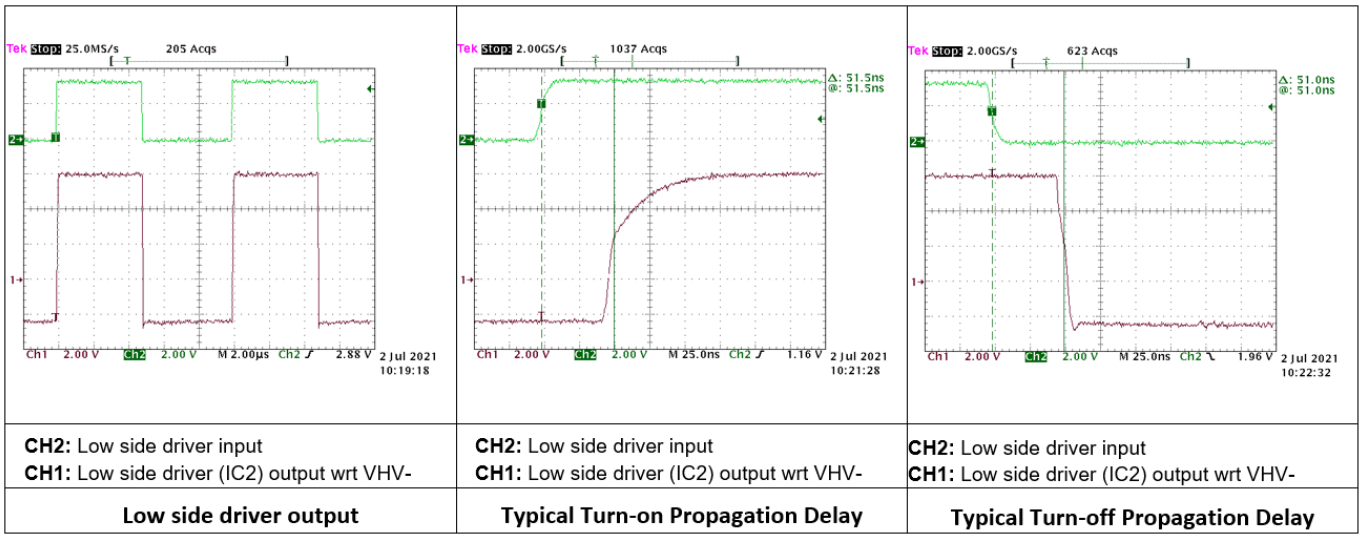


Figure 6: Bipolar Gate Drive Schematic

Propagation Delay

- V_{DRV} = 12 V
- Input = 100 kHz
- R_{PU} = 10 Ω, R_{PD} = 1 Ω
- Power train unloaded, i.e., VHV+ = 0 V.



CH2: Low side driver input **CH1:** Low side driver (IC2) output wrt VHV-	**CH2:** Low side driver input **CH1:** Low side driver (IC2) output wrt VHV-	**CH2:** Low side driver input **CH1:** Low side driver (IC2) output wrt VHV-
Low side driver output	**Typical Turn-on Propagation Delay**	**Typical Turn-off Propagation Delay**

Figure 7: Typical Driver Output at 100 kHz

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Double Pulse Test

Theory

The double pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.

For a low-side switch, the set up is as shown below:

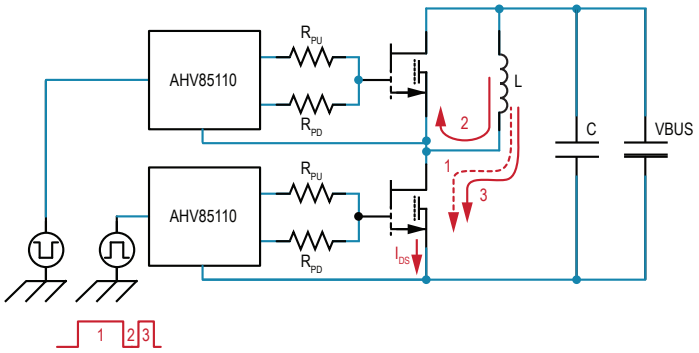

Figure 8: Double Pulse Test

The low-side switch is driven with two pulses as shown below. The high-side switch can be held off or driven with the inverse of the low-side gate switch (with adequate dead time).

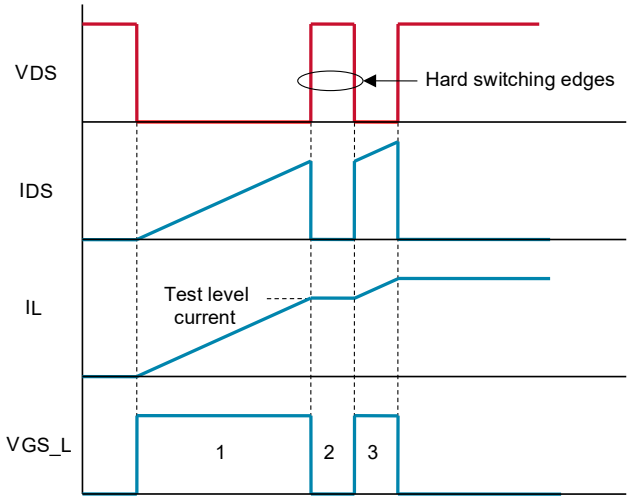

Figure 9: Double Pulse Test Waveforms

An inductor is placed in parallel with the high-side switch. The goal of this inductor is to establish the test level current in the low-side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = (V_{BUS} \times t_{ON\_1}) / L$$

During period 2, the inductor current will naturally decay. The duration of period 2 should not be too long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current will again rise. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn-off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn-on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

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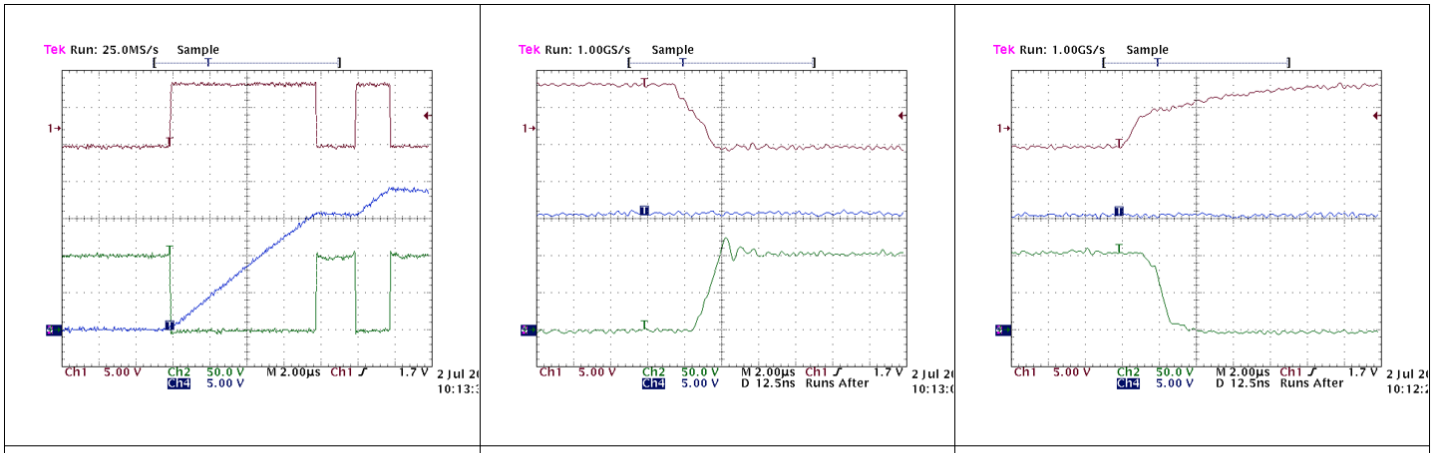
Test Results

Components	
Drivers:	Allegro AHV85110
Inductor:	49 µH, 360 mΩ Air Core
R_{PU}:	10 Ω
R_{PD}:	1 Ω

DPT Result 100 V, 15 A



CH1 (Red): Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current (1A/V)	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**
DPT Overview	**DPT Hard switching turn off**	**DPT Hard switching turn on Time base (12.5ns/div)**

Figure 10: DPT 100 V, 15 A

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DPT Result 400V – 62A

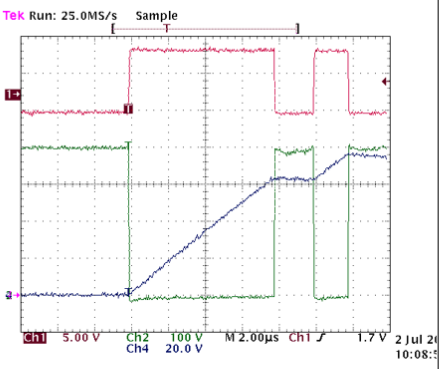	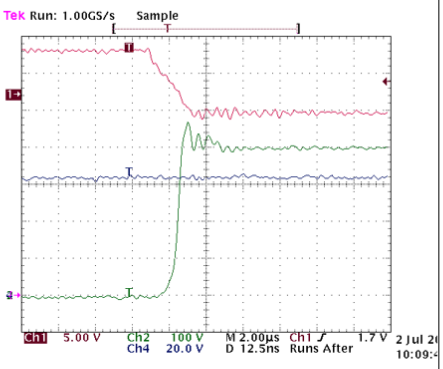	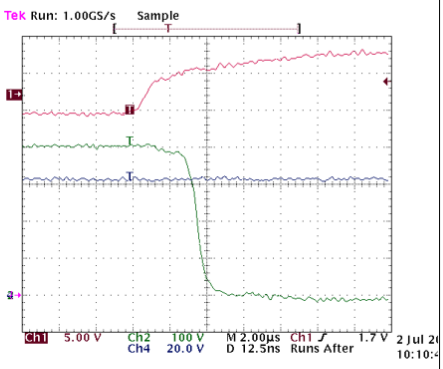
CH1 (Red): Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current (1A/V)	**CH1 (Red):** Low side output wrt VHV- **CH2 (Grn):** Switch Node (500MHz Probe) **CH4 (Blu):** Inductor Current **(1A/V)**
DPT Overview	**DPT Hard switching turn off**	**DPT Hard switching turn on Time base (12.5ns/div)**

Figure 11: DPT 400 V, 62 A

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APEK85110 SCHEMATIC

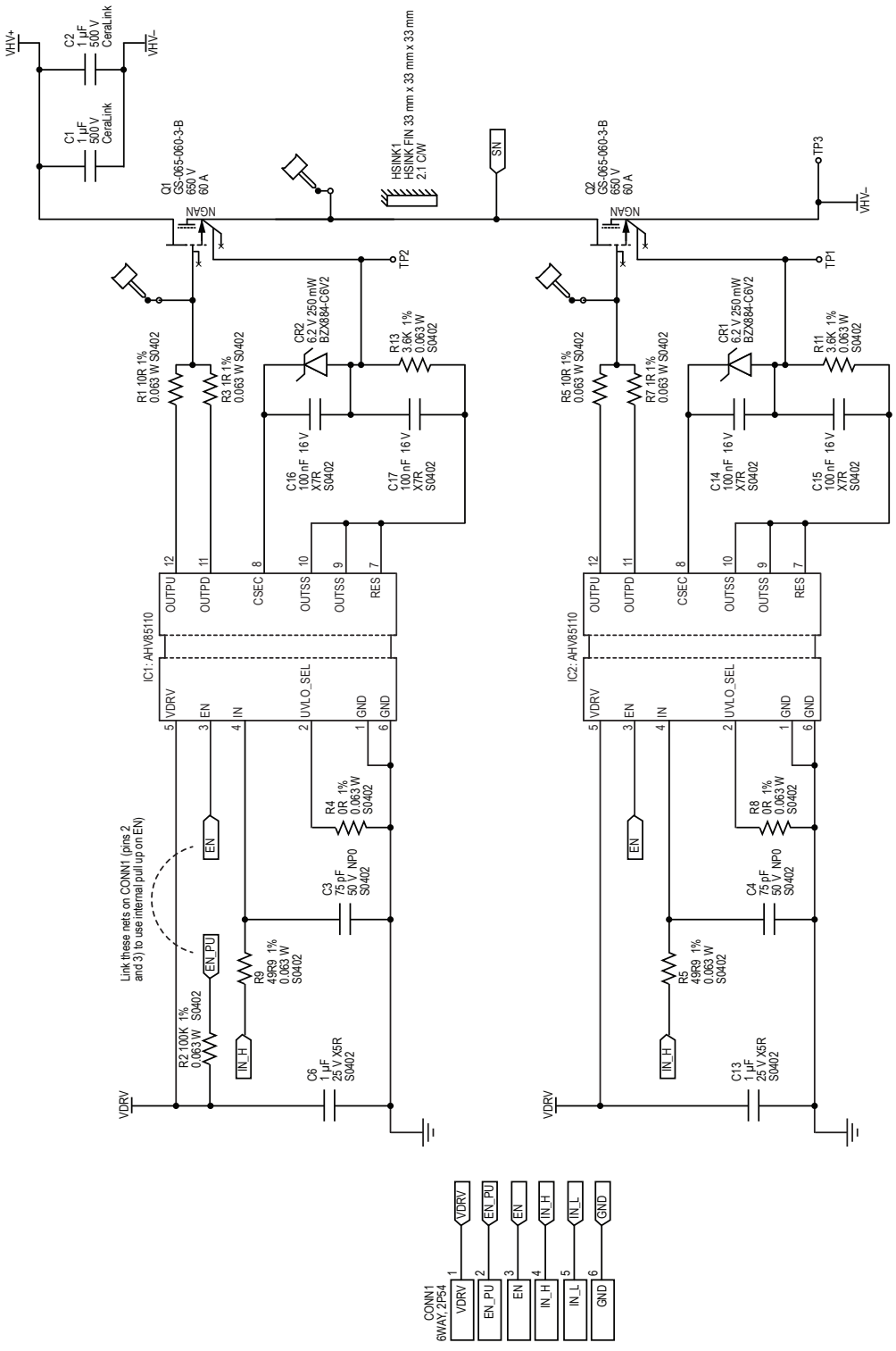

Figure 12: APEK85110 Schematic

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PCB Layout

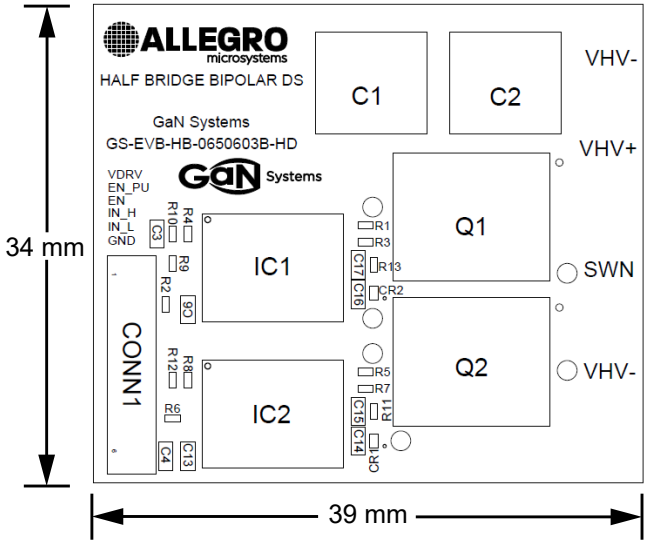

Figure 13: APEK85110 Silkscreen and Component Placement

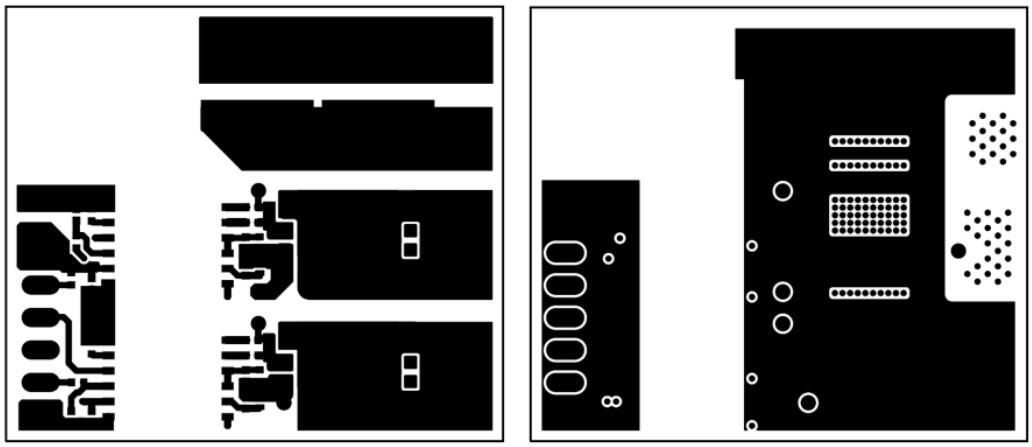

Figure 14: APEK85110 Top-Side Copper (L) and Layer 2 Copper (R)

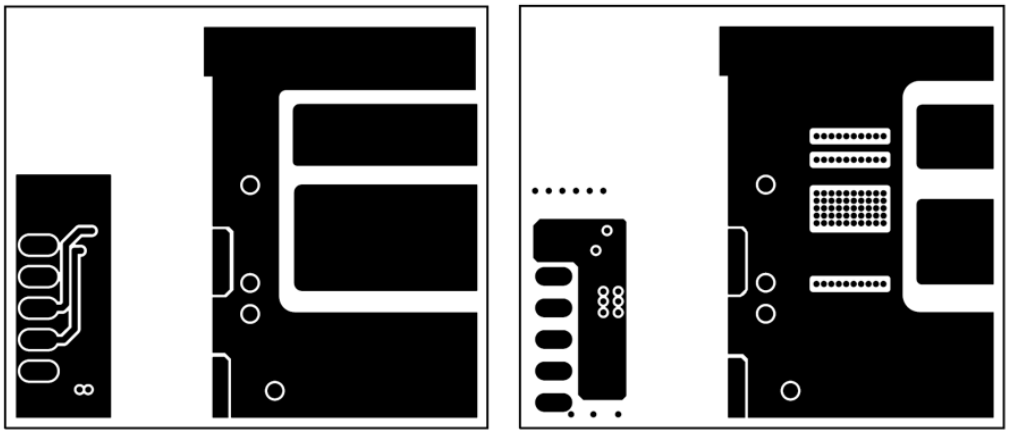

Figure 15: APEK85110 Layer 2 Copper(L) and Bottom-Side Copper (R)

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APEK85110 Half-Bridge Driver Switch Board Bill Of Materials

Table 1: Bill of Materials

Item	Ref Name	Description	Value	Qty	Manufacturer	Manufacturer PN
1	C1, C2	CAP CERALINK, 1 µF, 500 V PLZT	1 µF	2	TDK	B58031U5105M062
2	C14, C15, C16, C17	CAP, CER,100 nF,16 V, X7R, S0402	100 nF	4	KEMET	C0402C104K4RALTU
3	C3, C4	CAP, CER, 75 pF, 50 V, NP0, S0402	75 pF	2	KEMET	C0402C750J5GACTU
4	C6, C13	CAP, CER,1 µF, 25V, X5R, S0402	1 µF	2	MURATA	GRM155R61E105KA12D
3	CONN1	HEADER, 6 WAY, 2.54 mm	6WAY, 2P54	1	WURTH	61300611121
6	CR1, CR2	DIO ZEN, 6V2, 250 mW, 2%, SOD882	BZX884-C6V2	2	NEXPERIA	BZX884-B6V2,315
7	IC1, IC2	GaN FET Driver	AHV85110	2	HEYDAY IC	HEY1011-L12
8	Q1, Q2	NGAN GS-065-060-3-B 650V 60A	GS-065-060-3-B	2	GAN SYSTEMS	GS-065-060-3-B
9	R1, R5	RES, SMD, 10R, 0.063W, 1%, S0402	10 Ω	2	VISHAY	CRCW040210R0FKED
10	R11, R13	RES, SMD, 3K6, 0.063W, 1%, S0402	3.6 kΩ	2	PANASONIC	ERJ2RKF3601X
11	R2	RES, SMD, 100K, 0.063W, 1%, S0402	100 kΩ	1	PANASONIC	ERJ2GEJ104X
12	R3, R7	RES, SMD, 1R0, 0.063W, 1%, S0402	1 Ω	2	VISHAY	CRCW04021R00FKED
13	R4, R8	RES, SMD, 0R0, 0.063W, 1%, S0402	0 Ω	2	VISHAY	RCG04020000Z0ED
14	R6, R9	RES, SMD, 49R9, 0.063W, 1%, S0402	49.9 Ω	2	VISHAY	CRCW040249R9FKED

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Revision History

Number	Date	Description
–	August 30, 2022	Initial release
1	November 17, 2022	Corrected V_{DRV} range (page 1), changed APEK85110D1-E to APEK85110 (page 1), corrected quick start figure (page 3), and replaced several figures with high-resolution versions with updated product image and made minor editorial corrections (throughout).

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