

Description

The DIODES™ AP7583Q/AQ series are 300mA LDO for automotive battery-powered applications. The AP7583Q features 2.5µA quiescent current at light loads. Therefore, the AP7583Q/AQ are suitable solution to supply always power-on components, such as microcontroller (MCUs) and controller area network (CAN) transceivers.

The AP7583Q/AQ have features of wide input-voltage range, high accuracy, low-dropout voltage, current limit and ultra-low quiescent current, which make it ideal for automotive applications. The AP7583AQ has power-good indicator.

The IC consists of a voltage reference, an error amplifier, a resistor network for setting output voltage, a current-limit circuit for current protection, and a chip-enable circuit.

The AP7583Q/AQ both have 3.3V and 5V fixed output-voltage version, and adjustable version.

The AP7583Q is available in space-saving W-DFN2020-6 (SWP) (Type A1) package, and AP7583AQ has good power dissipation packages of MSOP-8EP, W-DFN2020-6 (SWP) (Type A1), and TO252-4 (Type C).

Features

- Wide Input-Voltage Range: 3V to 42V
- Maximum Output Current: 300mA
- Low-Dropout Voltage: $V_{DROP} = 320mV @ I_{OUT} = 300mA$ (Typ)
- Low Quiescent Current:
 - AP7583Q is 2.5µA (Typ)
 - AP7583AQ is 3µA (Typ)
- High Output-Voltage Accuracy: $\pm 1.5\%$
- Compatible with Low ESR Ceramic Capacitor
- Excellent Line/Load Regulation
- Thermal Shutdown Function
- Short Current Protection Function
- Output Current Limit
- AP7583AQ with Power-Good (PG) Output for Supply Monitoring and for Sequencing of Other Supplies
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP7583Q/AQ are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

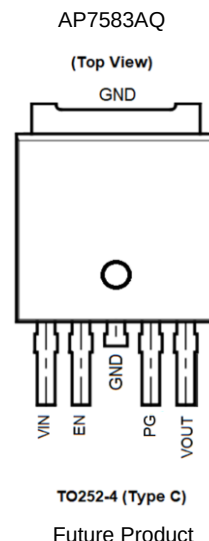
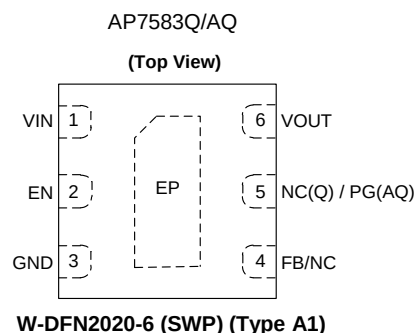
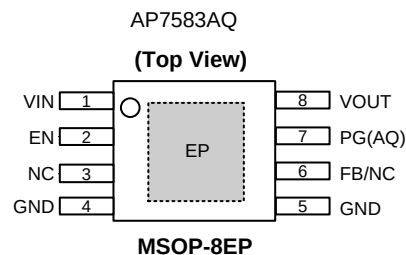
Applications

- Powering MCUs and CAN/LIN transceivers
- Automotive head units
- EV and HEV battery management systems
- Body control modules
- Transmission control units (TCU)

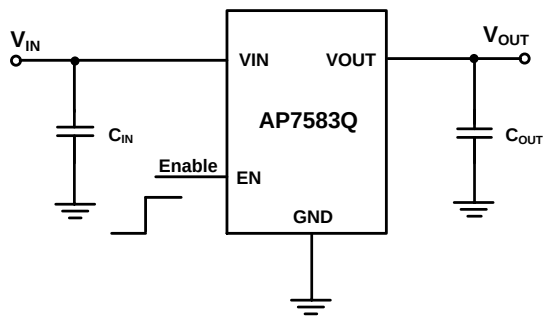
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

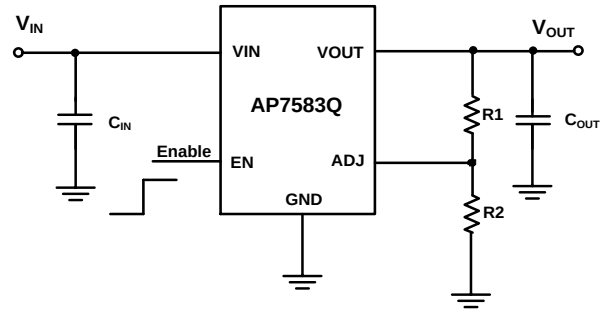
Pin Assignments



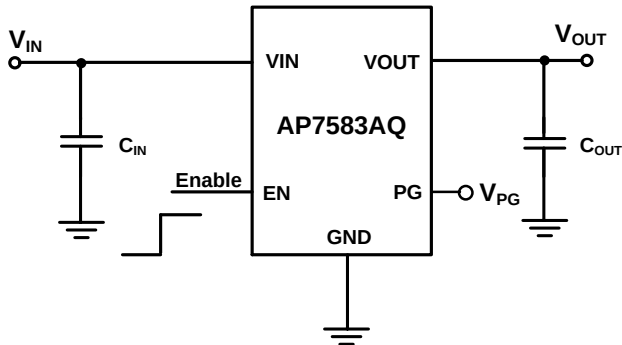
Typical Applications Circuit



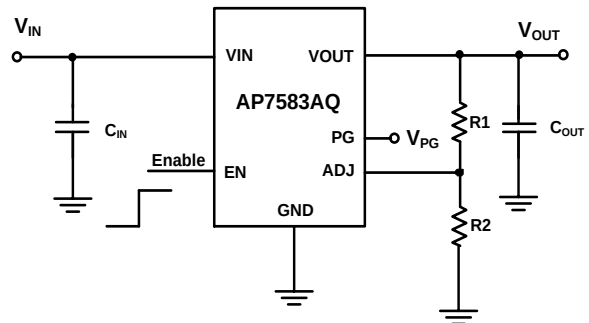
AP7583Q Fixed Version



AP7583Q Adjustable Output



AP7583AQ Fixed Version



AP7583AQ Adjustable Output

Pin Descriptions

Pin Number			Pin Name	Function
MSOP-8EP AP7583AQ	W-DFN2020-6 (SWP) (Type A1) AP7583Q/AQ	TO252-4 (Type C) AP7583AQ		
1	1	1	VIN	Input voltage
2	2	2	EN	Enable input, active high
3	5(Q)	—	NC	Not connected internally. Recommend connection to GND to maximize PCB copper for thermal dissipation.
7	5(AQ)	4	PG	Power-Good pin with one internal pull high resistor. When the VOUT is below the PG threshold, the PG pin is driven low; when the VOUT exceeds the threshold, the PG pin goes into a high-impedance state.
4, 5	3	3	GND	Ground
6	4	—	FB/NC	Adjustable voltage version only – a resistor divider from this pin to the OUT pin and ground sets the output voltage.
8	6	5	VOUT	Regulated output voltage
EP	EP	—	Exposed Pad	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone.

The diagram shows a buck converter circuit. The input is V_{IN} and the output is V_{OUT} . The input voltage V_{IN} is connected to the positive terminal of an inductor and to the positive terminal of a feedback divider consisting of resistors R_1 and R_2 . The output voltage V_{OUT} is connected to the negative terminal of the inductor and to the junction between R_1 and R_2 . The negative terminal of the inductor is also connected to the negative terminal of the feedback divider. The output voltage V_{OUT} is also connected to the positive terminal of a feedback divider consisting of resistors R_1 and R_2 . The negative terminal of the feedback divider is connected to GND. The output voltage V_{OUT} is also connected to the positive terminal of a feedback divider consisting of resistors R_1 and R_2 . The negative terminal of the feedback divider is connected to GND. The output voltage V_{OUT} is also connected to the positive terminal of a feedback divider consisting of resistors R_1 and R_2 . The negative terminal of the feedback divider is connected to GND.

[illegible][illegible]

The block diagram illustrates the internal architecture of the LT8602. It features a **Gate Driver** block that receives the **EN** (enable) signal and drives the gate of the high-side MOSFET. The high-side MOSFET's source is connected to **VIN** and its drain is connected to **VOUT**. A **Current Limit and Thermal Shutdown** block is connected to the drain of the high-side MOSFET and the gate of the low-side MOSFET. The **FB** (feedback) input is connected to the non-inverting input of the first op-amp, which has a reference voltage of **0.8V**. The inverting input of this op-amp is connected to the drain of the high-side MOSFET. The output of the first op-amp drives the gate of the low-side MOSFET. The low-side MOSFET's source is connected to **GND** and its drain is connected to **VOUT** through a resistor **R_{PU}**. The **PG** (power good) output is taken from the node between **R_{PU}** and the low-side MOSFET. The second op-amp, with a reference voltage of **0.72V**, has its non-inverting input connected to the **FB** node and its inverting input connected to the gate of the low-side MOSFET.

AP7583AQ Adjustable Version

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating		Unit
V _{IN}	Supply Input Voltage	-0.3 to 45		V
V _{OUT}	Regulated Output Voltage	-0.3 to 7		V
I _{OUT}	Output Current	300		mA
T _{LEAD}	Lead Temperature (Soldering, 10sec)	+260		°C
T _J	Operating Junction Temperature	+150		°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	MSOP-8EP	36.1	°C/W
		W-DFN2020-6 (SWP) (Type A1)	80.4	
		TO252-4 (Type C)	27.2	
θ _{JC}	Thermal Resistance (Junction to Case)	MSOP-8EP	6.532	°C/W
		W-DFN2020-6 (SWP) (Type A1)	26.4	
		TO252-4 (Type C)	7.5	
T _{STG}	Storage Temperature Range	-40 to +150		°C
CDM	ESD (Charge Device Model)	±1500		V
HBM	ESD (Human Body Model)	±2000		V

- Notes:
- Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period can affect device reliability.
 - Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3inch × 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions

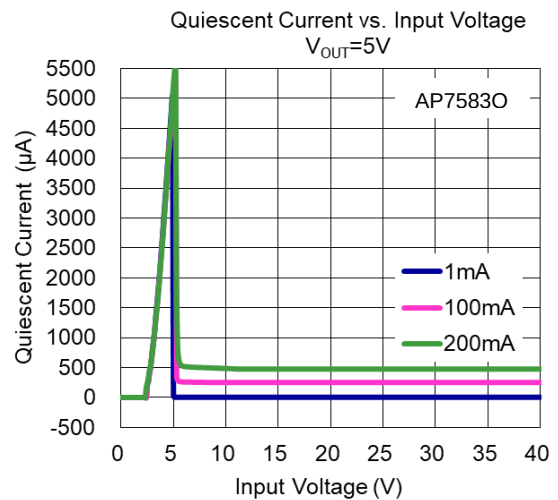
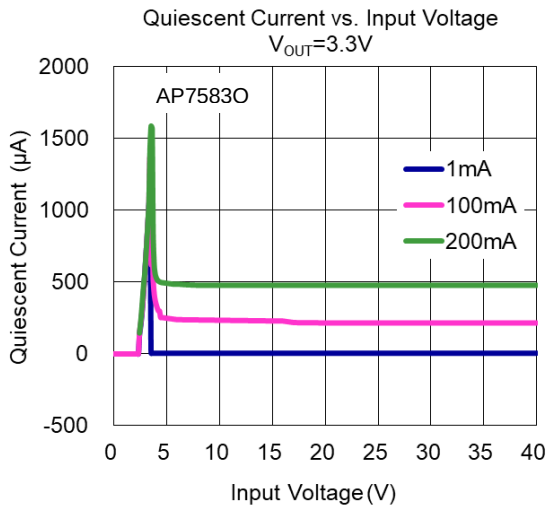
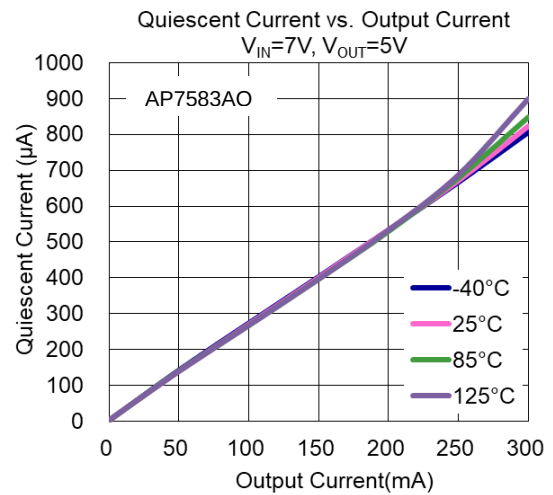
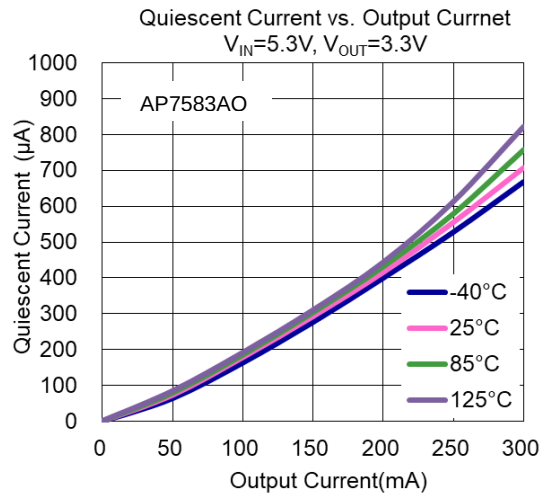
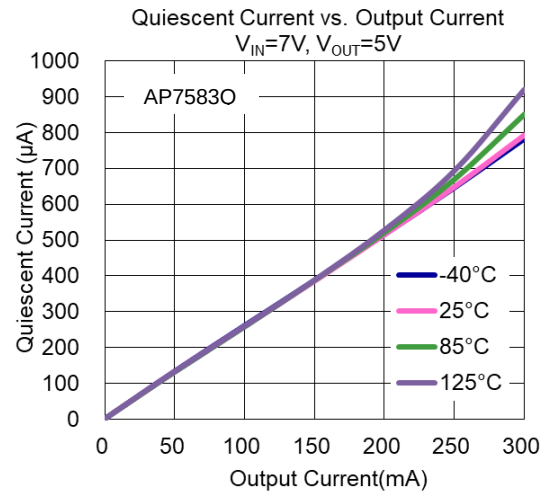
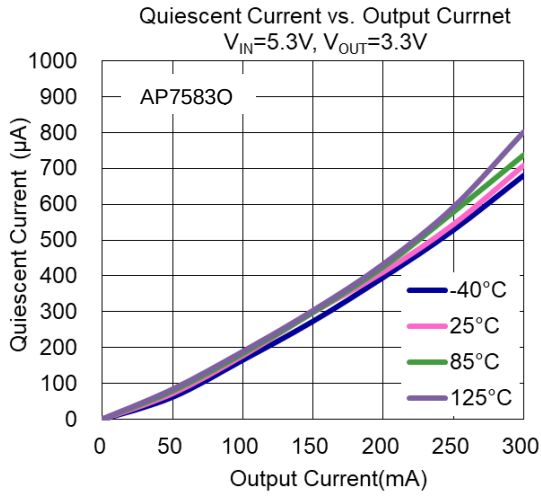
Symbol	Parameter	Min	Max	Unit
V _{IN}	Supply Input Voltage	3.0	42	V
V _{OUT}	Supply Output Voltage	1.2	5	V
T _J	Operating Junction Temperature	-40	+125	°C

Electrical Characteristics ($-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$, $I_{\text{OUT}} = 1\text{mA}$, $C_{\text{IN}} = C_{\text{OUT}} = 10\mu\text{F}$ ceramic capacitor, $V_{\text{IN}} = 14\text{V}$)

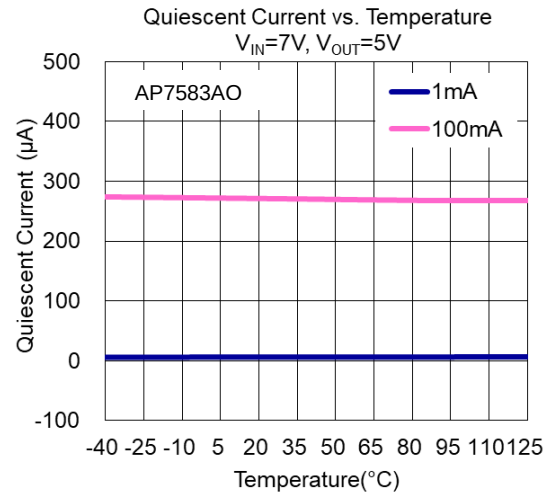
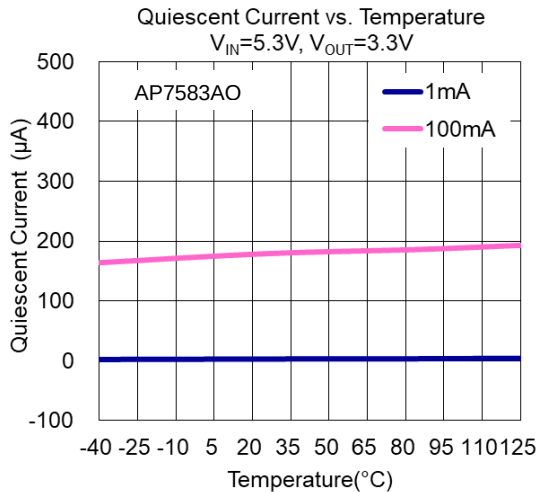
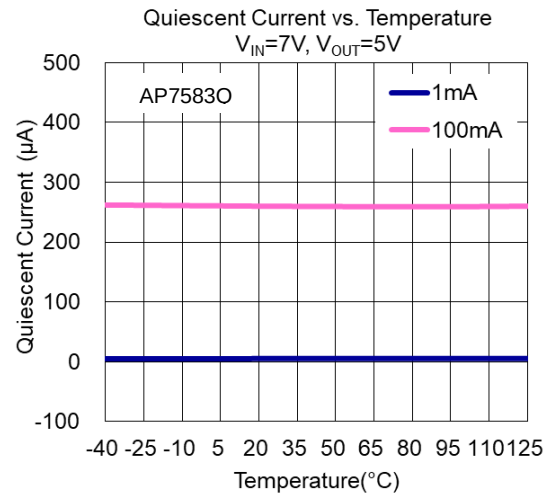
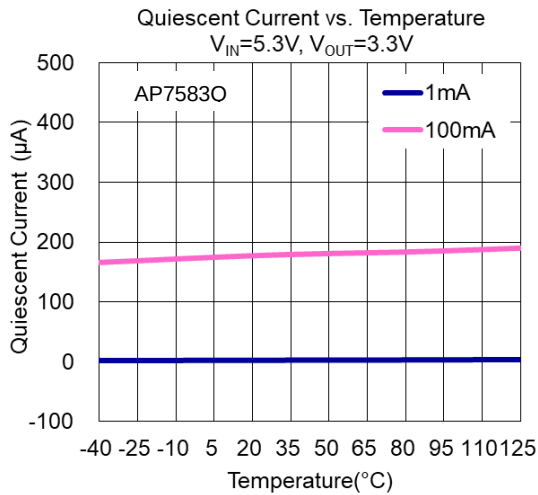
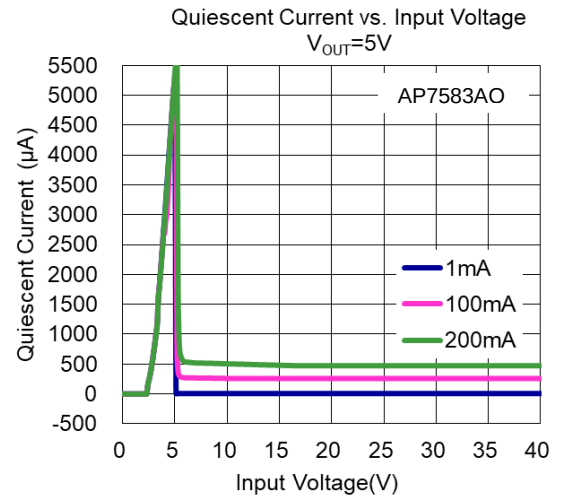
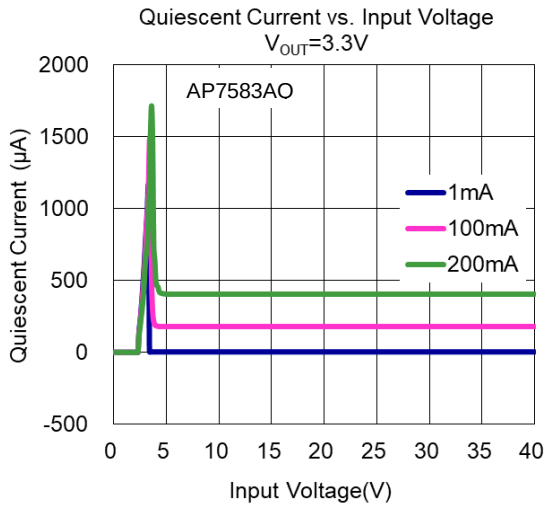
Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V _{OUT}	Output Voltage		Variation from Specified V _{OUT}	V _{OUT} * 98.5%	—	V _{OUT} * 101.5%	V
V _{IN}	Input Voltage		—	3.0	—	42	V
V _{FB}	Feedback Reference Voltage		—	1.183	1.207	1.231	V
I _{LIMIT}	Current Limit		V _{OUT} Short to 90% x V _{OUT}	310	510	690	mA
ΔV _{OUT} /ΔV _{IN}	Line Regulation		V _{IN} = V _{OUT} + 1V to 40V, I _{OUT} = 1mA	-10	—	10	mV
ΔV _{OUT} /V _{OUT}	Load Regulation		1mA ≤ I _{OUT} ≤ 300mA	-20	—	20	mV
V _{DROP}	Dropout Voltage (Note 5)		I _{OUT} = 300mA @V _{OUT} = 3.3V	—	450	700	mV
			I _{OUT} = 300mA @V _{OUT} = 5V	—	320	500	mV
I _Q	Quiescent Current	AP7583Q	I _{OUT} = 0A	—	2.5	4.0	μA
		AP7583AQ	I _{OUT} = 0A	—	3	6	μA
I _{SHUTDOWN}	Shutdown Current		EN = 0V	—	0.3	0.5	μA
V _{IL}	EN Input Logic-Low Voltage		—	0	—	0.3	V
V _{IH}	EN Input Logic-High Voltage		—	1.7	—	V _{IN}	V
ΔV _{OUT} /(V _{OUT} ΔT)	Output Voltage Temperature Coefficient		I _{OUT} = 100μA, -40°C ≤ T _J ≤ +125°C	—	±100	—	ppm/°C
T _{OTSD}	Thermal Shutdown Temperature		—	—	+175	—	°C
T _{HYOTSD}	Thermal Shutdown Hysteresis		—	—	+20	—	°C
PSRR	Power Supply Rejection Ratio		V _(Ripple) = 0.5V _{PP} , I _{OUT} = 10mA, frequency = 100Hz, C _{OUT} = 2.2μF	—	70	—	dB
UVLO	VIN Undervoltage Detection		Ramp V _{IN} up until the Output Turns on	2.1	2.4	2.7	V
			Hysteresis	—	0.2	—	V
I _{FB}	FB Leakage Current		FB = 0V (Adjustable Version)	-10	—	20	nA
AP7583AQ							
t _D	Output-Voltage Turn-On Delay Time		V _{EN} High to V _{OUT} Rising 10%	—	0.8	—	ms
t _{SS}	Output-Voltage Ramp-Up Time		V _{OUT} Rising 10% to 90%	—	200	—	μs
t _{PG}	PG React Time		V _{OUT} 90% to PG Active	—	30	—	μs
t _{PGF}	PG Off Deglitch Time		V _{FB} Falling to PG Low	—	3	—	μs
			EN Goes Low to PG Low				
V _{PGR}	PG Rising Threshold		V _{FB} Rising	90	—	94	%
V _{PGF}	PG Falling Threshold		V _{FB} Falling	88	—	92	%
V _{PGS}	PG Sinking Voltage		Sinking Current = 5mA	—	—	0.4	V

Note: 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.

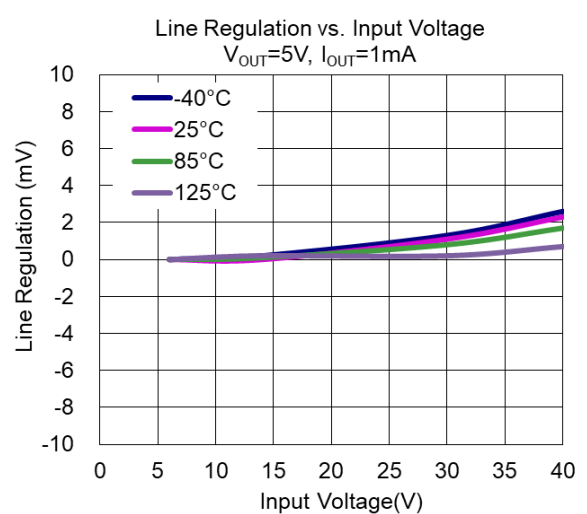
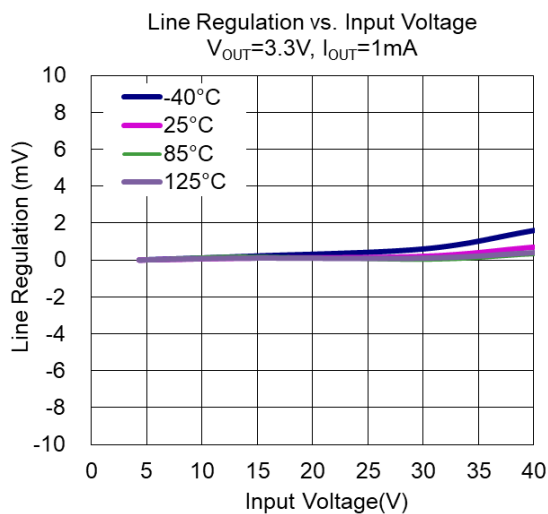
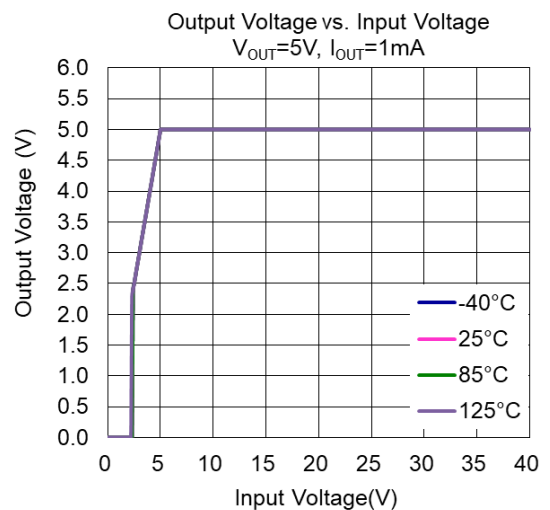
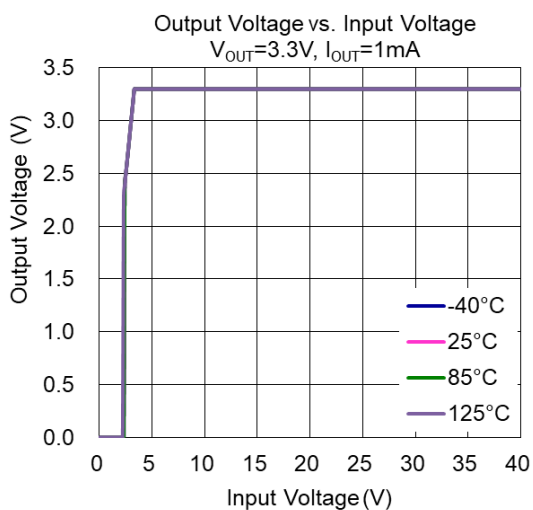
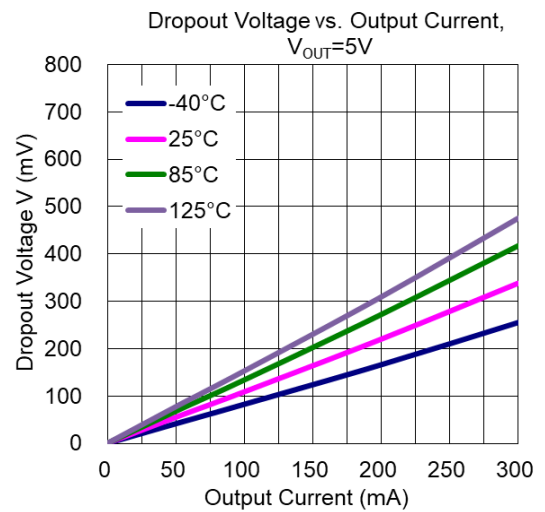
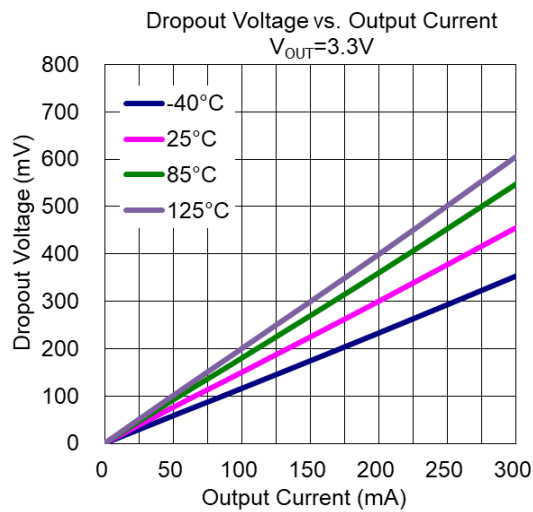
Typical Characteristics ($C_{IN} = C_{OUT} = 10\mu F$)



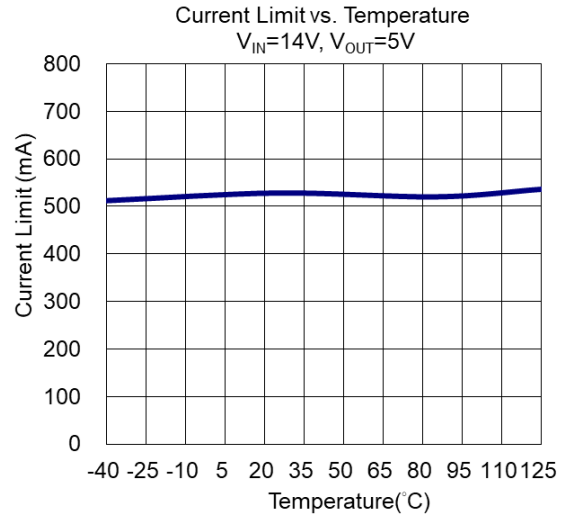
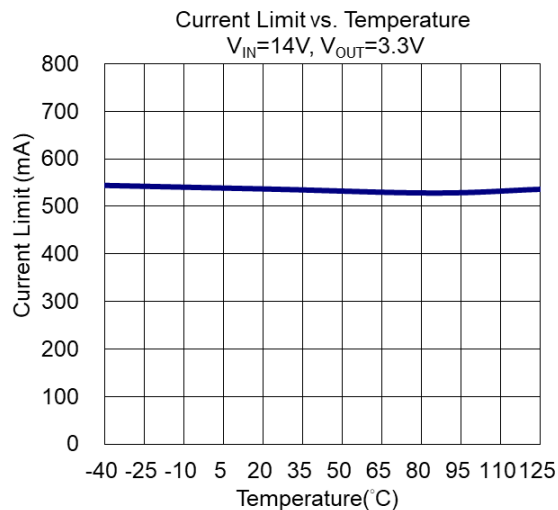
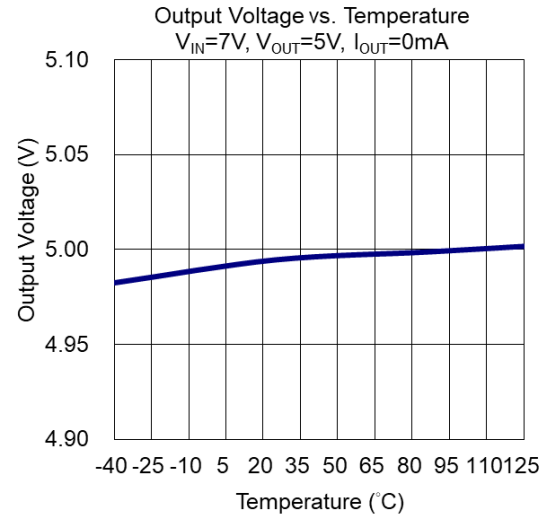
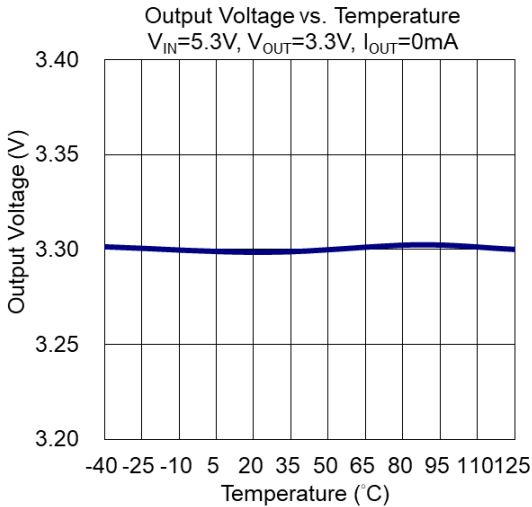
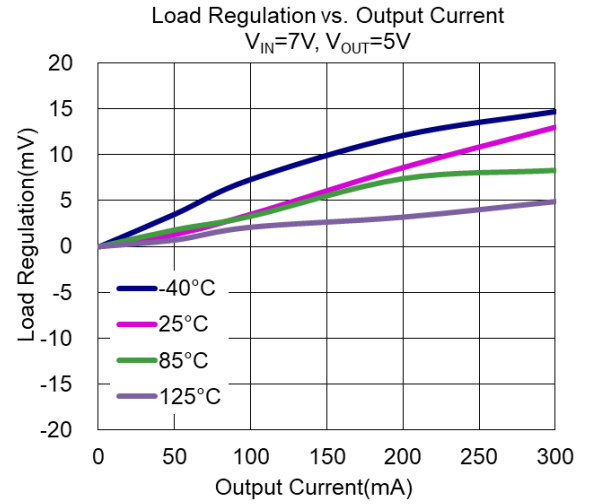
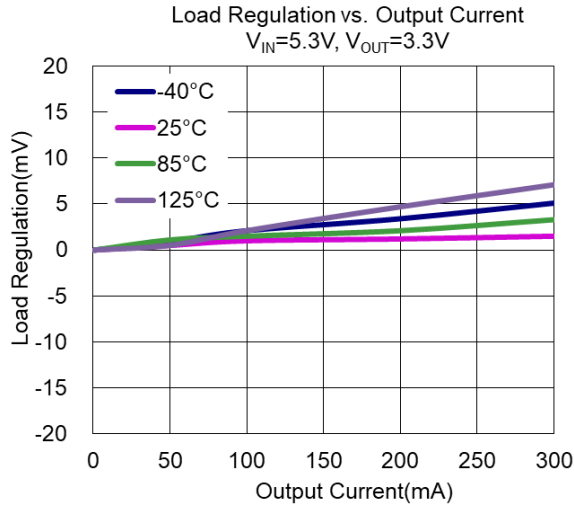
Typical Characteristics ($C_{IN} = C_{OUT} = 10\mu F$) (continued)



Typical Characteristics ($C_{IN} = C_{OUT} = 10\mu F$) (continued)



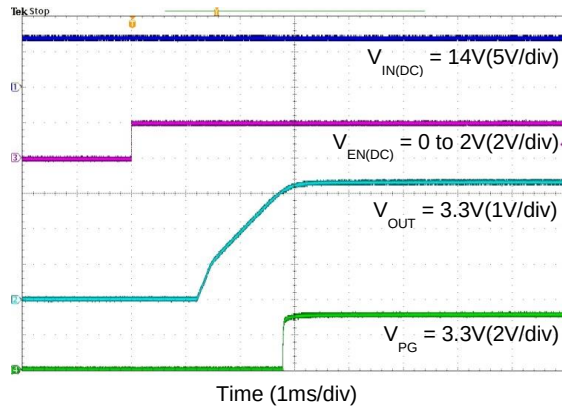
Typical Characteristics ($C_{IN} = C_{OUT} = 10\mu F$) (continued)



Typical Characteristics ($C_{IN} = C_{OUT} = 10\mu F$) (continued)

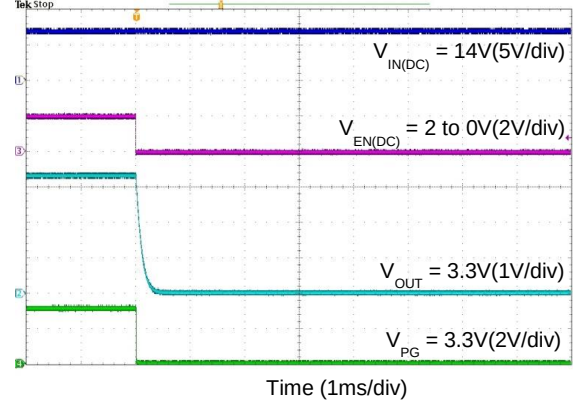
Enable Turn-on Response

$V_{OUT} = 3.3V$



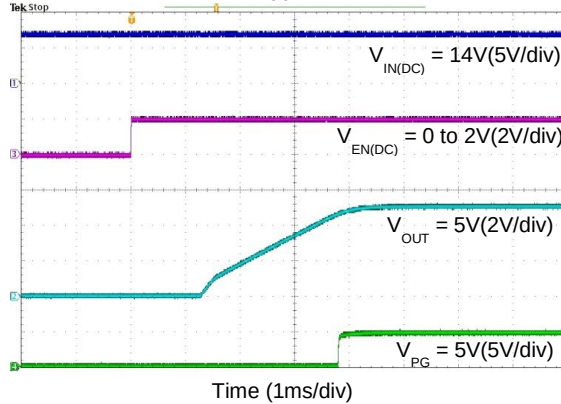
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$V_{OUT} = 3.3V$



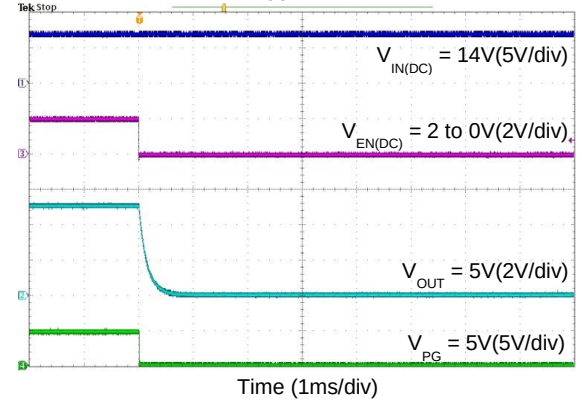
Enable Turn-on Response

$V_{OUT} = 5V$



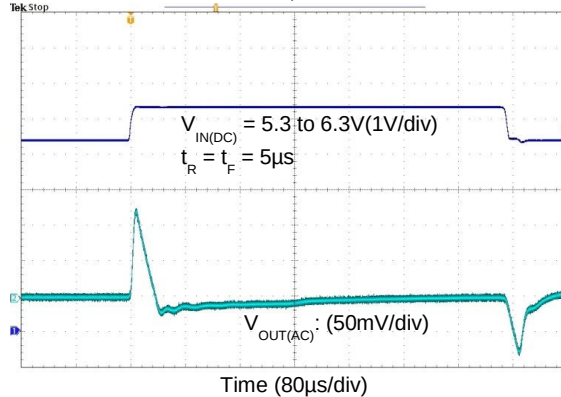
Enable Turn-off Response

$V_{OUT} = 5V$



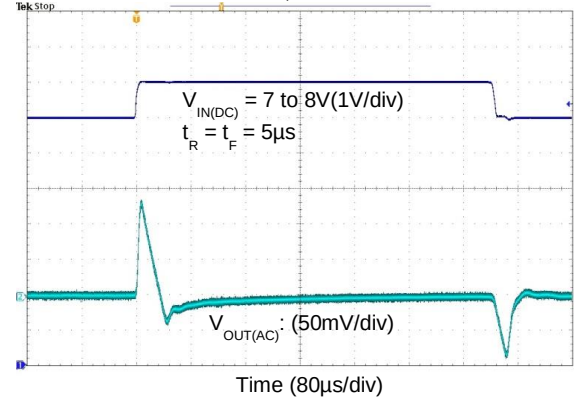
Line Transient Response

$V_{OUT} = 3.3V, I_{OUT} = 30mA$

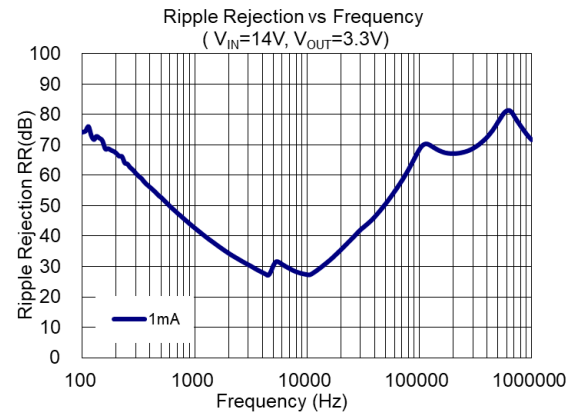
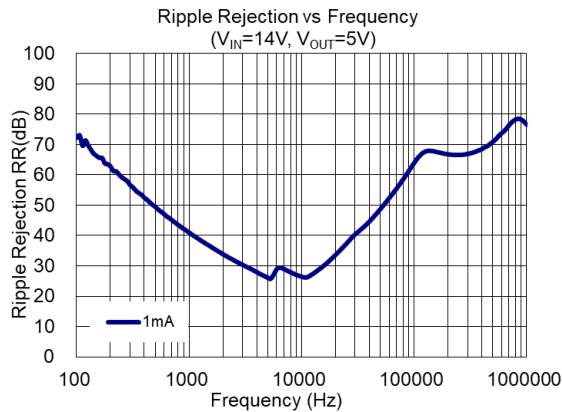
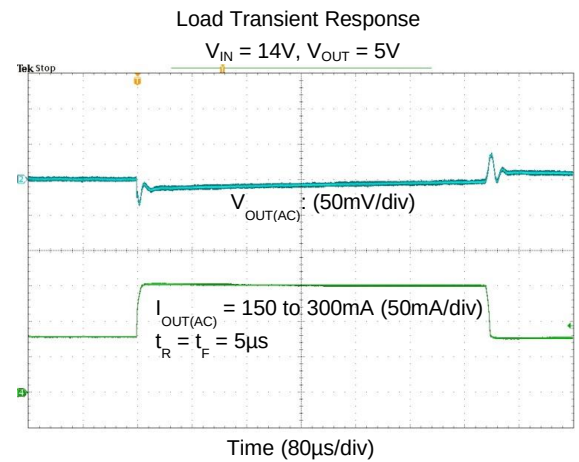
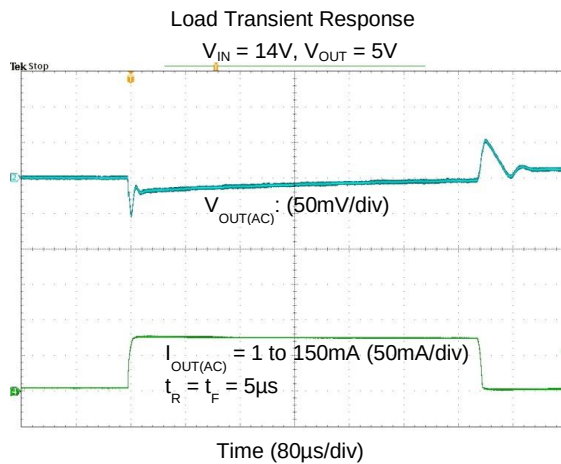
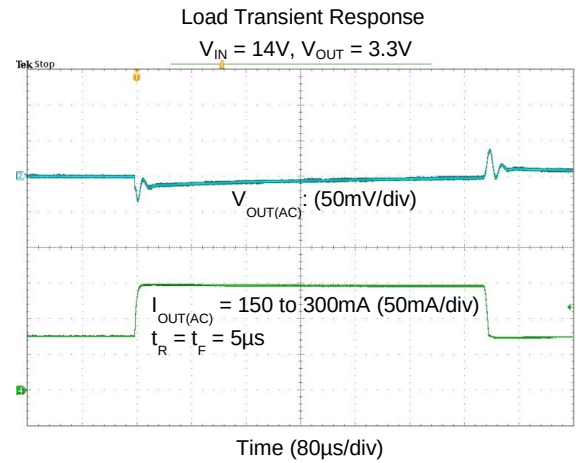
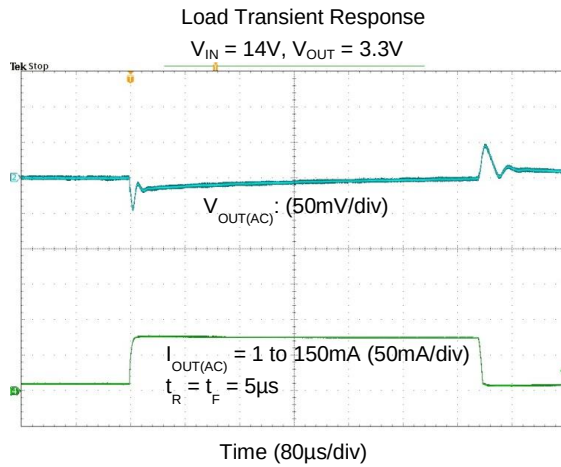


Line Transient Response

$V_{OUT} = 5V, I_{OUT} = 30mA$



Typical Characteristics ($C_{IN} = C_{OUT} = 10\mu F$) (continued)



Application Information

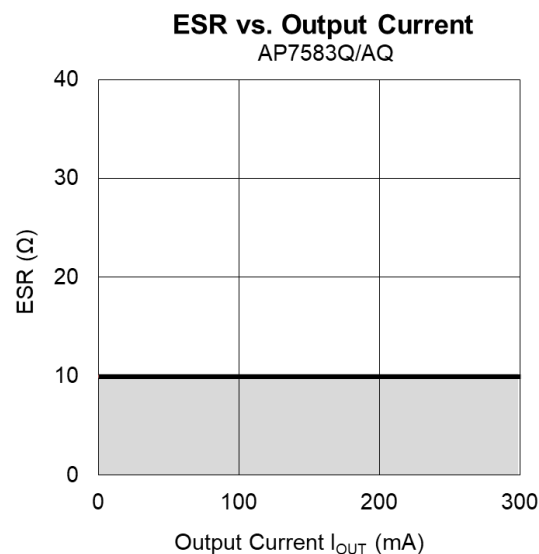
Input Capacitor

A 10 μ F ceramic capacitor is recommended between IN and GND pins to decouple input power-supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

Output Capacitor

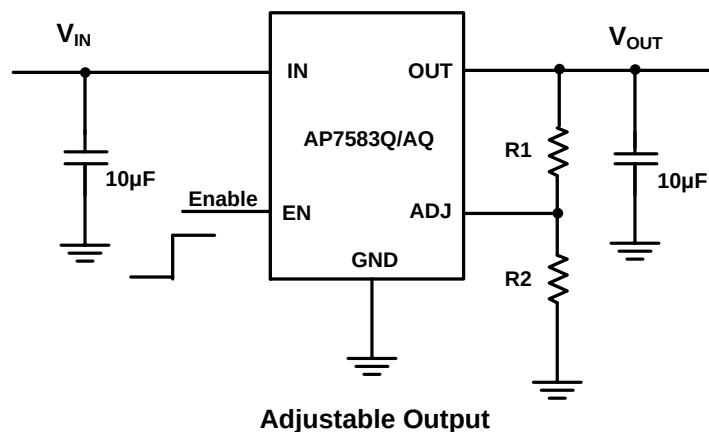
Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. One 10 μ F output capacitor is suggested, the AP7583Q/AQ series LDO would have stable output capacitance range from 4.7 μ F to 100 μ F. The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The stable region for the safety operating temperature (-40°C to +125°C) is marked as the gray area in the graph.

Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to +125°C.



Adjustable Operation

The AP7583Q/AQ provides output voltage from 1.2V to 5.0V through external resistor divider as shown below:



Application Information (continued)

The output voltage is calculated by:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$

Where $V_{REF} = 1.2V$ (the internal reference voltage).

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

To maintain the stability of the internal reference voltage, R_2 needs to be kept smaller than $80k\Omega$.

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ON/OFF Input Operation

The AP7583Q/AQ is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH} .

Current Limit Protection

When output current at OUT pin is higher than current-limit threshold, the current-limit protection will be triggered and clamp the output current to prevent overcurrent and to protect the regulator from damage due to overheating.

Power Good

The power-good (PG) pin is an open-drain output with one internal resistor. When the $V_{OUT} \geq V_{PGR}$, the PG output is high-impedance; if the V_{OUT} drops to below V_{PGF} , or the device is disabled, the PG pin is pulled to low by an internal MOSFET.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately $+175^{\circ}C$, allowing the device to cool down. When the junction temperature reduces to approximately $+155^{\circ}C$, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Power Dissipation

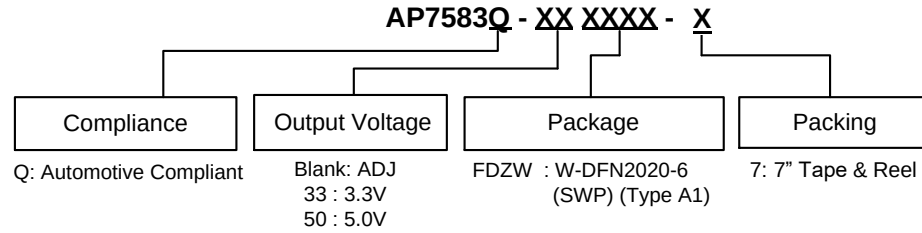
The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

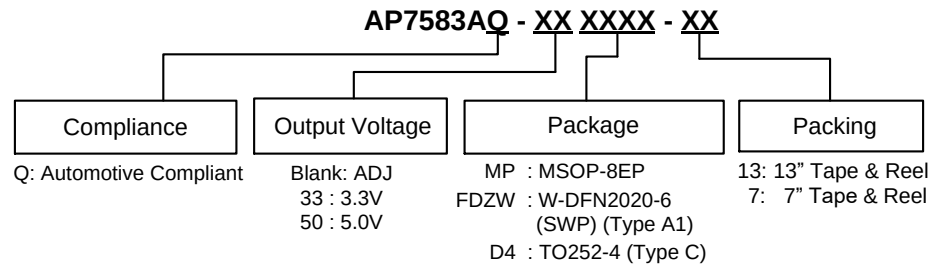
The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

$$P_D(\max@T_A) = \frac{(+150^{\circ}C - T_A)}{R_{\theta JA}}$$

Ordering Information



Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7583Q-XXFDZW-7	FDZW	W-DFN2020-6 (SWP) (Type A1)	3,000	7" Tape & Reel



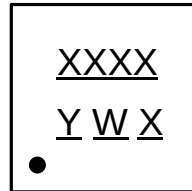
Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7583AQ-XXMP-13	MP	MSOP-8EP	2,500	13" Tape & Reel
AP7583AQ-XXFDZW-7	FDZW	W-DFN2020-6 (SWP) (Type A1)	3,000	7" Tape & Reel
AP7583AQ-XXD4-13(*)	D4	TO252-4 (Type C)	2,500	13" Tape & Reel

*: Future Product

Marking Information (AP7583Q)

(1) W-DFN2020-6 (SWP) (Type A1)

(Top View)



XXXX : Identification Code

Y : Year : 0~9

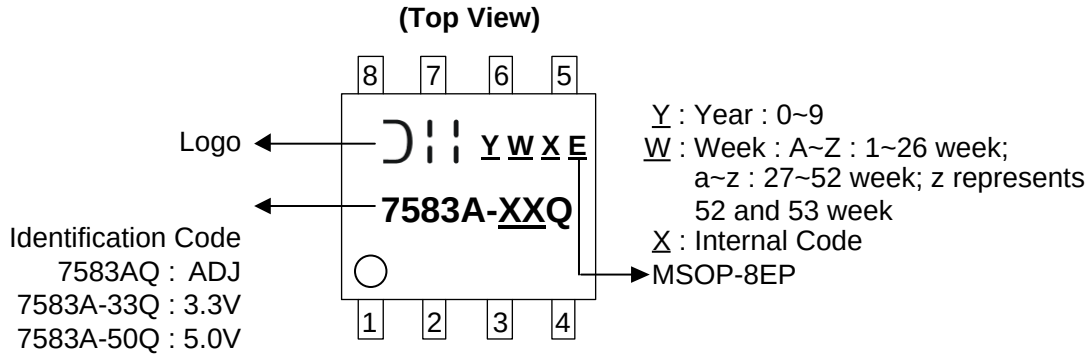
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week

X : Internal Code

Part Number	Package	Identification Code
AP7583Q-FDZW-7	W-DFN2020-6 (SWP) (Type A1)	F7AQ
AP7583Q-33FDZW-7	W-DFN2020-6 (SWP) (Type A1)	F7DQ
AP7583Q-50FDZW-7	W-DFN2020-6 (SWP) (Type A1)	F7EQ

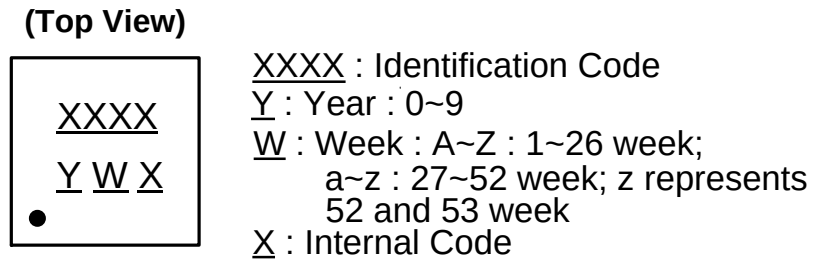
Marking Information (AP7583AQ)

(1) MSOP-8EP



Part Number	Package	Identification Code
AP7583AQ-MP-13	MSOP-8EP	7583AQ
AP7583AQ-33MP-13	MSOP-8EP	7583A-33Q
AP7583AQ-50MP-13	MSOP-8EP	7583A-50Q

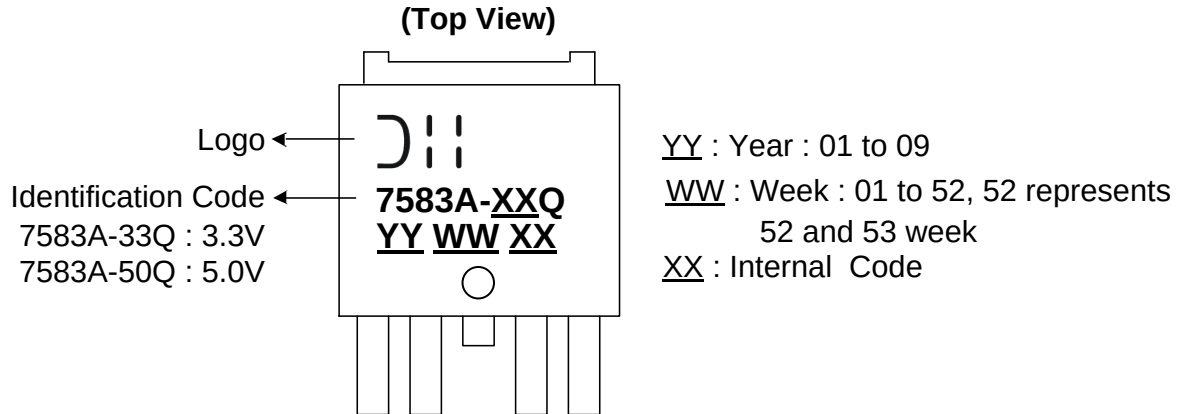
(2) W-DFN2020-6 (SWP) (Type A1)



Part Number	Package	Identification Code
AP7583AQ-FDZW-7	W-DFN2020-6 (SWP) (Type A1)	F8AQ
AP7583AQ-33FDZW -7	W-DFN2020-6 (SWP) (Type A1)	F8DQ
AP7583AQ-50FDZW -7	W-DFN2020-6 (SWP) (Type A1)	F8EQ

Marking Information (AP7583AQ) (continued)

(3) TO252-4 (Type C)

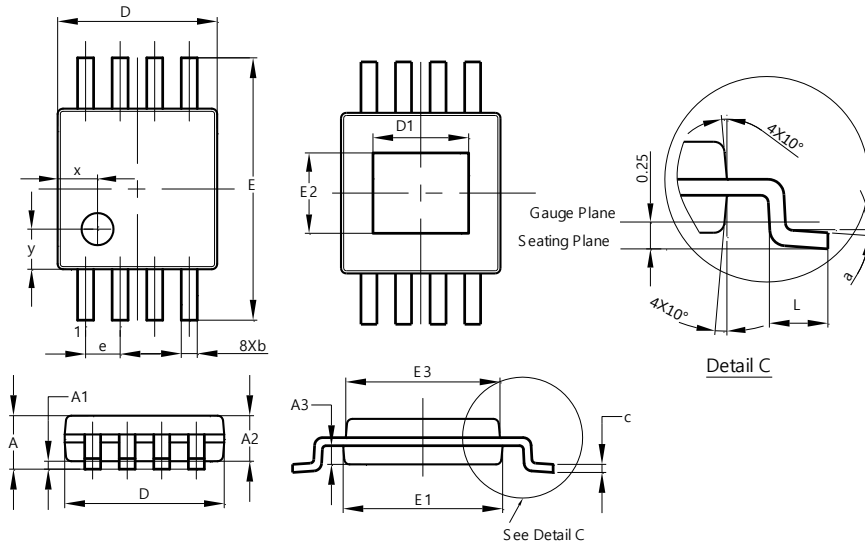


Part Number	Package	Identification Code
AP7583AQ-33D4-13	TO252-4 (Type C)	7583A-33Q
AP7583AQ-50D4-13	TO252-4 (Type C)	7583A-50Q

Package Outline Dimensions

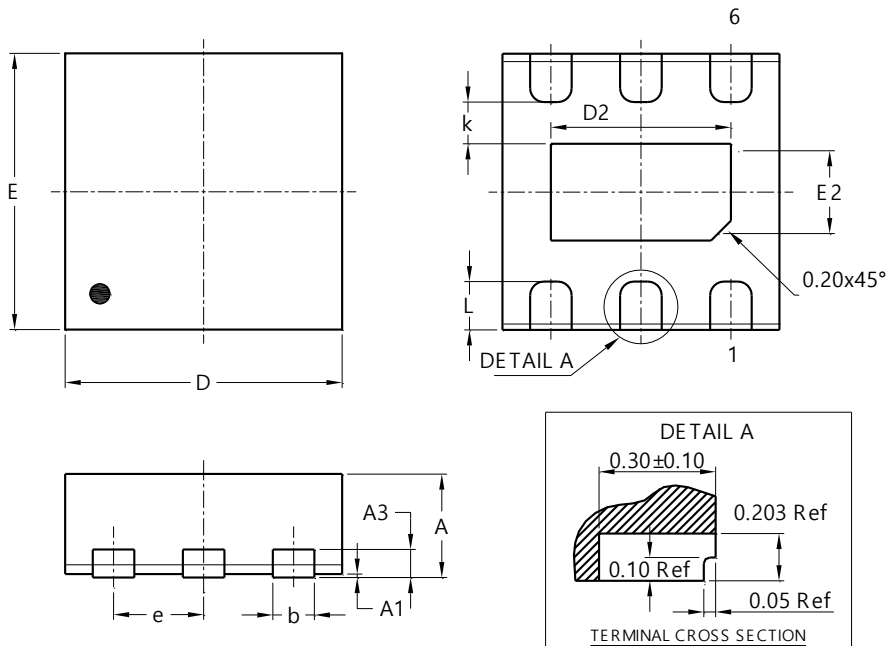
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) MSOP-8EP



MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

(2) W-DFN2020-6 (SWP) (Type A1)

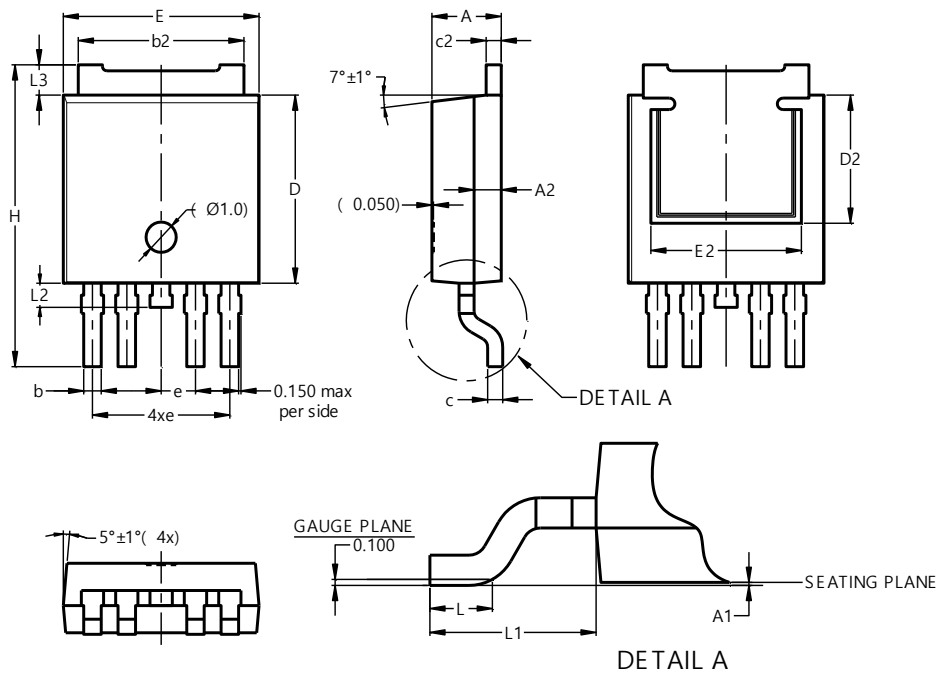


W-DFN2020-6 (SWP) (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.25	0.35	0.30
D	2.00 BSC		
D2	1.35	1.45	1.40
E	2.00 BSC		
E2	0.55	0.65	0.60
e	0.65 BSC		
k	0.20	—	—
L	0.20	0.40	0.30
All Dimensions in mm			

Package Outline Dimensions (continued)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(3) TO252-4 (Type C)

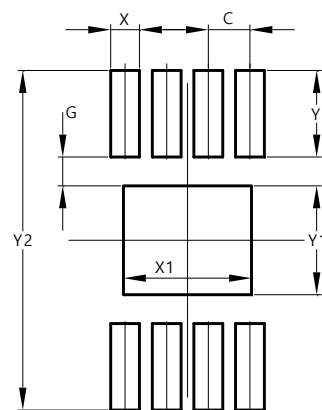


TO252-4 (Type C)			
Dim	Min	Max	Typ
A	2.20	2.35	--
A1	0.00	0.15	--
A2	0.80	1.00	--
b	0.50	0.70	0.60
b2	5.30	5.70	--
c	0.46	0.58	--
c2	0.46	0.58	--
D	6.02	6.22	--
D2	4.24REF		
e	1.14BSC		
E	6.45	6.65	--
E2	5.00REF		
H	9.48	10.48	9.98
L	0.60	--	--
L1	2.76REF		
L2	0.65	0.95	0.80
L3	0.90	1.10	1.00
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) MSOP-8EP

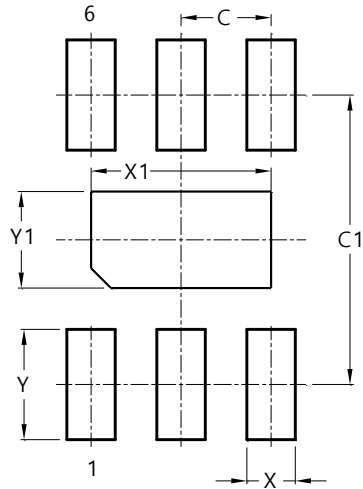


Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

Suggested Pad Layout (continued)

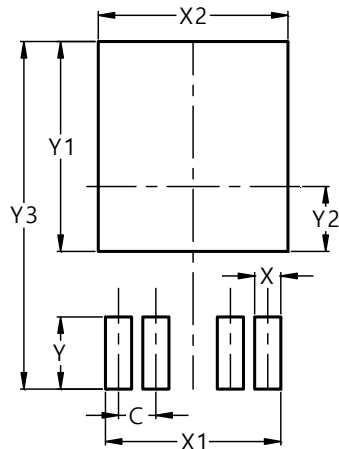
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(2) W-DFN2020-6 (SWP) (Type A1)



Dimensions	Value (in mm)
C	0.650
C1	2.100
X	0.350
X1	1.400
Y	0.800
Y1	0.600

(3) TO252-4 (Type C)



Dimensions	Value (in mm)
C	1.140
X	0.800
X1	5.360
X2	5.800
Y	2.200
Y1	6.400
Y2	1.980
Y3	10.600

Mechanical Data

- Moisture Sensitivity:
 - MSOP-8EP: Level 1 Per J-STD-020
 - W-DFN2020-6 (SWP) (Type A1): Level 1 Per J-STD-020
 - TO252-4 (Type C): Level 3 Per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ③
- Weight:
 - MSOP-8EP: 0.024 grams (Approximate)
 - W-DFN2020-6 (SWP) (Type A1): 0.01 grams (Approximate)
 - TO252-4 (Type C): 0.343 grams (Approximate)

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