4.2V TO 18V INPUT, 2A LOW IQ SYNCHRONOUS BUCK CONVERTER

Description

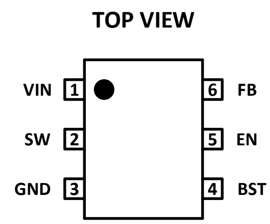
The AP62200 is a 2A, synchronous buck converter with a wide input voltage range of 4.2V to 18V. The device fully integrates a 90mΩ high-side power MOSFET and a 65mΩ low-side power MOSFET to provide high-efficiency step-down DC/DC conversion.

The AP62200 device is easily used by minimizing the external component count due to its adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

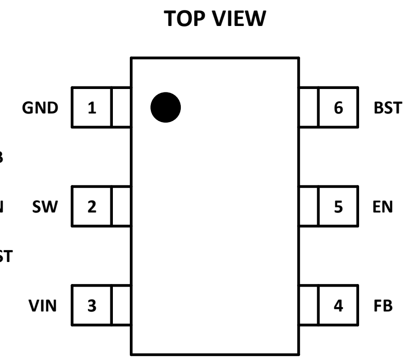
The AP62200 design is optimized for Electromagnetic Interference (EMI) reduction. It has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching.

The device is available in a SOT563 or TSOT26 package.

Pin Assignments



SOT563



TSOT26

Features

- VIN: 4.2V to 18V
- Output Voltage (VOUT): 0.8V to 7V
- 2A Continuous Output Current
- 0.8V ± 1% Reference Voltage (T_A = +25°C)
- 135µA Low Quiescent Current
- 740kHz Switching Frequency (VIN = 12V, VOUT = 5V)
- Up to 84% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Cycle-by-Cycle Valley Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Flat Screen TV Sets and Monitors
- Set Top Boxes
- Consumer Electronics
- Network Systems
- General Purpose Point of Load

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

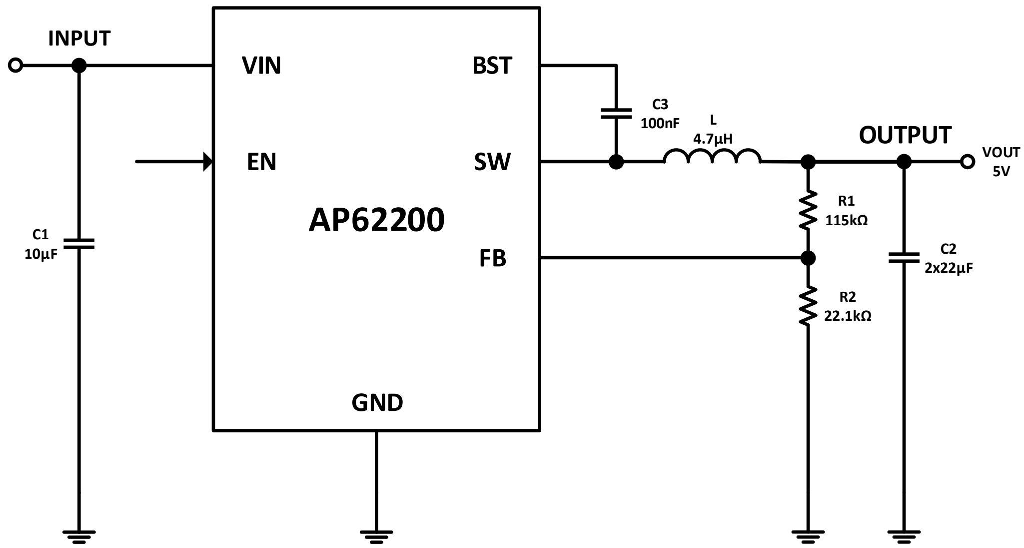


Figure 1. Typical Application Circuit

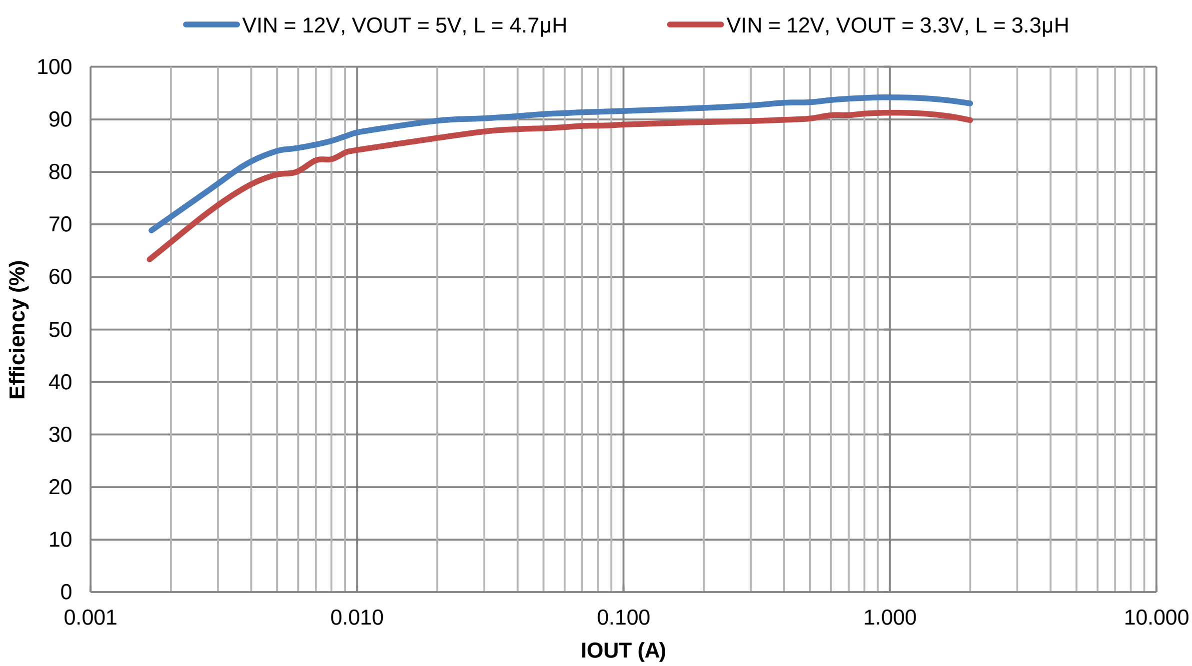


Figure 2. Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number		Function
	SOT563	TSOT26	
VIN	1	3	Power Input. VIN supplies the power to the IC as well as the step-down converter switches. Drive VIN with a 4.2V to 18V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
SW	2	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from BST to SW to power the high-side power MOSFET.
GND	3	1	Power Ground.
BST	4	6	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
EN	5	5	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Can be left open for automatic startup. The EN has a precision threshold of 1.18V for programing the UVLO. See **Enable** section for more details.
FB	6	4	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.

Functional Block Diagram

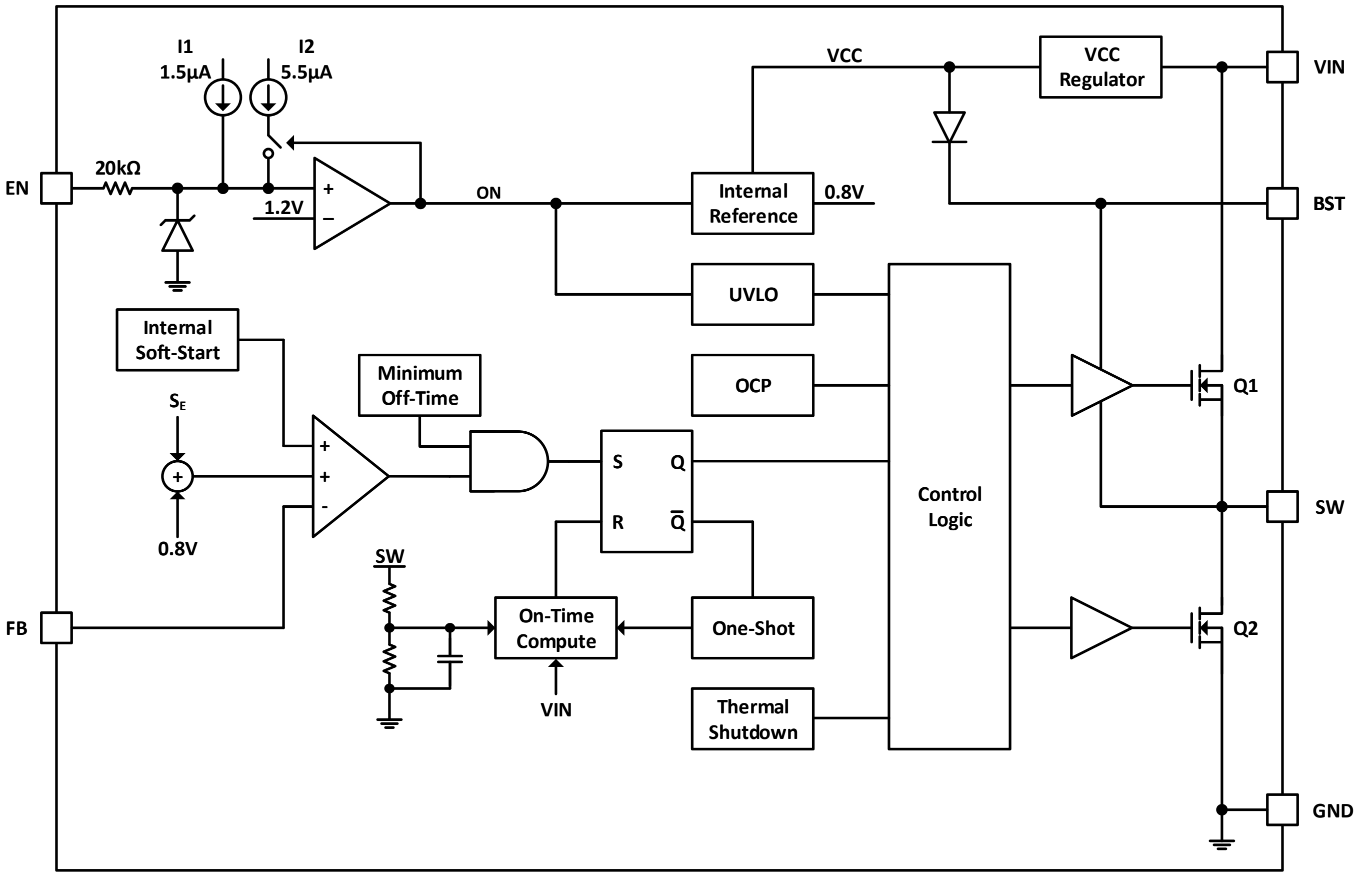


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (At T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +20.0 (DC)	V
		-0.3 to 22.0 (400ms)	
V_{SW}	Switch Pin Voltage	-1.0 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +6.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Mode	2000	V
CDM	Charge Device Model	500	V

Notes: 4. Stresses greater than the **Absolute Maximum Ratings** specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SOT563	110	°C/W
		TSOT26	70	
θ_{JC}	Junction to Case	SOT563	8	°C/W
		TSOT26	12	

Note: 6. Test condition for SOT563/TSOT26: Device mounted on FR-4 substrate, two-layer PCB, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (At T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	4.2	18.0	V
VOUT	Output Voltage	0.8	7.0	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended ambient temperature range, -40°C to +85°C, and input voltage range, 4.2V to 18V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	3	µA
I_Q	Supply Current (Quiescent)	V_{FB} = 0.85V	—	135	—	µA
UVLO	VIN Under Voltage Threshold, Rising	—	—	4.00	4.15	V
	VIN Under Voltage Threshold, Hysteresis	—	—	300	—	mV
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 8)	—	—	90	—	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 8)	—	—	65	—	mΩ
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	From source to drain	2.0	2.4	2.8	A
f_{SW}	Oscillator Frequency	VOUT = 5V, CCM	—	740	—	kHz
t_{ON_MIN}	Minimum On Time	—	—	90	—	ns
t_{OFF_MIN}	Minimum Off Time	—	—	200	—	ns
V_{FB}	Feedback Voltage	T_A = +25°C, CCM	0.792	0.800	0.808	V
		CCM	0.784	0.800	0.816	V
V_{EN_H}	EN Logic High	—	—	1.20	1.25	V
V_{EN_L}	EN Logic Low	—	1.04	1.10	—	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	7.0	—	µA
		V_{EN} = 1V	1.0	1.5	2.0	µA
t_{SS}	Soft-Start Period	—	—	2.5	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	155	—	°C
T_{Hys}	Thermal Hysteresis (Note 8)	—	—	20	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP62200 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.)

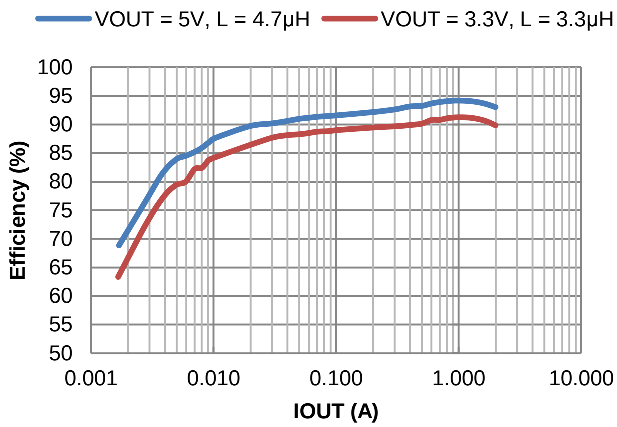


Figure 4. Efficiency vs. Output Current, VIN = 12V

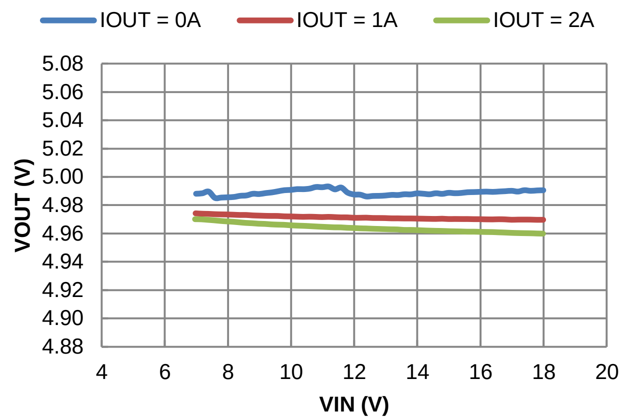


Figure 5. Line Regulation

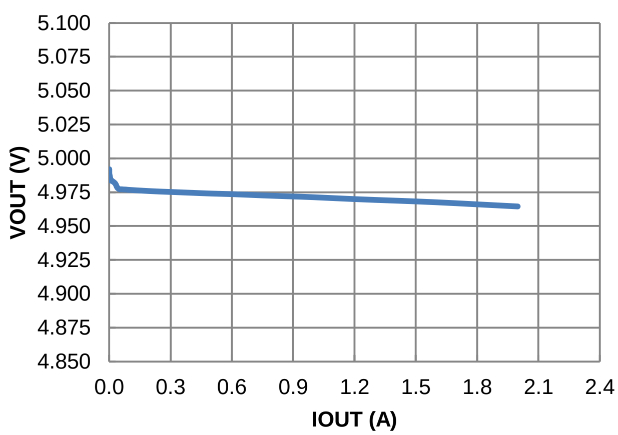


Figure 6. Load Regulation

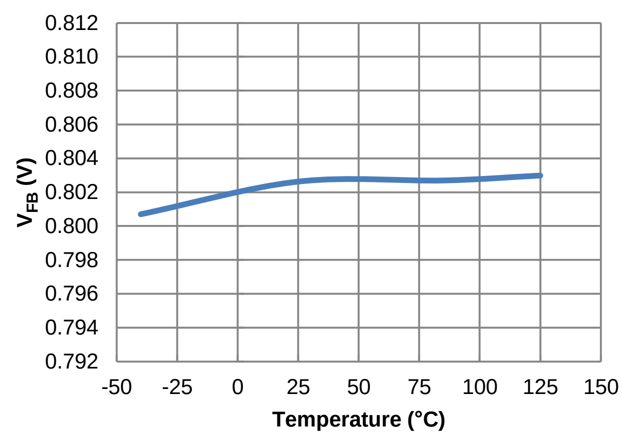


Figure 7. Feedback Voltage vs. Temperature

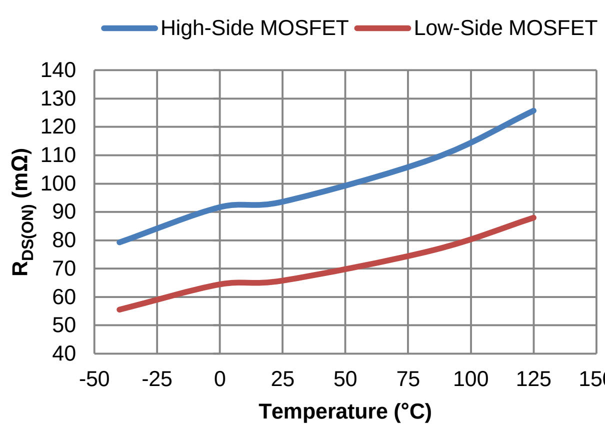


Figure 8. Power MOSFET $R_{DS(ON)}$ vs. Temperature

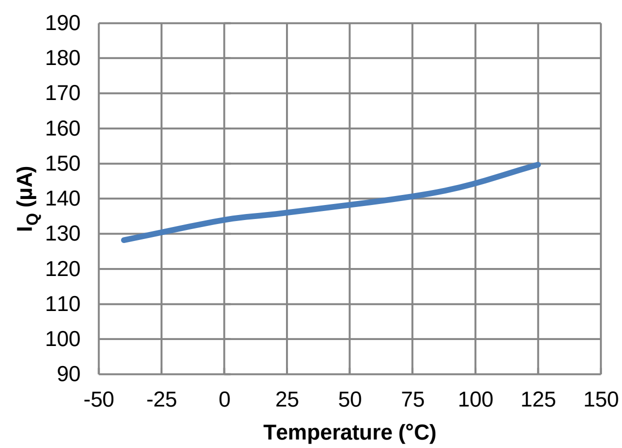


Figure 9. I_Q vs. Temperature

Typical Performance Characteristics (AP62200 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.)
(continued)

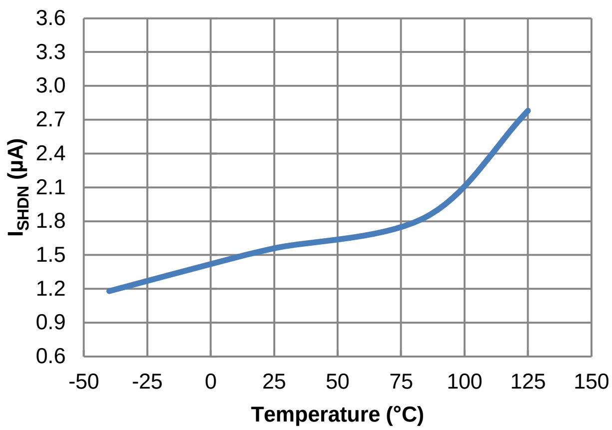


Figure 10. I_{SHDN} vs. Temperature

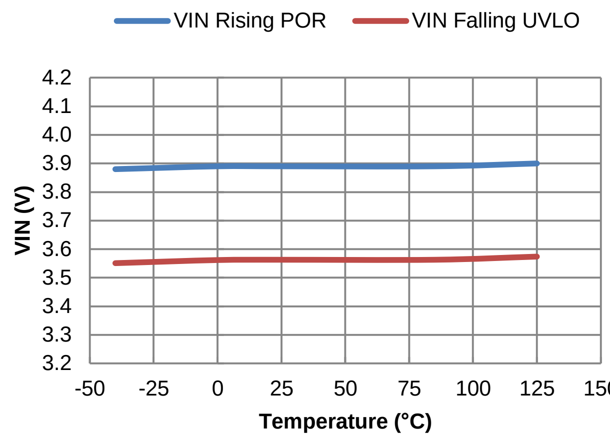


Figure 11. VIN Power-On Reset and UVLO vs. Temperature

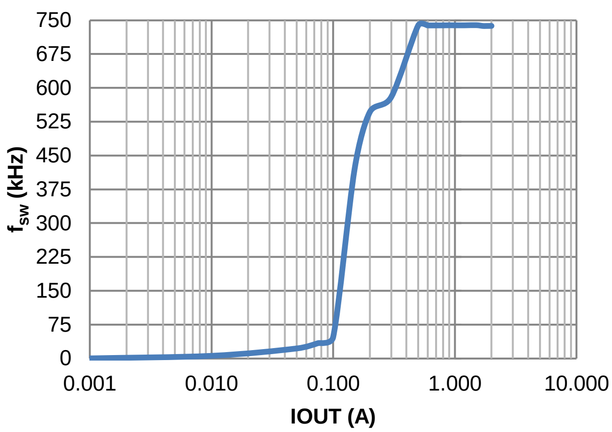


Figure 12. f_{SW} vs. Load

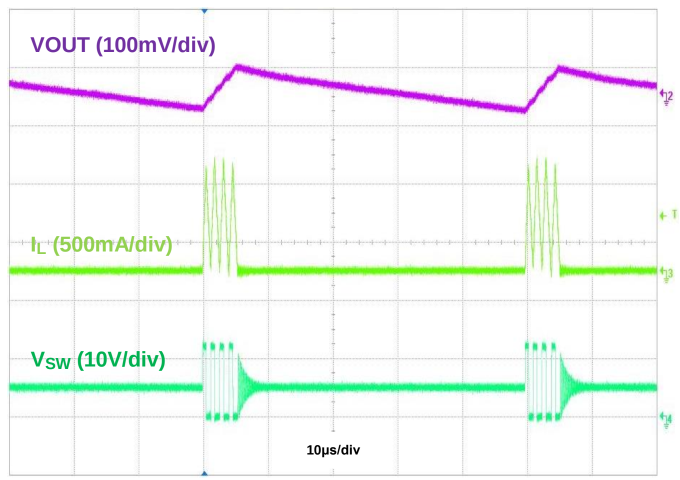


Figure 13. Output Voltage Ripple, IOUT = 50mA

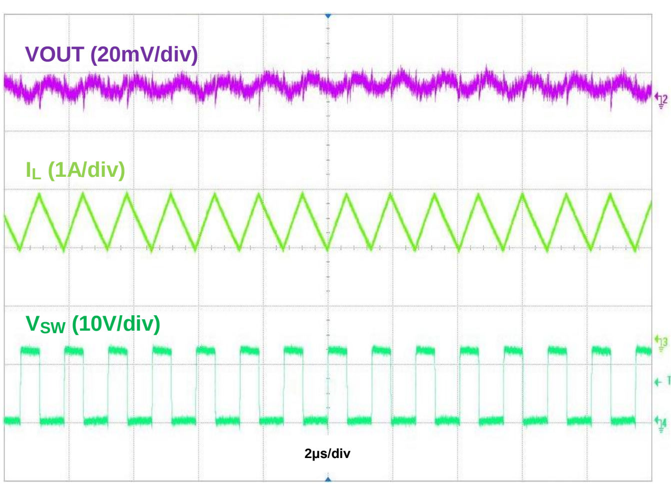


Figure 14. Output Voltage Ripple, IOUT = 2A

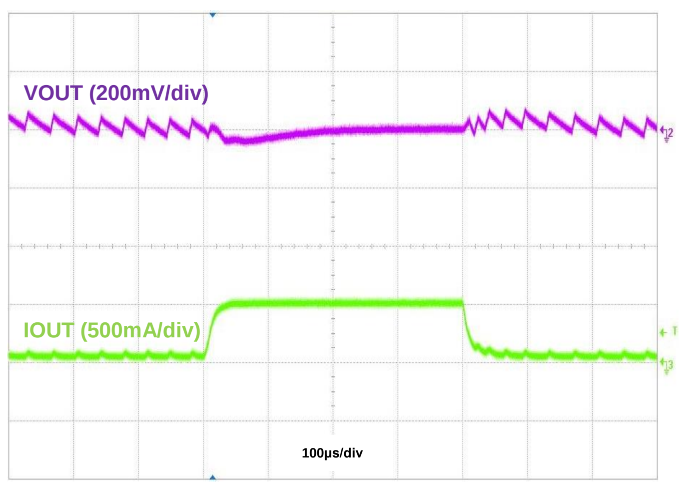


Figure 15. Load Transient, IOUT = 50mA to 500mA to 50mA

Typical Performance Characteristics (AP62200 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.) (cont.)

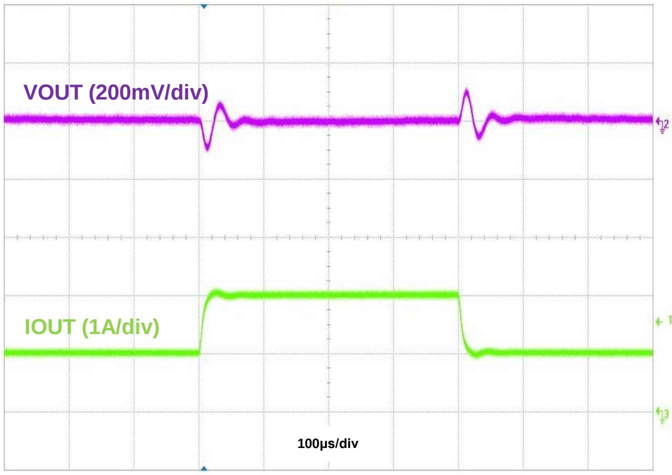


Figure 16. Load Transient, IOUT = 1A to 2A to 1A

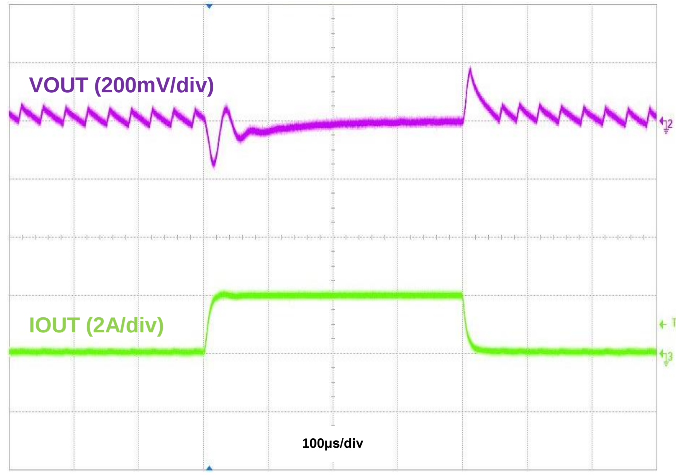


Figure 17. Load Transient, IOUT = 50mA to 2A to 50mA

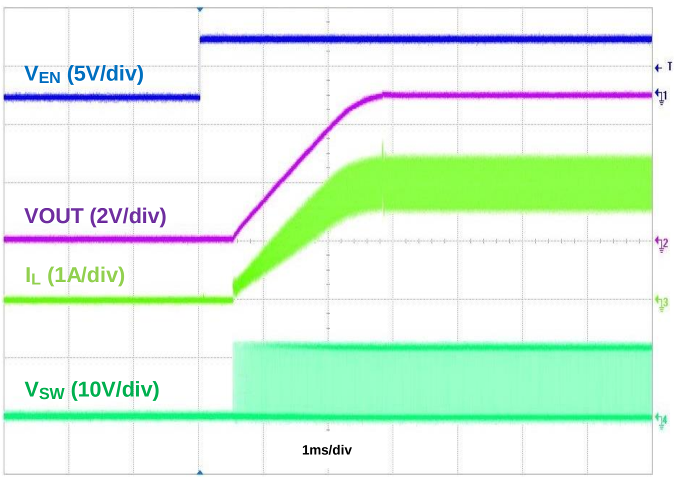


Figure 18. Startup Using EN, IOUT = 2A

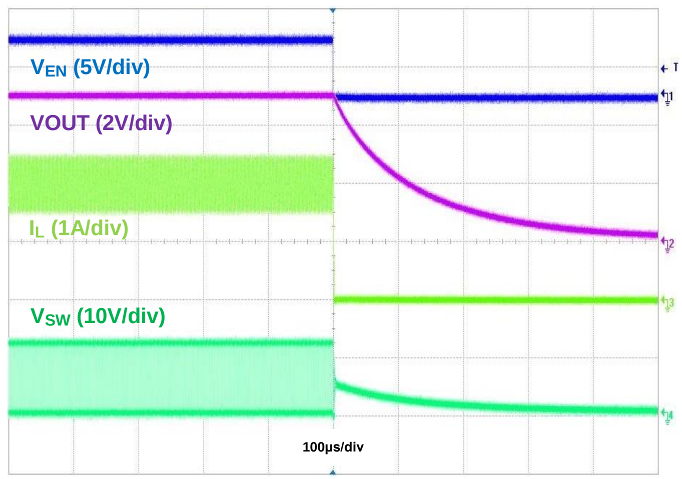


Figure 19. Shutdown Using EN, IOUT = 2A

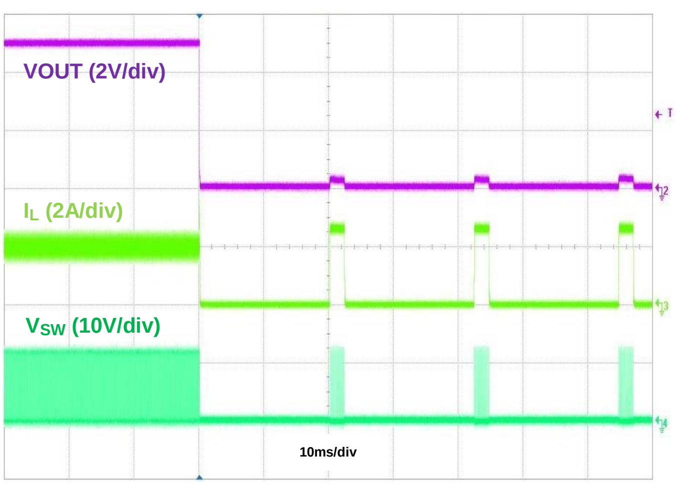


Figure 20. Output Short Protection, IOUT = 2A

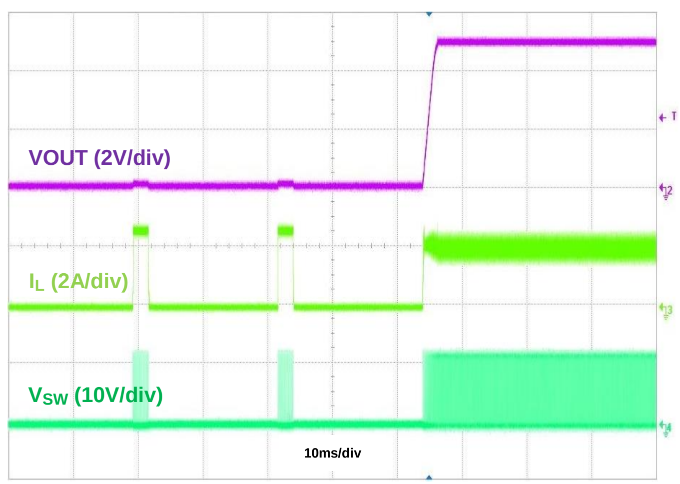


Figure 21. Output Short Recovery, IOUT = 2A

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP62200 device is a 4.2V-to-18V input, 2A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 3. The device employs constant on-time control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the one-shot pulse turns on the high-side power MOSFET, Q1, for a fixed on-time, t_{ON}. This one-shot on-pulse timing is calculated by the converter's input voltage and output voltage to maintain a pseudo-fixed frequency over the input voltage range. When Q1 is on, the inductor current rises linearly, and the device charges the output capacitor. Q1 turns off after the fixed on-time expires, and the low-side power MOSFET, Q2, turns on. Once the output voltage drops below the output regulation, Q2 is turned off. The one-shot timer is then reset and Q1 turns on again. The on-time is inversely proportional to the input voltage and directly proportional to the output voltage. It is calculated by the following equation:

$$\mathbf{t_{ON}} = \frac{\mathbf{VOUT}}{\mathbf{VIN \cdot f_{sw}}} \quad \textbf{Eq. 1}$$

Where:

- VIN is the input voltage
- VOUT is the output voltage
- f_{sw} is the switching frequency

The off-time duration is t_{OFF} and starts after the on-time expires. The off-time expires when the feedback voltage decreases below the reference voltage, which then triggers the on-time duration to start again. If the off-time becomes shorter than the minimum off-time, t_{OFF_MIN}, then the switching period extends on the next cycle to maintain regulation. The minimum off-time is 220ns (typical).

2 Pulse Frequency Modulation (PFM) Operation

AP62200 enters PFM operation at light load conditions for high efficiency. During light load conditions, the regulator automatically reduces the switching frequency. As the output current decreases, so too does the inductor current. The inductor current, I_L, eventually reaches 0A, marking the boundary between Continuous Conduction Mode (CCM) and Discontinuous Condition Mode (DCM). During this time, both Q1 and Q2 are off, and the load current is provided only by the output capacitor. When V_{FB} becomes lower than 0.8V, the next cycle begins, and Q1 turns on. Because the AP62200 works in PFM during light load conditions, it can achieve power efficiency of up to 84% at a 5mA load condition.

Likewise, as the output load increases from light load to heavy load, the switching frequency increases to maintain the regulation of the output voltage. The transition point between light and heavy load conditions can be calculated using the following equation:

$$\mathbf{I_{LOAD}} = \left(\frac{\mathbf{VIN - VOUT}}{\mathbf{2L}}\right) \cdot \mathbf{t_{ON}} \quad \textbf{Eq. 2}$$

Where:

- L is the inductor value

The quiescent current of AP62200 is 135µA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device's shutdown supply current is only 1µA. When applying a voltage higher than the EN upper threshold (typical 1.18V, rising), the AP62200 enables all functions, and the device initiates the soft-start phase. An internal 1.5µA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the EN upper threshold is reached. The AP62200 has a built-in 2.5ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its lower threshold (typical 1.1V, falling), the internal SS voltage is discharged to ground, and device operation is disabled.

The EN pin can also be used to program the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Alternatively, a small ceramic capacitor can be added from EN to GND. This delays the triggering of EN, which delays the startup of the output voltage. This is useful when sequencing multiple power rails to minimize input inrush current. The amount of capacitance is calculated by:

$$\mathbf{C_d[nF] = 1.27 \cdot t_d[ms]} \quad \textbf{Eq. 3}$$

Where:

- C_d is the time delay capacitance in nF
- t_d is the delay time in ms

Application Information (continued)

4 EMI Reduction with Ringing-free Switching Node

In buck converters, the switching node's (SW's) ringing amplitude and cycles are critical, especially in relation to the high frequency radiated EMI noise. The AP62200 device implements a multi-level gate driver scheme to achieve a ringing-free switching node without sacrificing neither the switching node's rise and fall slew rates nor the converter's power efficiency.

5 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP62200 device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. If the input voltage falls below 3.7V, the AP62200 is disabled. In this event, both the high-side and low-side power MOSFETs are turned off.

For applications requiring a higher VIN UVLO voltage than is provided by the default setup, a 5.5µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO voltage as shown in Figure 22.

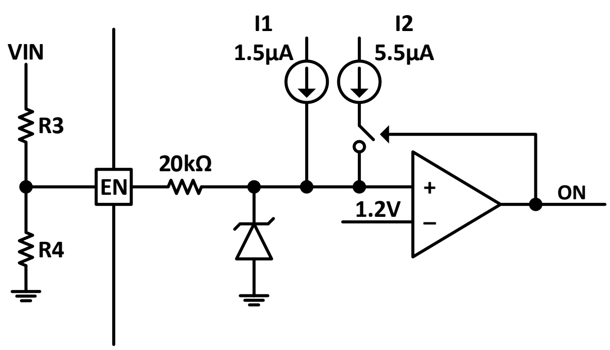


Figure 22. Programming UVLO

The resistive divider's resistor values are calculated by:

$$\mathbf{R3} = \frac{\mathbf{0.917 \cdot V_{ON} - V_{OFF}}}{\mathbf{5.625\mu A}} \quad \textbf{Eq. 4}$$

$$\mathbf{R4} = \frac{\mathbf{1.1 \cdot R3}}{\mathbf{V_{OFF} - 1.1V + 7\mu A \cdot R3}} \quad \textbf{Eq. 5}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 4.15V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 3.85V

6 Overcurrent Protection (OCP)

The AP62200 has cycle-by-cycle valley current limit protection by sensing the current through the internal low-side power MOSFET, Q2. While Q2 is on, its conduction current is monitored by the internal sensing circuitry. The overcurrent limit has a corresponding voltage limit, V_{LIMIT}. When the voltage between GND and SW is lower than V_{LIMIT} due to excessive current through Q2, the OCP triggers, and the controller turns off Q2. During this time, both Q1 and Q2 remain off. A new switching cycle begins only when the voltage between GND and SW rises above V_{LIMIT}. If Q2 consistently hits the valley current limit for 2.5ms, the buck converter enters hiccup mode and shuts down. After 20ms of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

Because the $R_{DS(ON)}$ values of the power MOSFETs increase with temperature, V_{LIMIT} has a temperature coefficient of 0.4%/°C to compensate for the temperature dependency of $R_{DS(ON)}$.

7 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of 155°C, the AP62200 shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (135°C typical), the device initiates a normal power-up cycle with soft-start.

Application Information (cont.)

8 Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})} \qquad \textbf{Eq. 6}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}} \qquad \textbf{Eq. 7}$$

Where:

- T_A is the ambient temperature of the environment

For the SOT563 and TSOT26 packages, the θ_{JA} is 110°C/W and 70°C/W, respectively. The actual junction temperature should not exceed the maximum recommended operating junction temperature of 125°C when considering the thermal design. Typical derating curves versus ambient temperature are shown in the figures below.

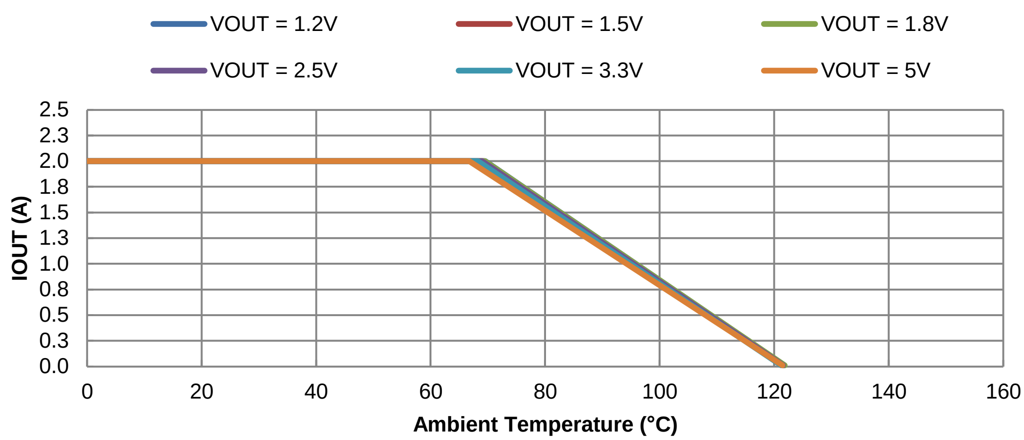


Figure 23. Output Current Derating Curve vs. Ambient Temperature, SOT563 Package, VIN = 12V

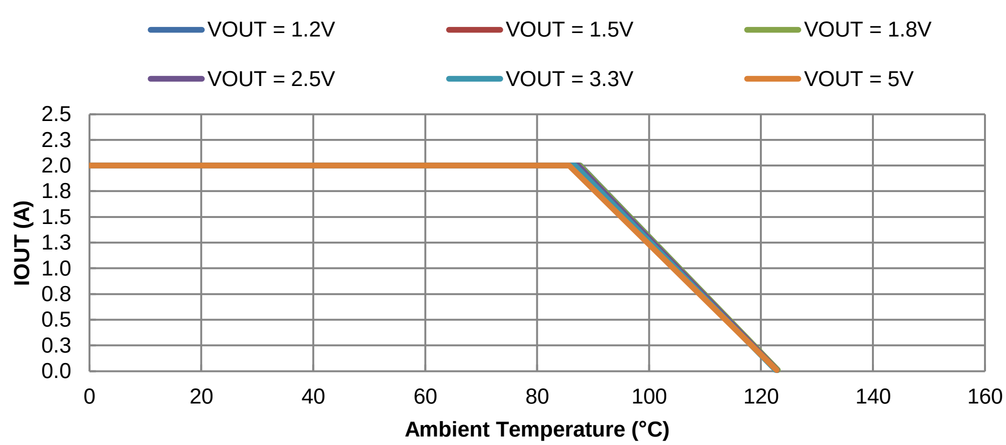


Figure 24. Output Current Derating Curve vs. Ambient Temperature, TSOT26 Package, VIN = 12V

Application Information (cont.)

9 Setting the Output Voltage

The AP62200 has adjustable output voltages starting from 0.8V using an external resistive divider. The resistor values of the feedback network are selected based on a design tradeoff between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{0.8V} - 1\right)} \quad \text{Eq. 8}$$

Table 1 shows a list of recommended component selections for common output voltages for AP62200 referencing Figure 1. Consult Diodes Incorporated for other output voltage requirements.

Table 1. Recommended Component Selections

AP62200						
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (µH)**	**C1 (µF)**	**C2 (µF)**	**C3 (nF)**
1.2	11.0	22.1	2.2	10	2 x 22	100
1.5	19.1	22.1	2.2	10	2 x 22	100
1.8	27.4	22.1	3.3	10	2 x 22	100
2.5	47.5	22.1	3.3	10	2 x 22	100
3.3	69.8	22.1	3.3	10	2 x 22	100
5.0	115.0	22.1	4.7	10	2 x 22	100

10 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{sw}}} \quad \text{Eq. 9}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP62200, choose ΔI_L to be 30% to 50% of the maximum load current of 2A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \quad \text{Eq. 10}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 1.2µH to 4.7µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 50mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (cont.)

11 Input Capacitor

The input capacitor reduces the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If a tantalum capacitor is used it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor greater than 10µF is sufficient for most applications.

12 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and sets the off-time to minimum to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and increases the off-time to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{sw}} \cdot \mathbf{COUT}}\right) \qquad \textbf{Eq. 11}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})}\right) \qquad \textbf{Eq. 12}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

13 Bootstrap Capacitor

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins. A 100nF ceramic capacitor is sufficient.

Layout

PCB Layout

1. The AP62200 works at 2A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See the figures below for more details.

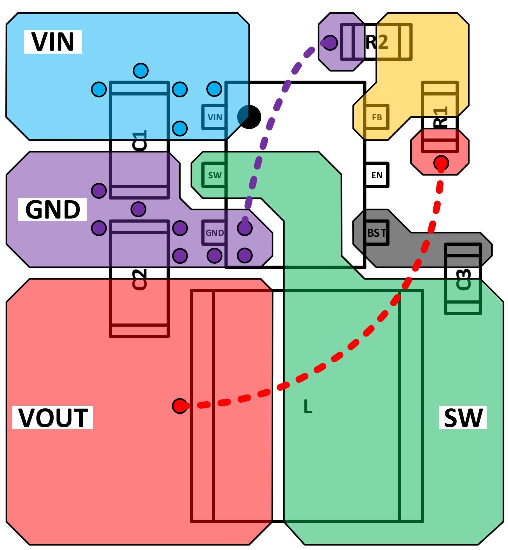


Figure 25. Recommended PCB Layout for SOT563 Package

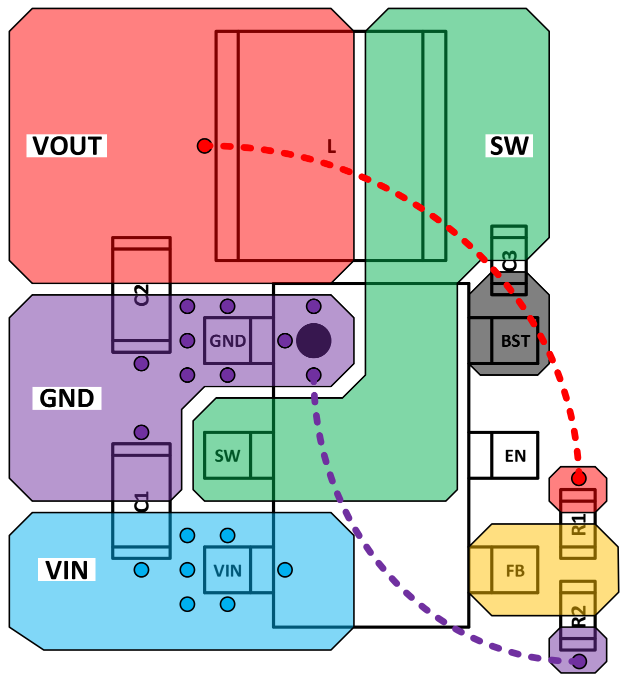
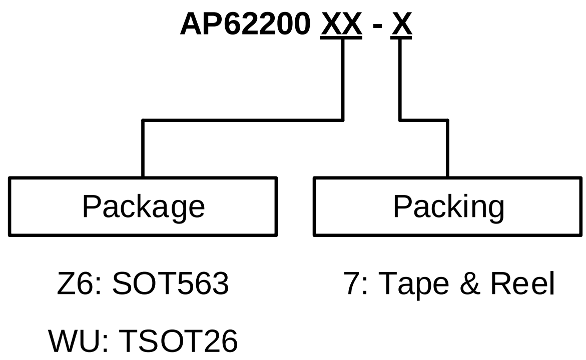


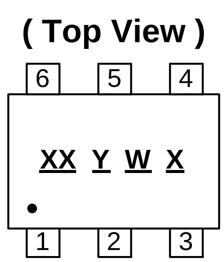
Figure 26. Recommended PCB Layout for TSOT26 Package

Ordering Information



Part Number	Package Code	Tape and Reel	
		Quantity	Part Number Suffix
AP62200Z6-7	Z6	3000	-7
AP62200WU-7	WU	3000	-7

Marking Information



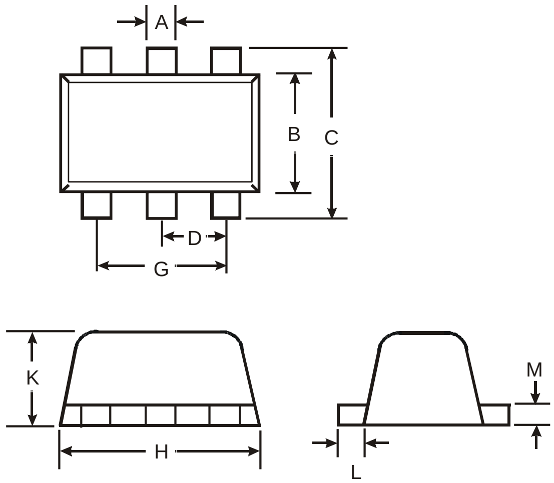
XX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP62200Z6-7	SOT563	HA
AP62200WU-7	TSOT26	HB

Package Outline Dimensions

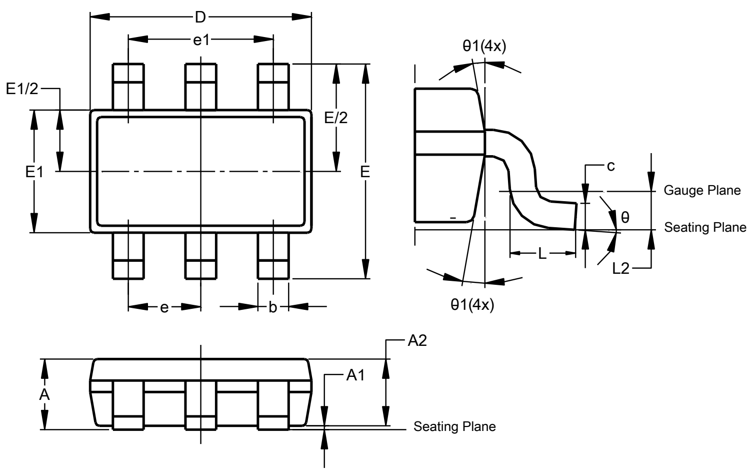
Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563



SOT563			
Dim	**Min**	**Max**	**Typ**
A	0.15	0.30	0.20
B	1.10	1.25	1.20
C	1.55	1.70	1.60
D	—	—	0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
K	0.55	0.60	0.60
L	0.10	0.30	0.20
M	0.10	0.18	0.11
All Dimensions in mm			

TSOT26

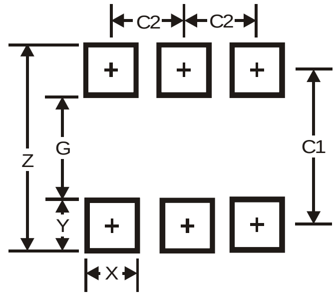


TSOT26			
Dim	**Min**	**Max**	**Typ**
A	—	1.00	—
A1	0.010	0.100	—
A2	0.840	0.900	—
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	—
c	0.120	0.200	—
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	—
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	—
All Dimensions in mm			

Suggested Pad Layout

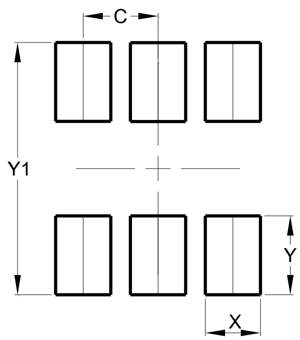
Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563



Dimensions	Value (in mm)
Z	2.2
G	1.2
X	0.375
Y	0.5
C1	1.7
C2	0.5

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com