HIGH-VOLTAGE USB PD VBUS SINK PATH POWER SWITCH

Description

The AP22950 is a uni-directional high-voltage power switch for USB PD featuring undervoltage lockout, overvoltage lockout, reverse current protection and overtemperature protection circuits.

The AP22950 features a low 30mΩ on-resistance and operates from 2.5V to 22.5V VBUS input voltage.

The reverse current protection features isolation from higher VINT than VBUS that allows supplying internal system power node from the highest voltage from multiple AP22950 that are connected together, which is suitable for portable devices that have multiple power inputs.

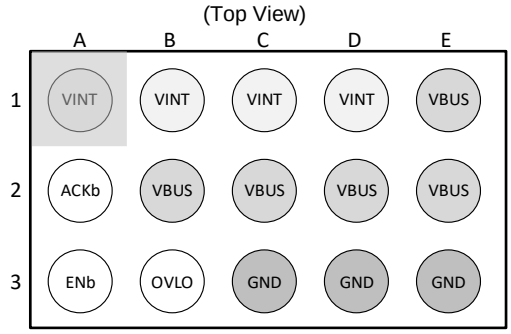
The AP22950 offers default 23V overvoltage protection threshold by default without resistor on OVLO and the threshold is adjustable from 4.0V to 23V by external resistor on OVLO pin. ACKb pin can be VBUS voltage status indicator.

The AP22950 is available in the U-WLB2515-15 package.

Applications

- Laptops and accessories
- Smartphones, tablet PCs
- Portable speakers, wearable devices

Pin Assignments



U-WLB2515-15

Features

- Wide Input-Voltage Range from 2.5V to 22.5V Complies with SPR (Standard Power Rating) Requirement of USB PD 3.X
- I_{SW} Maximum 5A Continuous Current
- 29V Tolerance on Both VBUS and VINT Pin
- 30mΩ Low ON Resistance
- Adjustable VBUS Overvoltage Protection Threshold
- Slew Rate Control for Inrush Current Limit
- Protection Features:
  - Thermal Shutdown (Overtemperature Protection)
  - Overvoltage Protection
  - Undervoltage Lockout
  - Reverse Current Protection
- Surge/ESD Protection:
  - IEC61000-4-5 Exceeds ±100V on VBUS Without Capacitor
  - IEC61000-4-5 Exceeds ±110V on VBUS with 22µF Capacitor
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit – Multi USB-C Ports

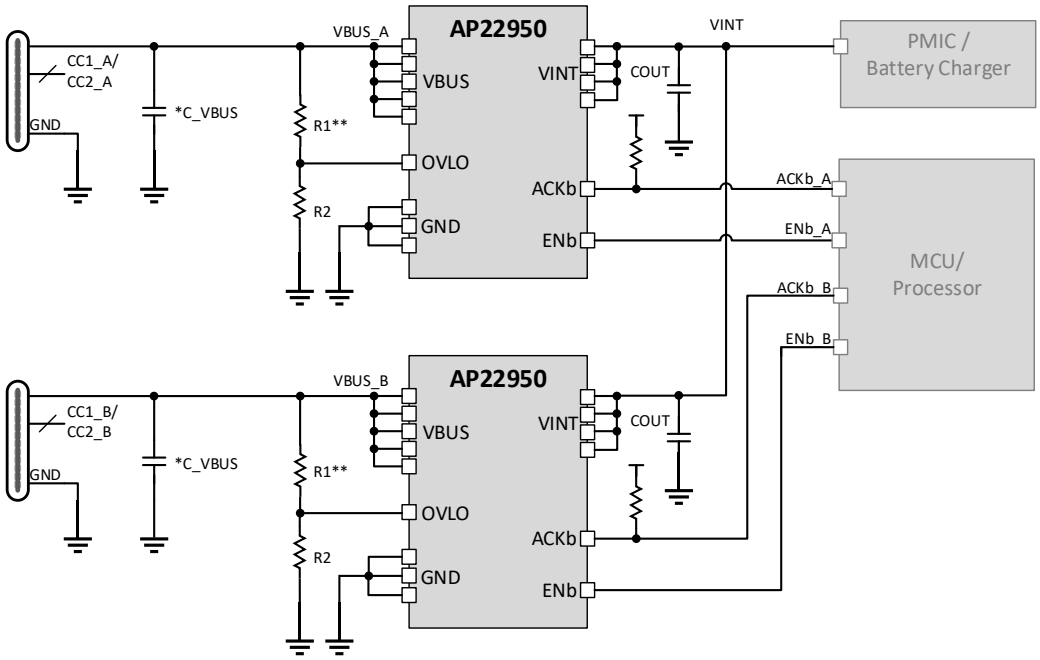


Figure 1. Typical Application Diagram - Multi USB-C® Ports

Notes: *C_VBUS requires larger than 22µF capacitance for 110V surge protection.
** R1 is recommended to use minimum 1MΩ.

Pin Descriptions

Pin Name	Pin Number	Type	Function
VBUS	B2, C2, D2, E1, E2	Power	Power Input
VINT	A1, B1, C1, D1	Power	Power Output
OVLO	B3	Input	Overvoltage threshold adjustment by external resistor (Default 23V if OVLO = GND)
ACKb	A2	Open Drain Output	Power-Good Acknowledge (Output Low for valid VBUS input)
GND	C3, D3, E3	Power	Gate driver out pin. Connects to gate of external MOSFET
ENb	A3	Input	Enable Control (Active Low)

Functional Block Diagram

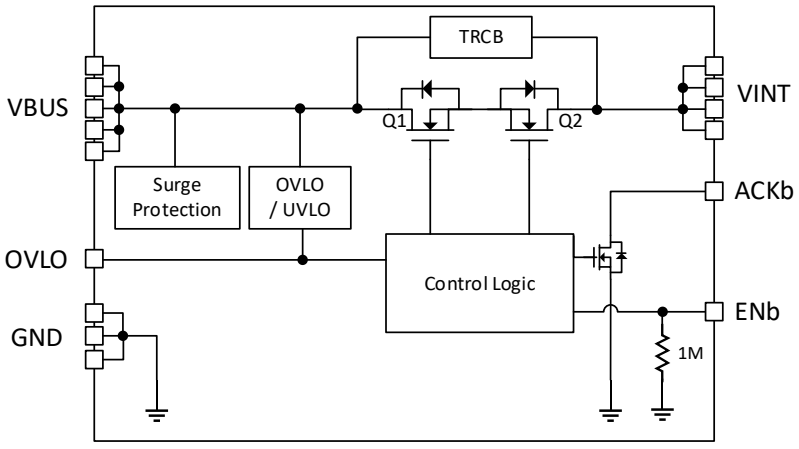


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter		Ratings	Unit
ESD HBM	Human Body ESD Protection		4	kV
ESD CDM	Charged Device Model ESD Protection		1	kV
VBUS	Input Voltage at VBUS		-0.5 to 29	V
VINT	Input Voltage at VINT		-0.5 to 29	V
ENb	Enable Control Input (Active Low)		-0.5 to 29	V
ACKb	Power-Good Acknowledge (Active Low)		-0.5 to 6	V
OVLO	OVLO Threshold Adjustment		-0.5 to VBUS	V
I_{SW}	Maximum Continuous Switch Current	T_A = +85°C	5.0	A
		T_A = +105°C	3.5	A
$T_{J(max)}$	Maximum Junction Temperature		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C

Note: 4. Stresses greater than *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

Package Thermal Information (Note 5)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	60.3	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	12.2	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	6.2	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	0.26	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	5.81	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	6.67	°C/W

Note: 5. $R_{\theta JA}$ and $R_{\theta JC}$ are measured at T_A = +25°C on a highly effective thermal conductivity four-layer test board per JEDEC 51-7.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Min	Max	Unit
VBUS	Input Voltage at VBUS		2.5	22.5	V
VINT	Input Voltage at VINT		0	22.5	V
ACKb	Power-Good Acknowledge Pullup Voltage		0	5.5	V
ENb	Enable Control		0	20	V
C_{IN}	Input Capacitance on VBUS (Note 6)	For IEC61000-4-5, 110V	22	—	µF
		For IEC61000-4-5, 100V	1	—	µF
C_{OUT}	Output Capacitance on VINT (Note 6)		10	1000	µF
T_J	Operating Junction Temperature		-40	+125	°C
T_A	Operating Ambient Temperature		-40	+85	°C

Note: 6. Refer to the typical application circuit.

Electrical Characteristics (T_J = -40°C to +85°C, VBUS = 2.5V to 22.5V, typical values are at VBUS = 5V and T_J = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBUS/VINT						
V_{BUS_CLAMP}	VBUS Clamp Voltage	I_{VBUS} = 10mA, T_A = +25°C	—	32	—	V
V_{UVLO}	UVLO Release Voltage	ENb = GND	2.0	2.3	2.5	V
V_{HYS_UVLO}	UVLO Hysteresis Voltage	Hysteresis of VBUS UVLO enter/release, ENb = GND $V_{UVLO\_Enter} = V_{UVLO} - V_{HYS\_UVLO}$	—	100	—	mV
I_Q	VBUS Quiescent Current	ENb = GND, VBUS = 5V, I_{LOAD} = 0mA	—	70	95	µA
		ENb = GND, VBUS = 20V, I_{LOAD} = 0mA	—	100	140	µA
I_{Q_SD}	VBUS Shutdown Current	ENb = High, VBUS = 5V, I_{LOAD} = 0mA	—	5	10	µA
		ENb = High, VBUS = 20V, I_{LOAD} = 0mA	—	15	30	µA
I_{OFF_VBUS}	VBUS Off Leakage Current	ENb = High, VBUS = 5V, VINT = GND	—	5	10	µA
		ENb = High, VBUS = 20V, VINT = GND	—	15	30	µA
I_{OFF_VINT}	VINT Off Leakage Current	ENb = High, VINT = 5V, VBUS = GND	—	1	5	µA
		ENb = High, VINT = 20V, VBUS = GND	—	4	16	µA
ENb Input						
V_{IL_ENb}	Enable Input Logic-Low	VBUS = 2.5V to 20V	—	—	0.4	V
V_{IH_ENb}	Enable Input Logic-High	VBUS = 2.5V to 20V	1.2	—	—	V
C_{IN_ENb}	Input Capacitance	VBUS = 5.0V	—	4.5	—	pF
$R_{PULL\_DOWN\_ENb}$	Internal Pulldown Resistance	—	—	1	—	MΩ
ACKb Output						
V_{OL_ACK}	ACKb Output Logic-Low	IO = 8mA; VBUS = 2.5V to 20V	—	—	500	mV
OVLO						
V_{OVLO_TH}	OVLO Set Voltage Threshold	ENb = GND	1.164	1.227	1.287	V
$V_{OVLO\_DEF\_RISING}$	Default OVLO Rising Threshold	OVLO = GND	—	23	—	V
$V_{OVLO\_DEF\_FALLING}$	Default OVLO Falling Threshold	OVLO = GND	—	22.5	—	V
I_{IN_OVLO}	OVLO Input Leakage Current	$V_{OVLO} = V_{OVLO\_TH}$	—	—	50	nA
Switch						
R_{ON_5V}	On Resistance	I_{LOAD} = 1A, VBUS = 5.0V	—	30	—	mΩ
R_{ON_20V}	On Resistance	I_{LOAD} = 1A, VBUS = 20.0V	—	30	—	mΩ
Reverse Current Protection						
V_{RCP_TRIG}	RCP Triggering Voltage	V_{RCP_TRIG} = VINT - VBUS	—	45	—	mV
V_{FRCP_TRIG}	Fast RCP Triggering Voltage to Turn Off Switch Without Deglitch Time	$V_{F\_RCP\_TRIG}$ = VINT - VBUS	—	120	—	mV
$V_{RCP\_RECOVERY}$	RCP Recovery Voltage	$V_{RCP\_RECOVERY}$ = VBUS - VINT	—	70	—	mV

Electrical Characteristics (T_J = -40°C to +85°C, VBUS = 2.5V to 22.5V, typical values are at VBUS = 5V and T_J = +25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing Characteristics						
t_{EN}	Enable Delay Includes 15ms of Debounce Time	Timing from ENb = Low or V_{UVLO} < VBUS < V_{OVLO} to VINT = 10% of VBUS VBUS = 5.0V, C_{LOAD} = 100µF, R_{LOAD} = 100Ω	—	21.9	—	ms
t_{RISE_5V}	VINT Rising Time at VBUS = 5.0V	VINT from 10% to 90% of VBUS, C_{LOAD} = 100µF, R_{LOAD} = 100Ω	—	3.4	—	ms
t_{RISE_20V}	VINT Rising Time at VBUS = 20.0V	VINT from 10% to 90% of VBUS, C_{LOAD} = 100µF, R_{LOAD} = 100Ω	—	6.9	—	ms
t_{OFF}	Switch Off Delay	Timing from ENb = High to VINT = 10% of VBUS, VBUS = 5.0V, C_{LOAD} = 100µF, R_{LOAD} = 100Ω	—	23	—	ms
t_{OVP}	OVP Switch Off Time	Timing from VBUS > $V_{OVLO\_DEF\_RISING}$ to VINT = 80% of VBUS, VBUS = 5.0V, C_{LOAD} = 0µF, R_{LOAD} = 100Ω, OVLO = GND	—	100	—	ns
$t_{RCP\_DEGLITCH}$	RCP Deglitch Time	Timing from VINT > VBUS + V_{RCP_TRIG} to Starting t_{RCP_OFF} for switch off	2.6	3.7	5.0	ms
t_{RCP_OFF}	RCP Switch Off Time	Timing from VINT > VBUS + V_{FRCP_TRIG} to switch off	—	10	—	µs
$t_{RCP\_RELEASE}$	RCP Release Time	Timing from VINT < VBUS - $V_{RCP\_RECOVERY}$ to switch on	—	10	—	µs
Thermal Protection						
T_{SD}	Thermal Shutdown	—	—	+150	—	°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	—	—	+20	—	°C

Typical Timing Characteristics

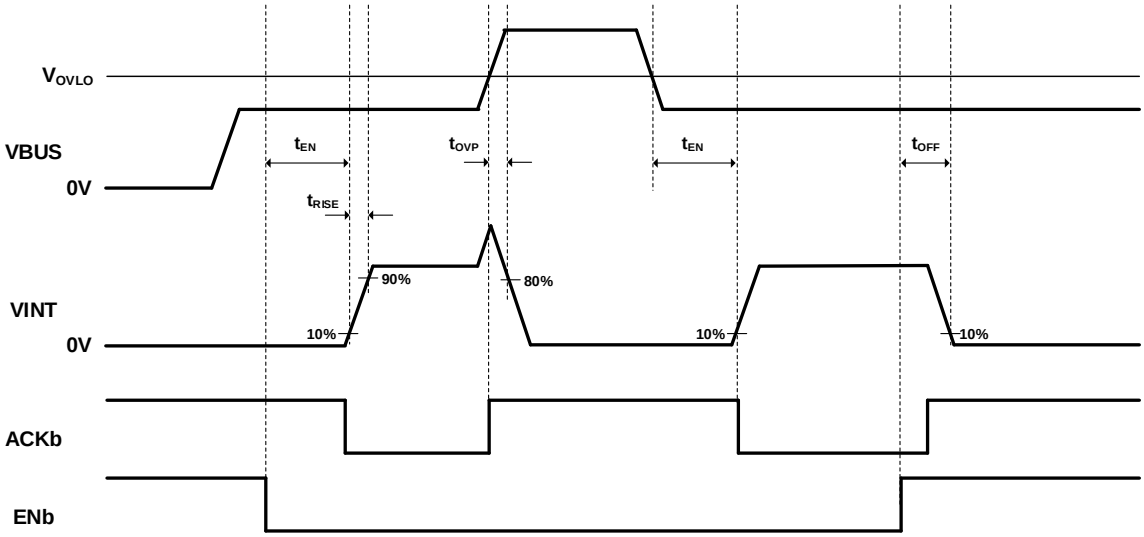


Figure 3. Timing Diagram: Overvoltage Protection, Turn On/Off

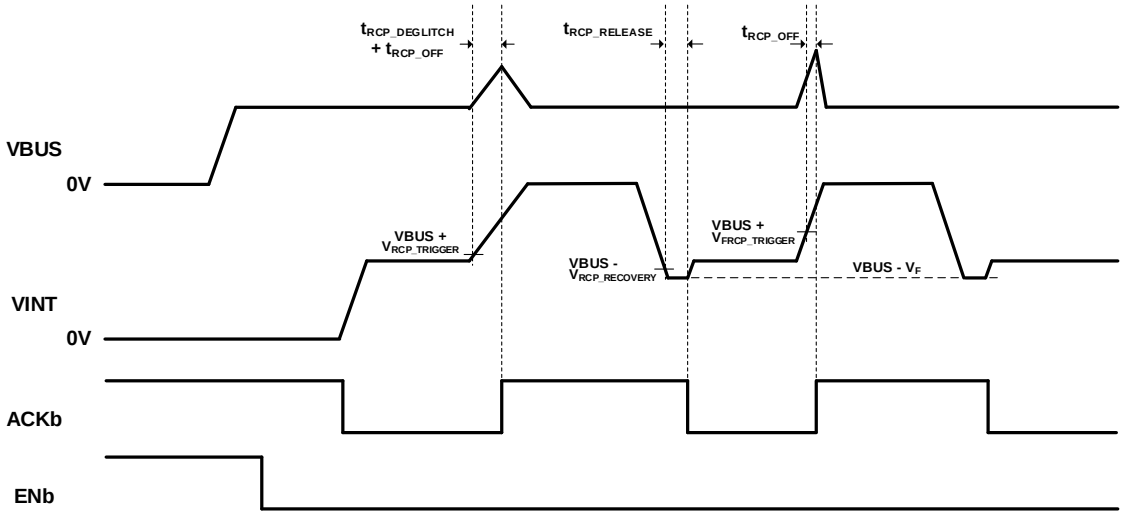


Figure 4. Timing Diagram: Reverse Current Protection

Application Information

Enable/Disable Control

The ENb pin controls the state of the power switch. Logic-high on ENb disables AP22950 and the AP22950 is enabled when the ENb pin is asserted low. The built-in 1MΩ pulldown resistor on ENb pin ensures AP22950 stays in conduction mode even if entire system is in a dead battery or depleted battery condition. A 15ms debounce timer filters out glitch on control signal that prevent from fault enable.

Input/Output Capacitor

The AP22950 has a built-in circuit for surge protection. This circuitry requires an external 22µF capacitor on VBUS pin for 110V surge protection and 100V surge protection is achievable without 22µF capacitor. Minimum 1µF capacitor is required and placed as close as possible to the VBUS pin and GND to minimize parasitic effect. Minimum 1µF capacitor on VINT pin is required.

Undervoltage Lockout

When ENb is low and VBUS < VUVLO, the undervoltage lockout (UVLO) detection circuits disable the AP22950. Once VBUS exceeds VUVLO and there is no other protection circuit is triggered, the AP22950 is controlled by the ENb pin.

Overvoltage Lockout

When ENb is low and VBUS > $V_{OVLO\_DEF\_RISING}$ (If OVLO = GND or < 0.1V) or OVLO > $OVLO_{TH}$, the overvoltage lockout (OVLO) circuit disables the AP22950 and ACKb asserts Hi-Z state. Once VBUS < $V_{OVLO\_DEF\_RISING}$ (If OVLO = GND or < 0.1V) or OVLO < $VOVLO_{TH}$ and no other protection circuit is triggered, the AP22950 resumes normal operation.

The OVLO pin is used to configure the overvoltage threshold. The default overvoltage threshold is 23V when OVLO pin shorts to GND (OVLO < 0.1V). Connecting a resistor divider to the OVLO pin adjusts the overvoltage threshold from 4V to 23V using the equation below.

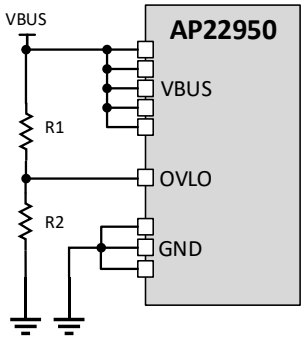


Figure 5. OVLO External Resistor Configuration

$$VOVLO = VOVLOth \times \frac{R1 + R2}{R2}$$

Note: V_{OVLO_TH} (typ) = 1.227V

R1 is recommended to use minimum 1MΩ.

Overtemperature Protection

When EN is low and the device temperature reaches T_{SD} (typ +150°C), the overtemperature protection (OTP) circuit disables the AP22950 and asserts the ACKb output Hi-Z. Once the device temperature decreases below T_{SD} - T_{SD_HYS} (120°C = 150°C - 30°C) and no other protection circuit is active, the AP22950 returns back to normal operation being controlled by the ENb pin status.

Acknowledge Flag Output (ACKb)

The ACKb output is an open-drain output that requires an external pullup resistor. The ACKb pin indicates the state of the power switch. When no fault condition is triggered and power switch is conducting, ACKb asserts output low; otherwise it stays Hi-Z state. 10kΩ to 200kΩ of external pullup resistor is recommended.

Application Information (continued)

Reverse Current Protection

The AP22950 monitors voltage difference between VBUS and VINT. Once V_{RCP_TRIG} (typ 45mV) < VINT - VBUS < V_{FRCP_TRIG} (typ 120mV), control logic turn Q2 switch by internal reverse current protection circuit trigger after $t_{RCP\_DEGLITCH}$ (typ 3.7ms) and the control logic turn Q2 switch off immediately if VINT - VBUS > V_{FRCP_TRIG} (120mV) by fast reverse current protection circuit.

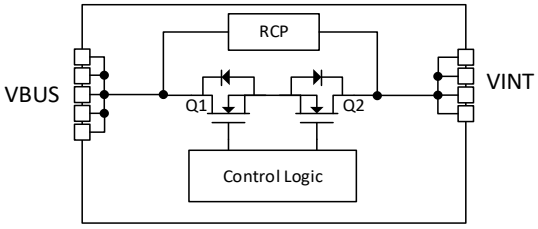


Figure 6. Power Switch Block

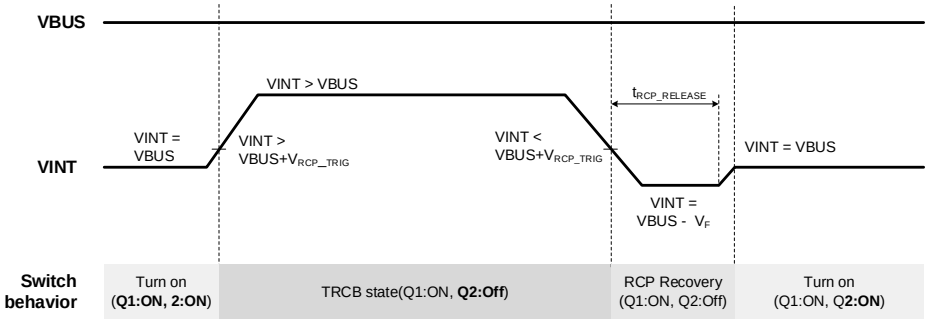


Figure 7. Switch Behavior in RCP Operation

In the multi-port system application, while Q2 switch is off, VBUS is able to supply VINT whenever VINT becomes lower than VBUS through Q2 body diode path. This is to prevent a portable system from losing system power supply when the first high-voltage charger is plugged out while the second high-voltage charger remains plugged in. System shall stay in operation mode upon any plugging in and out any port occurs as long as one port has plugged-in charger.

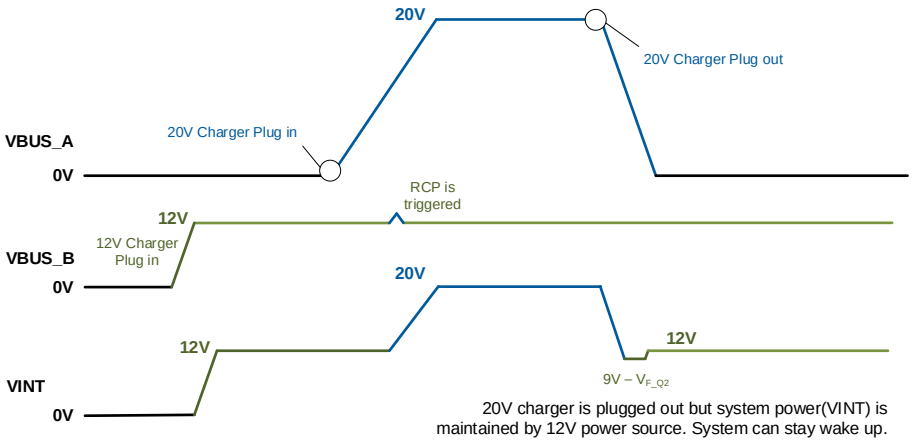
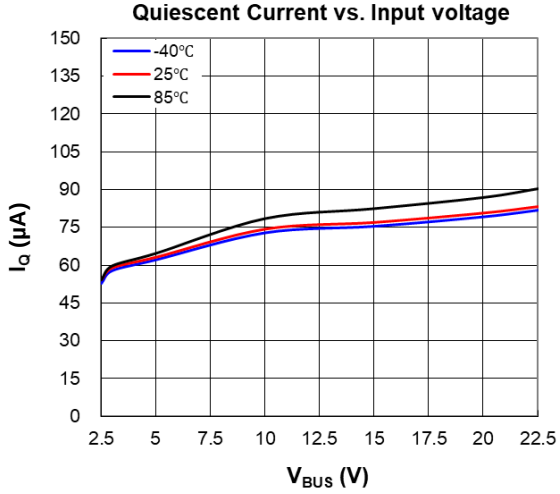


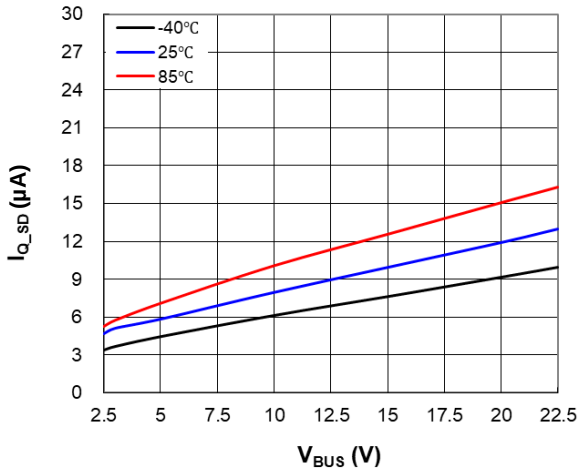
Figure 8. VINT Power Transition in Multi-Ports System

Typical Performance Characteristics (T_J = -40°C to +85°C, VBUS = 2.5V to 22.5V, typical values are at VBUS = 5V and T_J = +25°C, unless otherwise specified.)

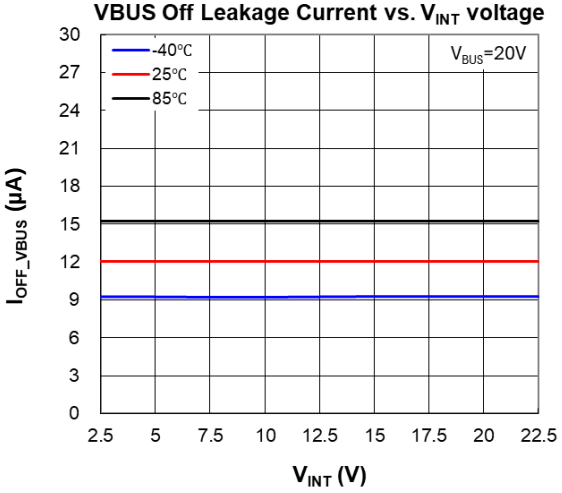
Quiescent Current vs. Input voltage



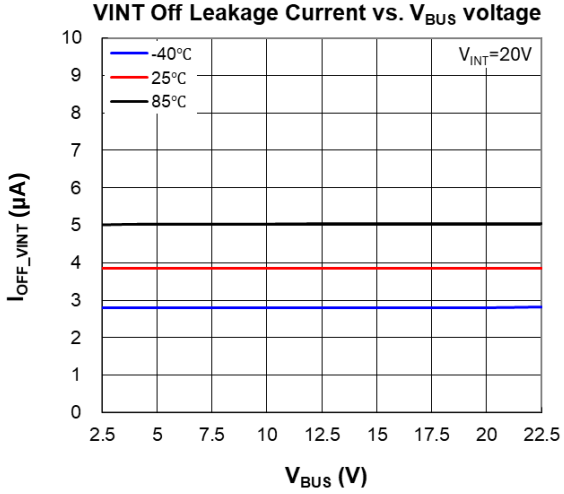
Shutdown Current vs. Input voltage



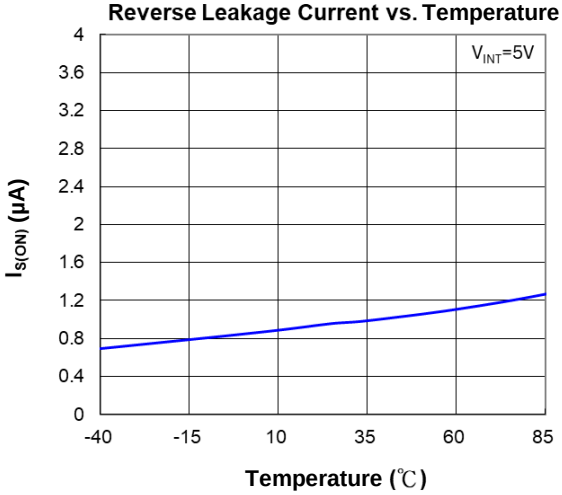
VBUS Off Leakage Current vs. V_{INT} voltage



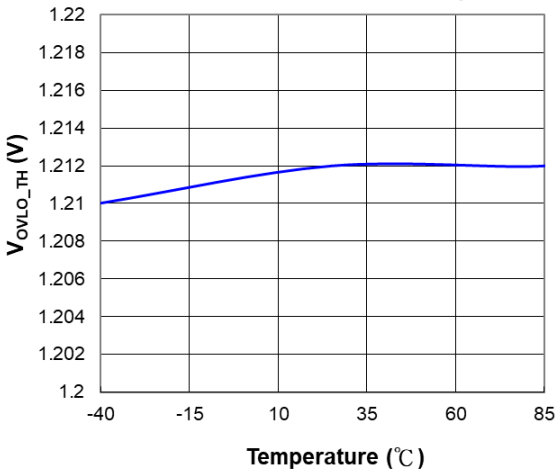
VINT Off Leakage Current vs. V_{BUS} voltage



Reverse Leakage Current vs. Temperature

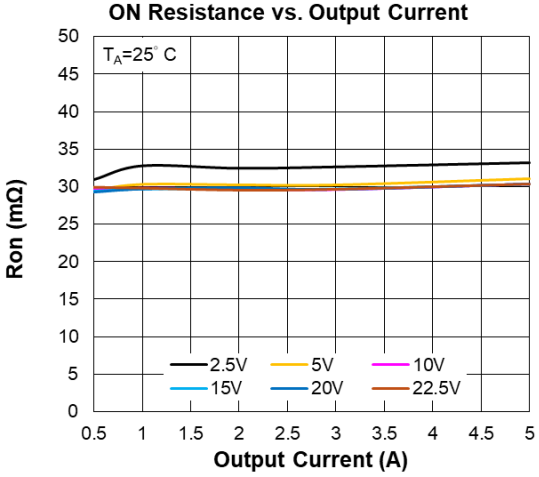


External OVLO threshold vs. Temperature

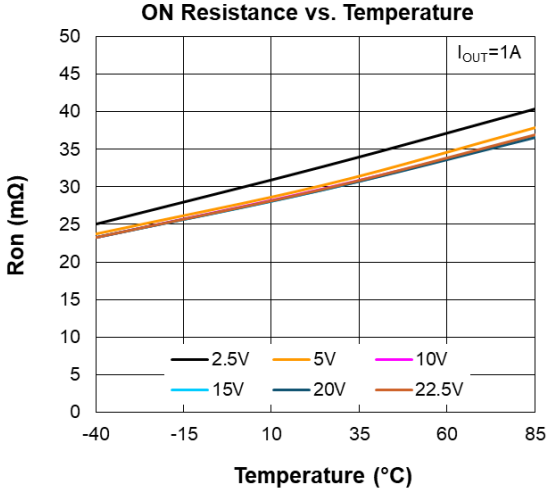


Typical Performance Characteristics (TJ = -40°C to +85°C, VBUS = 2.5V to 22.5V, typical values are at VBUS = 5V and TJ = +25°C, unless otherwise specified.) (continued)

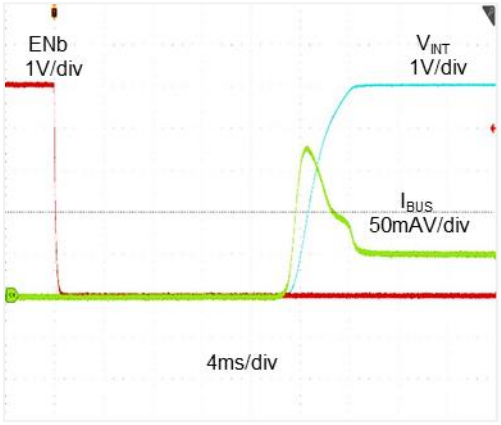
ON Resistance vs. Output Current



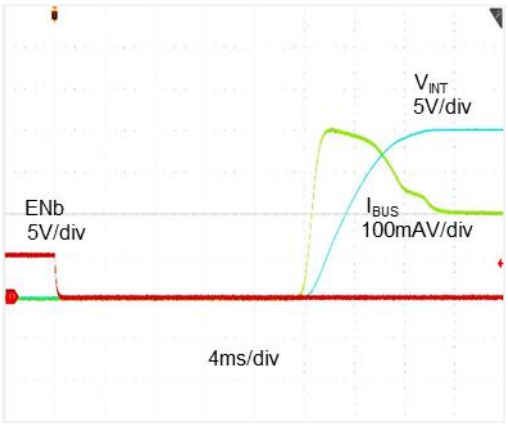
ON Resistance vs. Temperature



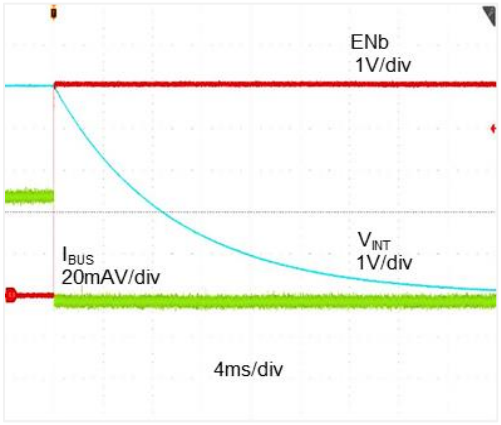
Turn-on Time and In-rush Current at VBUS = 5.0V



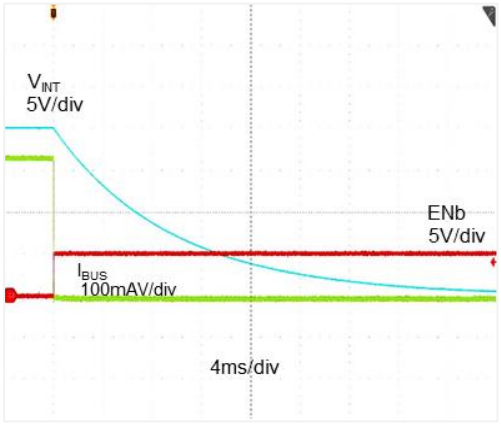
Turn-on Time and In-rush Current at VBUS = 20.0V



Turn-off Time at VBUS = 5.0V

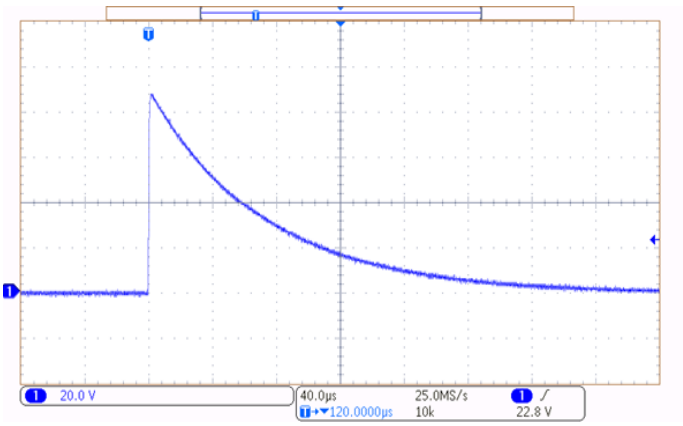


Turn-off Time at VBUS = 20.0V

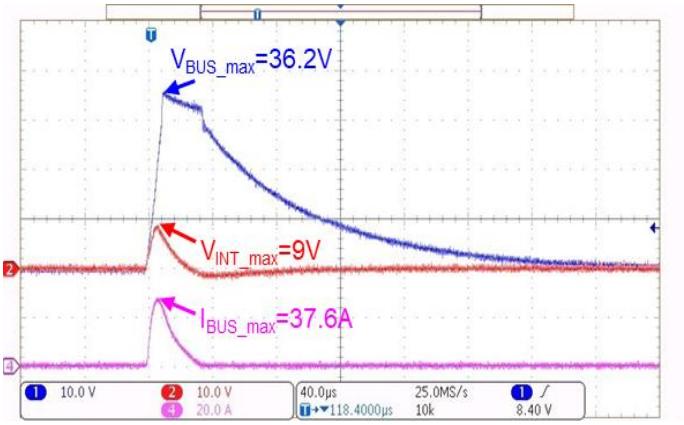


Typical Performance Characteristics (T_J = -40°C to +85°C, VBUS = 2.5V to 22.5V, typical values are at VBUS = 5V and T_J = +25°C, unless otherwise specified.) (continued)

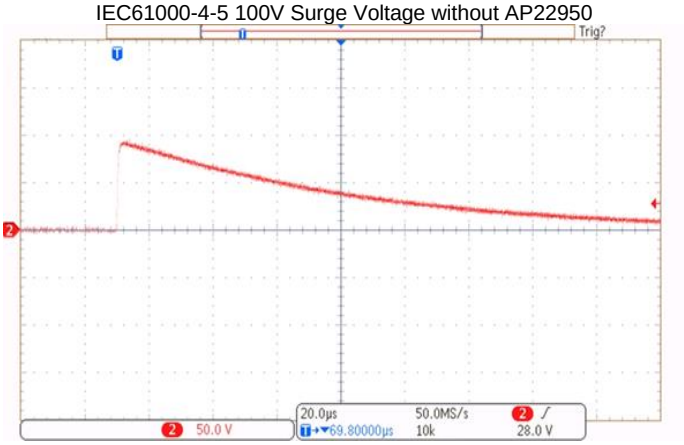
IEC61000-4-5 90V Surge Voltage without AP22950



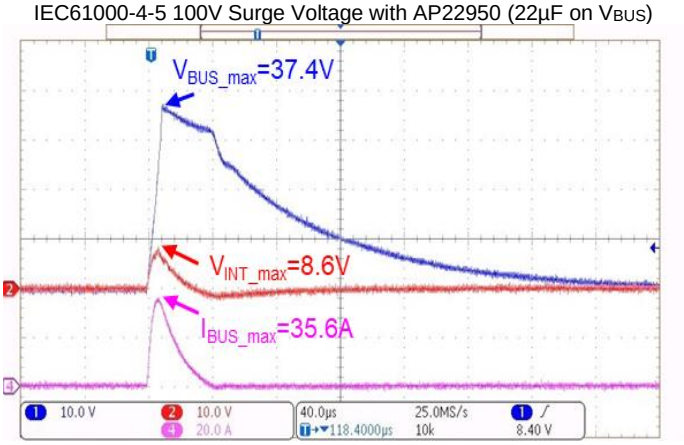
IEC61000-4-5 90V Surge Voltage with AP22950



IEC61000-4-5 100V Surge Voltage without AP22950



IEC61000-4-5 100V Surge Voltage with AP22950 (22µF on V_{BUS})



PCB Layout Recommendation

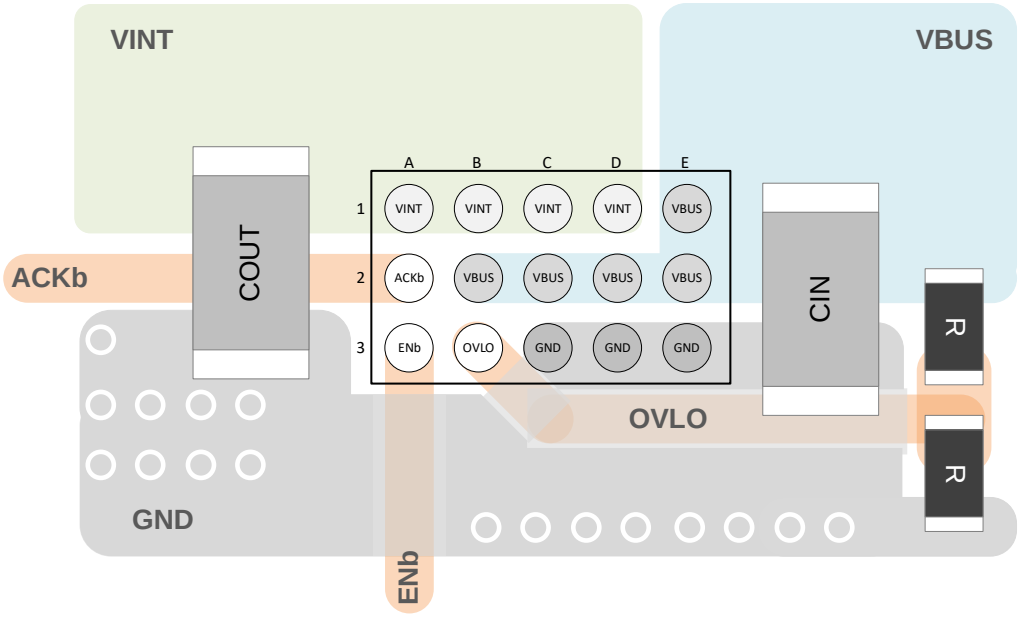
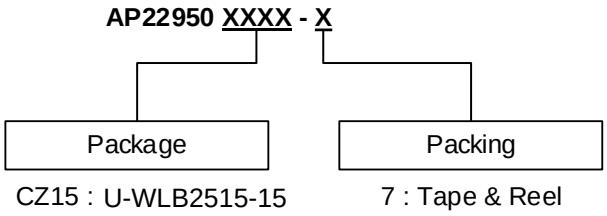


Figure 9. Recommended PCB Layout

Ordering Information (Note 7)



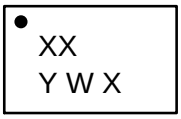
Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP22950CZ15-7	CZ15	U-WLB2515-15	3,000	Tape and Reel

Note: 7. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-WLB2515-15

(Top View)



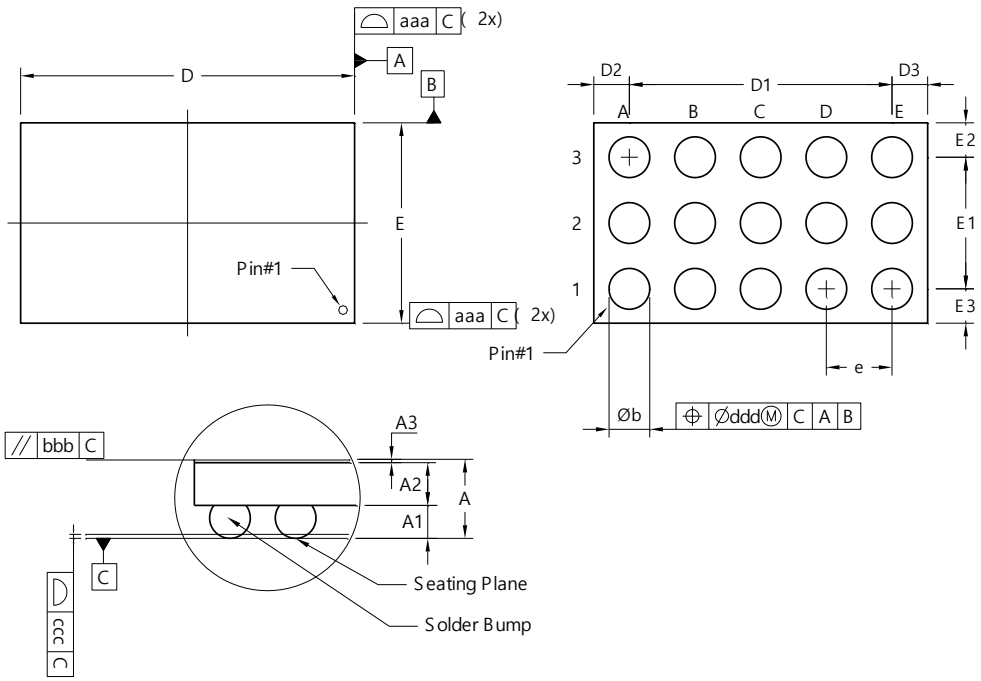
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Orderable Part Number	Package	Identification Code
AP22950CZ15-7	U-WLB2515-15	G5

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB2515-15

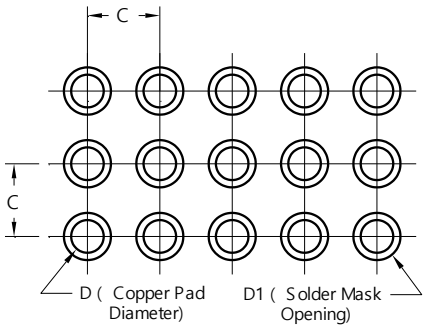


U-WLB2515-15			
Dim	**Min**	**Max**	**Typ**
A	0.5470	0.6530	0.6000
A1	0.2250	0.2750	0.2500
A2	0.3000	0.3500	0.3250
A3	0.0220	0.0280	0.0250
b	0.2635	0.3565	0.3100
D	2.5150	2.5700	2.5425
D1	--	--	2.000
D2	--	--	0.2713
D3	--	--	0.2713
E	1.4950	1.5500	1.5225
E1	--	--	1.000
E2	--	--	0.2613
E3	--	--	0.2613
e	--	--	0.50
aaa	--	--	0.0275
bbb	--	--	0.0600
ccc	--	--	0.0300
ddd	--	--	0.1500
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB2515-15



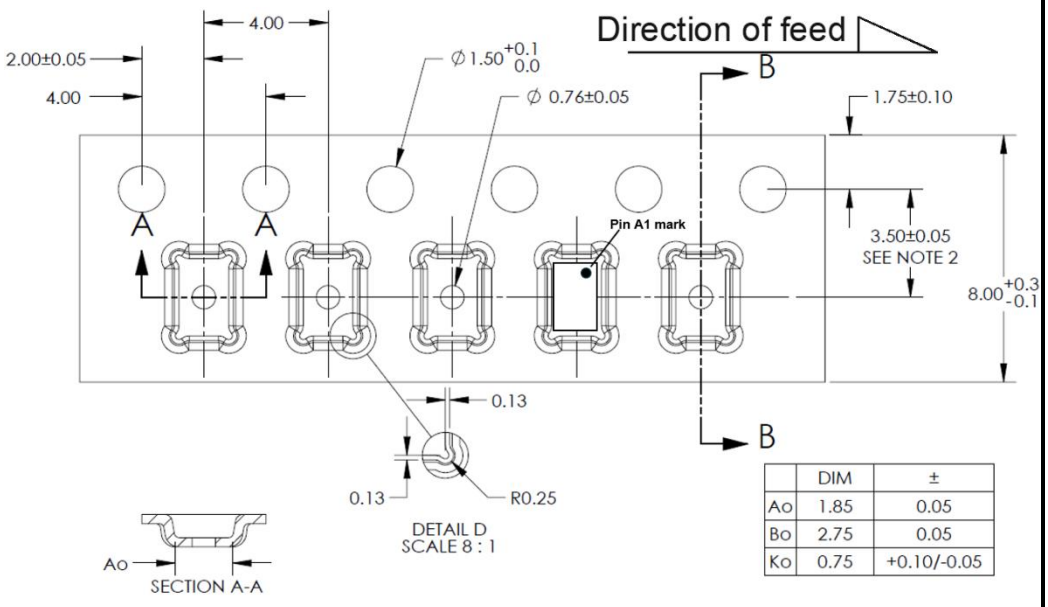
Dimensions	Value (in mm)
C	0.500
D Ø	0.225
D1 Ø	0.325

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the "Z" dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high-voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

Device Taping Orientation

Package Type: U-WLB2515-15

Tape Width	Part Number Suffix	Tape Orientation
8mm	-7	

Note: For part marking, refer to *Marking Information*.
Note: Tape and package drawings are not to scale and are shown for device tape orientation only.
Note: The taping orientation of the other package type can be found on our website at https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf.

Mechanical Data

- Surface-Mount Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Tin Silver Copper (SnAgCu), Solderable per MIL-STD-202, Method 208 e1
- Weight: 0.00472 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

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