DESIGN AND APPLICATION GUIDE FOR AHV85110

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ABSTRACT

This application note will describe how to choose components and their placement when designing with AHV85110 isolated gate driver.

INTRODUCTION

The AHV85110 is a self-powered isolated gate driver. Allegro's patented Power-Thru technology allows the transfer of both PWM signal and gate power across a single transformer-based isolation barrier. This eliminates the need to provide an isolated bias supply to power the isolated side of the driver, greatly simplifying the system design. Only an external decoupling capacitor is required on the isolated side.

The AHV85110 driver has been optimized for driving the gate of typical Schottky-gate Enhancement-mode (E-mode) GaN FETs, such as those available from GaN Systems, Innoscience, ST, Nexperia, GaN Power International, Taiwan Semiconductor, Rohm and others. In addition, some Transphorm cascode-GaN devices can also be driven, where low-voltage logic-level MOS devices are used inside the cascode. An online FET selection tool can be downloaded from the Allegro website to assist system designers, to check compatibility of various FET devices with the driver. The maximum drive capability is 30 nC at 6 V V_{GS}.

The isolated V_{SEC} bias rail on the secondary is derived open-loop from the primary 12 V supply V_{DRV}. The V_{SEC} rail level regulates quite well versus PWM switching frequency F_{SW} at the IN pin, for a given fixed V_{DRV} level, and for a fixed load C_{OUT} at the OUTx drive pins (the load presented by the gate of the GaN FET being driven). This is because the charge delivered per PWM cycle naturally increases in tandem with the charge consumed by the FET gate, so there is a good charge balance across a wide frequency range.

However, the V_{SEC} rail does vary with effective loading of the gate of FET being driven; as V_{SEC} level falls, more charge is available to be delivered to the secondary side, while the charge consumed by the FET gate decreases with falling V_{SEC} level. Therefore, the V_{SEC} rail will droop as far as needed until the charge delivered matches the charge consumed. For this reason, it's also very important to minimize the amount of charge diverted into any external loads. For example, a very low bias power external circuit can be powered using V_{SEC}, but the consumption should be minimal, to minimize the charge diverted away from the gate of FET. Similarly, if a gate-source pull-down resistor is desired on the load FET (to prevent false turn-on in the case of a manufacturing fault, such as an open-circuit gate turn-on resistor), the resistor value should be as large as possible. The recommended value is 100 kΩ, to minimize DC loading on V_{SEC}. Since DC load current converts to equivalent charge as $Q = I \times t$, DC loading effects will become significantly more pronounced at lower PWM frequency, as the time duration t gets longer.

Since there is just a single magnetic isolation barrier to transfer both PWM signal and gate power, this also greatly reduces the total parasitic capacitance between the primary-side and isolated-side, to typically < 1 pF total for both signal and power channels. This is much less than the typical total parasitic capacitance value for a solution using a conventional isolated gate driver with a separate isolated DC-DC bias supply, where the capacitance contribution from the DC-DC isolation transformer could be as high as 10 pF or more. This reduction in isolation capacitance greatly reduces the level of noise injected back into the low-voltage control circuit by the high-voltage and high dv/dt switching nodes in the power stage half-bridge legs, reduces system level Common-Mode (CM) EMI, and saves on power loss that occurs through repetitive charging and discharging of this parasitic capacitance between the high bus voltage level and ground.

PIN-BY-PIN DESCRIPTION

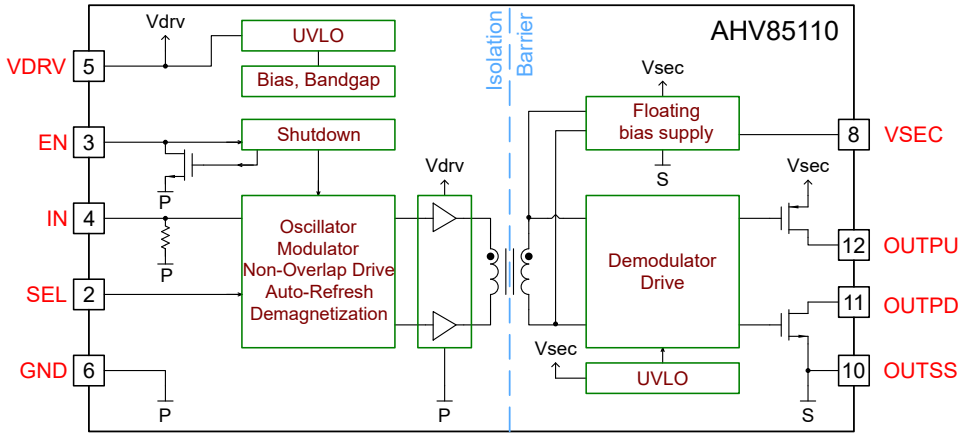


Figure 1: AHV85110 Block Diagram

Pin Table

Number	Name	Function
Input Pins		
1, 6	GND	Primary side ground reference, internally connected to GND net. It is recommended to connect PIN 1 externally to PIN 6 to improve thermal impedance. Note that PIN 6 is the main GND pin, and must always be connected to the system ground. Thermal performance of the package can be improved by connecting the GND pins to a large ground plane, and by adding thermal vias to inner ground plane layers.
2	SEL	Selection pin. Internal use only. This pin MUST be tied to VDRV.
3	EN	Bidirectional enable pin. This pin requires an external resistor pull-up to the VDRV pin. The EN pin should never be left floating. When pulled low through an external open-drain pull-down, the driver is disabled and goes into a low power standby mode.
4	IN	PWM Input referenced to GND. It is recommended to add a low pass RC filter with small time constant to filter out any noise coupled to the input. The IN pin can be driven by standard 5 V or 3.3 V logic levels but is also compatible with higher-voltage logic signals since it is rated up to V_{DRV} voltage levels. This allows the IN pin to be interfaced directly to 12 V PWM signals, such as the outputs of typical analog PWM controllers.
5	VDRV	Primary side 12 V bias supply voltage, referenced to GND. V_{DRV} is rated to operate at a drive voltage within over 10.5 V to 13.2 V range. A good quality ceramic decoupling capacitor is required between VDRV and GND. It is recommended to use a 1 µF capacitor, located as close to the device as possible, and connected directly between pins 5 and 6.
Output Pins		
7, 9, 10	OUTSS	Isolated output return pin. These pins are internally connected to the OUTSS net. Note that pins 9 and 10 are the main OUTSS pins and must always be connected to the isolated system ground. Thermal performance of the package can be improved by connecting the OUTSS pins to a large ground plane, and by adding thermal vias to inner ground plane layers. It is recommended to connect PIN 7 externally to PINS 9 and 10 to improve thermal impedance, but pin 7 can be left floating, depending on layout requirements.
8	VSEC	This is the isolated secondary-side bias rail, which is internally generated. An external decoupling capacitor is required from this pin to OUTSS. It is recommended to place the capacitor directly between VSEC and OUTSS, located as close to the device as possible.
11	OUTPD	Isolated output drive pull-down pin; Place a resistor between the OUTPD and FET gate input to control the turn-off speed of the transistor. Ensure that these resistors are high power rated and have high power surge withstanding capability. See Component Selection section.
12	OUTPU	Isolated output drive pull-up pin; Place a resistor between the OUTPU and FET gate input to control the turn-on speed of the transistor. Ensure that these resistors are high power rated and have high power surge withstanding capability. See Component Selection section.

DESIGN EXAMPLE

Figure 2 shows a typical application for driving a GaN transistor APEK85110KNH-01-T-MH with a bipolar drive arrangement.

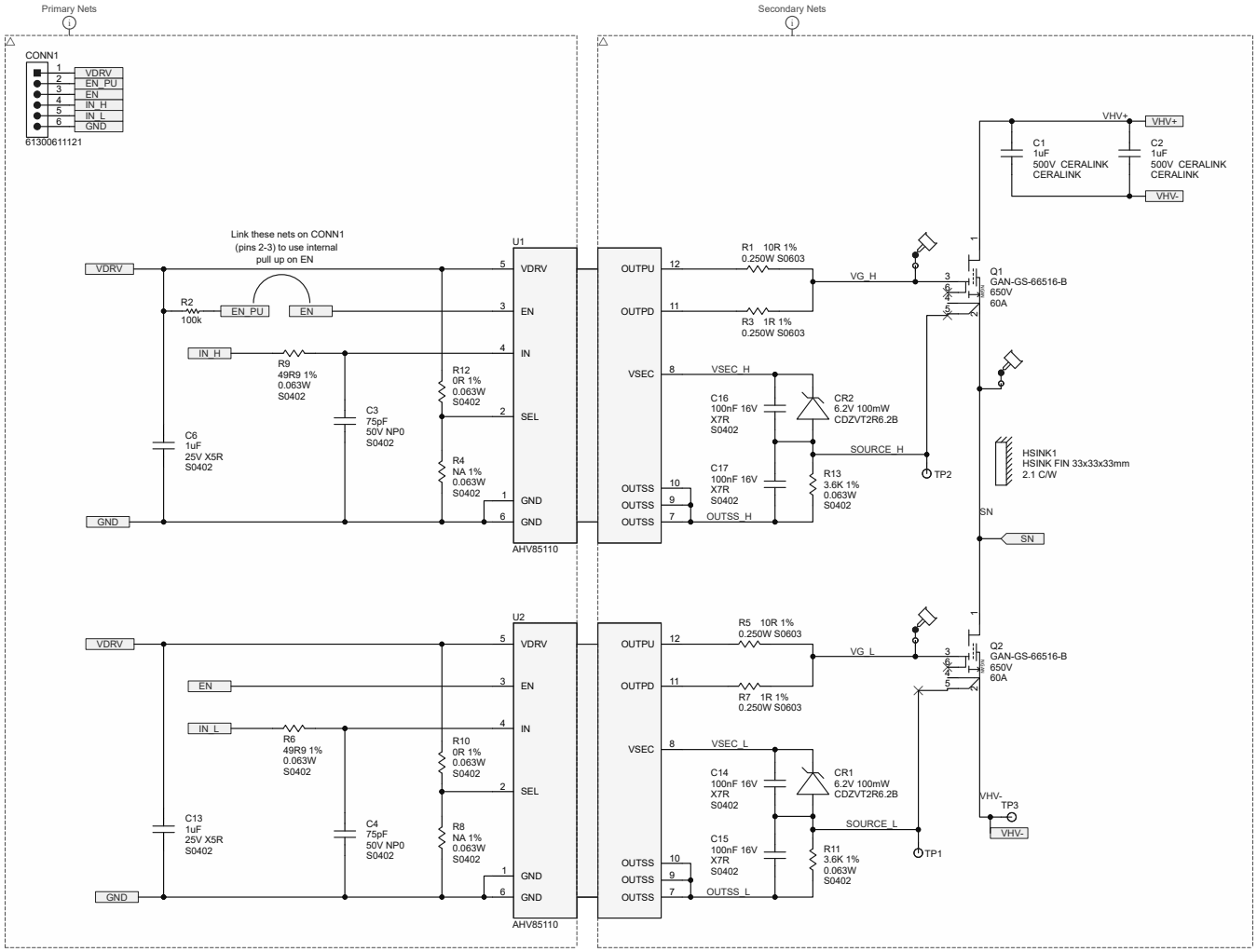


Figure 2: APEK85110KNH-01-T-MH Typical Application

Table 1: Design Parameters

Parameter	Value	Unit
V_{DRV}	10.8–13.2	V
Maximum Switching Frequency	1000 [1]	kHz
C_{SEC}	50	nF
V_{SEC_RIPPLE}	5–10	%

[1] Frequency depends on factors like heat sinking, temperature, high voltage decoupling capacitance and IN PWM duty cycle range.

Component Selection

Input Filter for VDRV

In high-voltage switching applications, the dV/dt of the half-bridge switch-nodes can be very high. Switching noise can be coupled into other circuit nodes due to the parasitic inductances and coupled capacitances around the driver, and can be made worse as a result of poor PCB layout.

It is important to place decoupling capacitors very close to both VDRV & VSEC pins. They must be connected directly between VDRV/GND and VSEC/OUTSS, respectively, with the shortest possible low-inductance loop.

Input Filter for IN

Some filtering at the IN pin is recommended to filter out high frequency noise. In the application example, there is a small filter with resistor and capacitor.

EN

Place a 100 kΩ pull-up resistor between the EN pin and VDRV. In the application example, there is a provision to use EN-PU signal to control the driver enable functionality externally.

OUTPU and OUTPD resistor

The AHV85110 driver splits the gate outputs OUTPU and OUTPD to allow use of separate pull-up (turn-on) and pull-down (turn-off) resistors. This allows for independent control of the turn-on and turn-off speeds of the transistor. These resistors determine the peak source and sink current by the equations below:

$$I_{source\_pk} = \frac{V_{SEC}}{R_{PU} + R_{PUint}}$$

where $R_{PUint} = 2.8\ \Omega$

$$I_{sink\_pk} = \frac{V_{SEC}}{R_{PD} + R_{PDint}}$$

where $R_{PDint} = 1\ \Omega$

In the application example, $R_{PU} = 10\ \Omega$ and $R_{PD} = 1\ \Omega$, which will give the following calculations:

$$I_{source\_pk} = \frac{V_{SEC}}{R_{PU} + R_{PUint}} = \frac{6.2}{10 + 2.8} = 485\ mA$$

$$I_{sink\_pk} = \frac{V_{SEC}}{R_{PD} + R_{PDint}} = \frac{6.2}{1 + 1} = 3.1\ A$$

Ensure that the resistors can withstand these high peak currents while choosing components.

Note that these resistors are not mandatory, only if the design require control of the switching turn-on and turn-off speed, then it is possible to use these resistors based on the equations above. Ensure that the resistors can withstand these peak currents while choosing components.

Unipolar configuration

It is recommended to connect a capacitor C_{SEC} between VSEC and OUTSS pins and place this capacitor as close to the device as possible. It is also recommended to use a total V_{SEC} cap value of 20 times the load capacitance, to minimize switching frequency ripple.

$$C_{SEC} = 20 \times C_{GATE}$$

Bipolar Configuration

A popular method to mitigate the effects of false turn-on, is through the use of a bipolar output drive, as shown in the application example below:

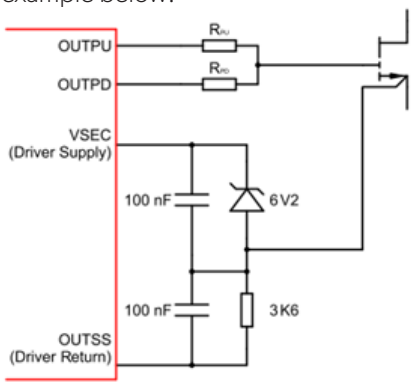


Figure 3: Bipolar output drive schematic

Using the above configuration, positive and negative supply voltages, V_{SECP} and V_{SECN}, respectively:

$$V_{SECP} = V_{zener}$$

$$V_{SECN} = V_{zener} - V_{SEC}$$

It is critical to calculate load capacitance correctly, to identify the voltage at VSEC pin of the driver. Total gate charge Qg is listed under the Dynamic characteristics of the transistor.

APEK85110KNH-01-T-MH uses a GaN Systems transistor: GS66516B, Q_G = 14.2 nC at V_{GS} = 6 V it is possible to calculate the gate capacitance as:

$$Q_G = C_{GATE} \times V_{GS}$$

$$C_{GATE} = \frac{Q_G}{V_{GS}} = 2.37\ nF$$

The user should refer to the curve in Figure 4 to determine VSEC voltage. For V_{DRV} = 12 V, and C_{GATE} = 2.2 nF, VSEC = 7.6 V. Therefore at C_{GATE} = 2.37 nF, it's estimated that V_{SEC} will be approximately 7.4 V. Therefore, the result is:

$$V_{SECP} = 6.2\ V \text{ and } V_{SECN} = (6.2 - 7.4) = -1.2\ V$$

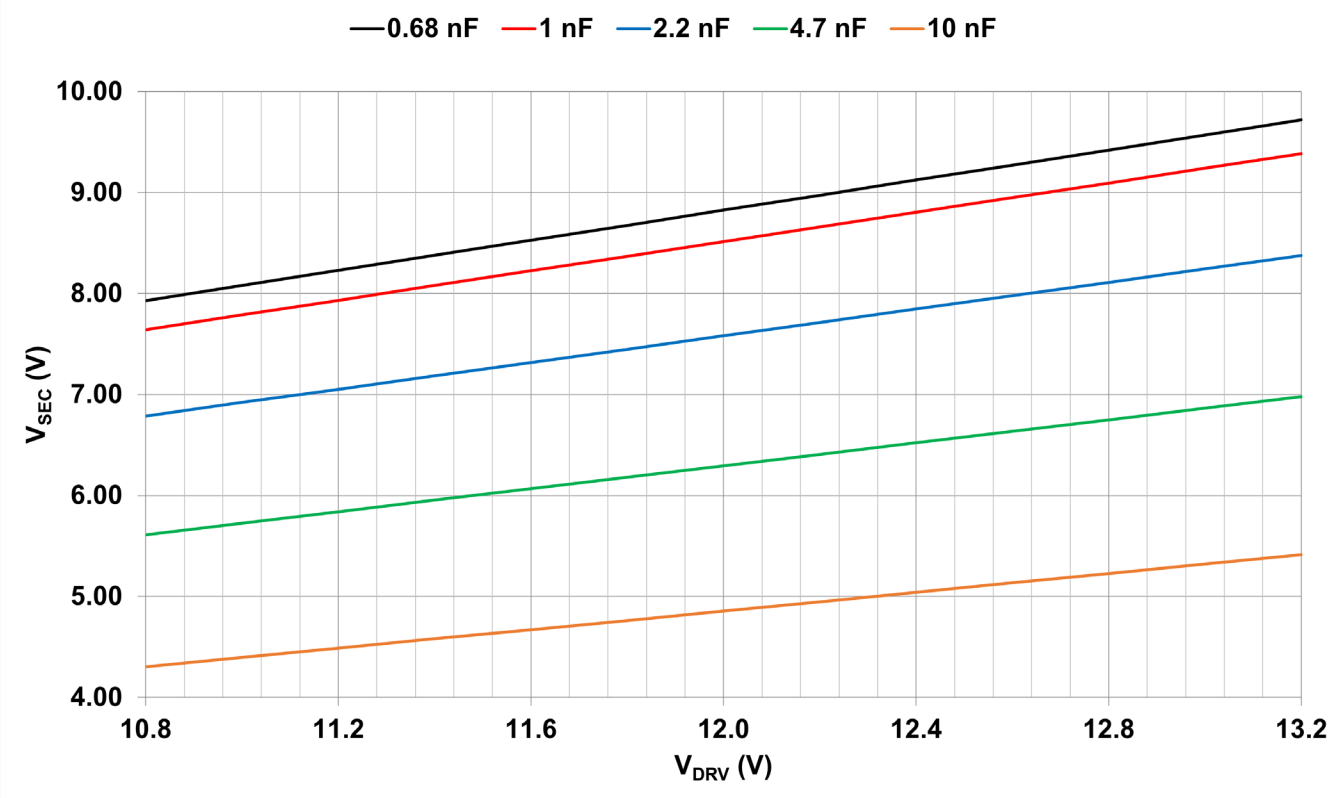
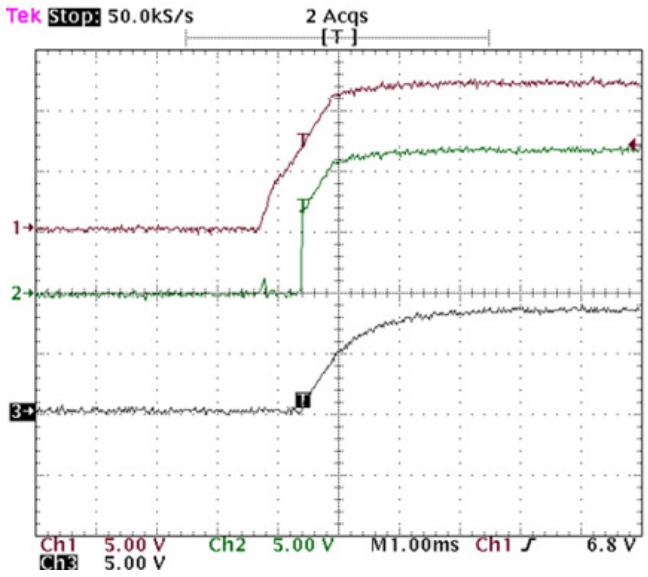


Figure 4: Typical V_{SEC} versus V_{DRV} for five C_{OUT} capacitors; Conditions: f_{IN} = 100 kHz, D = 50%, $C_{SEC} = 20 \times C_{OUT}$

PCB layout is critical for the correct performance of power switching circuits. The AHV85110 driver pinout easily facilitates this bipolar drive circuit without compromising on the key PCB layout guidelines.

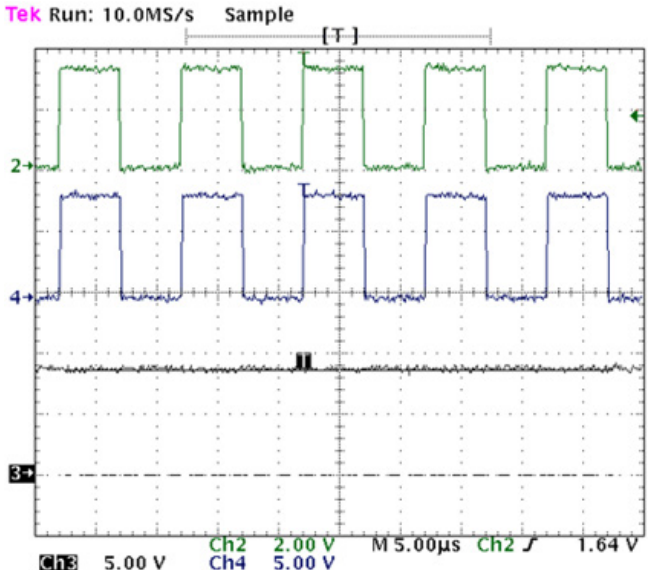
EVALUATION BOARD CHARACTERISTICS

IN = PWM @ 100 kHz, VDRV = 12 V, C_{GATE} = 1 n
Startup Behaviour



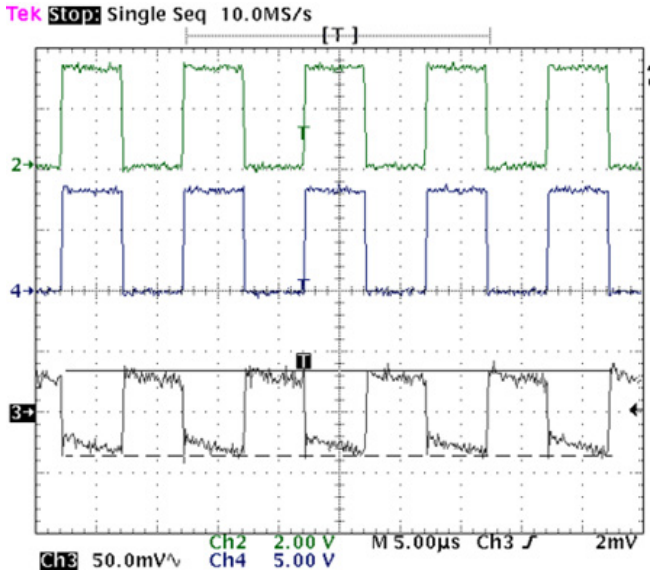
CH1 (Red): VDRV
CH2 (Grn): EN (pull-up to VDRV)
CH3 (Blk): VSEC

IN = 0, EN = 1, VDRV = 12 V, C_{GATE} = 1 n
Steady state



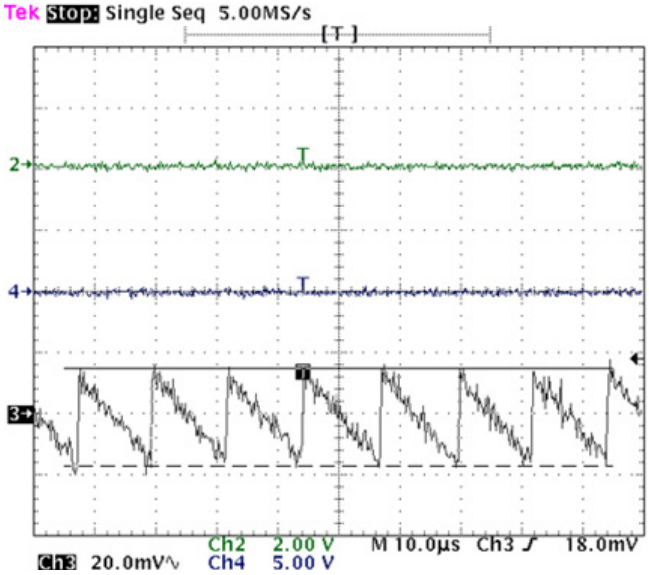
CH2 (Grn): Driver input
CH4 (Blu): Driver output
CH3 (Blk): VSEC

IN = PWM @ 100kHZ, EN = 1, VDRV = 12 V, C_{GATE} = 1 n
Steady State ripple



CH2 (Grn): Driver input
CH4 (Blu): Driver output
CH3 (Blk): VSEC_ripple

IN = 0, EN = 1, VDRV = 12 V, C_{GATE} = 1 n
Refresh State ripple



CH2 (Grn): Driver input
CH4 (Blu): Driver output
CH3 (Blk): VSEC_ripple

For further information, reference TED-4124.

PCB LAYOUT RECOMMENDATIONS

Since the Power-Thru drivers use an internal miniature transformer to magnetically couple both PWM signal and gate bias power, precautions must be exercised in the system design and PCB layout to minimize unwanted coupling of stray magnetic fields.

These stray fields can be generated by explicit magnetic components in the systems, such as PFC chokes, EMI filter chokes, LLC resonant inductors, power stage transformers. Since these unwanted stray fields also can cause EMI issues, it makes good design sense to carefully partition these magnetic components from each other, from the EMI filter, etc.. These types of magnetic components should also be carefully placed as far as possible with respect to the isolated drivers, to minimize unwanted stray field coupling.

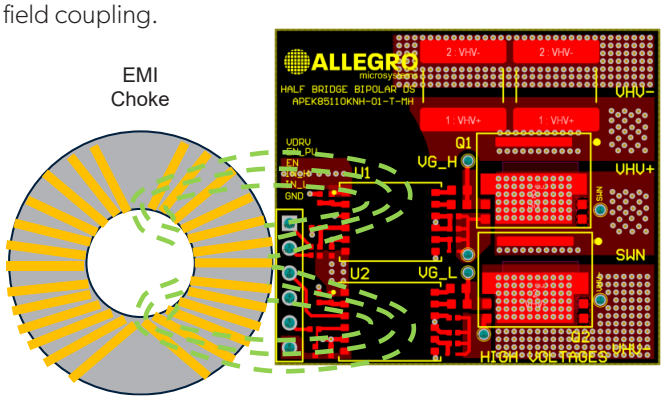


Figure 5: Example of unwanted magnetic coupling due to poor placement of EMI filter choke – too close to the isolated gate drivers

Besides the explicit inductive component sources of stray magnetic fields, there can also be unintended sources. These can arise when high currents flow in large loops in PCB traces, board-to-board interconnect, and system wiring. It's important to minimize the loop area of these high-current loops by routing the out and return traces close together. This ideally occurs on adjacent PCB layer-pairs, right on top of each other.

In particular, avoid routing high-current PCB traces adjacent to or around the isolated gate drivers, to minimize unintended stray magnetic field coupling to the driver. Since the area right under the driver needs to be kept free of copper traces to meet isolation requirements, it's recommended to keep all other layers under the driver also free of copper traces, to minimize risk of generating stray fields due to high currents flowing in internal power planes.

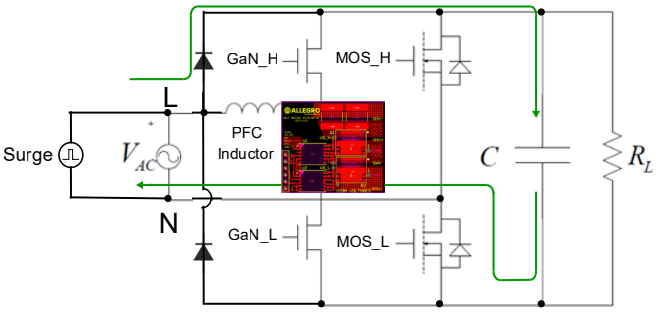


Figure 6: Example of unwanted magnetic coupling due to poor routing of high-current loop under the isolated gate drivers

SYSTEM SURGE MANAGEMENT

During various system-level events, large transient currents can flow for short periods. Examples of this include lightning surge testing to IEC61000-4-5, and system-level ESD testing to IEC61000-4-2. During these events, the large transient currents that flow can also create large stray magnetic fields, and these can also couple unintentionally to the isolated gate driver.

Careful system-level design and PCB layout are of course always important to make sure that the system can pass these required tests. In all cases, defined low-impedance paths must be provided in the PCB design and system wiring to ensure that the surge currents follow defined conduction paths, and are kept away from any sensitive or low-voltage circuits, to prevent malfunction or damage.

For similar reasons, careful system design should be deployed to also steer these large transient surge currents away from the isolated gate driver, to minimize coupling of stray magnetic fields generated by the surge current flow.

For example, in the case of a lightning surge event per IEC61000-4-5, a low-impedance path is often provided via bypass diodes, to conduct the surge current from Live/Neutral lines directly to the Power-Factor-Correction (PFC) bus capacitor, to avoid having this current flow through the PFC choke and power stage switches. Similarly, inrush current surges at startup would follow the same path directly to the bus capacitor, avoiding potential saturation of the PFC choke and potential damage to the power devices. This is particularly important for GaN power switches, which have a high source-drain voltage-drop when conducting in the third quadrant (compared to MOSFET, assuming the GaN FET is not explicitly turned on during reverse conduction). It's important to carefully place these bypass diodes and route the traces as far away as possible from the isolated gate driver to minimize the risk of coupling the transient magnetic field that will be generated by the flow of high surge current to the bus capacitor.

In many systems designs, circuitry and software to detect and react to surge events may already be implemented and used to activate a system-level protection inhibit signal. For example, such an inhibit signal may be used to temporarily disable the PWM signals to power stages, to temporarily halt the switching activity under high-voltage transient conditions in order to reduce the risk of power switch over-stress.

For increased system robustness, the same surge-detection-inhibit signal should additionally be used to disable the isolated gate driver enable (EN) pins. Since the EN pins are open-drain with an external pull-up resistor, the EN pins of several drivers can be connected together to create a shared single-line EN, which can then be pulled low via an open-drain pull-down, driven by the system-level surge-detection-inhibit signal.

An example of the use of this surge-detection-inhibit architecture is shown in figure 7, for a Totem-Pole PFC power stage. When the surge event is detected, the system controller inhibits the PWM gate drive signal to both GaN and MOS legs, and also pulls down the open-drain Enable (EN) lines to all drivers. This ensures a robust response to the surge event.

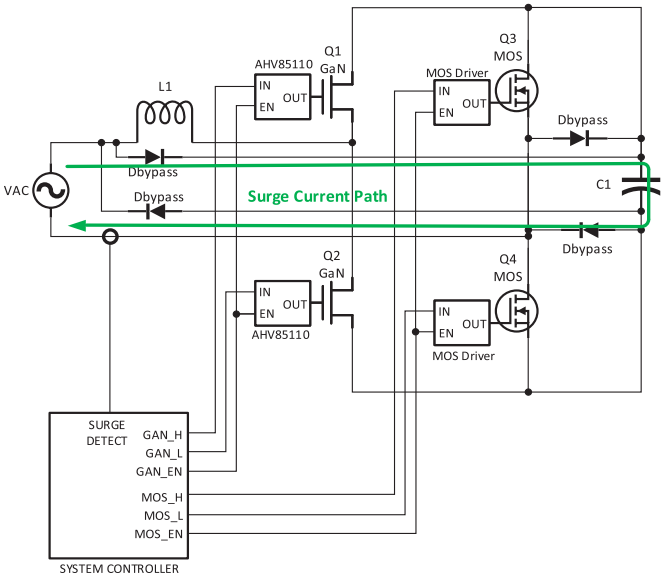


Figure 7: Block diagram of system level surge-detection inhibit signal used to disable isolated gate drivers using the EN pins

The waveforms in Figure 8 show the operation of the inhibit protection, and Figure 9 shows example measurement waveforms taken in the lab.

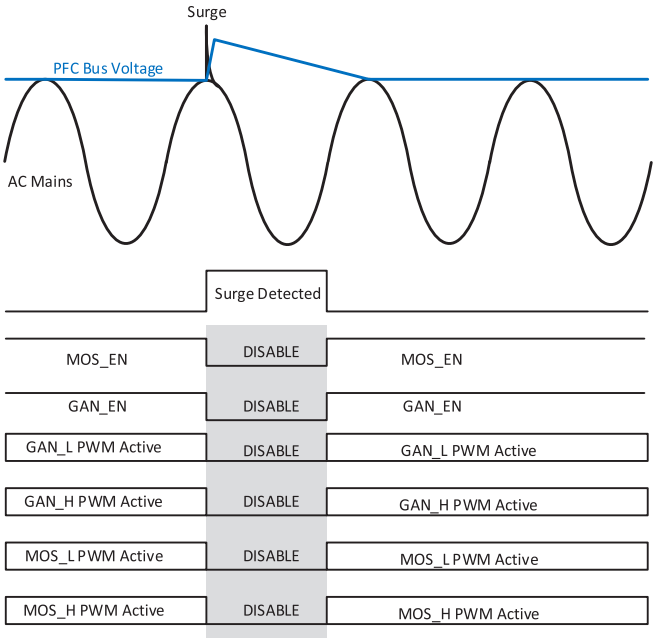


Figure 8: Timing diagram showing use of EN pins to disable isolated gate drivers

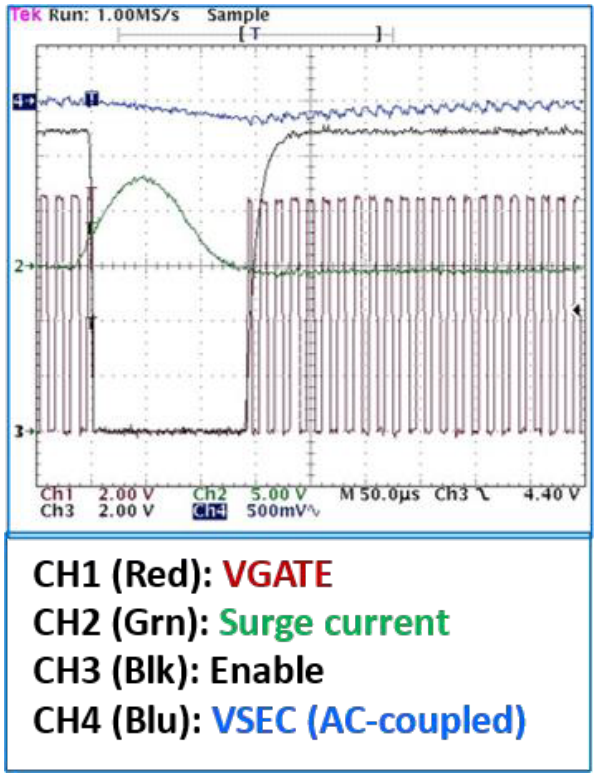


Figure 9: Bench measurement of surge event, showing use of EN pins to disable isolated gate drivers

PCB LAYOUT

Layout Guidelines

The following are some key points to consider while doing the PCB layout for the best performance with AHV85110:

- Place the AHV85110 gate driver as close as possible to the transistor. This is necessary to minimize the path of the high peak currents. This arrangement will also minimize the loop inductance and noise injection on the gate signals.

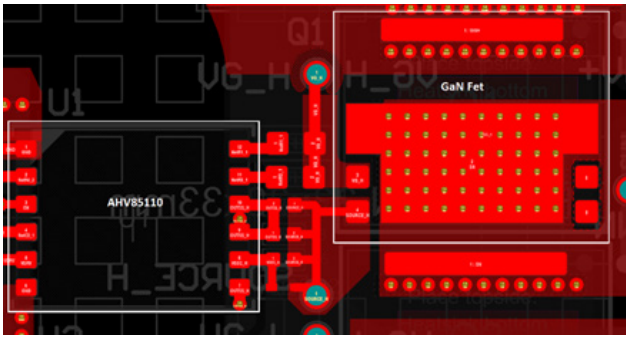


Figure 10: AHV85110 placement

- Ensure that the resistors connected between the isolated output drive pins to the gate of the transistor are high power rated and have high power surge withstanding capability.
- Decoupling capacitors must be connected close to the VDRV/GND and VSEC/OUTSS pin-pairs.

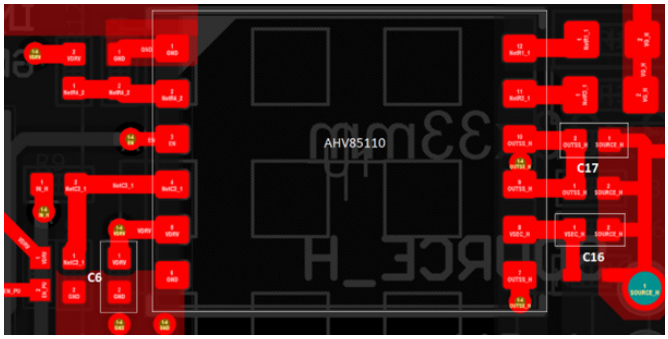


Figure 11: Decoupling capacitor placement

- The path connecting to the source of the transistor should be minimized to avoid large parasitic inductances.

The layout should have good thermal relief to help dissipate heat from the gate driver to the PCB. It is recommended to use vias to maximize thermal conductivity.

LAYOUT EXAMPLE

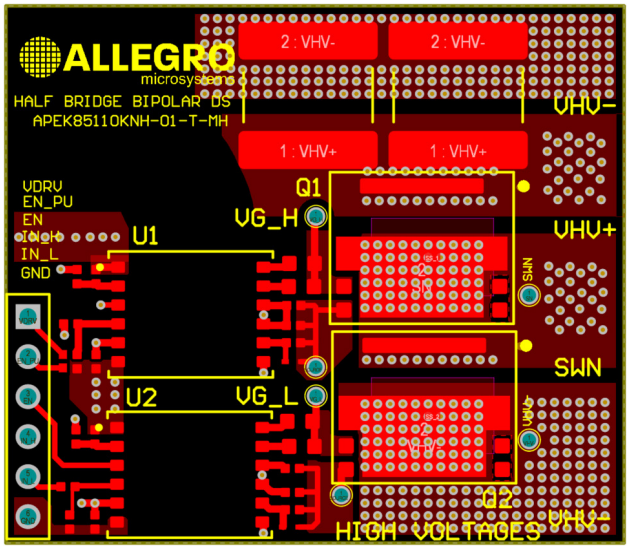


Figure 12 : Layout example

PCB Layers

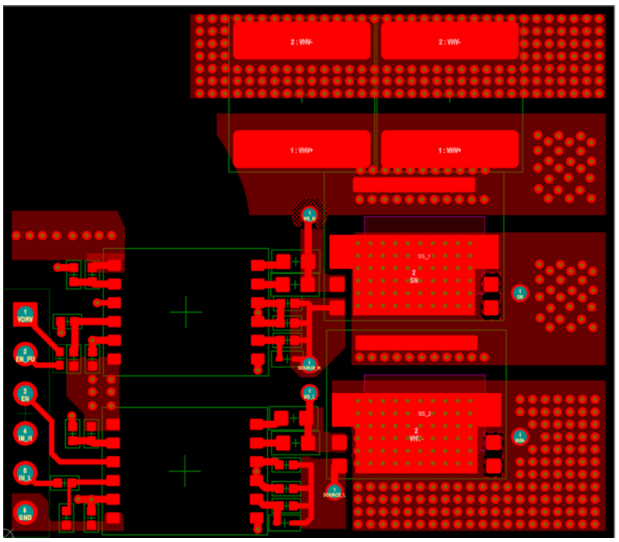


Figure 13: PCB Top Layer

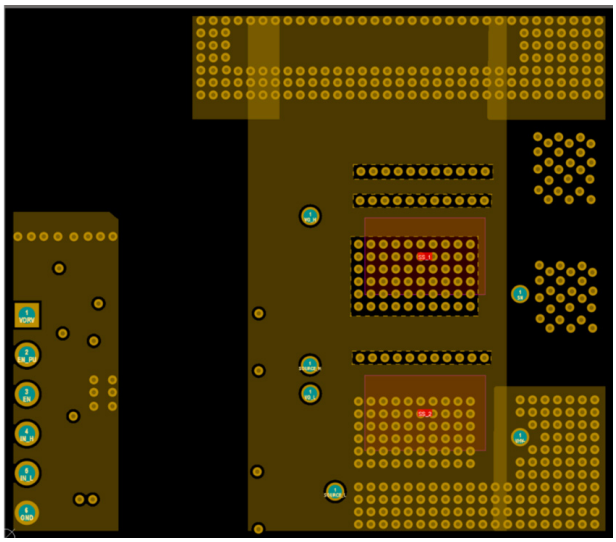


Figure 14: PCB Mid Layer 1

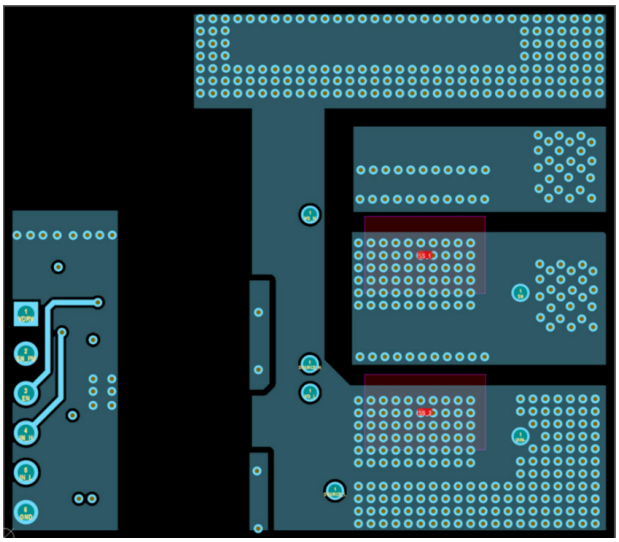


Figure 15: PCB Mid Layer 2

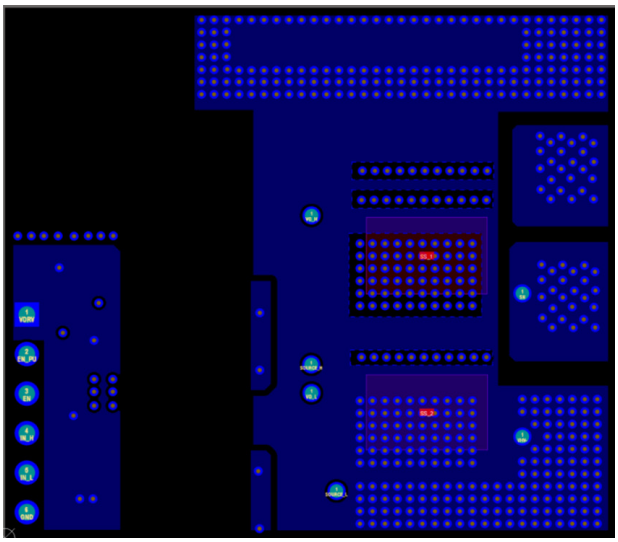


Figure 16: PCB Bottom Layer

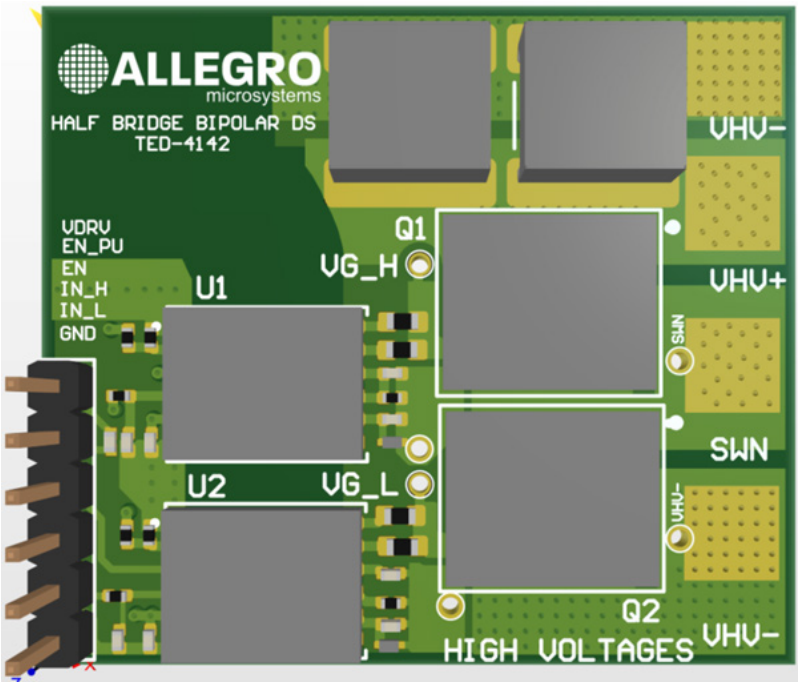


Figure 17: 3D view of PCB layout

Bill of Materials

Table 2: TED-4142 Bill of Materials

Designator	Comment	Description	Quantity	Manufacturer	Manufacturer Part Number
C14, C15, C16, C17	100 nF 16 V	SMD Multilayer Ceramic Capacitor, 0.1 uF, 16 V, 0402 [1005 Metric], ±10%, X7R, CC Series	4	Yageo	CC0402KRX7R7BB104
R2	RC0402FR-07100KL		1	Yageo	RC0402FR-07100KL
CONN1	61300611121	THT Vertical Pin Header WR-PHD, Pitch 2.52 mm, Single Row, 6 pins	1	Wurth Electronics	61300611121
C1, C2	1 uF	SMD Multilayer Ceramic Capacitor, 1 uF, 500 V, SMD, ±20%, Ceralink	2	TDK	B58031U5105M062
CR1, CR2	6.2 V 100 mW	Zener Single Diode, 6.2 V, 100 mW, SOD-923, 2 pins, 150°C, Surface Mount	2	ROHM	CDZVT2R6.2B
R3, R7	1R 1%	SMD Chip Resistor, 1 Ω, ±5%, 250 mW, 0603 [1608 Metric], Thick Film, Anti-Surge	2	ROHM	ESR03EZPJ1R0
C3, C4	75 pF	SMD Multilayer Ceramic Capacitor, 75 pF, 50 V, 0402 [1005 Metric], ±5%, C0G/NP0,MC	2	OR_Equivalent	OR_Equivalent
R4, R8, R10, R12	0R 1%	O Ω Resistor, Jumper, 0402 [1005 Metric], Thick Film, 63 mW, 1.5 A, Surface Mount Device	4	OR_Equivalent	OR_Equivalent
R6, R9	49R9 1%	SMD Chip Resistor, 49.9 kΩ, ±1%, 262.5 mW, 0402 [1005 Metric],Thick Film, General Purpose	2	OR_Equivalent	OR_Equivalent
R11, R13	3.6K 1%		2	OR_Equivalent	OR_Equivalent
C6, C13	1 uF	SMD Multilayer Ceramic Capacitor, 1 uF, 25 V, 0402 [1005 Metric], ±10%, X5R, GRM Series	2	Murata	GRM155R61E105KA2D
Q1, Q2	GAN-GS-66516-B	GaN Systems GS-66516-B, 650 V, 60 A, 25 mΩ	2	GaN Systems	GS66516B-MR
R1, R5	10R 1%	SMD Chip Resistor, 10 Ω, ±1%, 250 mW, 0603 [1608 Metric], Thick Film, Anti-Surge, [NoValue]	2	Bourns	CMP0603AFX-10R0ELF
U1, U2	AHV85110	Single Channel Isolated GaN Driver	2		

PCB Material

Use a standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

CONCLUSION

For applications that require high power density or higher switching frequency AHV85110 is a perfect easy to use isolated driver solution designed specifically for E-mode GaN Fets. With the advantage of a built-in isolated bias supply for the gate, the AHV85110 eliminates extra circuitry and allows for compact solution.

Revision History

Number	Date	Description	Responsibility
–	June 21, 2023	Initial release	Sonal Singh

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