AN11261

RC Thermal Models

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Document information

Information	Content
Keywords	RC thermal, SPICE, Models, Zth, Rth, MOSFET, Power, Foster, Cauer
Abstract	Analysis of the thermal performance of power semiconductors is necessary to efficiently and safely design any system utilizing such devices. This article presents a quick and inexpensive way to infer the thermal performance of power MOSFETs using a thermal electrical analogy.

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1. Introduction

The thermal behaviour of power semiconductor devices can be predicted using RC thermal models. The model types presented in this application note are known as Foster and Cauer models, consisting in networks of resistors and capacitors. Foster and Cauer models are equivalent representations of the thermal performance of a MOSFET and they can be used within a SPICE environment. This document provides some basic theory behind the principle, and how to implement Foster and Cauer RC thermal models. For convenience, Foster and Cauer RC thermal models are referred to as RC models in the rest of this application note. Several methods of using RC thermal models, including worked examples, will be described.

2. Thermal impedance

RC models are derived from the thermal impedance (Z_{th}) of a device (see Fig. 1). This figure represents the thermal behavior of a device under transient power pulses. The Z_{th} can be generated by measuring the power losses as a result of applying a step function of varying time periods.

A device subjected to a power pulse of duration > ~1 second, i.e. steady-state, has reached thermal equilibrium and the Z_{th} plateaus becomes the R_{th}. The Z_{th} illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses.

The Z_{th} curves for repetitive pulses with different duty cycles, are also shown in Fig. 1. These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

To assist this discussion, the thermal resistance junction to mounting base ($R_{th(j\text{-}mb)}$) from the BUK7S1R0-40H data sheet, has been included in Table 1. The Z_{th} in Fig. 1 also belongs to the BUK7S1R0-40H data sheet.

Table 1. Steady state thermal impedance of BUK7S1R0-40H

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base			-	0.35	0.4	K/W

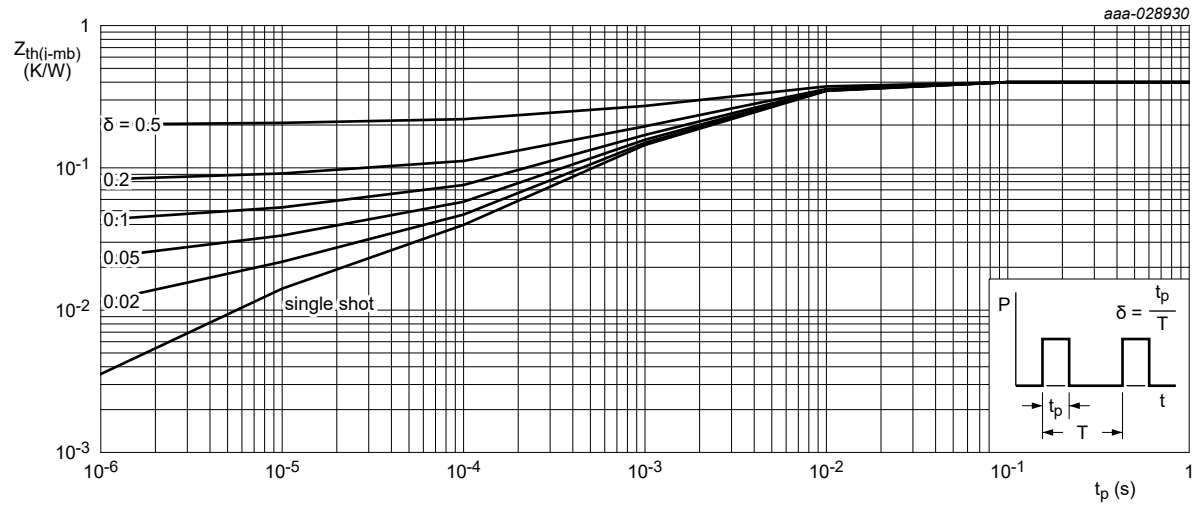


Fig. 1. Transient thermal impedance from junction to mounting base as a function of pulse duration for the BUK7S1R0-40H

3. Calculating junction temperature rise

To calculate the temperature rise within the junction of a power MOSFET, the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the thermal impedance can be read from the Z_{th} chart. The product of this value with the power gives the temperature rise within the junction.

If constant power is applied to the device, the steady state thermal impedance can be used i.e. R_{th}. Again the temperature rise is the product of the power and the R_{th}.

For a transient pulse e.g. sinusoidal or pulsed, the temperature rise within the MOSFET junction becomes more difficult to calculate.

The mathematically correct way to calculate T_j is to apply the convolution integral. The calculation expresses both the power pulse and the Z_{th} curve as functions of time, and use the convolution integral to produce a temperature profile (see Ref. 2).

$$T_{j(rise)} = \int_0^{\tau} P_{(t)} \cdot \frac{d}{dt} Z_{th}(\tau - t)\, dt \quad (1)$$

However, this is difficult as the $Z_{th(\tau-t)}$ is not defined mathematically.

An alternative way is to approximate the waveforms into a series of rectangular pulse and apply superposition (see Ref. 1).

While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model the waveform accurately.

To represent Z_{th} as a function of time, we can draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Z_{th} can then be represented in a SPICE environment for ease of calculation of the junction temperature.

4. Association between Thermal and Electrical parameters

The thermal electrical analogy is summarized in Table 2. If the thermal resistance and capacitance of a semiconductor device is known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

Table 2. Fundamental parameters

Type	Resistance	Potential	Energy	Capacitance
Electrical (R = V/I)	R = resistance (Ohms)	V = PD (Volts)	I = current (Amps)	C = capacitance (Farads)
Thermal (R_{th} = K/W)	R_{th} = thermal resistance (K/W)	K = temperature difference (Kelvin)	W = dissipated power (Watts)	C_{th} = thermal capacitance (thermal mass)

5. Foster and Cauer RC thermal models

Foster models are derived by semi-empirically fitting a curve to the Z_{th}, the result of which is a one-dimensional RC network Fig. 2. The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as can be in other modeling techniques. Finally, a Foster RC model cannot be divided or interconnected through, i.e. have the RC network of a heat sink connected.

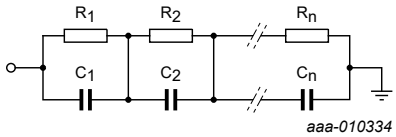


Fig. 2. Foster RC thermal models

Foster RC models have the benefit of ease of expression of the thermal impedance Z_{th} as described at the end of Section 2. For example, by measuring the heating or cooling curve and generating a Z_{th} curve, Equation 2 can be applied to generate a fitted curve Fig. 3:

$$Z_{th(t)} = \sum_{i=1}^{n} R_i \cdot \left[1 - \exp\left(- \frac{t}{\tau_i} \right) \right] \quad (2)$$

Where: $\tau_i = R_i \cdot C_i$ (3)

The model parameters R_i and C_i are the thermal resistances and capacitances that build up the thermal model depicted in Fig. 2. The parameters in the analytical expression can be optimized until the time response matches the transient system response by applying a least square fit algorithm.

The individual expression, “i”, also draws parallels with the electrical capacitor charging equation. Fig. 3 shows how the individual R_i and C_i combinations, sum to make the Z_{th} curve.

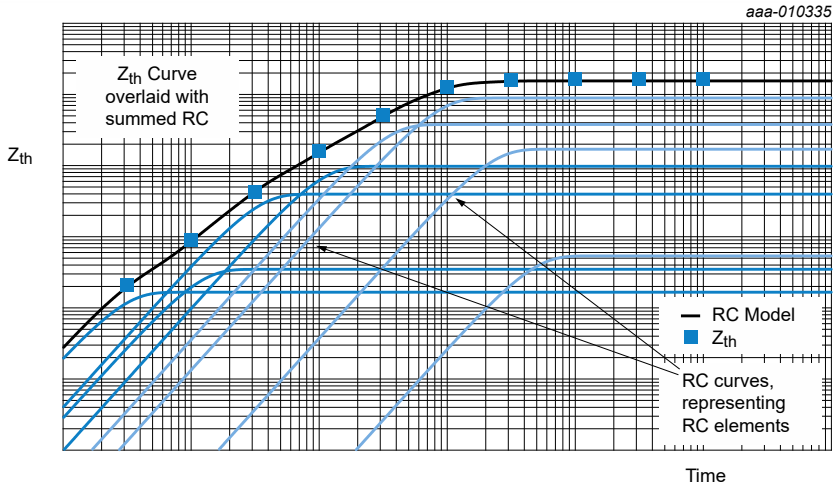


Fig. 3. Foster RC thermal models

Foster models have no physical meaning since the node-to-node heat capacitances have no physical reality. However, a Foster model can be converted into its Cauer counter-part by means of a mathematical transformation (see Ref. 4).

An n-stage Cauer model can be derived from an n-stage Foster model and they will be equivalent representations of the device thermal performance.

As seen for the Foster model, the Cauer Model also consists of an RC network but the thermal capacitances are all connected to the thermal ground, i.e. ambient temperature as represented in Fig. 4. The nodes in the Cauer Model can have physical meaning and allow access to the temperature of the internal layers of the semiconductor structure.

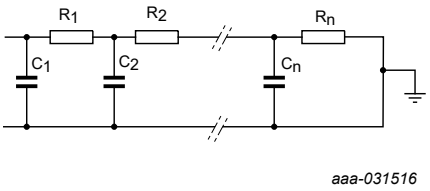


Fig. 4. Cauer RC thermal models

Nexperia provides Foster and Cauer RC models for most of their Automotive Power MOSFET products on the Product Information Pages, e.g. http://www.nexperia.com/products/mosfets/automotive-mosfets/BUK7S1R0-40H.html

The models can be found under the tabs “Documentation” and “Support” “BUK7S1R0-40H” as demonstrated in Fig. 5.

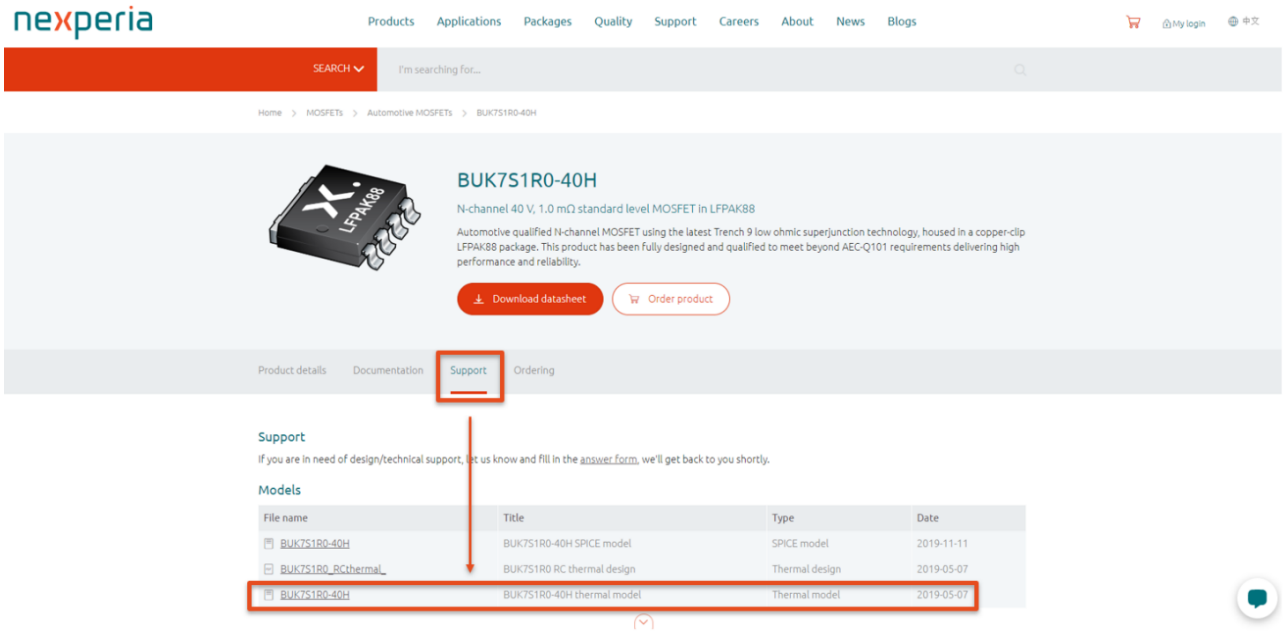


Fig. 5. Nexperia RC thermal model documentation

Foster and Cauer RC thermal models allow application engineers to perform fast calculations of the transient response of a package to complex power profiles.

In the following sections several examples of using RC thermal models will be presented. Foster models and Cauer models are equivalent representations of the device thermal behaviour but in the described examples Cauer models will be used as more representative of the physical structure of the device.

As shown in Fig. 8, a schematic file is available on Nexperia website for BUK7S1R0-40H Cauer model. Other products may not have this schematic file available and may be provided with a netlist file for the Cauer network as shown in Fig. 6:

```
*Part: BUK7S1R0-40H

.subckt cauer 1 6 7
R1    1    2    0.00272144
R2    2    3    0.0220255
R3    3    4    0.00713124
R4    4    5    0.185679
R5    5    6    0.182443
C1    1    7    9.29451e-05
C2    2    7    0.000514739
C3    3    7    0.00195047
C4    4    7    0.00305028
C5    5    7    0.0279554
.end cauer
```

Fig. 6. BUK7S1R0-40H Cauer model netlist

The netlist describes the same Cauer network as in Fig. 8, and can be used to build the same schematic. Pin 1 in the netlist can be identified as the junction temperature pin T_j in the schematic. Similarly pins 6, 7 as the T_{amb} pins in the schematic.

In order to simulate only the MOSFET pins 6 and 7 will both be tied to the ambient voltage source, as shown in Fig. 8.

However, one of the advantages of using Cauer models is to allow to add external networks to the MOSFET model, for example to model PCBs, heatsinks etc. In order to do so pin 7 will be tied to ambient and pin 6 to the first pin of the external Cauer network. For correct results, it is fundamental to make sure that the end pin of the external Cauer network is tied to the ambient source.

6. Thermal simulation examples

6.1. Example 1

RC thermal models are generated from the Z_{th} curve. This example shows how to work back from an RC model and plot a Z_{th} curve within a SPICE simulator. It allows for greater ease when trying to read values of the Z_{th} curve from the data sheet.

This and subsequent examples use the RC thermal model of BUK7S1R0-40H. T_{mb} represents the mounting base temperature. It is treated as an isothermal and for this example it is set as 0 °C. A single shot pulse of 1 W power is dissipated in the MOSFET. Referring to Fig. 7; for a single shot pulse, the time period between pulses is infinite and therefore the duty cycle δ = 0. Then the junction temperature T_j represents the transient thermal impedance Z_{th}.

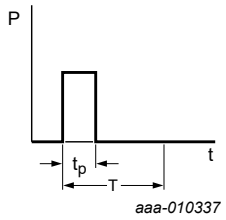


Fig. 7. Single-shot pulse

$$T_j = T_{mb} + \Delta T = 0\,°C + \Delta T = \Delta T \quad (4)$$

$$\Delta T = P \cdot Z_{th} = 1W \cdot Z_{th} \quad (5)$$

Equation 5 demonstrates that with P = 1 W, the magnitude of Z_{th} equates to ΔT.

The following steps are used to set up and run simulations:

1. set up the RC thermal model of BUK7S1R0-40H in SPICE as shown in Fig. 8
2. set the value of voltage source V_{mb} to 0, which is the value of T_{mb}
3. set the value of the current source I1 to 1
4. create a simulation profile and set the run time to 1 s
5. run the simulation
6. Plot the voltage at node T_j

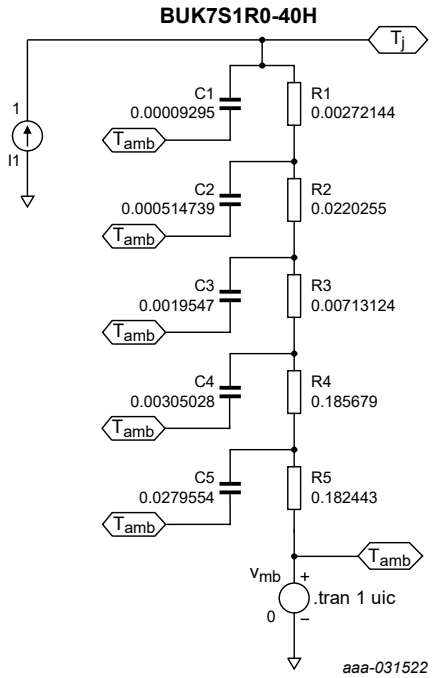


Fig. 8. BUK7S1R0-40H thermal model setup in SPICE

The simulation result in Fig. 9 shows the junction temperature (voltage at T_j) which is also the thermal impedance of BUK7S1R0-40H. The values of Z_{th} at different times can be read using the cursors on this plot within SPICE.

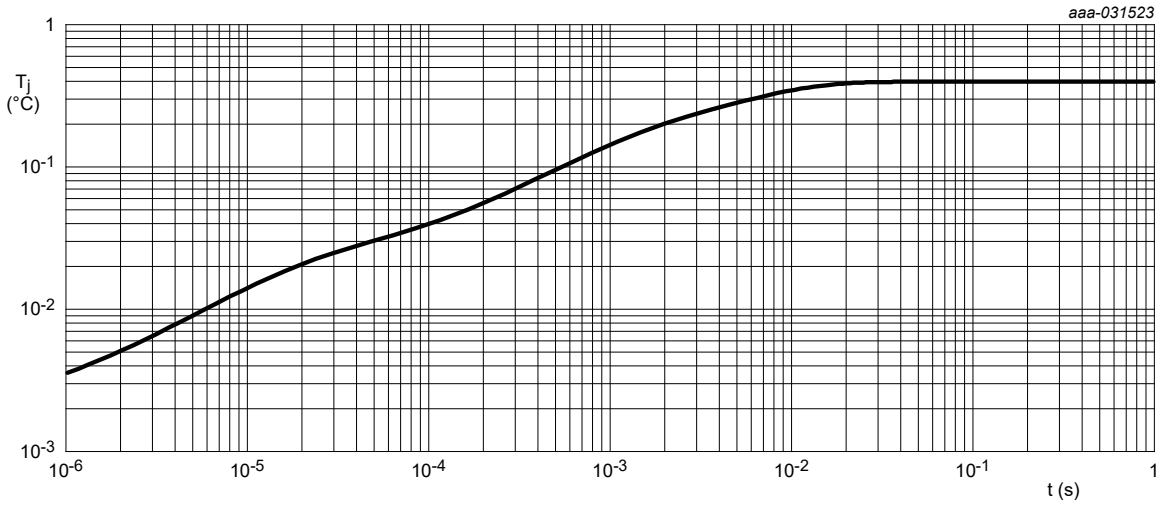


Fig. 9. A plot of T_j from simulation

The value of the current source in this example is set to 1 A to represent 1 W dissipating through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses.

6.2. Example 2

Another method of generating the power profile, is to use measurements from the actual circuit. This information is presented to the SPICE simulation in the form of a comma-separated value (CSV) file giving pairs of time/power values. It can be generated either as a summary of observations showing the points of change or from an oscilloscope waveform capture.

Two further methods of generating a power profile are discussed. One method is using a PWL file. The other is to generate the power from an MOSFET electrical circuit modeled in SPICE. The former is outlined first.

A source within a SPICE simulator can use a PWL file as an input. The contents of a typical PWL file is shown in Table 3. It can list the current, voltage or in this example, power over time. These files can be generated by typing values into a spreadsheet editor and saving as a .csv file, or alternatively exporting waveforms from an oscilloscope. The actual file itself should not contain any column headings.

To implement this procedure within a SPICE environment, follow the same steps as described in Section 6.1 “Example 1”, but with the exceptions:

1. Set the property value of the current source to read from a PWL FILE and point it to a .csv file for example: C:\Pulse file\filepulse.csv, which contains the power profile listed in Table 3
2. Set the mounting base T_{mb} (V_{mb}) to 125 °C
3. Set the simulation run time to 0.6 s

Table 3. Data example for use in a PWL file

Time (seconds)	Power (Watts)
0.000000	0
0.000001	120
0.004000	120
0.004001	24
0.004002	24
0.100000	24
0.100001	24
0.100002	80
0.200000	80
0.200002	80
0.200003	0
0.300000	0
0.300001	80
0.315000	80
0.315001	24
0.400000	24
0.400001	0
0.500000	0
0.500001	120
0.515000	120

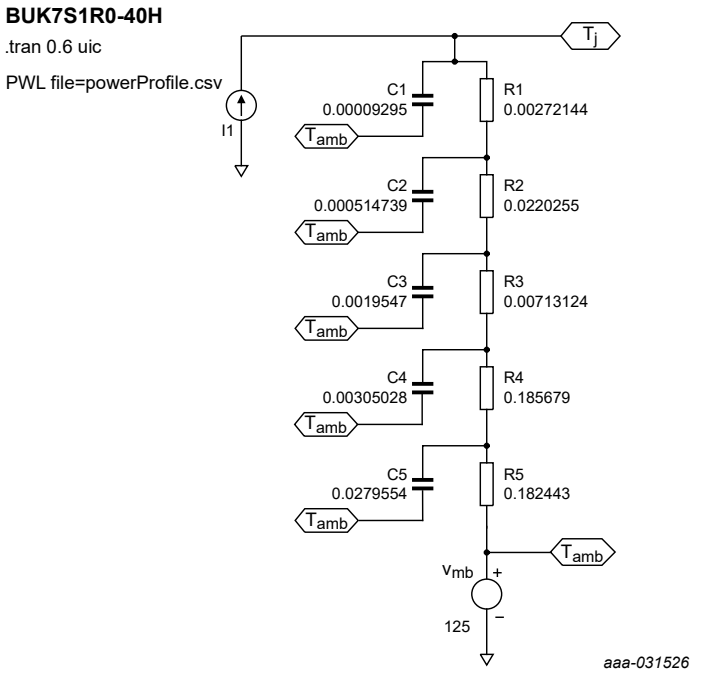


Fig. 10. SPICE circuit implementing a PWL file with the thermal model of the BUK7S1R0-40H

The simulation result is shown in Fig. 11. The junction temperature and thermal impedance values labeled in Fig. 11 demonstrate that the Z_{th} value at 4 ms, and R_{th} value, are in line with Fig. 12. It represents the thermal impedance waveform shown in the BUK7S1R0-40H data sheet.

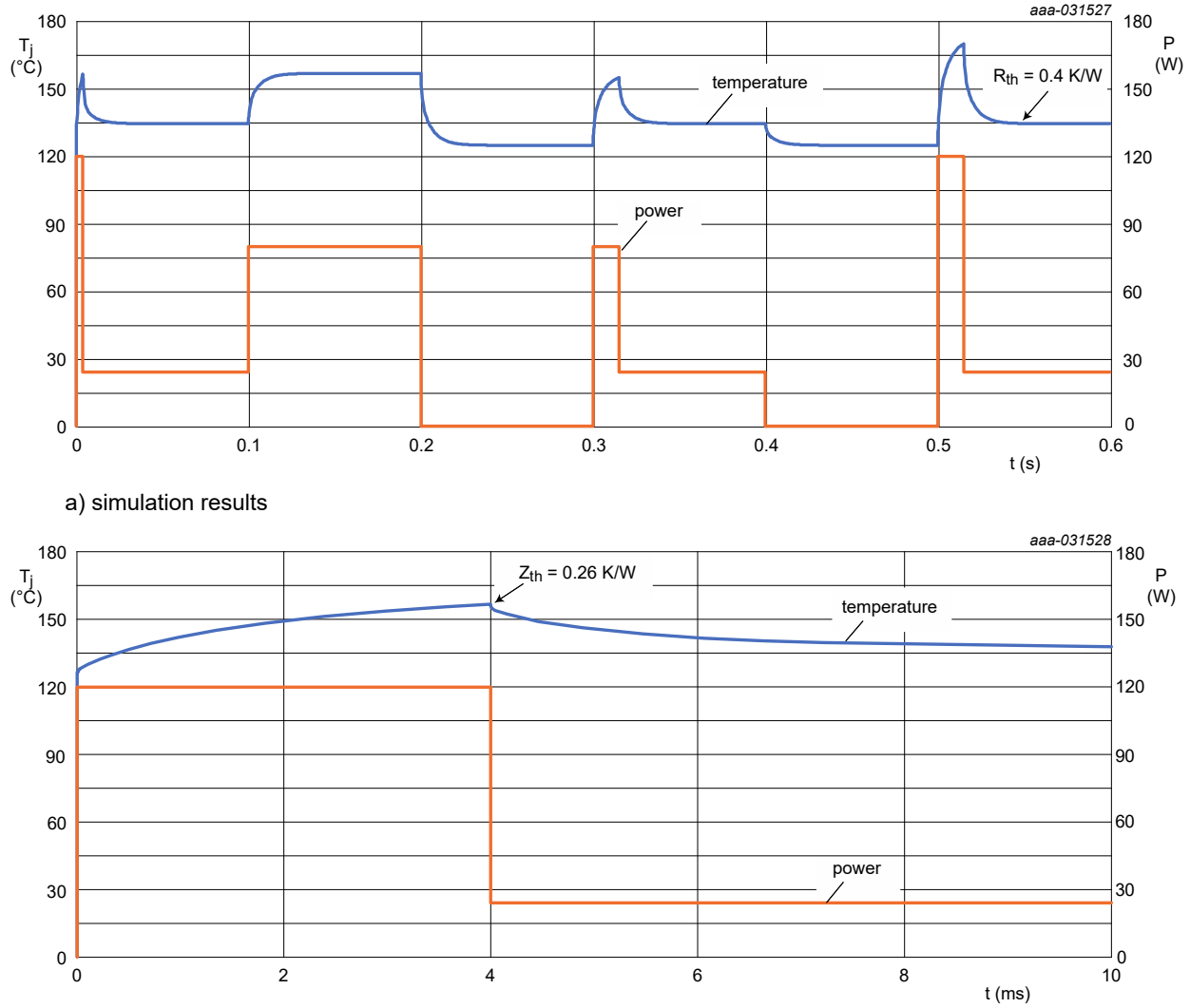
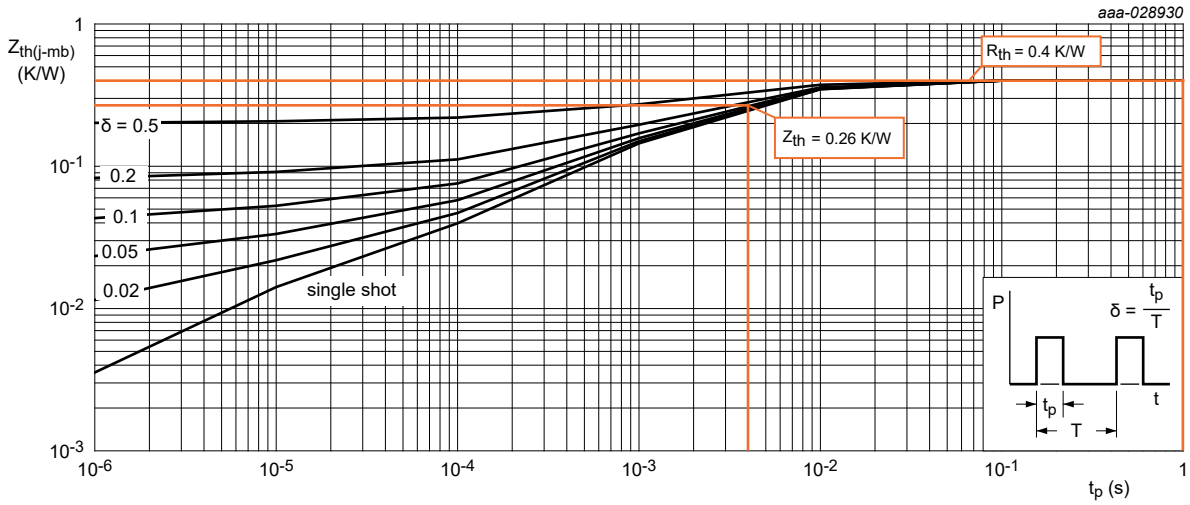


Fig. 11. Simulation results and first power pulse



The red lines highlight the thermal resistance and impedance for the example shown in Fig. 11

Fig. 12. Transient thermal impedance for BUK7S1R0-40H

6.3. Example 3

The aim of this example is to show how to perform thermal simulation using the power profile generated from a MOSFET circuit.

Following the steps in Section 6.1, set up the thermal model of BUK7S1R0-40H, and set the mounting base temperature to 85 °C.

To set the power value in the current source, construct a MOSFET electrical circuit as provided in Fig. 13. The power supply is 12 V. The gate drive supply is assigned a value of 10 V. It is set to run for 50 cycles with a 1 ms period and a 50 % duty cycle.

The power dissipated in the MOSFET can be calculated from Equation 6 or for greater accuracy; the gate current can be included into the calculation to give Equation 7:

$$P = V_{ds} \cdot I_d \tag{6}$$

To improve accuracy:

$$P = V_{ds} \cdot I_d + V_{gs} \cdot I_g \tag{7}$$

The current source into the thermal model can now be defined as:

$$I = V_{(d)} \cdot I(V_d) + V_{(g)} \cdot I(V_g) \tag{8}$$

Fig. 13 demonstrates the link between the electrical circuit and the thermal model circuit.

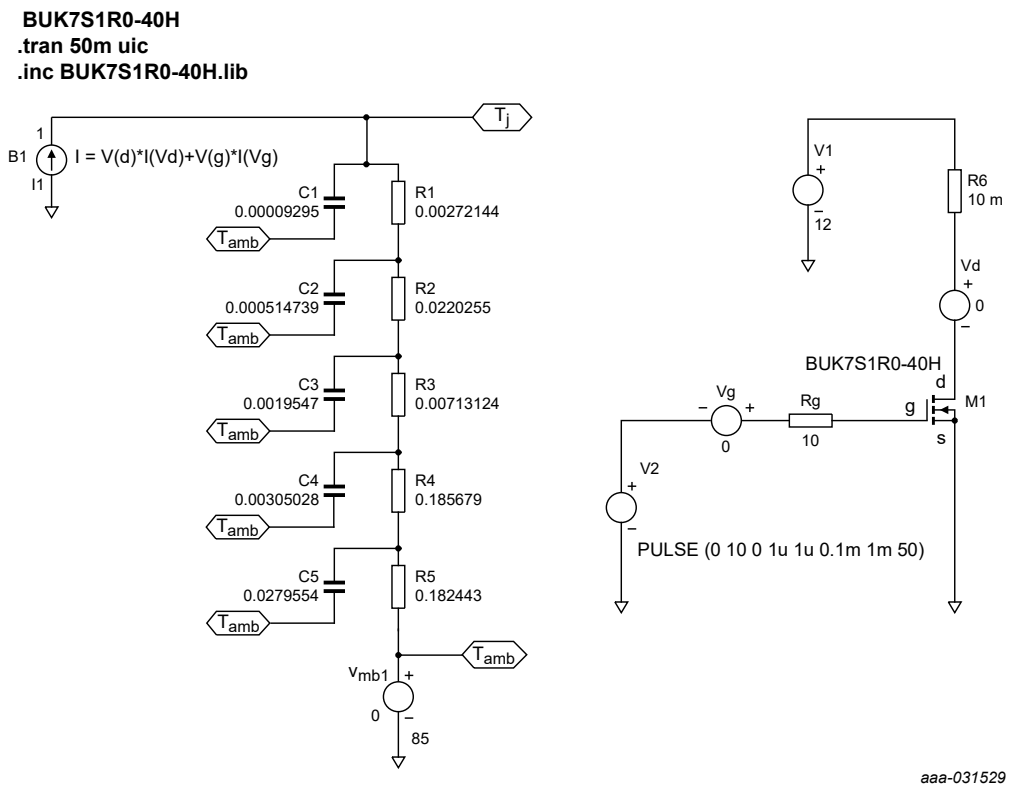


Fig. 13. SPICE circuit illustrating how to integrate an electrical circuit with a thermal model

The resultant plot of T_j is shown in Fig. 14. The maximum temperature of the junction can once again be calculated from data sheet values by following the steps outlined in Ref. 1.

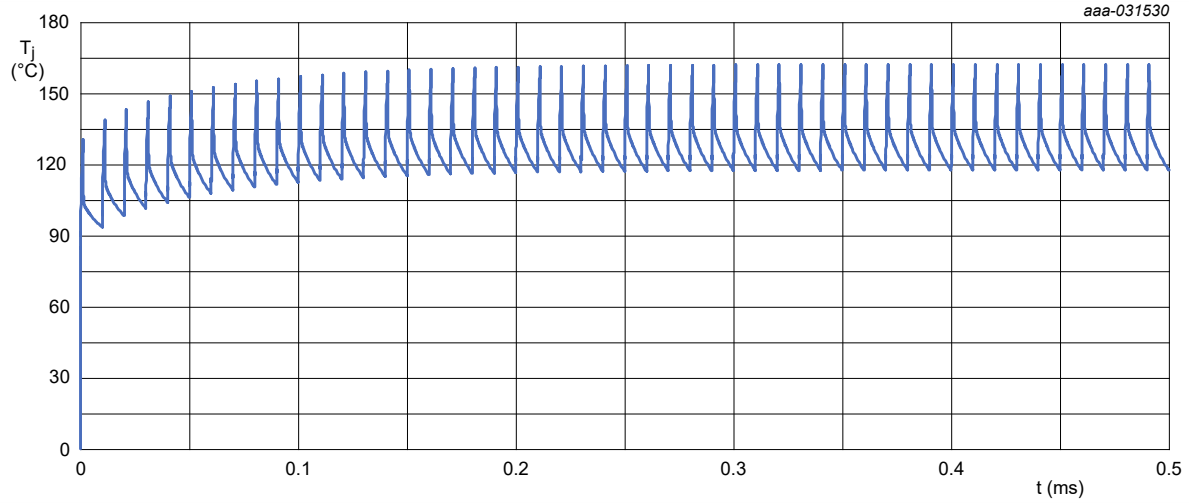


Fig. 14. Inferred junction temperature (T_j) rise provided by Fig. 12

7. Discussions

RC thermal models are not perfect. The physical materials used to build Semiconductors have temperature-dependent characteristics. These characteristics mean that thermal resistance is also a temperature-dependent parameter. Whereas in Ohm's law, the Ohmic resistance is usually considered to be constant and independent of the voltage. So the correspondence between electrical and thermal parameters is not perfectly symmetrical but gives a good basis for fundamental thermal simulations.

In power electronic systems, the thermal resistance of silicon amounts to 2 % to 5 % of the total resistance. The error resulting from the temperature dependence is relatively small and can be ignored for most cases. To obtain a more accurate analysis, replace the passive resistors in the RC model with voltage-dependent resistors. In these resistors, the change in temperature can correspond to change in voltage.

A further limitation of the models presented is that the mounting base temperature of the MOSFET T_{mb}, is set as an isothermal. This is rarely the case in real applications where a rise in the mounting base temperature must be considered. This rise is determined by calculating the temperature rise due to the average power dissipation (i.e. the heat flow) from the mounting base through to ambient. It means that the models are of limited use for pulses greater than 1 s, where heat begins to flow into the environment of the MOSFET. In this situation, the thermal model for the MOSFETs, PCB, heat sink and other materials in proximity must be included.

8. Summary

RC thermal models are available for Nexperia power MOSFETs on the Nexperia website. The models can be used in SPICE or other simulation tools to simulate the junction temperature rise in transient conditions. They provide a quick, simple and accurate method for application engineers to perform the thermal design.

9. Abbreviations

Table 4. Key to symbols used in equations

Symbol	Description
$P_{(t)}$	power as a function of time
$Z_{th(t)}$	transient thermal impedance
R_{th}	thermal resistance
τ	total time of heating pulse
τ_i	thermal time constant
R_i	constituent thermal resistance element
C_i	constituent thermal capacitance element
T_{mb}	mounting base temperature of the MOSFET
T_j	junction temperature of the MOSFET
$T_{j(rise)}$	junction temperature rise in the MOSFET
ΔT	change in temperature
V_{ds}	drain to source voltage of the MOSFET
V_{gs}	gate to source voltage of the MOSFET
I_d	drain current

10. References

1. Application note AN11156 - “Using Power MOSFET Z_{th} Curves”. Nexperia Semiconductors
2. Application note AN10273 - “Power MOSFET single-shot and repetitive avalanche ruggedness rating”. Nexperia Semiconductors
3. Combination of Thermal Subsystems Modeled by Rapid Circuit Transformation. Y.C. Gerstenmaier, W. Kiffe, and G. Wachutka
4. JEDEC Standard JESD51-14 Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat Flow Through a Single Path

11. Revision history

Table 5. Revision history

Revision number	Date	Description
4.0	20200511	Modifications: • Section 5 updated to include Cauer model netlist.
3.0	20200504	Modifications: • Updated to include Cauer models. • Simulations have been updated using latest released technology T9 and replacing Foster models with Cauer models. • The format of this application note has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate.
2.0	20140519	Second issue. Modifications: • Fig. 9 is updated.
1.0	20140129	first issue

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