

Description

The AL58263A is a 16-channel constant-current LED driver featuring 16-bit grayscale Adaptive Pulse Density Modulation (APDM) for high-accuracy dimming and enhanced visual performance. The APDM dimming architecture improves output current linearity by mitigating non-ideal transient behavior and increases system refresh rate by effectively separating frame waveform components.

The device operates from 3.0V to 5.0V input supply, supports output channel voltages up to 15V, and interfaces with a 25MHz DCK clock. Each channel delivers up to 45mA of precise, programmable LED current. Channel-level current settings are configurable through the digital interface, while the overall output current range is established using a single external sensing resistor together with two independent 4-bit global current-gain controls, providing separate current adjustment for Group A and Group B channel banks.

The AL58263A integrates comprehensive fault detection and diagnostic, including LED open/short detection. Diagnostic results are stored in internal registers for MCU access via the serial interface.

Compact Wettable Flank W-QFN4040-24/SWP (Type A1) package available, the device is specified for operation across -40°C to +105°C ambient temperature range, making it well-suited for demanding automotive lighting applications.

Features

- **Output Current Range:**
 - 2mA to 45mA @ 5.0V
- **16 Constant-Current Sink Output Channels**
 - 16-bit Grayscale Resolution
 - Two 4-bit Global Current Control
 - ±1.5% (typ) Channel-to-Channel LED Current Accuracy
 - ±3% (typ) Chip-to-Chip LED Current Accuracy
 - Staggered Output Delay for EMI Reduction
 - Supporting Cascaded Devices
- **Detection and Diagnostics**
 - LED Open, LED Short, Output Port Leakage
 - Output Short-to-GND, Output Short-to-Power
 - REXT Short-to-GND
 - Pre-Overtemperature Warning
- **4-Wire Serial Interface + GCK (LAT, DI, DO, DCK + GCK)**
 - Double-Edge Grayscale Clock (GCK) up to 16MHz
 - External GCK Watchdog Timer
 - Zero-Data and Sleep Modes for Power Saving
- **Register-Programmable Options**
 - Regular PWM or Adaptive Pulse Density Modulation
 - Internal PWM Generator or External Grayscale Clock (GCK)
 - Selectable Short-Detection Thresholds: 2V/3V/4V/4.5V
- **Environmental Compliance**
 - **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
 - **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**
<https://www.diodes.com/quality/product-definitions/>

Notes:

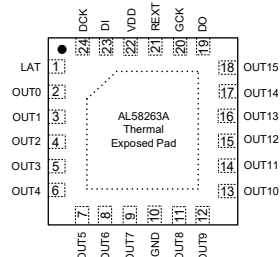
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignments

(3D Photo – Not to Scale)



(Top View – Not to Scale)

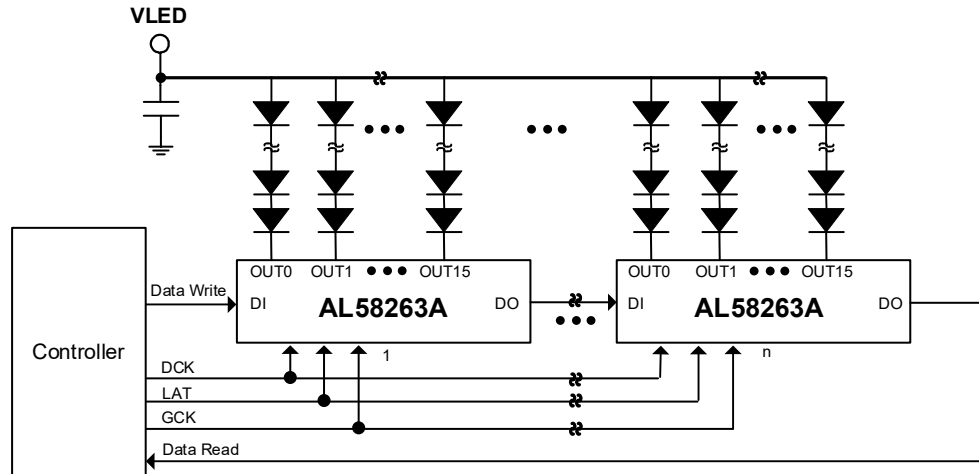


W-QFN4040-24/SWP (Type A1)

Applications

- Interior lighting
- RGB lighting
- HVAC control panels
- Exterior lighting

Typical Applications Circuit

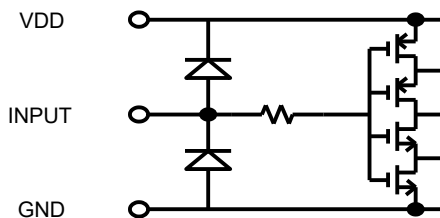


Pin Descriptions

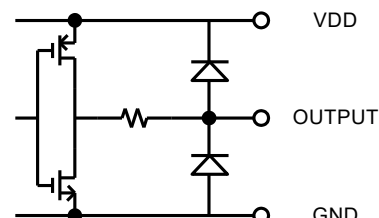
Pin Name	Pin Number	Description
	W-QFN4040-24/SWP (Type A1)	
LAT	1	Input terminal of data strobe and mode setting. Combine DCK with LAT signal to execute the mode control.
OUT0 to OUT7	2 to 9	Sink constant-current outputs (open-drain) of group A.
OUT8 to OUT15	11 to 18	Sink constant-current outputs (open-drain) of group B.
GND	10	Ground terminal.
DO	19	Serial data output terminal.
GCK	20	External double-edge grayscale clock input for APDM operations.
REXT	21	External resistors connected between REXT and GND for output current value setting.
VDD	22	Supply voltage terminal.
DI	23	Serial data input terminal.
DCK	24	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.

Equivalent Circuit of Inputs and Outputs

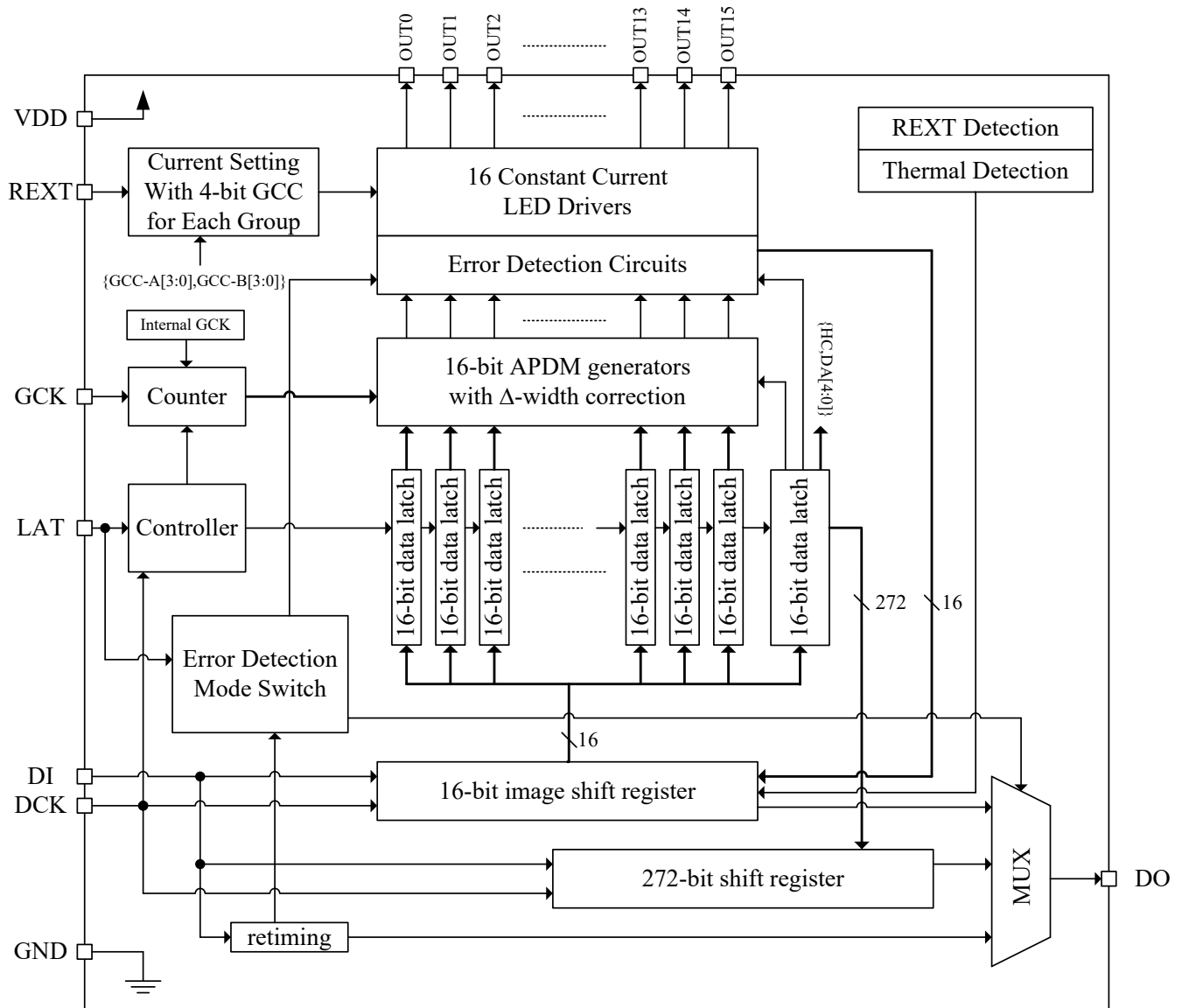
1. DCK, DI, LAT, GCK Terminals (INPUT)



2. DO Terminal (OUTPUT)



Functional Block Diagram



Absolute Maximum Ratings (Notes 4 & 5)

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage	-0.3 to 7.0	V
V _{DI} , V _{DCK} , V _{GCK} , V _{LAT}	Input Voltage	-0.3 to V _{DD} +0.3	V
I _{OUT}	Output Current	60	mA
V _{OUT}	Output Voltage	-0.3 to 16	V
f _{DCK}	Input Clock Frequency	25	MHz
f _{GCK}	Input Grayscale Frequency	16	MHz
I _{GND}	GND Terminal Current	960	mA

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. All voltage values are with respect to ground terminal.

ESD Ratings

Symbol	Parameter	Value	Unit
V _{ESD}	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	750	V

Package Thermal Information (Note 6)

Symbol	Thermal Resistance	Device	Unit
		W-QFN4040-24/SWP (Type A1)	
R _{θJA}	Junction-to-Ambient Thermal Resistance	31.16	°C/W
R _{θJC(top)}	Junction-to-Case (Top) Thermal Resistance	17.25	°C/W
R _{θJB}	Junction-to-Board Thermal Resistance	9.34	°C/W
Ψ _{JT}	Junction-to-Top Characterization Parameter	0.41	°C/W
Ψ _{JB}	Junction-to-Board Characterization Parameter	9.14	°C/W
R _{θJC(bot)}	Junction-to-Case (Bottom) Thermal Resistance	3.33	°C/W

Note: 6. Measured on EIA/JESD51-7, 4-layer PCB. For better thermal performance, larger copper pad for heatsink is needed

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Operating Supply Voltage	3.0	3.3	5.0	V
I _{OUT}	Output Current (Note 7)	2	—	45	mA
V _{OUT}	Output Voltage	1	—	15	V
T _A	Ambient Temperature (Note 7)	-40	—	+105	°C
T _J	Junction Temperature	-40	—	+125	°C
T _{STG}	Storage Temperature	-55	—	+150	°C

Note: 7. Dependent on ambient temperature, LED voltage, package thermal limitation, and PCB layout.

Electrical Characteristics (V_{DD} = 5.0V @T_A = -40°C to +105°C, unless otherwise specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage "H" Level	V _{IH}	CMOS logic level	0.7V _{DD}	—	V _{DD}	V
Input Voltage "L" Level	V _{IL}	CMOS logic level	GND	—	0.3V _{DD}	
Output Leakage Current	I _{LK}	V _{OUT} = 15V	—	—	0.2	μA
Driving Current (DO)	I _{OL}	V _{OL} = 0.4V	1	3.4	5	mA
	I _{OH}	V _{OH} = V _{DD} -0.4	-5	-3.4	-1	
Output Current Skew (Channel-to-Channel) (Note 8)	dI _{OUT1}	V _{OUT} = 1.0 V R _{REXT} = 870Ω	—	±1.5	±3.5	%
Output Current Skew (Chip-to-Chip) (Note 9)	dI _{OUT2}	GCC-A/B = 1111 T _J = +25°C	—	±3	±6	%
Output Voltage Regulation (Note 10)	%/V _{OUT}	R _{REXT} = 870Ω V _{OUT} = 1V to 3V	—	±0.1	±.1	% / V
Supply Voltage Regulation (Note 11)	%/V _{DD}	R _{REXT} = 870Ω V _{DD} = 3V to 5.0V	—	±0.6	±1	
Supply Current (Note 12)	I _{DD1(off)}	R _{REXT} = 870Ω All outputs turn off	1	5.5	9.7	mA
	I _{DD2(on)}	R _{REXT} = 870Ω All outputs turn on	1	5.5	9.7	
Thermal Alarm Temperature	T _{AL}	—	—	+155	—	°C
Thermal Alarm Temperature Hysteresis	T _{AL_HYS}	—	—	+15	—	°C

Notes: 8. Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{I_{out_n}}{(I_{out_0} + I_{out_1} + \dots + I_{out_{15}})} - 1 \right] * 100\%$$

9. Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{(I_{out_0} + I_{out_0} + \dots + I_{out_{15}})}{16} - (Ideal\ Current\ at\ Temperature) \right] * 100\%$$

10. Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{I_{out_n}(@V_{out_n} = 3V) - I_{out_n}(@V_{out_n} = 1V)}{I_{out_n}(@V_{out_n} = 3V)} \right] * \frac{100\%}{3V - 1V}$$

11. Supply voltage regulation is defined by the formula below:

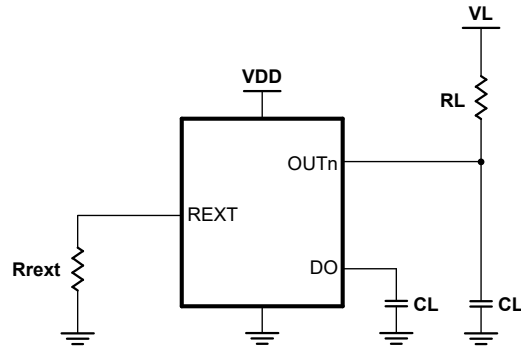
$$\Delta(\%/V) = \left[\frac{I_{out_n}(@V_{DD} = 5.5V) - I_{out_n}(@V_{DD} = 3V)}{I_{out_n}(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

12. IO excluded.

Switching Characteristics ($V_{DD} = 5.0V$ @ $T_A = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise specified, guaranteed by design.)

Characteristic		Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay ('L' to 'H')	DCK-DO	t_{pLH3}	$V_{IH} = V_{DD}$ $V_{IL} = GND$ $R_{REXT} = 870\Omega$ $V_L = 5.0V$ $R_L = 150\Omega$ $C_L = 13pF$	—	30	60	ns
Propagation Delay ('H' to 'L')	DCK-DO	t_{pHL3}		—	30	60	
Pulse Duration	LAT	$tw_{(LAT)}$		50	—	—	
	GCK	$tw_{(GCK)}$		20	—	—	
	DCK	$tw_{(DCK)}$		20	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		20	—	—	
	DI	$tsu_{(D)}$		5	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		5	—	—	
Hold Time of Instruction		$th_{(CM)}$		20	—	—	
LED Error Detection Time		t_{err1}		500	—	—	
Short-to-Ground Detection Time		t_{err3}		500	—	—	
Interval Between Two Command Pulses		t_{pls}		230	250	—	
Wake-up Time from Sleep or 0-Data Mode		$twake$		—	—	4000	μs
Data Clock Frequency		f_{DCK}		—	—	25	MHz
Grayscale Clock Frequency (Double-Edge)		f_{GCK}		—	—	16	

Switching Characteristics Test Circuit

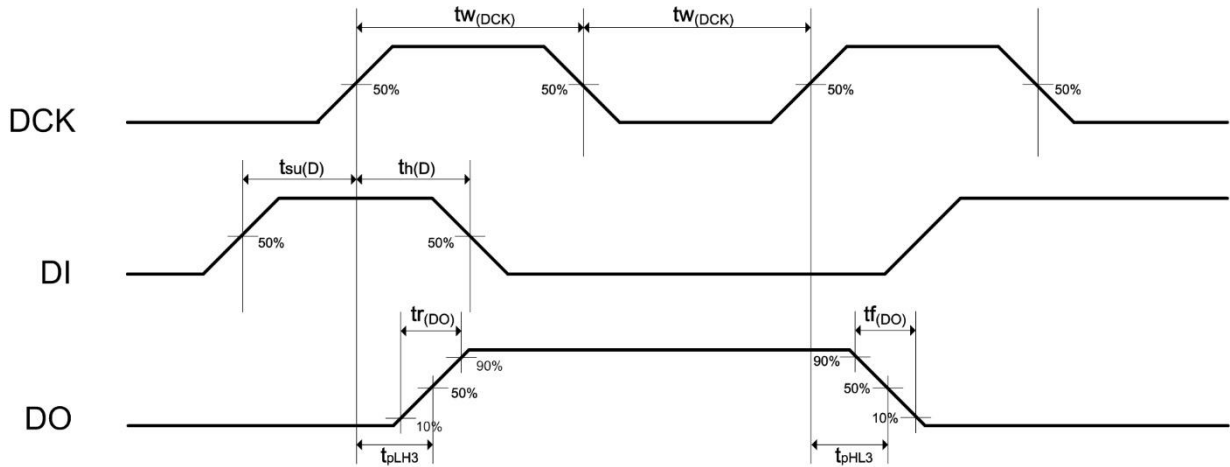


Switching Characteristics Test Circuit

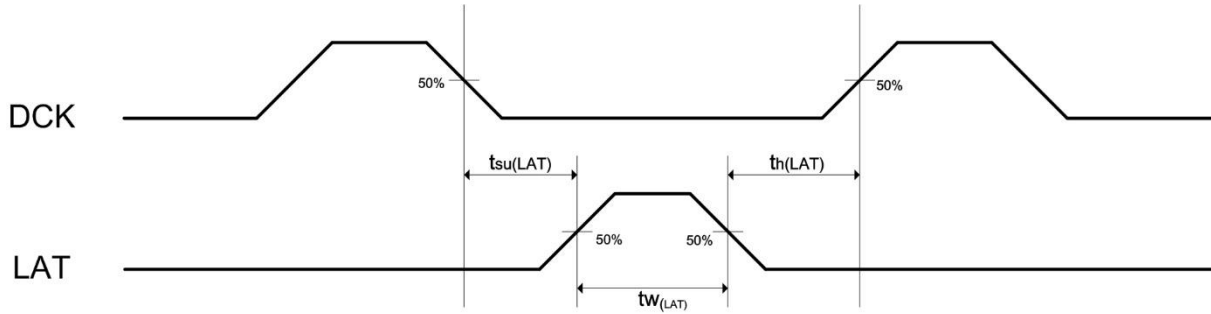
Timing Characteristics

Timing Diagram

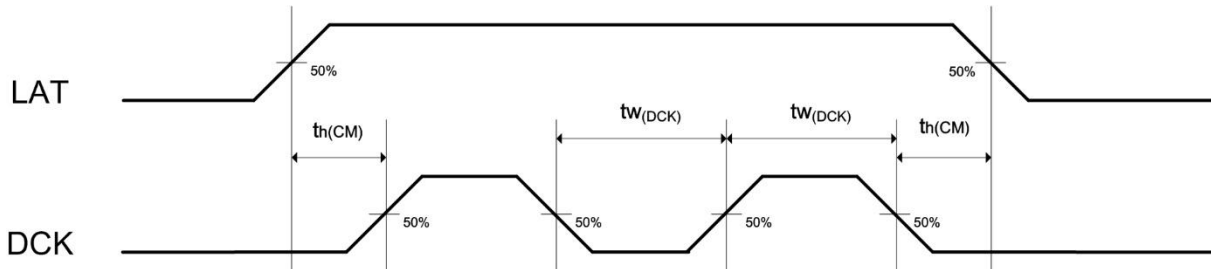
1. DCKI-DI, DO



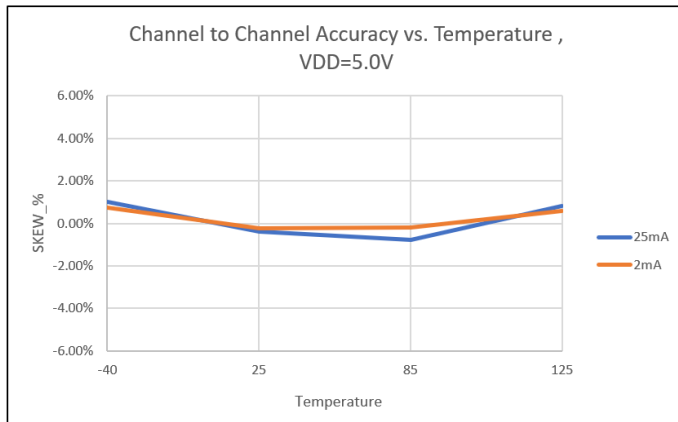
2. GCK-LAT



3. LAT-DCK (Instruction)

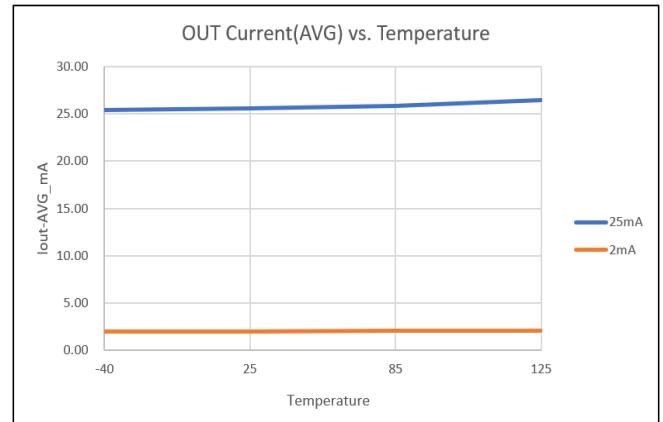


Typical Performance Characteristics ($V_{DD} = 5V$, $-40^{\circ}C < T_A < +105^{\circ}C$, unless otherwise specified.)



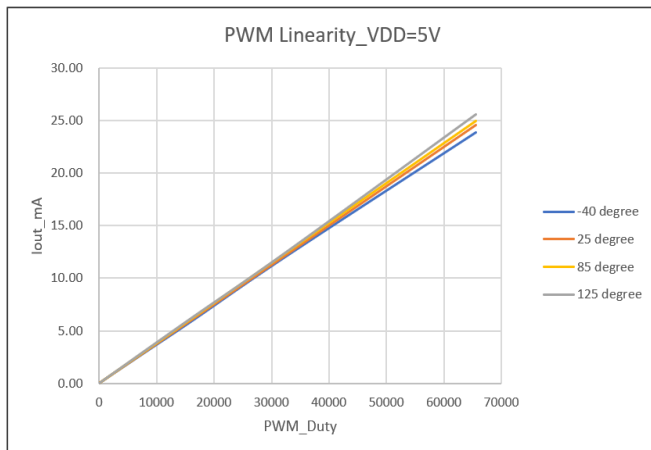
$V_{DD} = 5V$, $I_{OUT} = 25mA$, $2mA$

Figure 1. Channel to Channel Accuracy vs. Temperature



$V_{DD} = 5V$, $I_{OUT} = 25mA$, $2mA$

Figure 2. Output Current (AVG) vs. Temperature



$V_{DD} = 5V$, $I_{OUT} = 25mA$

Figure 3. PWM Linearity vs. Temperature

Functional Descriptions

Fast Transient Response

The AL58263A supports the fast transient response to make high image resolution possible. The GCK period of 50ns is enough to get a complete V_{OUT} waveform.

Stagger Outputs Delay

Large inrush currents will be induced when the system activates all the outputs at once. To reduce this interference of EMI, the AL58263A is designed to have a constant length of delay time (around 16ns) between two output groups. The first group is OUT2n and the second group is OUT2n+1 (n = 0 to 7).

Global Current Control (GCC)

The AL58263A provides 4bits global current control (GCC) for each output group, where command bit GCC-A[3:0] is set for output group A (out0 to 7) and GCC-B[3:0] is set for output group B (out8 to 15). The relationship between the Gain value and GCC bits is described below:

GCC-A[3:0]	Gain-A
0	7.7%
1	15.4%
2	23.1%
3,4	30.8%
5	38.5%
6	46.2%
7,8	53.8%
9	61.5%
10	69.2%
11,12	76.9%
13	84.6%
14	92.3%
15	100.0%

GCC-B[3:0]	Gain-B
0	7.7%
1	15.4%
2	23.1%
3,4	30.8%
5	38.5%
6	46.2%
7,8	53.8%
9	61.5%
10	69.2%
11,12	76.9%
13	84.6%
14	92.3%
15	100.0%

Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$I_{out}(mA) \approx \frac{22.7 \times \text{Gain}}{R_{EXT}(k\Omega)}$$

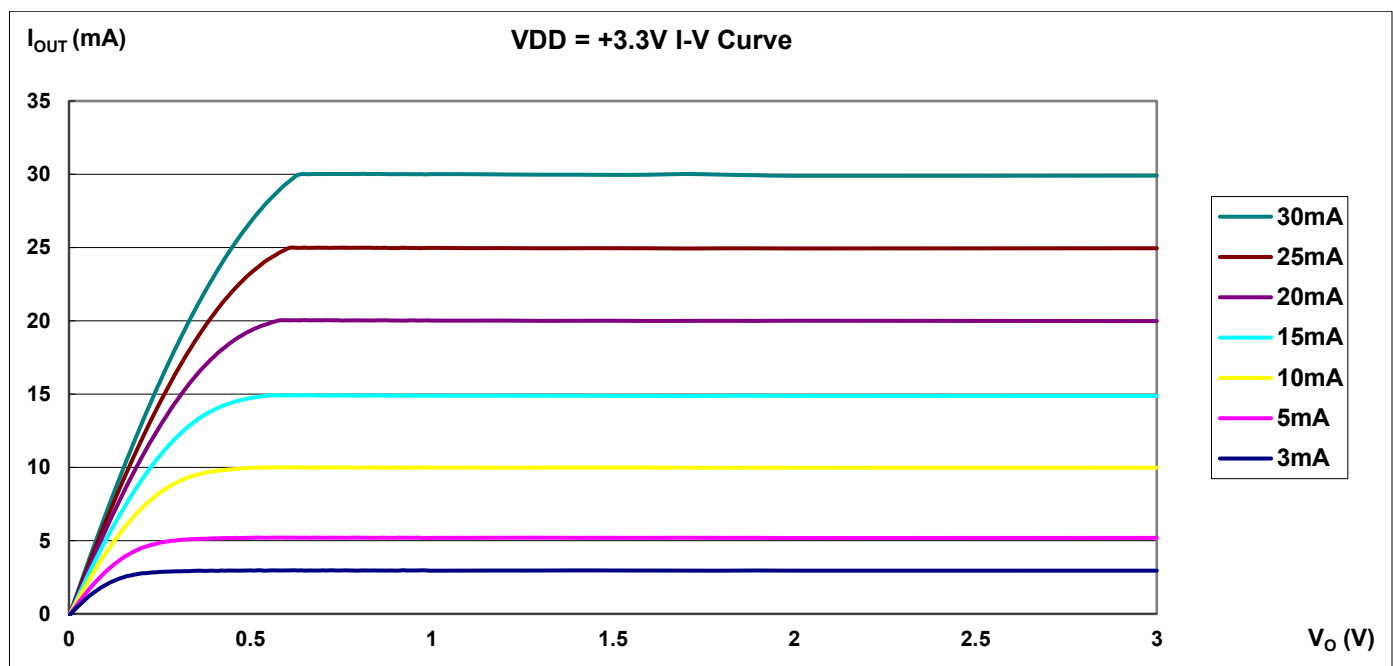
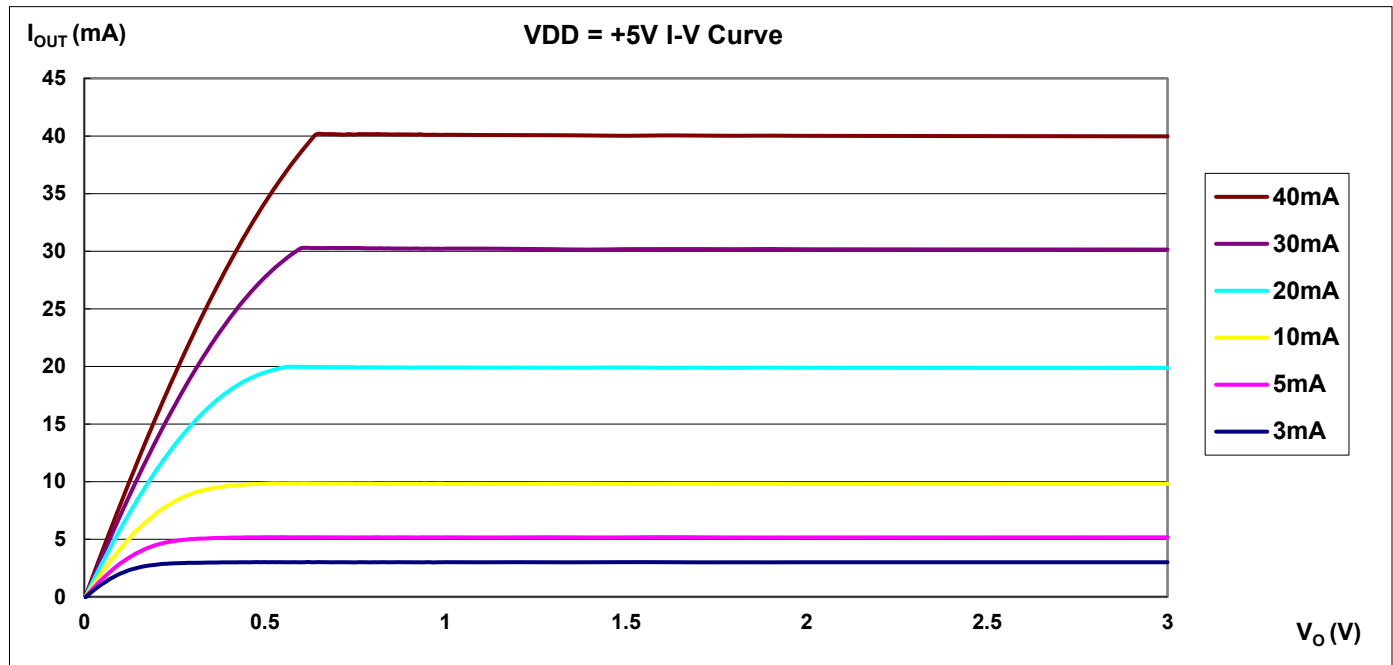
This constant value 22.7 may need to be adjusted slightly based on users' application and test conditions.

Where R_{EXT} is a resistor placed between REXT and GND.

Functional Descriptions (continued)

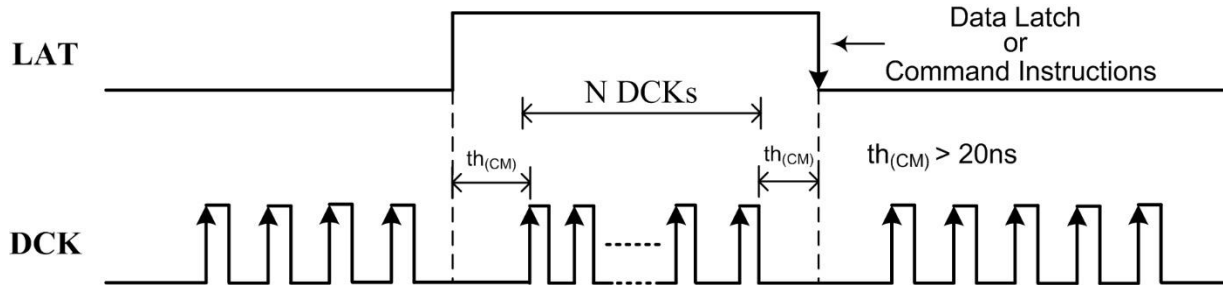
Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the AL58263A could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage that should be determined in order to maintain an excellent performance.



Functional Descriptions (continued)

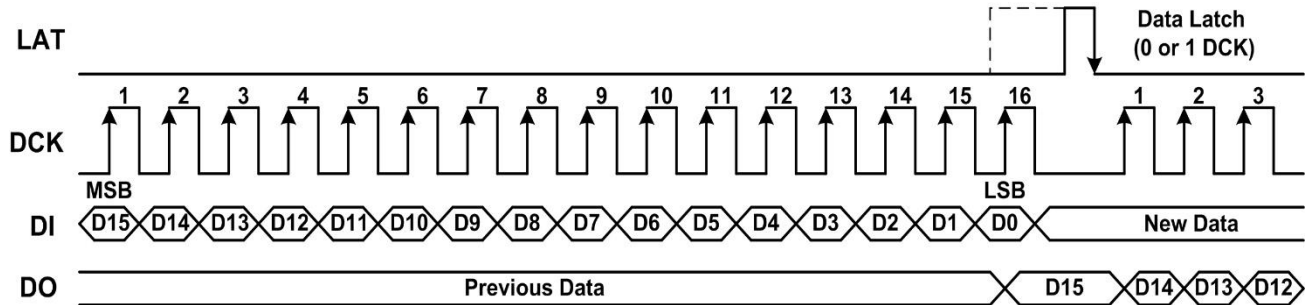
Control Instructions



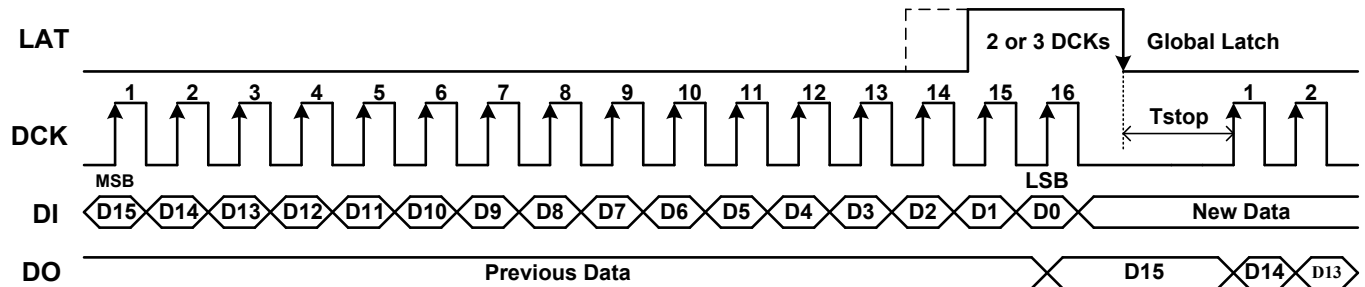
Instruction Name	Number of DCK Pulses when LAT is at High	Function Description
Data Latch	0 or 1	Strobes image data into temporary registers. In this time, constant current outputs are not updated to a new frame data.
Global Latch	2 or 3	Strobes image data from temporary registers into an APDM/PWM generator. In this time, constant current outputs are updated to a new frame data.
Reading Image Data and Command Data	6 or 7	Read out image data and command data from the latch cell to the 272bits shift registers. And the read data could shift out from DO pin by serial DCK pulses.
Return to Normal Mode	8 or 9	Switch Back from the reading data mode to the normal operating mode.
Writing Command	10 or 11	Strobes command data from the 16bits shift register into the command latch cell.

Functional Descriptions (continued)

Data Latch

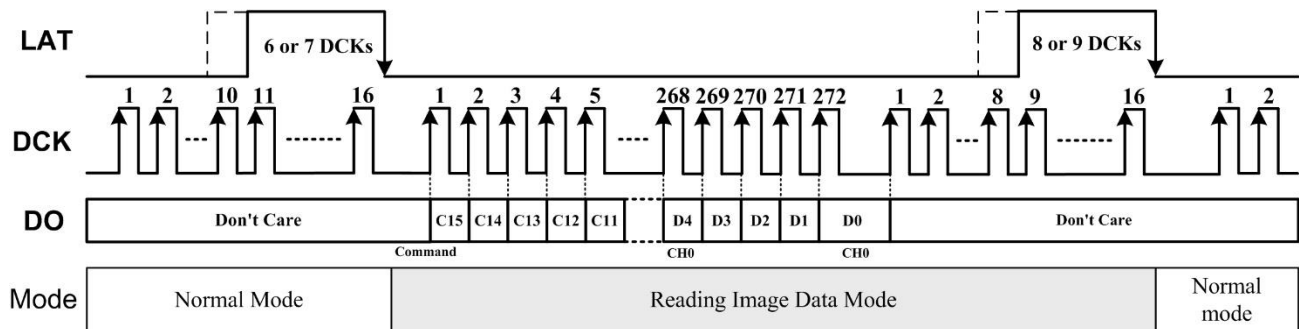


Global Latch

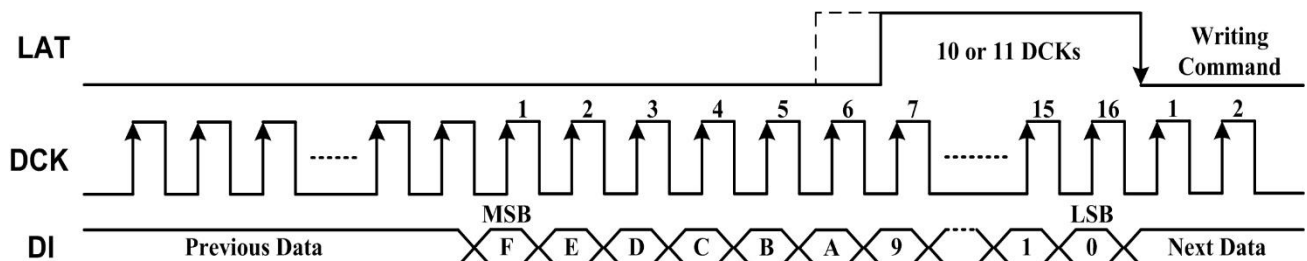


The DCK after the falling edge of Global Latch must wait a Tstop time, where Tstop must be longer than 2 grayscale clock cycle time of GCK or internal oscillator.

Reading Image Data and Command Data

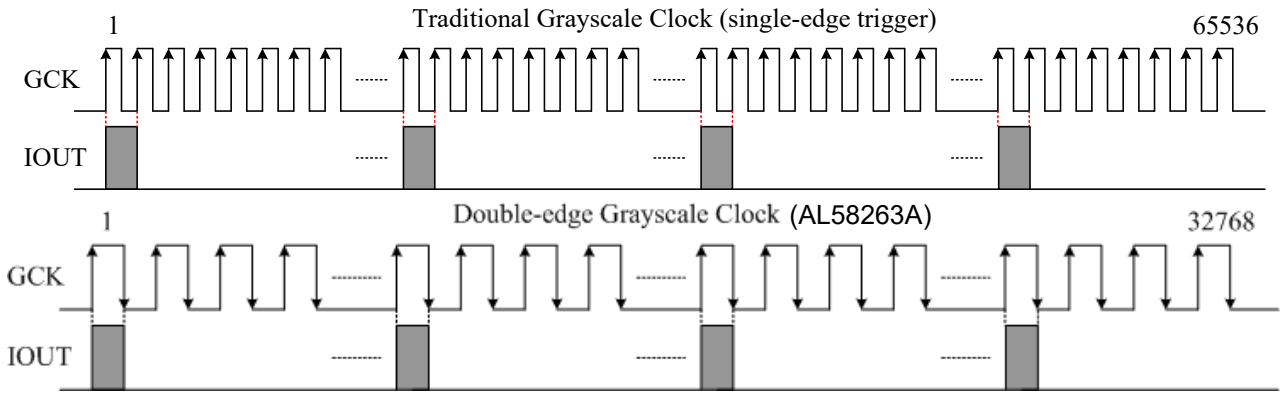


Writing Command



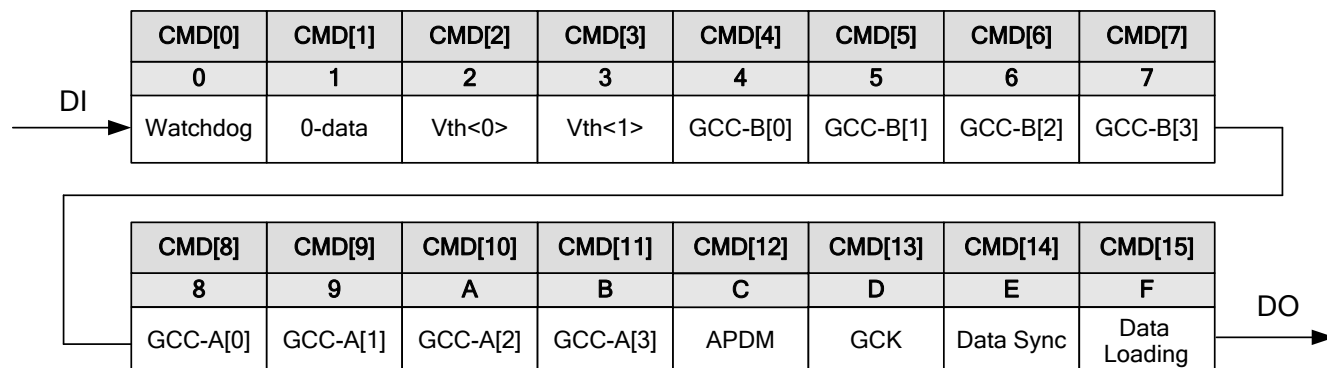
Functional Descriptions (continued)

EMI Reduction Grayscale Clock (Double-Edge Grayscale Clock)



A whole period of 16bits resolution must be composed by 65536 traditional grayscale clocks because constant current outputs only are triggered at the rising edge of clocks. Therefore, a controller has to transmit fast grayscale clocks in order to accomplish high refresh rate when users adopt traditional PWM chips. The AL58263A supports a specific mode of double-edge grayscale clocks which trigger both at rising and falling edges of clocks. By this approach, a whole period of 16bits resolution is composed of only 32768 double-edge grayscale clocks and the electromagnetic interference would be decreased substantially due to slow grayscale clocks.

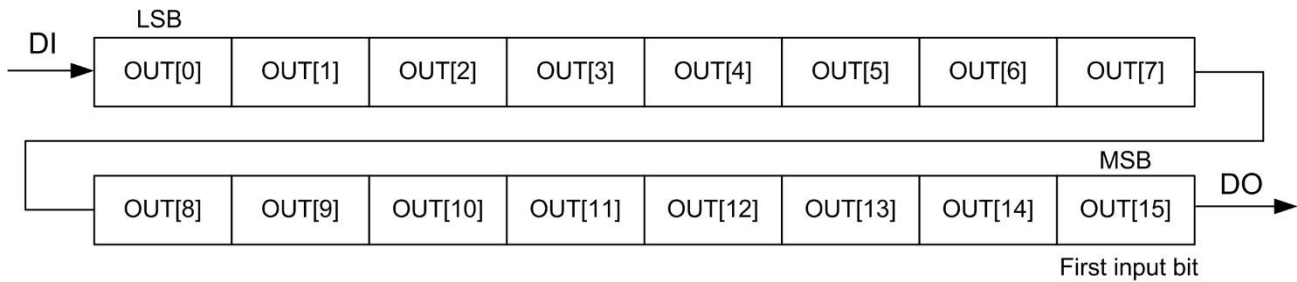
Functional Descriptions (continued)

Command Data Format


CMD Bit	Initial Value	Value	Function	Description
CMD[15]	1'b0	1'b0	Mode0	Data transmitting format: 15 times of data latch + one global latch
		1'b1	Mode1	Data transmitting format: 16 times of data latch + one global latch
CMD[14]	1'b0	1'b0	Auto Synchronization	When the device receives a latch signal, the new frame is updated until the end of old frame.
		1'b1	Manual Synchronization	When the device receives a latch signal, the new frame is updated immediately
CMD[13]	1'b0	1'b0	External GCK	The GCK signal stems from an external source.
		1'b1	Internal GCK	The GCK signal stems from an internal oscillator, typ 1.7MHz at 3.3V and 2.8MHz at 5V (When CMD[13] = "1", please set CMD[0] = "0")
CMD[12]	1'b0	1'b0	High Refresh Rate	Refresh rate of APDM selection: when CMD[12] = 1'b0 => High refresh rate when CMD[12] = 1'b1 => Low refresh rate
		1'b1	Low Refresh Rate	
CMD[11:8]	4'b0010	4'b0000 to 4'b1111	GCC-A[3:0]	4bits global current control for output group A
CMD[7:4]	4'b1011	4'b0000 to 4'b1111	GCC-B[3:0]	4bits global current control for output group B
CMD[3:2]	2'b00	2'b00 2'b01 2'b10 2'b11	2.0V 3.0V 4.0V 4.5V	Threshold voltage for LED short detection (Both at V _{DD} = 5V and 3.3V)
CMD[1]	1'b0	1'b0	Disable	Enter 0-data power saving mode when 16bits PWM data of 16ch are all zeros.
		1'b1	Enable	
CMD[0]	1'b0	1'b0	Disable	GCK watchdog All IOUTs will be turned off automatically when GCK keeps high or low level over ~15ms. (Result can be read out by "Thermal Detection Mode" or "REXT Detection Mode")
		1'b1	Enable	

Functional Descriptions (continued)

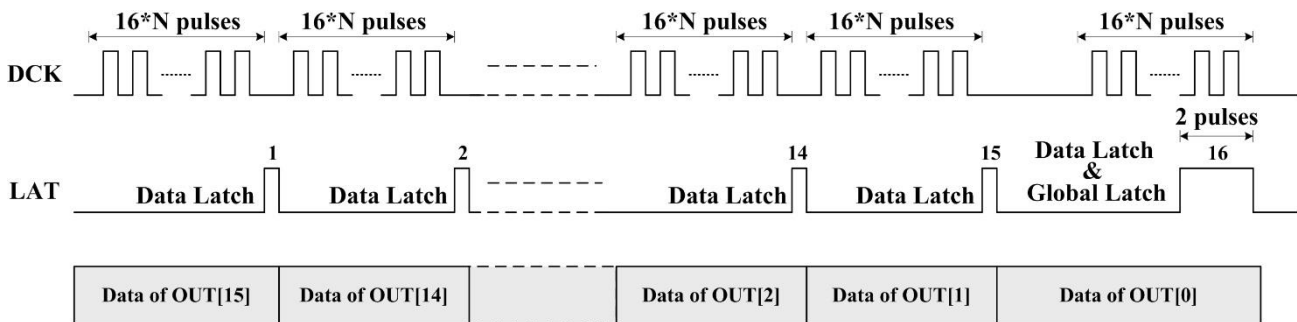
Image Data Format



16bits APDM/PWM data are transmitted into the 16bits shift register according to the format illustrated above. The first input bit is the most significant bit of each channel.

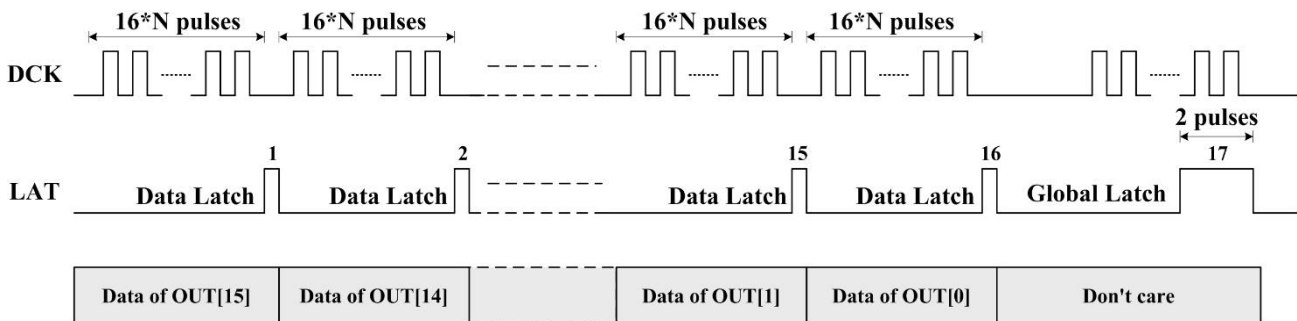
Data Transmitting Protocol

MODE0 (CMD[15] = "0")



This data transmitting mode is comprised of 15 data latches and one global latch. The first data latch strobes image data for **OUT[15]**. And the last global latch strobes image data for **OUT[0]** and loads all image data of 16 channels into the APDM/PWM generator. N is the number of devices in series.

MODE1 (CMD[15] = "1")

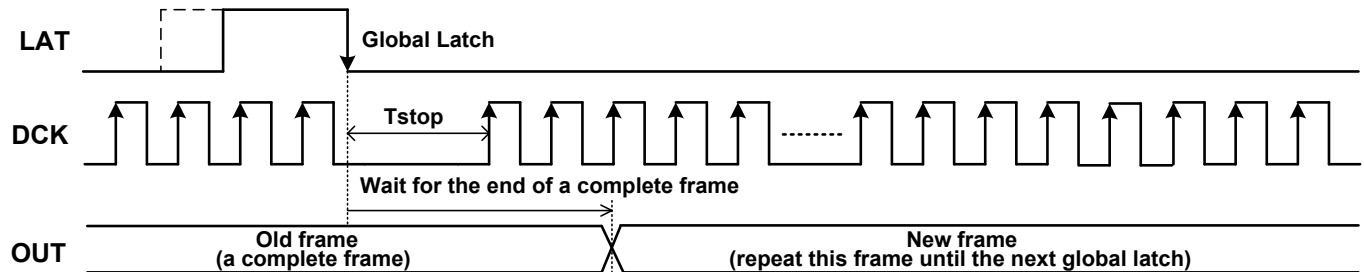


This data transmitting mode is comprised of 16 data latches and one global latch. The first data latch strobes image data for **OUT[15]**. And the last global latch loads all image data of 16 channels into the APDM/PWM generator but doesn't strobe any image data for output channels. N is the number of devices in series.

Functional Descriptions (continued)

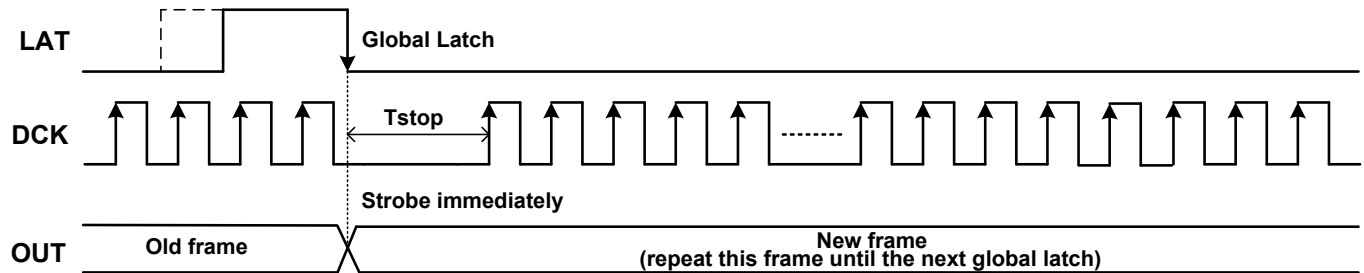
Data Synchronization

Auto Synchronization (CMD[14] = "0")



The AL58263A could abate the grayscale loss during the renewal of frame by this approach of auto synchronization. When the command bit CMD[14] is set to "0", this function could be executed automatically. After a global latch, all OUTs would accomplish a complete frame of old data and then update new frame data. Therefore, each frame maintains the fixed time and the assigned grayscale. A controller can just provide a free-running GCK or use the internal oscillator for grayscale display in this mode.

Manual Synchronization (CMD[14] = "1")



When the command bit CMD[14] is set to "1", the new frame data would be updated, and the grayscale counter would be reset immediately. The old frame loses probably a little grayscale due to a non-complete frame time. In this mode, a controller must calculate carefully the number of GCKs to synchronize the frame.

Functional Descriptions (continued)

Adaptive Pulse Density Modulation with Δ -Width Correction

Adaptive Pulse Density Modulation (APDM) is a technique to improve output current waveform distortion and increase visual refresh rate. And the Δ -width correction ($\Delta \neq 0$) is used to compensate for the non-ideal output current transient response.

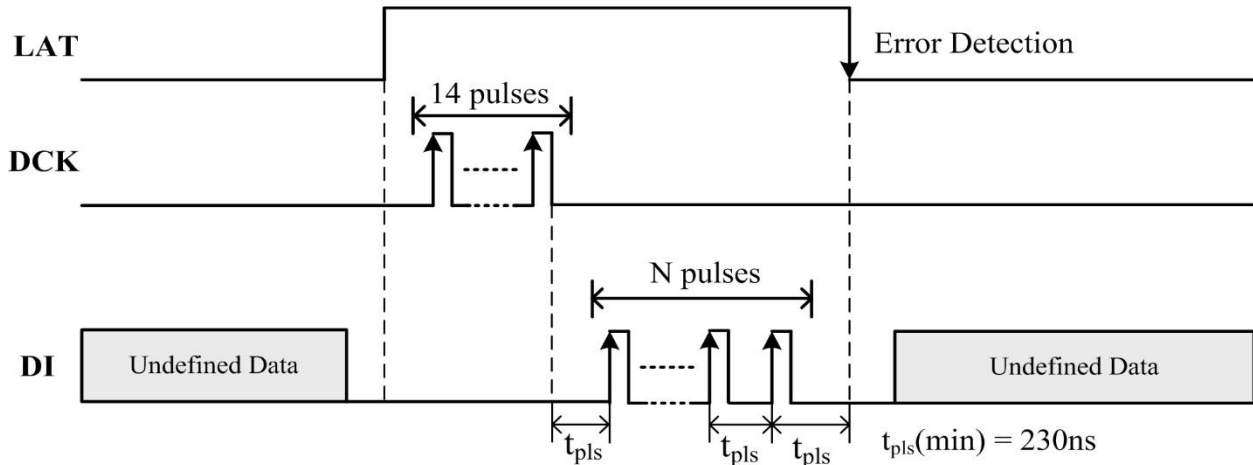
When CMD[12] = "0", the output waveform operates at high refresh rate mode. The output waveform is divided into 512 segments to increase visual refresh rate. The visual refresh rate = $(\text{GCK frequency} \times 2) / (65536 / 512)$.

When CMD[12] = "1", the output waveform operates at low refresh rate mode. The output waveform is divided into only 4 segments. The visual refresh rate = $(\text{GCK frequency} \times 2) / (65536 / 4)$. It's suitable to drive high power LED and decrease the transient loss.

Functional Descriptions (continued)

Diagnosis and Protections

Error Detection Mode Instructions



Instruction Name	Number of DI Pulses when LAT is at High	Function Description
LED Open Detection	2	Execute the LED Open Detection no matter what the image data is. The image strobe will occur at the falling edge of LAT signal.
LED Short Detection	4	Execute the LED Short Detection no matter what the image data is. The image strobe will occur at the falling edge of LAT signal.
Short-to-GND Detection	6	Execute the Short-to-GND Detection no matter what the image data is. The device will detect each IOUT pin if short-to-ground or not. The image strobe will occur at the falling edge of LAT signal.
Thermal Detection & Watchdog Result Read Out	8	The device will load thermal detection result and watchdog detection result into the 16 th and 1 st image shift register by this instruction. The thermal error occurs when the junction temperature is over +155°C.
LED Smart Detection	10	Execute the LED Smart Detection no matter what the image data is. The device will detect LED Open and LED Short error simultaneously by this instruction. The image strobe will occur at the falling edge of LAT signal.
Sleep Mode	12	This instruction forces the device into Sleep Mode at the falling edge of LAT signal, then keeps GCK = high most internal circuits will shut down. The device will be activated in the following LAT signal.
REXT Pin Detection & Watchdog Result Read Out	14	The device will load REXT detection result and watchdog detection result into the 16 th and 1 st image shift register by this instruction. The REXT error occurs when the REXT pin is short-to-GND or above 2.5V.

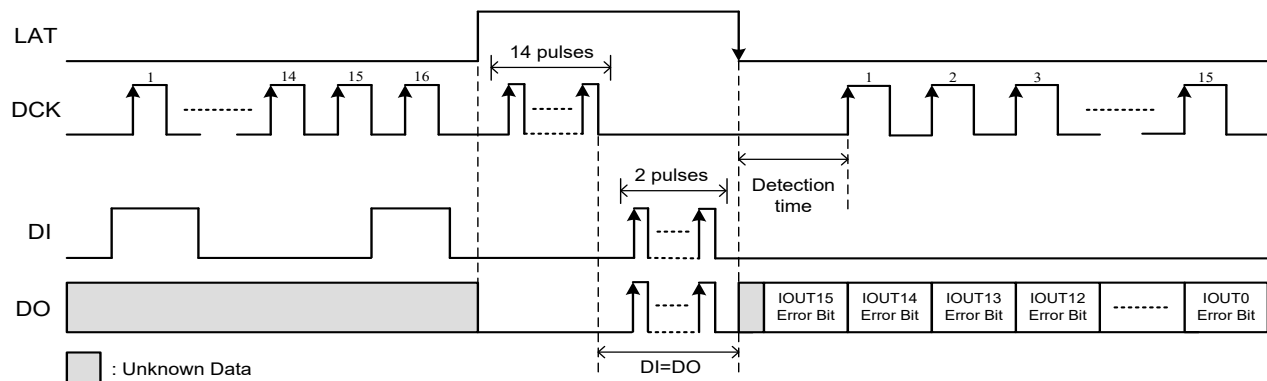
Functional Descriptions (continued)

Diagnosis and Protections (continued)

Error Bit

Error Bit	Symbol	Description
0	Error	When errors, such as open errors, short errors, short-to-GND errors, and thermal errors (PreOTP), are detected in the channel, the error bit, zero, will be loaded into the corresponding image shift register.
1	Normal	In the detecting mode, the bit, one, will be loaded into the corresponding image shift register if the device is under normal operating conditions.

LED Open Error Detection



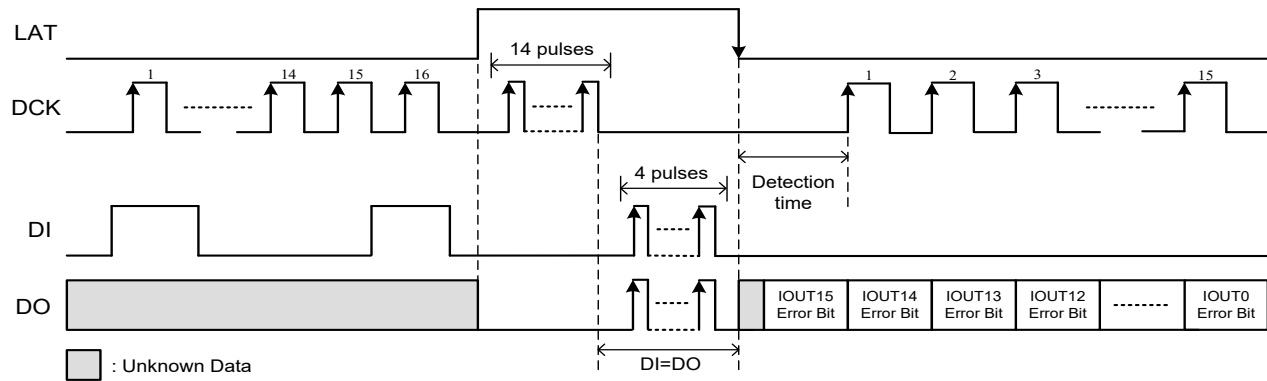
When the LED open error detection instruction is executed, it is necessary to input two DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263A will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK.

When the voltage of IOUT pins is below 0.3V, the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications.

Functional Descriptions (continued)

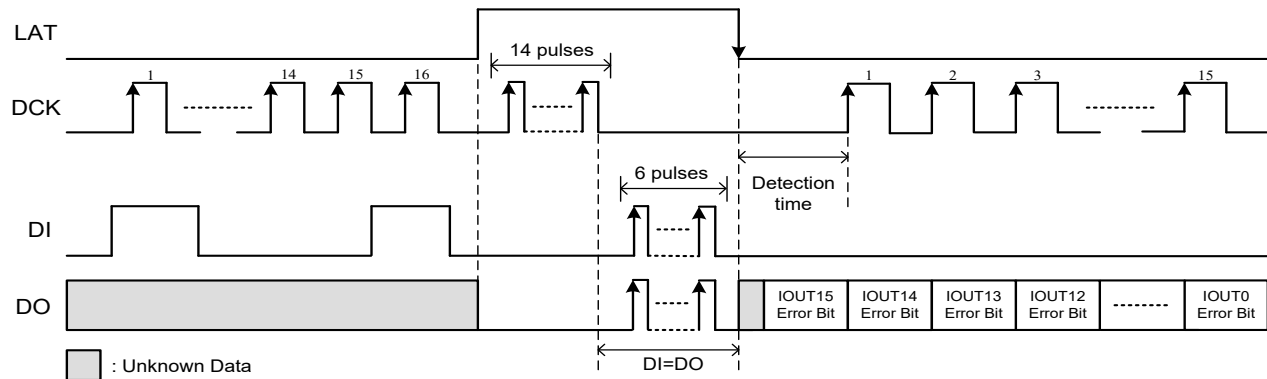
Diagnosis and Protections (continued)

LED Short Error Detection (Output Short-to-Power Included)



When the LED short error detection instruction is executed, it is necessary to input four DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263A will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK. When the voltage of IOUT pins is above the threshold voltage of LED short detection determined by CMD[14:13], the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications.

Short-to-GND Error Detection (Output Port Leakage Included)



When the short-to-GND error detection instruction is executed, it is necessary to input six DI pulses in the Error Detection Mode. No matter what the image latch data is, this instruction forces the output ports of the AL58263A to turn off for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK.

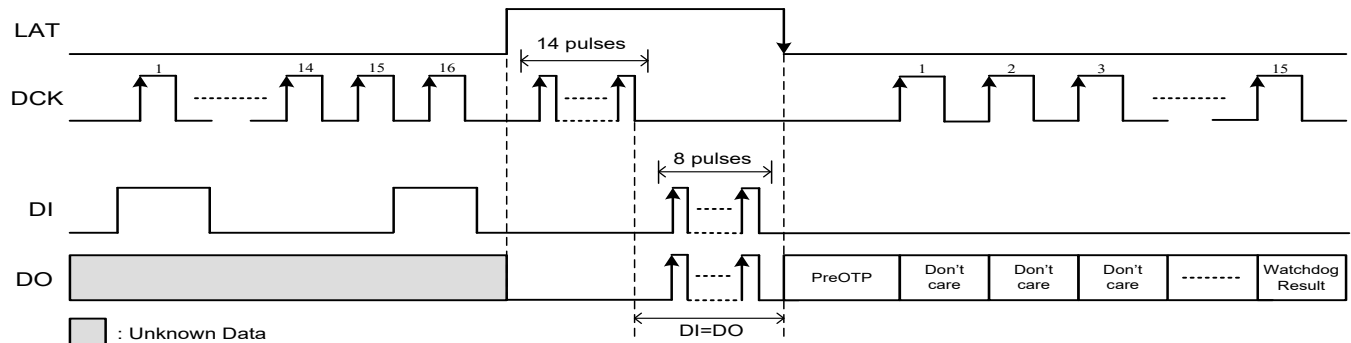
When the voltage of IOUT pins is below 0.3V, the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications.

Functional Descriptions (continued)

Diagnosis and Protections (continued)

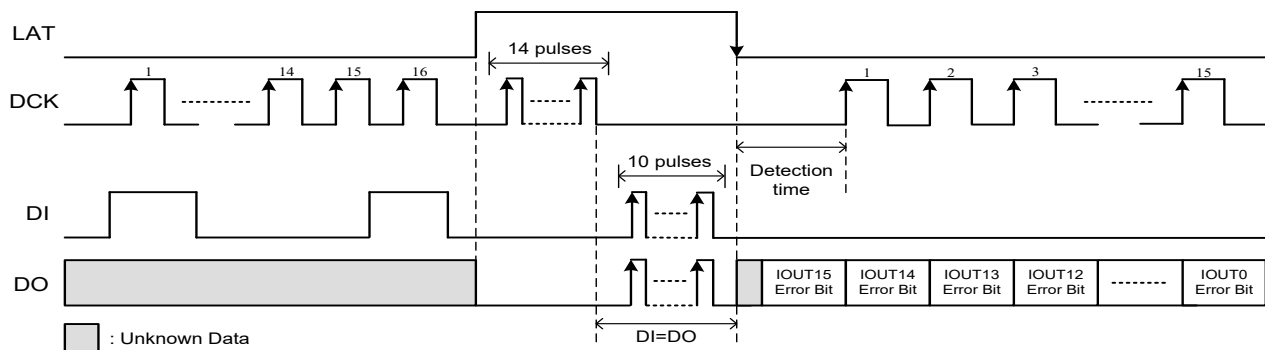
Pre-OTP Warning - Thermal Detection & Watchdog Result Read Out

The AL58263A has pre-thermal warning threshold of +155°C (typical).



When the thermal detection instruction is executed, it is necessary to input eight DI pulses in the Error Detection Mode. The AL58263A will judge junction temperature by the instruction. If the junction temperature is over +155°C, it will lead to thermal error. The device will load the PreOTP and watchdog result into the 16th and 1st image shift register and fill out the other image shift registers with bit code, 1. The error report will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications. When CMD[0] = 1 and GCK keeps low or high over 30ms, the watchdog result would be "0", otherwise it would be "1".

LED Smart Detection

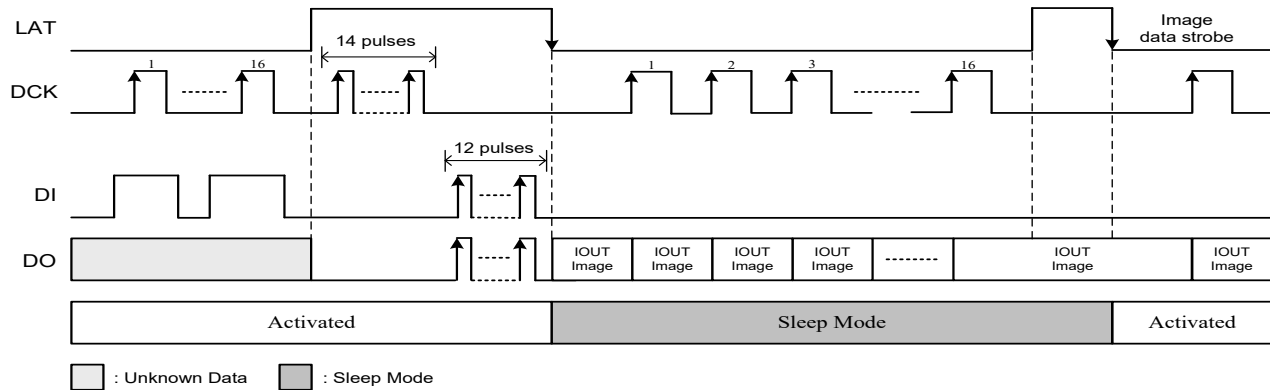


When the LED smart detection instruction is executed, it is necessary to input ten DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263A will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK. When the voltage of IOUT pins is below 0.3V for LED open detection or above the threshold voltage of LED short detection determined by CMD[14:13], the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications.

Functional Descriptions (continued)

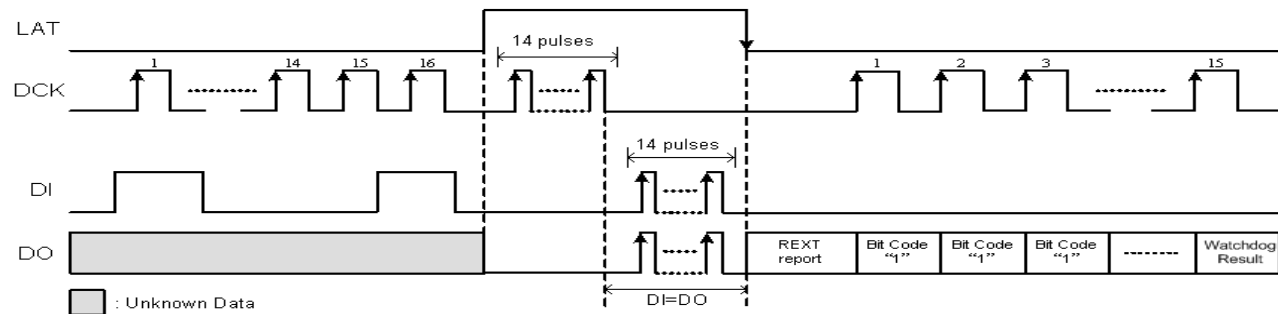
Diagnosis and Protections (continued)

Sleep Mode



For power saving, the AL58263A supports the sleep mode to turn off most circuits. It is necessary to input twelve pulses in the Error Detection Mode to execute this instruction and then keep GCK = high at sleep mode. In the sleep mode, the supply current maintains < 0.1mA because most analog circuits are shut down, but the digital interface is still activated in order to receive external digital data. The AL58263A will enter sleep mode at the falling edge of this LAT signal and revive at the falling edge of following LAT signal. The serial image data will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications.

REXT Detection & Watchdog Result Read Out



When the REXT detection instruction is executed, it is necessary to input fourteen DI pulses in the Error Detection Mode. The AL58263A will detect the voltage of REXT pin by the instruction. If the REXT pin is open or above 2.5V or below 0.15V, it will lead to REXT error. The device will load the REXT report and watchdog result into the 16th and 1st image shift register and fill out the other image shift registers with bit code, 1. The error report will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays at a high level for cascading applications. When CMD[0] = 1 and GCK keeps low or high over 30ms, the watchdog result would be "0", otherwise it would be "1".

Functional Descriptions (continued)

Power Dissipation

When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

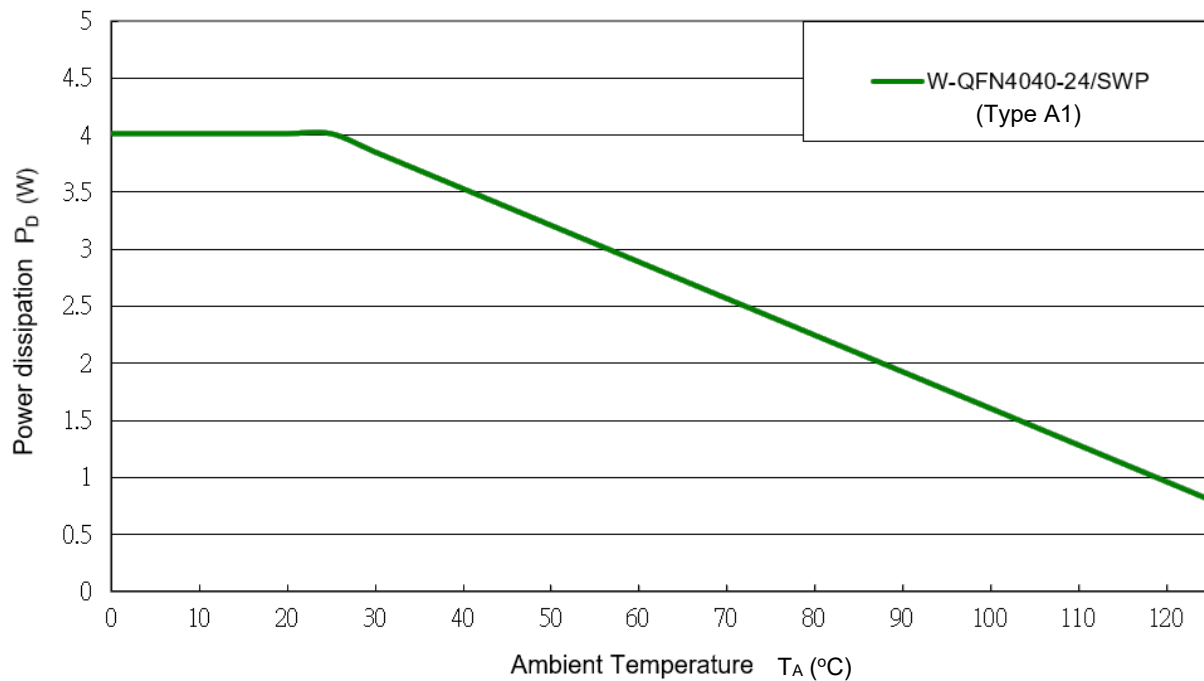
$$PD (practical) = V_{DD} \times I_{DD} + V_{out(0)} \times I_{out(0)} \times Duty_{(0)} + \dots + V_{out(N)} \times I_{out(N)} \times Duty_{(N)}, \text{ where } N=1 \text{ to } 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD (max) = \frac{T_j(max)(^{\circ}C) - T_a(^{\circ}C)}{R_{th(j-a)}(^{\circ}C/Watt)}$$

The PD(max) declines as the ambient temperature rises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature.

Maximum Power Dissipation v.s. Ambient Temperature

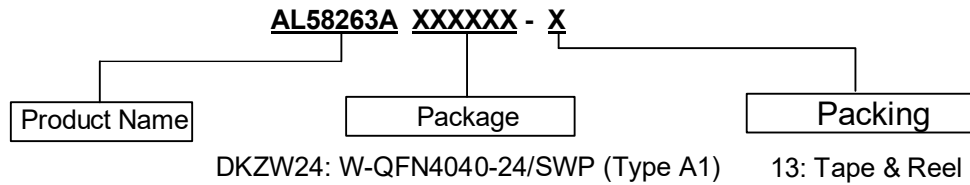


Design Tools (Note 13)

- AL58263A Demo Boards
- AL58263A Calculator
- Demo Board Gerber File for PCB Layout Reference

Note: 13. Diodes Incorporated's design tools can be found on our website at <https://www.diodes.com/design/tools/>.

Ordering Information (Note 14)

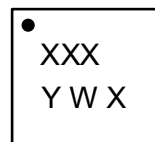


Orderable Part Number	Package	Packing	
		Qty.	Carrier
AL58263ADKZW24-13	W-QFN4040-24/SWP (Type A1)	3,000	Tape and Reel

Note: 14. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

(Top View)



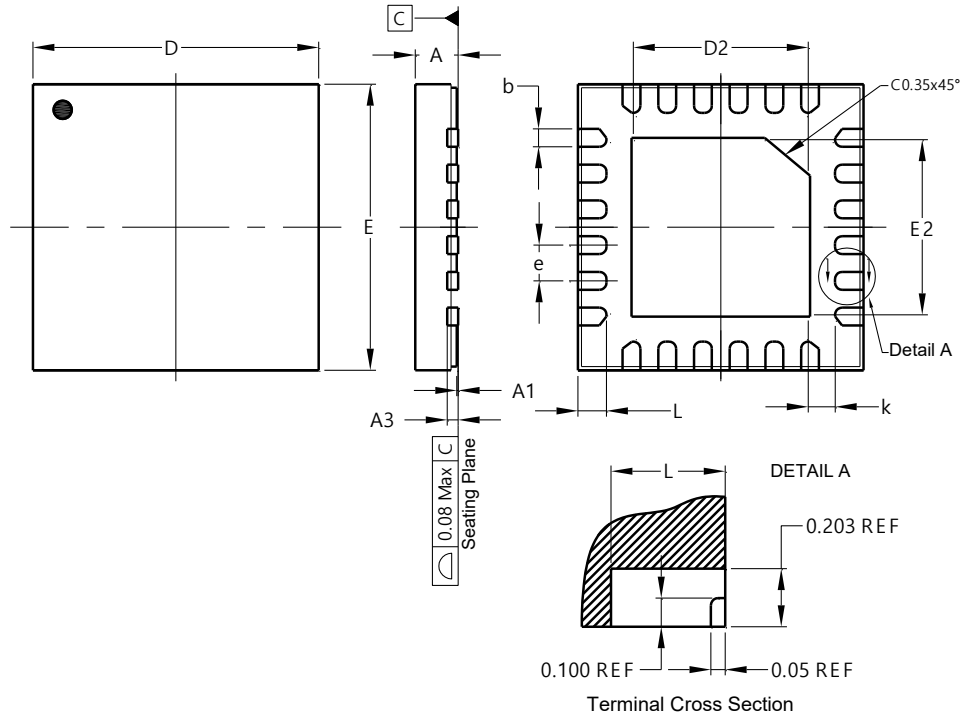
XXX : Identification Code
 Y : Year : 0 to 9 (ex: 6 = 2026)
 W : Week : A to Z : week 1 to 26;
 a to z : week 27 to 52; z represents
 week 52 and 53
 X : Internal Code

Orderable Part Number	Package	Identification Code
AL58263ADKZW24-13	W-QFN4040-24/SWP (Type A1)	JF

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

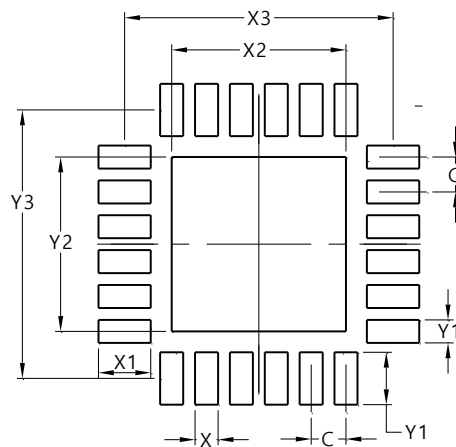
W-QFN4040-24/SWP (Type A1)



Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-QFN4040-24/SWP (Type A1)



Tape and Reel Information

Please see <https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf> for tape and reel details.

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads. Solderable per JESD22-B102 (e3)
- Weight: 0.037 grams (Approximate)

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