Integrated Transceivers Enable Small Form Factor Phased-Array Radar Platforms

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Abstract

Phased-array radar systems utilize many transmit and receive channels to function. Historically, these platforms were built using separate transmit and receive integrated circuits (ICs). These systems used separate chips for digital-to-analog converters (DACs) in the transmit (Tx) circuitry and analog-to-digital converters (ADCs) in the receive (Rx) circuitry. This separation has led to many large footprint, high cost, high power consumption systems in order to realize the channel count necessary to achieve the desired function. These systems also generally require long time-to-market due to manufacturing and calibration complexities. However, a recent approach utilizing integrated transceivers combines many functions once considered disparate into single ICs. Using these ICs enables small form factor, lower power consumption and cost, high channel-count phased-array radar platforms with a quicker time-to-market.

Introduction to Integrated Transceivers

Integrated transceivers, such as the one shown in Figure 1, combine multiple functions onto a single IC. For example, the new transceiver integrates DACs, ADCs, local oscillator (LO) synthesizers, microprocessors, mixers, and more into a single 12 mm × 12 mm monolithic product. In addition, this product combines two receive channels and two transmit channels, as well as digital signal processing (DSP) components to achieve the desired instantaneous bandwidths required for the system. An application program interface (API) is also provided to operate the transceiver on a customer platform. Gain and attenuation control can be achieved by utilizing the on-chip front-end networks. Built-in initialization and tracking calibration routines are offered to provide the performance required for many communication and military applications.

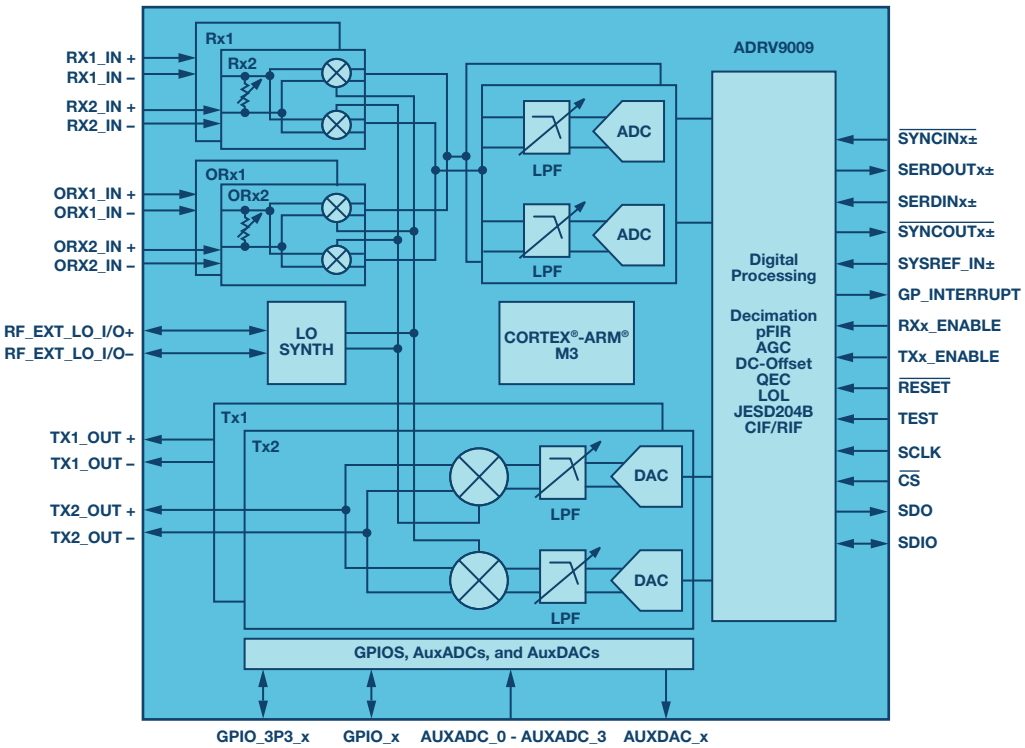

Figure 1. The ADRV9009 is an example of an integrated transceiver that combines many functions into a single IC.

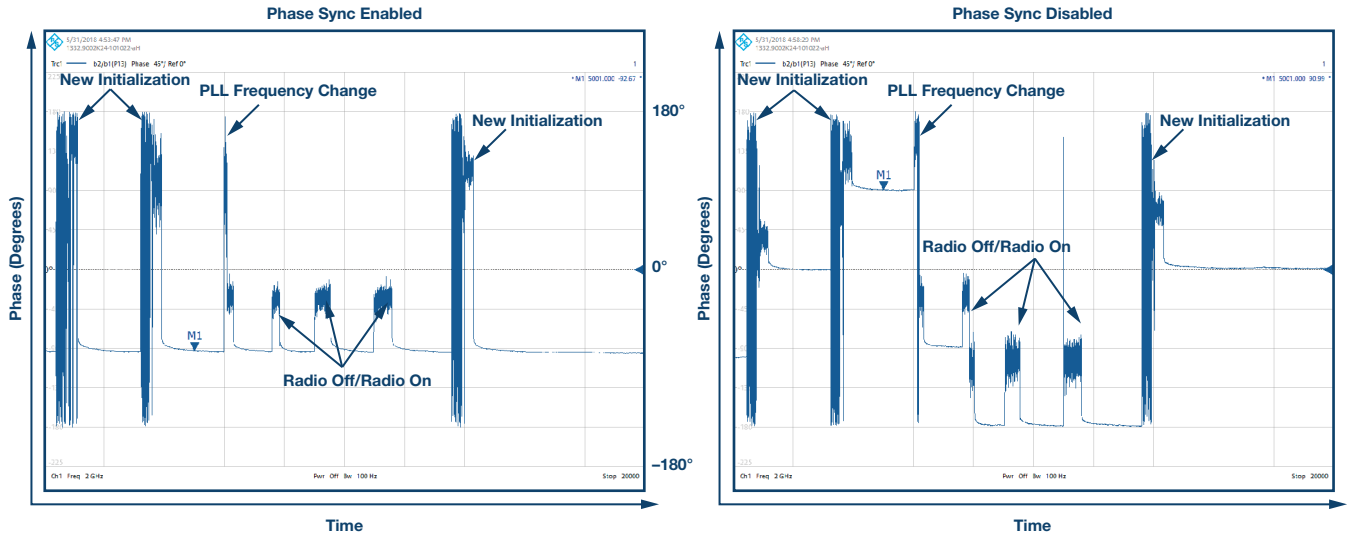

Figure 2. The built-in RFPLL phase sync feature provides a system with a deterministic phase relationship with respect to a master reference source.

These integrated transceivers are capable of creating all the clock signals needed for the transmitters and receivers by injecting a single reference clock signal known as REF_CLK. On-chip phase-locked loops (PLLs) then synthesize all required clocks for the DAC/ADC sampling, LO generation, and microprocessor clock. If the internal LO phase noise is not sufficient for a customer's application, the user can alternatively inject their own low phase noise external LO.

Data from the part is offloaded via a standardized JESD204b multigigabit serial data interface. This interface enables large amounts of simultaneous data reception and transmission. The new integrated transceiver solution can help to provide the interface IP to streamline a customer's time-to-market. If deterministic latency and data synchronization is needed, the user can utilize the built-in multichip synchronization (MCS) feature and issue a SYS_REF signal to act as a master timing reference for an initial lane alignment sequence (ILAS).[1]

Additionally, the LO phase of a Tx or Rx channel can be made deterministic with respect to a master reference phase using the built-in RFPLL phase sync feature. By utilizing both the MCS and the RFPLL phase sync features, phase alignment can be replicated when either initializing the part, frequency tuning, or toggling the radio on and off in software. An example of the new integrated transceiver providing deterministic phase with these features enabled is shown in Figure 2.

Using Multiple Integrated Transceivers

If more than two receivers and two transmitters are required for a system, the user can still benefit from the small size achieved with monolithic Rx and Tx channels by using multiple integrated transceivers. An example of this technique is shown in Figure 3. It is possible to synchronize multiple integrated transceivers by utilizing concurrent SYS_REF pulses to trigger internal dividers for all ICs at the same time. These SYS_REF pulses can be issued by either clock chips or baseband processors with programmable delays to account for any length mismatches between routes to the various ICs. Both the data paths and the multiple LOs across the multiple chips are capable of being deterministic.

Integrated Transceivers As the Backbone of Phased-Array Radar Platforms

Increasing channel counts by using synchronized integrated transceivers then allows these devices to serve as the backbone of phased-array radar platforms. When combining phase- and amplitude-aligned Tx and Rx channels, using multiple integrated transceivers has demonstrated system-level dynamic range, spurious, and phase noise improvements.

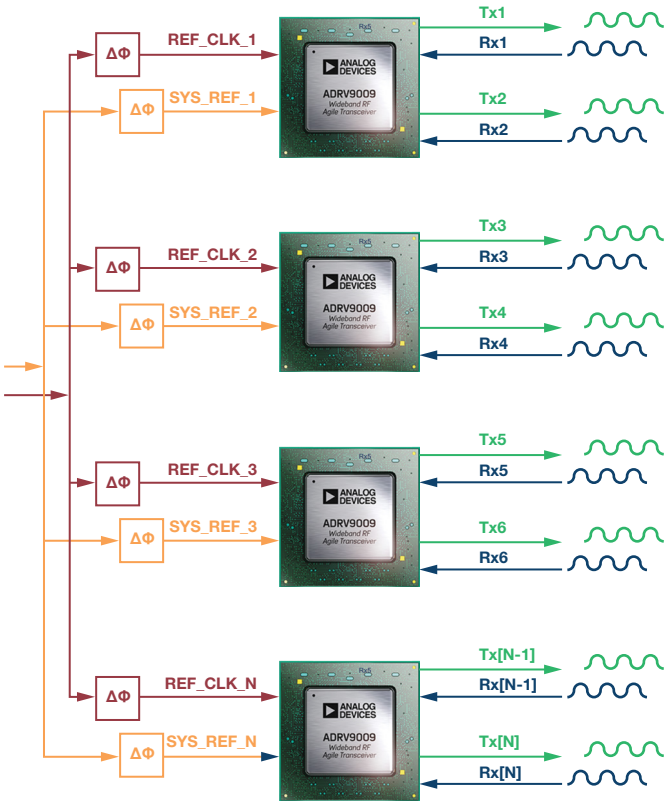

Figure 3. Multiple integrated transceivers can be used to increase the channel count of a system.

On-chip DSP features such as numerically-controlled oscillators (NCOs) and digital upconverters (DUCs) or digital downconverters (DDCs) enable system-level spurious decorrelation methods now within a single IC.[2]

Combining receiver channels using multiple integrated transceivers has demonstrated both improved system-level noise spectral densities (NSDs) and improved spurious performance. This has improved the dynamic range of a phased-array radar system by lowering the effective noise floor of the system but maintaining the channel full-scale power. Figure 4 shows measured system-level results when combining up to eight integrated transceiver Rx channels to effectively increase the number of bits achieved in a phased-array system. Note that the NSD, and the calculated noise floor

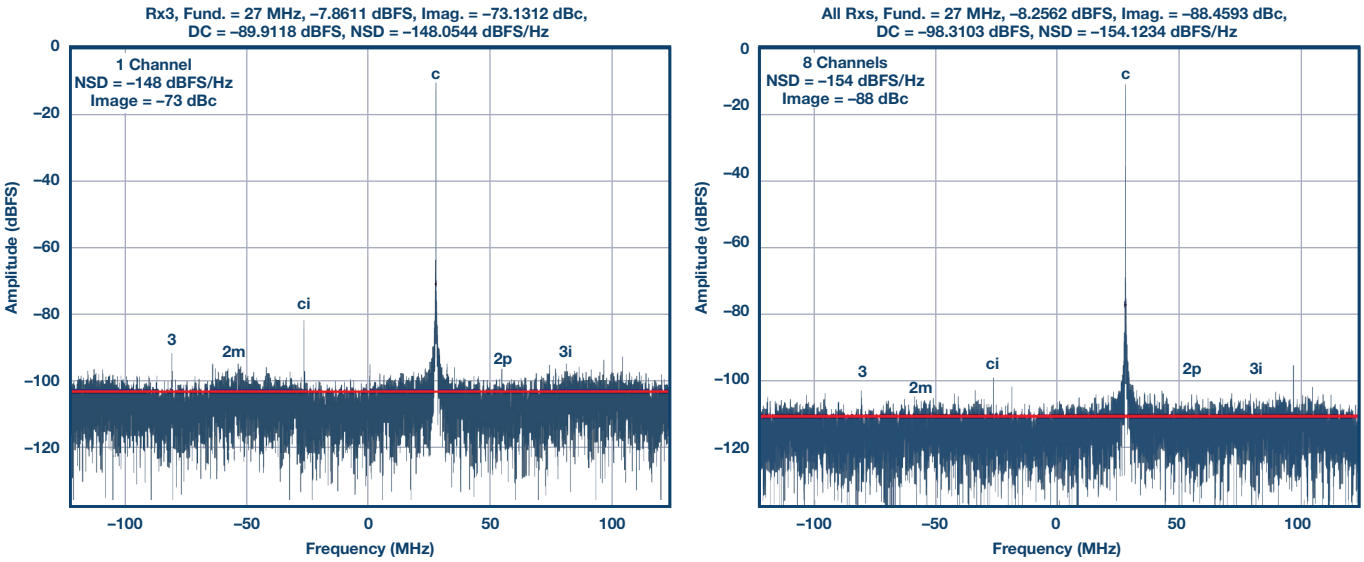

Figure 4. Combining Rx channels using the ADRV9009 integrated transceiver leads to lowering noise spectral densities and improved dynamic range.

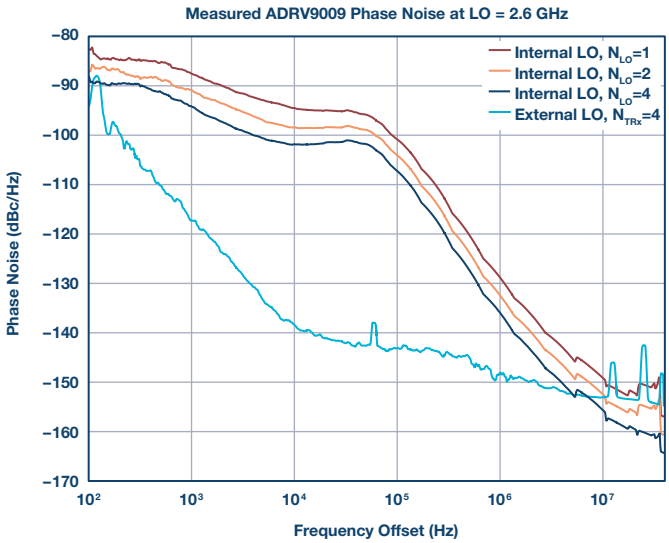

Figure 5. Combining Tx channels of multiple ADRV9009s when using the internal LO leads to improved system-level phase noise performance. External LO injection provides an improved starting phase noise for the subarray.

as indicated by the red line in each plot, is improved by ~6 dB when going from one channel to eight channels. This is because, although there are eight channels total, there are only four distinct, uncorrelated LOs (that is, $N_{LO}=4$) among the four integrated transceivers used to create those eight channels. This leads to an improvement of

$$NSD\ Improvement = 10\log_{10}(N_{LO}) = 10\log_{10}(4) \approx 6\ \text{dB}$$

which comes close to the experimental results provided by the integrated transceiver. Additionally, undesired image frequencies sum in an uncorrelated manner to achieve system-level spurious performance improvements. With increased channel counts, this improvement can be further enhanced, leading to a scalable system.

Additionally, after phase aligning and combining multiple integrated transceiver channels, the phase noise of the phased-array system can be improved. The top three traces of Figure 5 show measured results indicating improved phase noise performance when combining eight transmit channels using the internal LOs of four integrated transceiver ICs. Once again, in the case when there are four distinct and uncorrelated LOs (that is, $N_{LO} = 4$), the phase noise is improved by ~6 dB when going from one Tx channel to eight Tx channels. Increasing channel count can further improve the phase noise of the phased-array radar system. Alternatively, one could inject an external LO to each subarray composed of N_{TRx} integrated transceivers and improve the starting phase noise at the subarray level, as is shown with the blue trace in Figure 5. However, this is at the expense of each element within that subarray being correlated since they all share the same LO source, and they are thereby not capable of providing channel summing improvements within the subarray itself. For the external LO phase noise data shown in Figure 5, a Rohde and Schwarz SMA100B signal generator is used for the external LO source.

Integrated DSP features such as NCOs, digital phase shifters, and DUCs/DDCs allow for baseband phase- and frequency-shifting in the digital domain, thereby enabling digital beamforming in a multichannel, integrated-transceiver-based, phased-array radar system. Due to this bundling of functions on a single IC, a system is now capable of achieving antenna lattice spacings with the integrated transceivers in many pertinent phased-array applications. Increasing channel counts with more transceivers can generally result in narrower beams, but at the expense of increasing system footprint. However, with the multiple functions now in a single monolithic IC, this increase in footprint is now smaller than in the past. After simulating radiation patterns using MATLAB®, Figure 6 shows how increasing from N = 2^3 to N = 2^{10} channels results in a narrowing of the beam and a deeper theoretical lobe amplitude. The power nulls in practice will be dictated by the antenna design.

Conclusion

The integration of multiple digital and analog functions within a single IC allows for smaller form factor phased-array radar systems. These systems can enable both digital beamforming and hybrid beamforming, depending on the system specifications. System-level performance improvements using Analog Devices' ADRV9009 have been demonstrated. These integrated devices enable a new variety of systems which serve multiple applications with the same hardware.

References

[1] Harris, J. What Is JESD204 and Why Should We Pay Attention to It? Analog Devices Technical Article, MS-2374, 1-4. October 2013.

[2] Delos, P., Jones, M., and Robertson, M. RF Transceivers Enable Forced Spurious Decorrelation in Digital Beamforming Phased Arrays. Analog Devices Technical Article. August 2018.

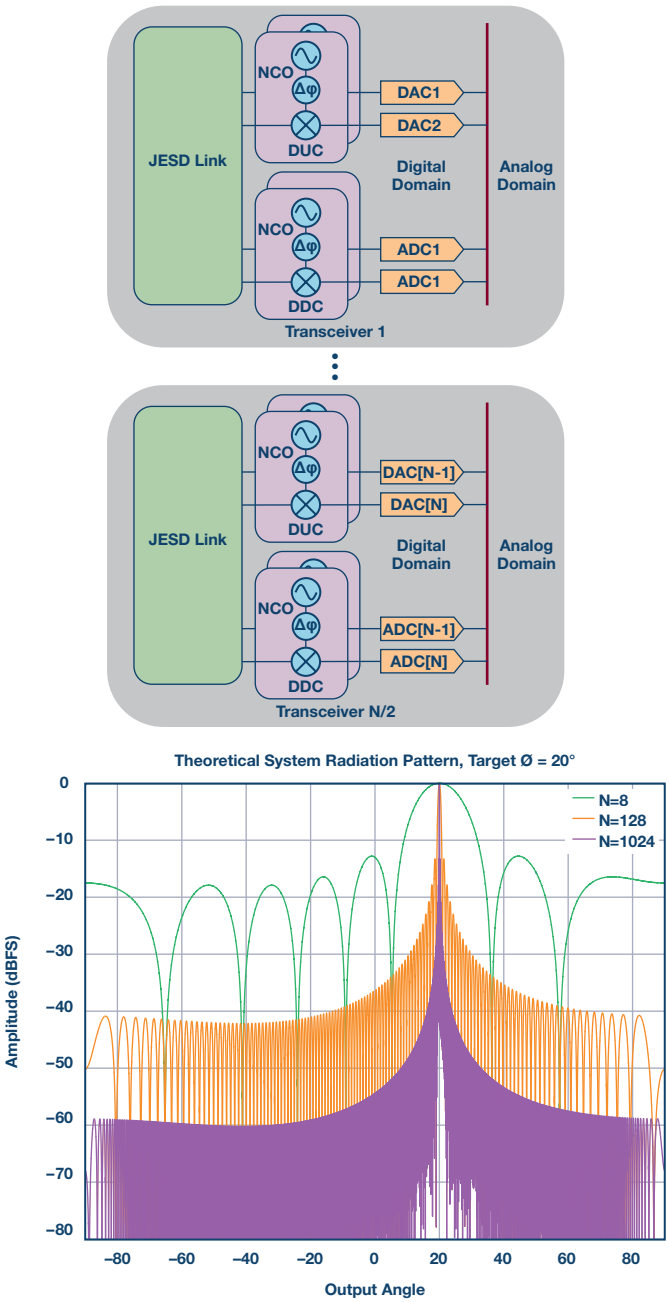

Figure 6. DSP features now enable digital phase shifting using the on-chip NCOs and DDCs/DUCs. Increasing channel count and optimum phase shifting can result in a narrowing of the beam formed by the integrated transceivers.

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