

# Negative Linear Regulator Features 0.8 $\mu\text{V}$ RMS Noise and 74 dB Power Supply Rejection Ratio at 1 MHz

Molly Zhu

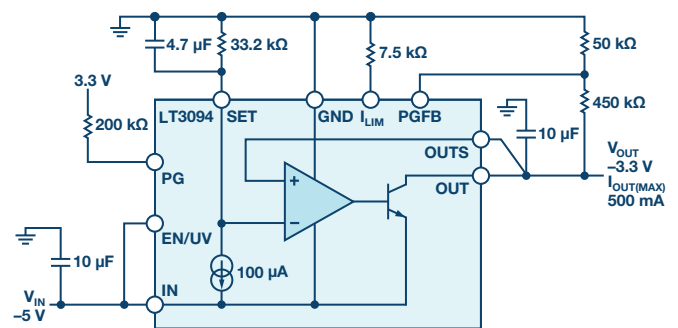
Analog Devices, Inc.

Low dropout (LDO) linear regulators have been widely used in noise-sensitive applications for decades. Nevertheless, noise requirements have become tougher to meet as the latest precision sensors, high speed and high resolution data converters (ADCs and DACs), and frequency synthesizers (PLLs/VCOs) challenge conventional LDO regulators to produce ultralow output noise and ultrahigh power supply ripple rejection (PSRR). For instance, when powering a sensor, the supply noise directly affects the measurement result accuracy. Switching regulators are often used in power distribution systems to achieve higher overall system efficiency. To build a quiet power supply, an LDO regulators usually postregulates the output of a relatively noisy switching converter without using bulky output filtering capacitors. The high frequency PSRR performance of the LDO regulator becomes a predominant feature.

The **LT3042**, introduced in 2015, is the industry's first linear regulator with only 0.8  $\mu\text{V}$  rms output noise and 79 dB PSRR at 1 MHz. Two similar devices, the **LT3045** and **LT3045-1**, increased the higher rating and added features. All of these devices are positive LDO regulators. When a system has bipolar instruments, such as op amps or ADCs, a negative LDO regulator must be used in a polarity power supply design. **LT3094** is the first negative LDO regulator that has ultralow output noise and ultrahigh PSRR. Table 1 lists the main features of the LT3094 and related devices.

## Typical Application

The LT3094 features a precision current source reference followed by a high performance output buffer. The negative output voltage is set with a  $-100\ \mu\text{A}$  precision current source flowing through a single resistor. This current-reference based architecture offers a wide output voltage range (0 V to  $-19.5\ \text{V}$ ) and provides virtually constant output noise, PSRR, and load regulation independent of the programmed output voltage. Figure 1 shows a typical application and the demonstration board is shown in Figure 2. The overall solution size is only about 10 mm  $\times$  10 mm.



Pin Not Used in This Circuit: VIO

Figure 1.  $-3.3\ \text{V}$  output low noise solution.



Figure 2. Demo circuit shows a tiny  $-3.3\ \text{V}$  solution.

Table 1. Features of the LT3094 and Low Noise LDOs

	LT3015	LT3090	LT3042	LT3045-1	LT3094
Positive/Negative Output	Negative	Negative	Positive	Positive	Negative
Output Current (A)	1.5	0.6	0.2	0.5	0.5
Output Noise (10 Hz to 100 kHz) ( $\mu\text{V}$ )	60	18	0.8	0.8	0.8
Spot Noise at 10 kHz ( $\text{nV}/\sqrt{\text{Hz}}$ )	240	57	2	2	2
PSRR at 1 MHz (dB)	30	20	79	76	74
Programmable Current Limit		•	•	•	•
Programmable Power Good			•	•	•
VIOC				•	•
Directly Parallelable		•	•	•	•
Fast Start-Up Capability			•	•	•

The LT3094 has ultralow output noise, 0.8  $\mu\text{V}$  rms from 10 Hz to 100 kHz, and ultrahigh PSRR, 74 dB at 1 MHz. Moreover, the LT3094 has programmable current limit, programmable power good threshold, fast start-up capability, and programmable input-to-output voltage control (VIOC). When the LT3094 postregulates a switching converter, the voltage across the LDO regulator remains constant by the VIOC function if the LDO regulators output voltage is variable.

The LT3094 avoids damage through internal protection, including internal current limit with foldback, thermal limit, reverse current, and reverse voltage.

Direct Paralleling for Higher Current

The LT3094 can be easily paralleled to increase output current. Figure 3 shows a solution using two LT3094s paralleled to achieve 1 A output current. To parallel two devices, the SET pins are tied together, and one SET resistor,  $R_{\text{SET}}$ , is placed between SET pin and ground. The current flowing through  $R_{\text{SET}}$  is 200  $\mu\text{A}$ , twice the amount of the SET current in one device. For good current sharing, a small 20 m $\Omega$  ballast resistor is used at each output of the LT3094.

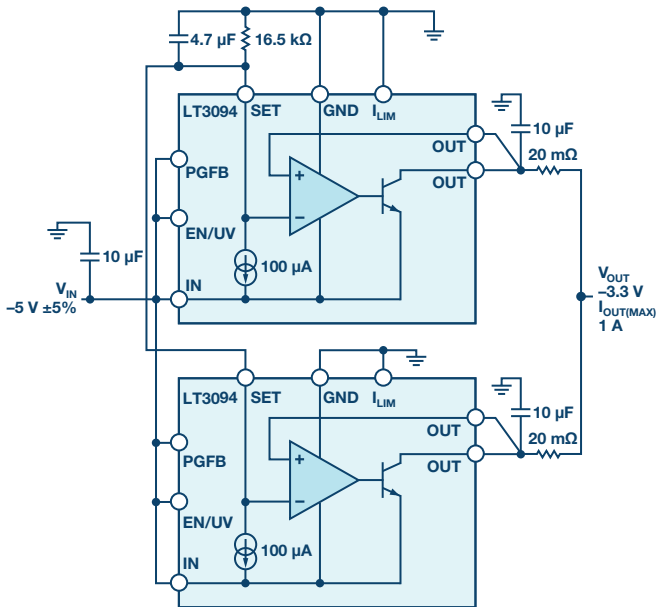


Figure 3. Schematic of two paralleled LT3094s.

Figure 4 shows the thermal performance of the circuit in Figure 3 with  $-5\text{ V}$  input voltage and  $-3.3\text{ V}$  output voltage running at 1 A load current. The temperature of each part rises to about 50°C, indicating the heat is distributed equally. There is no limit on the number of devices that can be paralleled for even high output current and low output noise.

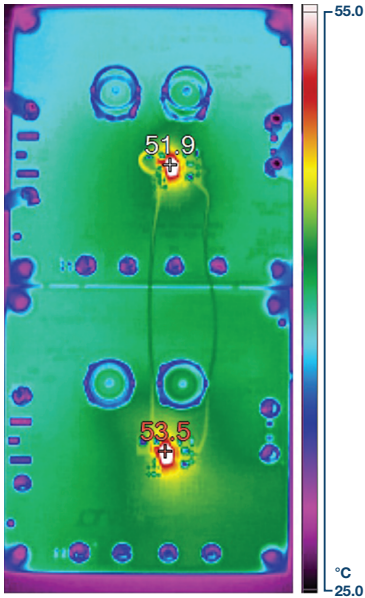


Figure 4. Thermal image of two paralleled LT3094s.

Dual Positive and Negative Power Supply with Variable Output Voltages

A power supply is generally built with a switching converter post-regulated by an LDO regulator to achieve low output noise and high system efficiency. The optimized voltage difference between the LDO regulators input and output is about  $-1\text{ V}$  in order to maintain a good trade-off between power dissipation and PSRR. Maintaining this voltage difference is complicated in a variable output voltage system, but the LT3094 includes a tracking feature, VIOC, which keeps the voltage across the LDO regulator constant even as the output voltage varies.

Figure 5 is the schematic of a dual power supply using LT8582, LT3045-1, and LT3094. The LT8582 is a dual channel PWM dc-to-dc converter with internal switches that can generate both positive and negative outputs from a single input. The first channel of LT8582 is configured as a SEPIC to generate a positive output, and the second channel is an inverting converter to generate the negative rail. In the negative rail, the voltage across the LT3094 is controlled by VIOC voltage as

$$\begin{aligned} V_{LDO(IN2)} - V_{LDO(OUT)} &= V_{IOC} \\ &= V_{FBX2} - R2 \times I_{FBX} \end{aligned} \quad (1)$$

where  $V_{FBX2}$  is 0 mV and  $I_{FBX}$  is 83.3  $\mu$ A. Setting R2 to 14.7 k $\Omega$  sets the VIOC voltage at 1.23 V over the variable output voltage. The resistor R1, at 133 k $\Omega$ , limits the input voltage of LT3094 to 16.5 V, calculated by

$$V_{LDO(INMAX)} = V_{FBX} (1 + R1/40 \text{ k}\Omega) - R1 \times I_{FBX} \quad (2)$$

The thermal images of the circuit running at 12 V input are shown in Figure 6. When output voltage changes from  $\pm 3.3$  V to  $\pm 12$  V, the temperature rise of the LT3094 remains constant. Table 2 lists the voltage and current of all three devices. Figure 7 shows the transient response of the  $\pm 5$  V power supply running at 12 V input.

In Figure 5, no additional capacitor other than the output capacitors at LT8582 is placed at the input of the LT3094. Generally, an input capacitor reduces the output ripple, but this is not the case for the LT3094. If the LT3094 has input capacitors, the switching currents from the switching converter will flow through the input capacitor, causing the electromagnetic coupling from the switching converter to the LT3094's output. The output noise will be increased, degrading the PSRR. Provided that the switching regulator is placed within two inches of the LT3094, we recommend not placing a capacitor at LT3094's input to achieve best PSRR performance.

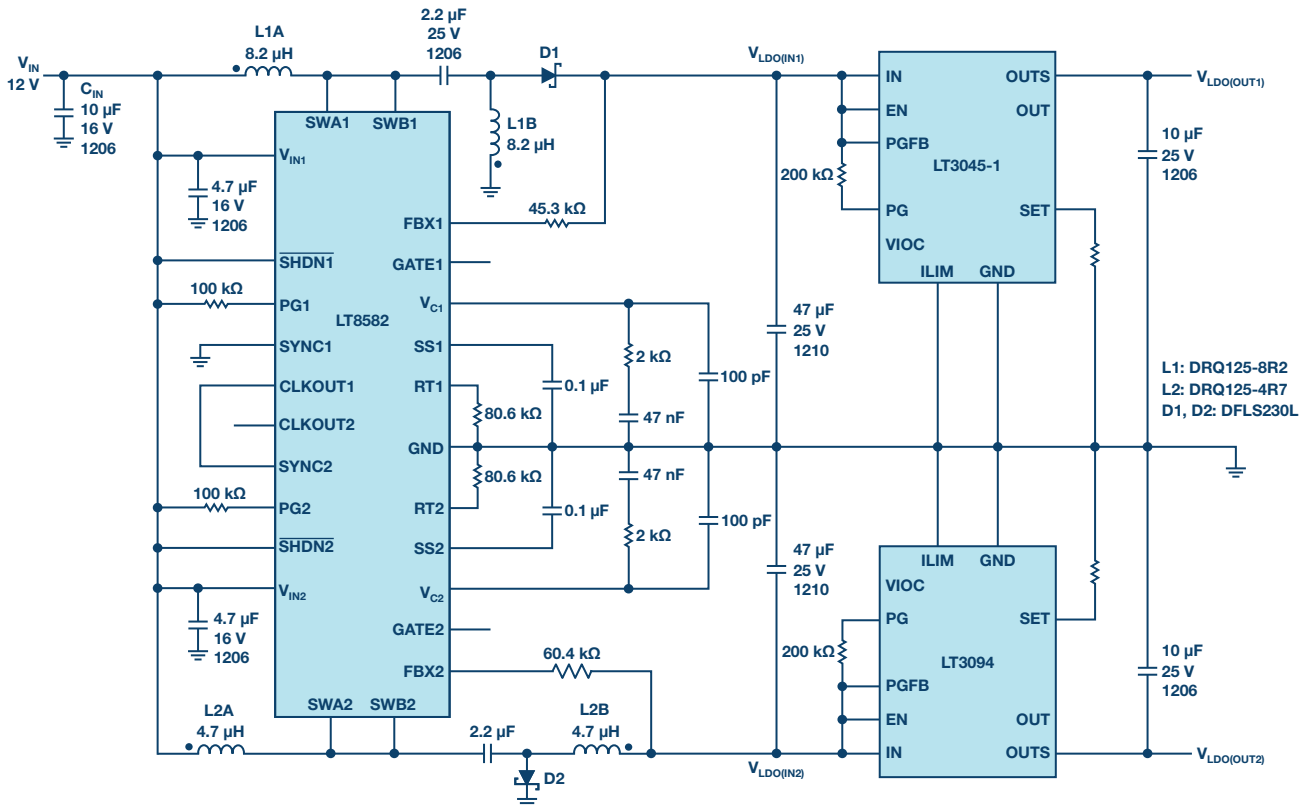


Figure 5. Adjustable dual output, positive/negative power supply features high ripple rejection and cool operation.

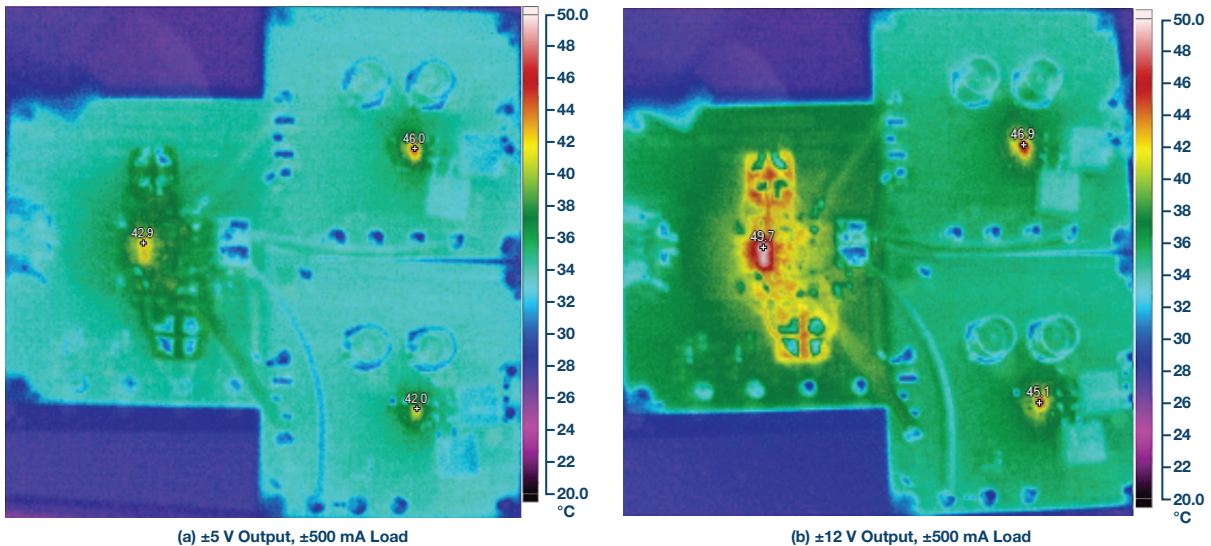


Figure 6. Thermal image of a dual power supply at 12 V input.

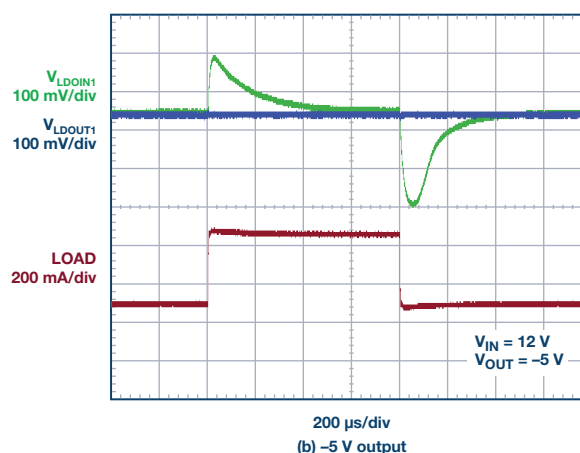
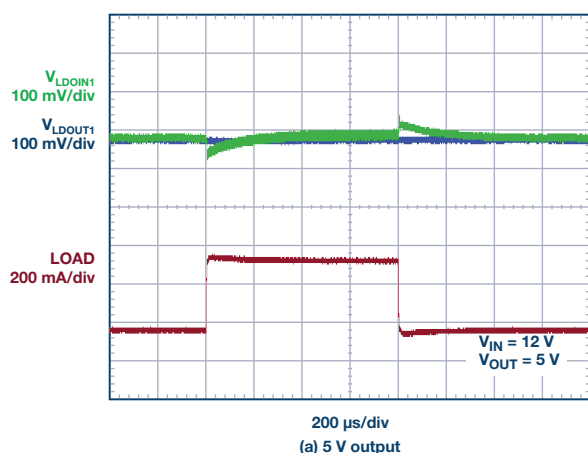


Figure 7: Transient response of dual power supply at 12 V input,  $\pm 5$  V output.

Table 2. Circuit Performance of Dual Output Positive/Negative Power Supply at 12 V Input,  $\pm 500$  mA Load

$V_{LDO(OUT)}$ (V)	$V_{LDO(IN)}$ (V)	$V_{DROP}$ (V)	LT3094 Temperature Rise	$I_{IN}$ (A)	System Efficiency
$\pm 3.3$	$\pm 4.55$	1.25	8°C	0.48	57%
$\pm 5$	$\pm 6.25$	1.25	8°C	0.65	65%
$\pm 12$	$\pm 13.22$	1.22	9°C	1.25	78%

## Conclusion

The LT3094 is a negative LDO regulator featuring ultralow noise and ultrahigh PSRR. It features a current reference-based architecture that keeps noise and PSRR performance independent of the output voltage, and enables multiple LT3094s to be easily paralleled for increased load current and reduced output noise. The VIOC function minimizes the power dissipation of the LDO regulator when the LT3094 postregulates a switching converter, making it ideal in variable output voltage applications.

## About the Author

Huiyu (Molly) Zhu is a senior applications engineer in Analog Devices' Power by Linear™ Group. She received her B.S.E.E. and M.S. degrees from Tsinghua University, China in 1998 and 2000, respectively, and a Ph.D. degree in electrical engineering from Virginia Polytechnic Institute and State University, Blacksburg, Virginia in 2005. She can be reached at [huiyu.zhu@analog.com](mailto:huiyu.zhu@analog.com).

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