GN001 Application Brief

How to drive GaN Enhancement mode HEMT

Updated on Apr-26-2016

GaN Systems Inc.

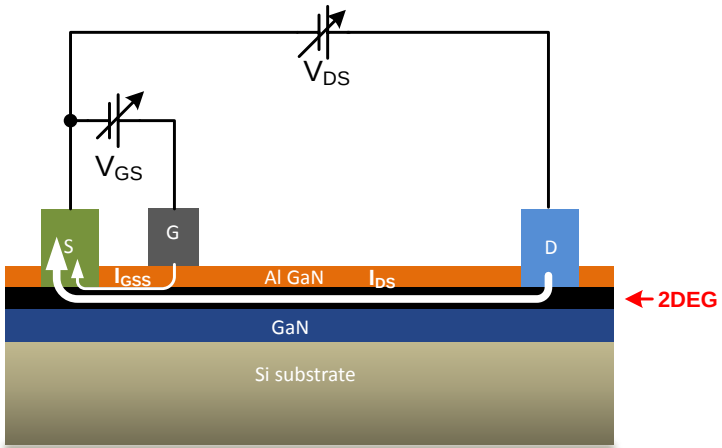
- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

Latest update Apr 26th, 2016
Please visit http://www.gansystems.com/whitepapers.php for latest version of this document

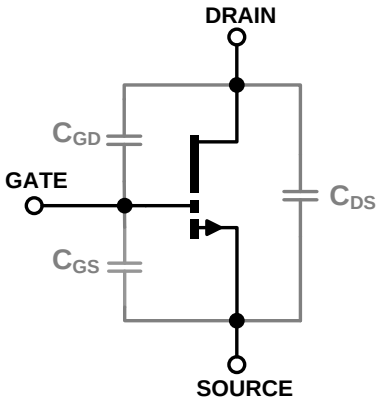
Fundamentals of GaN Systems E-HEMT

GaN Enhancement mode High Electron Mobility Transistor (E-HEMT):

- Lateral 2DEG (2-dimensional electron gas) channel formed between AlGaN and GaN layers
- Positive gate bias opens up 2DEG channel
- 0V or negative gate voltage shuts off 2DEG and block forward conduction
- Voltage driven: Gate driver charges/discharges (C_{GD} + C_{GS})
- No DC gate driving current needed: gate leakage current only (I_{GSS})



GaN E-HEMT simplified structure



E-HEMT circuit model

Gate Characteristics GaN E-HEMT vs. other technologies

- Similar gate drive requirement to Silicon MOSFET/IGBT
- Much Smaller gate charge – Lower drive loss, faster rise & fall time
- **Lower gate voltage – Select right gate driver UVLO**
- Easy **5 to 6.5V** gate drive with maximum rating +7V and +10V transient
- 0V to turn off, typical V_{GTH}=1.5V.
- Negative voltage improves gate drive robustness **but is optional**
- Easy slew rate control using gate resistor

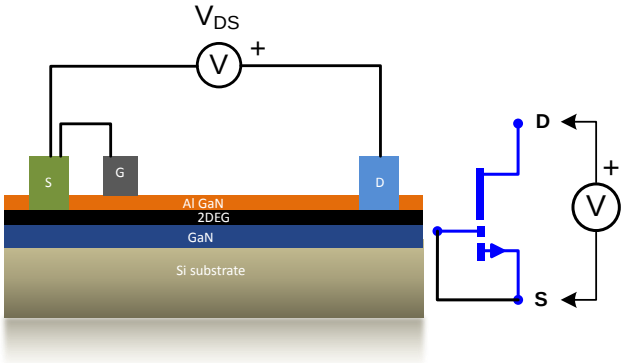
Gate drive voltage level	GaN Systems GaN E-HEMT	Si MOSFET	IGBT	SIC MOSFET
Maximum rating	**-10/+7V**	**+/-20V**	**+/-20V**	**-8/+18V**
Transient maximum	**-20/+10V***		**+/-30V**	
Typical operational values	**0 or -3/+5-6.5V**	**0/+10-12V**	**0 or -9/+15V**	**-4/+15V**

[*] pulse width < 1uS

GaN E-HEMT Reverse Conduction

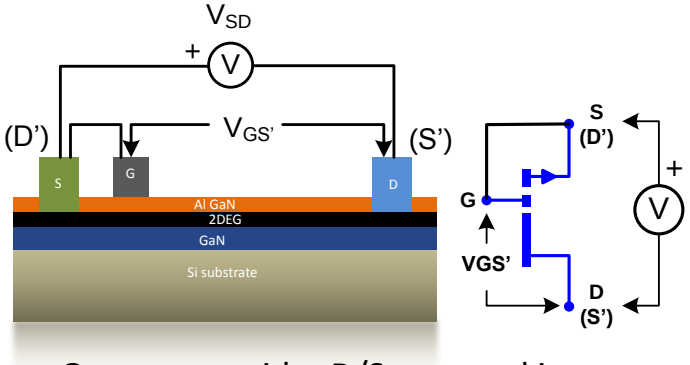
- No parasitic body diode: **Zero Q_{RR}** Loss & very **high dv/dt** ruggedness
- GaN E-HEMT is naturally capable of reverse conduction, **without external diode**
- Unlike MOSFETs/IGBT, reverse current flow through same 2DEG channel as forward conduction
- "Diode" like reverse behavior is V_{GS} dependent

Drain-source forward bias:



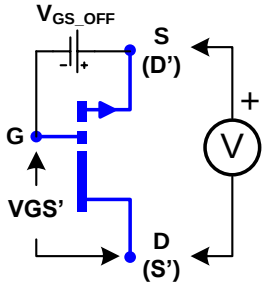
When $V_{GS} \leq 0V$: no channel conduction

Reverse bias V_{GS}=0V:



- One can consider D/S swapped in reverse bias mode
- 2DEG channel starts to conduct when $V_{SD} = V_{GS'} (V_{GD}) > V_{GTH} = \sim 1.5V$
- Reverse current flows in 2DEG

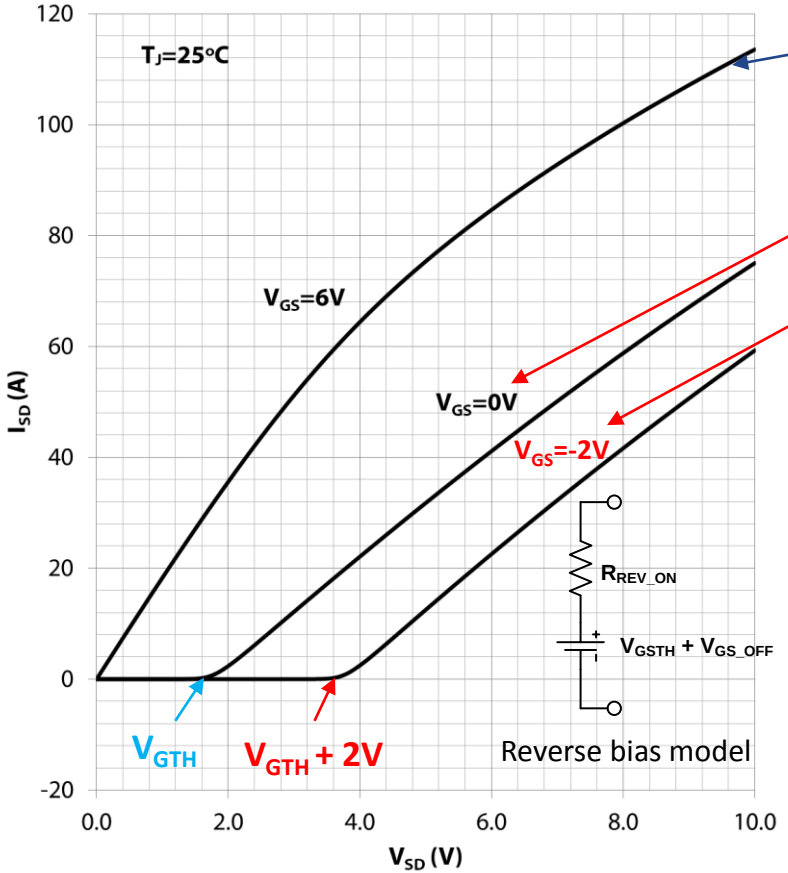
Reverse bias with -V_{GS}:



- 2DEG starts to conduct when $V_{SD} = V_{GTH} + V_{GS\_OFF}$
- -V_{GS} increases reverse voltage drop V_{SD}

Reverse Conduction Loss model

GS66508T reverse I/V characteristics



V_{GS} = 6V (on-state):

- 2-quadrant bidirectional current flow in 2DEG channel
- Reverse Rds(on) same as forward conduction
- $P_{loss\_rev} = I_{SD}^2 x\ R_{DS(ON),\ Tj}$

V_{GS} ≤ 0V (off-state):

- Modeled as "diode" with V_F + channel resistance R_{rev_on} that is higher than $R_{DS(ON)}$ in forward conduction
- V_{SD} increases with the negative gate voltage applied
- $P_{loss\_rev} = I_{SD}^2\ X\ R_{REV(ON)} + I_{SD}\ x\ (V_{GTH} + V_{GS\_OFF})$

How does it affect the design:

- **No external anti-parallel diode** required
- No **Q_{RR}** Loss (Q_{OSS} loss only), perfect fit for half bridge where hard commutation is required – **Higher efficiency and more robust without body diode**
- Higher reverse conduction loss, for optimal efficiency:
  - Minimize dead time and utilize synchronous drive
  - Prefer **0V** for turn-off

Reduce Losses using Dead time & Synchronous driving

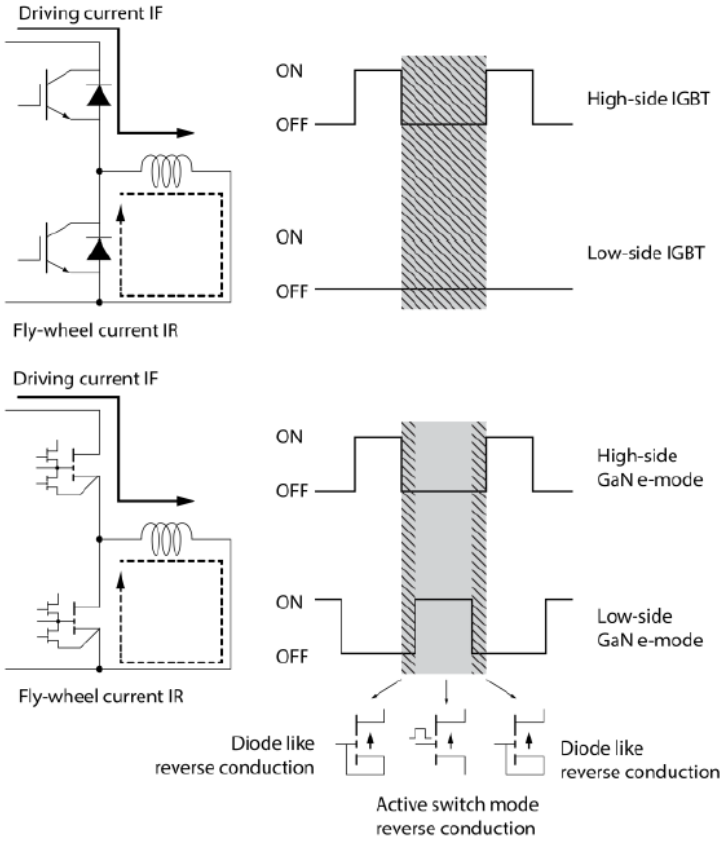
- Synchronous driving with minimum dead time is recommended for optimum efficiency
- Dead time can be selected by considering the worst case gate driver propagation delay skewing + turn-off delay time + fall time
  - For 650V GS66508T/P: typical **50-100ns**
  - For 100V GS61008P: typical **15-20ns**

25ns Delay difference for Si8261 Isolated gate driver

Propagation Delay Difference[5]	PDD	$t_{PHLMAX} - t_{PLHMIN}$	-1	—	25	ns

Total switching time **26ns** for GS66508T (R_G=10Ω, T_J=125°C)

GS66508T T_J=125°C				
Parameters	**Symbol**	**Value**	**Unit**	**Conditions**
Turn-on delay time	$t_{d(on)}$	4.5	ns	V_{DD}=400V, V_{GS}=6V,
Rise time	t_r	6.3	ns	I_D=16A, R_G=10Ω
Turn-off delay time	$t_{d(off)}$	9.3	ns	
Fall time	t_f	5.4	ns	



Design Considerations

- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

Optimizing Gate Resistors

Select right gate resistance

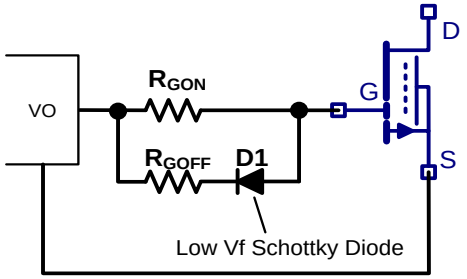
- E-HEMT switching speed can be controlled by gate resistors
- R_G is critical for optimum switching performance and gate drive stability
- Separate R_G for turn-on and off is recommended

Turn-on gate resistor R_{GON}:

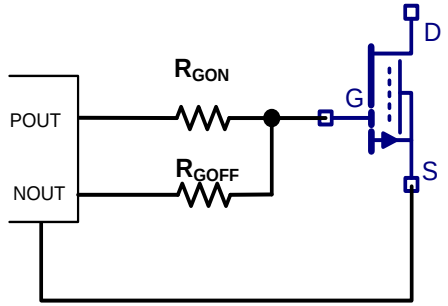
- Control the turn-on slew rate dv/dt
- For GS66508x: Recommended to start with R_{GON} = **10-20Ω**
- Too small R_{GON}: High dv/dt; drain current and V_{GS} ringing
  - Higher switching loss due to gate ringing
  - Risk of miller turn-on and gate oscillation

Turn-off gate resistor R_{GOFF}:

- R_{GOFF} smaller than R_{GON} is recommended:
  - Provide strong pull-down for robust gate drive
- Typical value R_{GOFF} = **1-3Ω**



For driver with single output



For driver with separate pull-up/down outputs

Preferred Approach

R_{GOFF} Effects on power loss

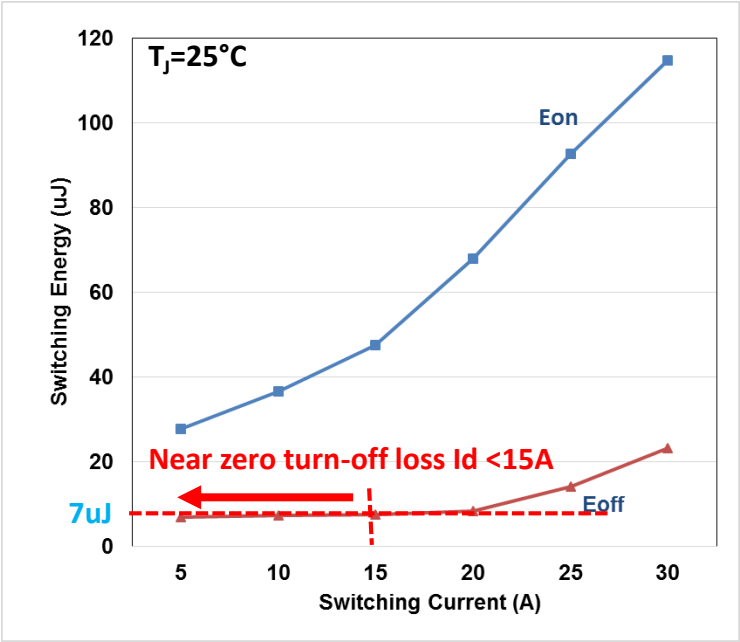
Effect of R_{GOFF} on power loss

- Smaller R_{GOFF} reduce E_{OFF}.
- Too small R_{GOFF} may create V_{GS} undershoot and ringing :
  - Higher switching and dead time conduction loss
  - Potential gate oscillation
- Recommended to start with **1-3Ω** and adjust empirically

Wide range of near zero E_{OFF} can be easily achieved with GaN:

- Extreme low Q_G → 2DEG channel turns off fast enough → gate no longer controls turn-off V_{DS} dv/dt (no plateau period)
- Turn-off dv/dt solely determined by how fast load current (L_{OUT}) charges C_{OSS}.
- Measured E_{OFF} includes E_{OSS}, which is NOT part of E_{OFF} and will be dissipated at next turn-on transient.

GS66508P Measured E_{ON}/E_{OFF} (V_{DS}=400V, R_{GON}=10Ω, R_{GOFF}=1Ω)



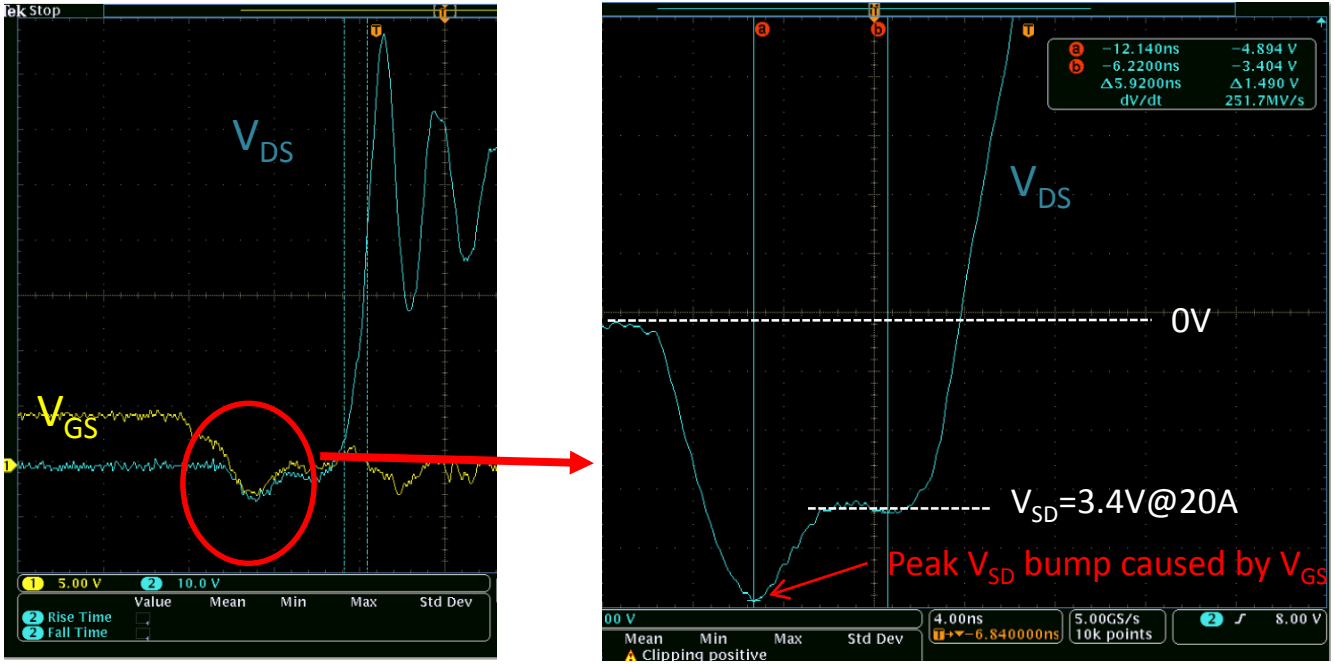
GS66508P: Eoss@400V = 7uJ

Minimum turn-off loss when Id <15A (R_{GOFF} = 1Ω)

R_{GOFF} effects on reverse losses

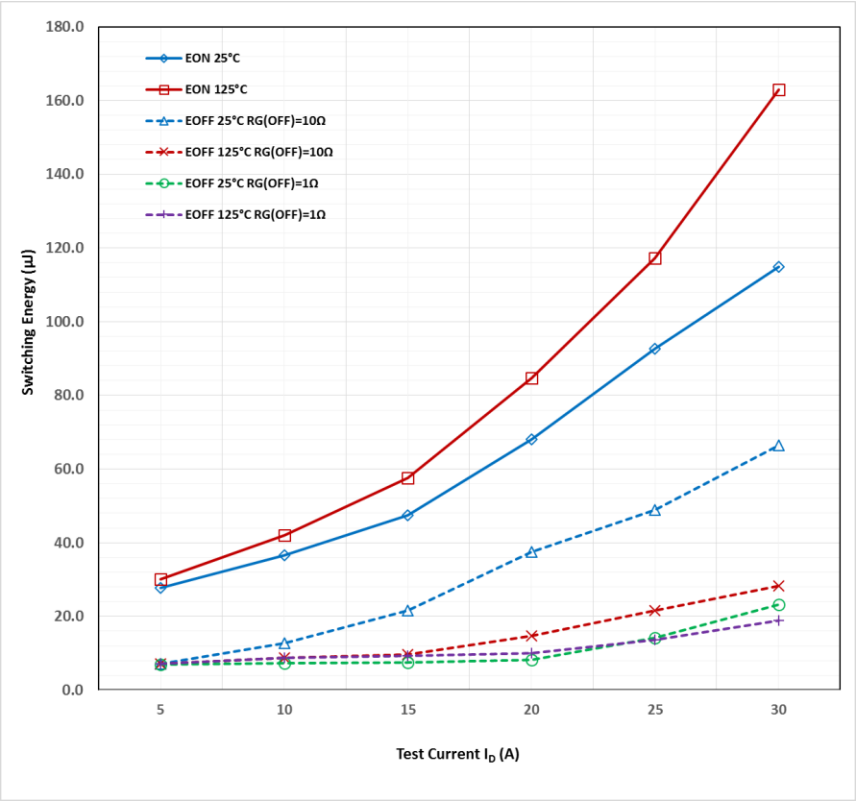
Effect of V_{GS} undershoot on dead time loss:

- Example 48-12V Sync Buck I_{SW} = 20A (GS61008P)
- LS V_{GS} turn-off undershoot adds to the V_{SD} drop during dead time → higher dead time loss
- Optimize R_{GOFF} to balance between E_{OFF} and dead time loss → **more critical for VHF application and 100V device**



Eon and Eoff vs Current vs Gate Resistance

GS66508P Switching Loss measurements



Switching energy loss tested on half bridge with inductive load:
V_{DS} = 400V, V_{GS} = 6V, $R_{G(ON)}$ = 10Ω, L_P = 10nH*, L = 40uH, Gate driver IXDN609SI.

	T_J = 25°C			T_J = 125°C		
I_D (A)	E_{ON} 25°C	E_{OFF} 25°C $R_{G(OFF)}$=10Ω	E_{OFF} 25°C $R_{G(OFF)}$=1Ω	E_{ON} 125°C	E_{OFF} 125°C $R_{G(OFF)}$=10Ω	E_{OFF} 125°C $R_{G(OFF)}$=1Ω
5	27.8	7.1	7.0	30.0	7.2	7.1
10	36.7	12.7	7.3	42.1	8.7	8.7
15	47.5	21.5	7.5	57.6	9.7	9.3
20	68.0	37.5	8.3	84.7	14.7	10.0
25	92.7	48.8	14.2	117.2	21.6	13.6
30	114.8	66.4	23.2	163.0	28.3	19.0

* - Parasitic loop inductance

Notes:

- Measured E_{OFF} includes the energy that charges the output capacitance (E_{OSS}), which will be dissipated during turn-on at next switching cycle for hard switching application.
- For resonant soft-switching topology, Energy stored in C_{OSS} is recycled and should not be included in switching loss calculation. The actual E_{OFF} can be calculated by:

$$E_{OFF} = E_{OFF\_Measured} - ½*C_{O(er)}*V_{DS}\text{^}2$$

Where $C_{O(er)}$ is energy related capacitance @V_{DS}=400V and can be found on datasheet

Miller turn-on – how to prevent it

1) Design for low pull-down impedance on the gate:

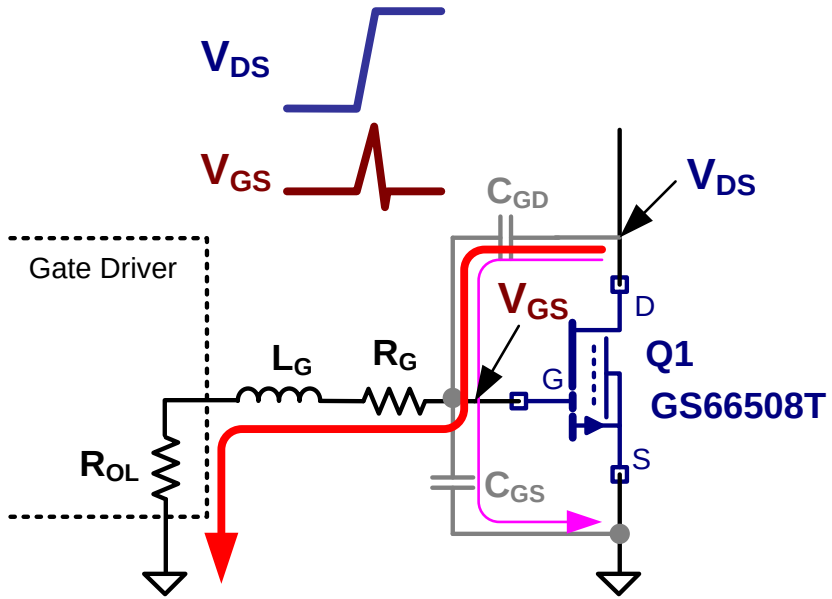
- Select driver with low source R_{OL}
- Optimize R_{GON} in half bridge
- Use small R_{GOFF} for turn-off
- Reduce gate loop inductance L_G

2) Adding external C_{GS}?

- Provides additional miller current shunt path
- Be careful when adding C_{GS} to the gate:
  - Slow down switching; increases gate drive loss
  - *Potential gate oscillation combined with parasitic inductance →Ext. C_{GS} provides low Z path for high-frequency gate current ringing*

2) Negative gate voltage?

- Increase noise immunity against miller turn-on
- Typical **-2** to **-3V** is recommended
- Reduce turn-off loss
- Higher reverse conduction loss -> design **trade-off**

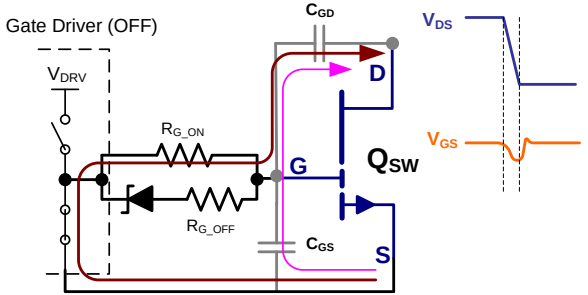


Miller current path

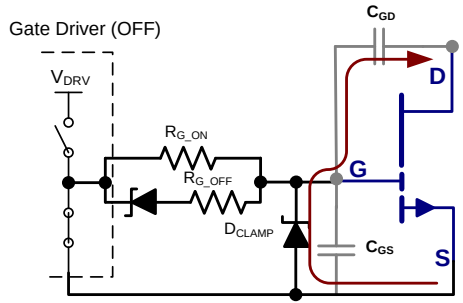
Clamping Diode

For gate driver with single output, a clamping diode is recommended

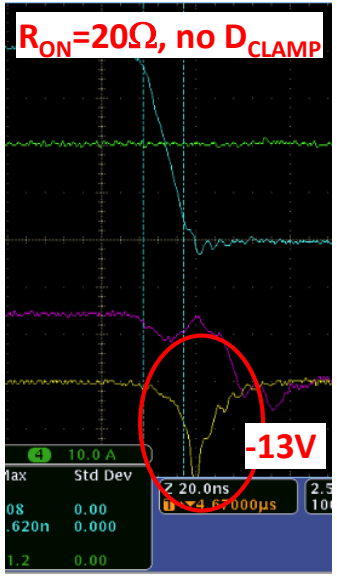
- High dV/dt at the Drain induces Miller Current flow (Source-to-Gate)
- R_{G_OFF} does not help with high dV/dt (i.e., blocked by series Diode)
- Negative voltage spike increases with higher R_{G_ON}
- Use a fast schottky diode or zener between G and S:
  - Be careful with gate ringing induced by zener diode

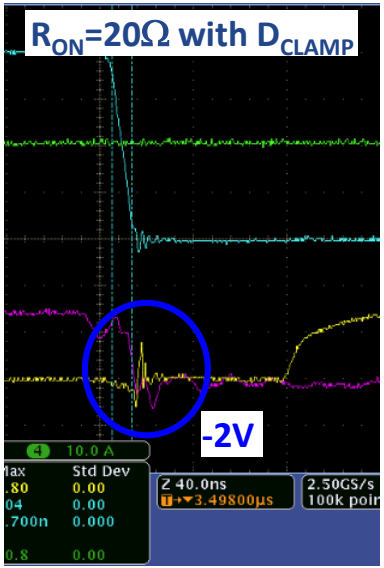


Miller Current flow, –dV/dt (**No Diode**)



With Clamping Diode

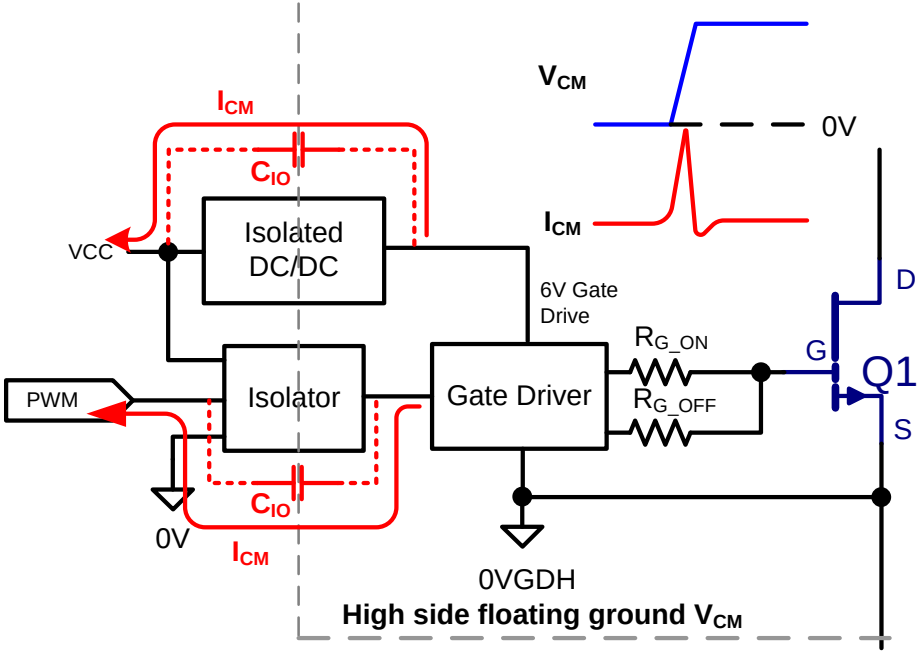




High side driver considerations

High side gate drive

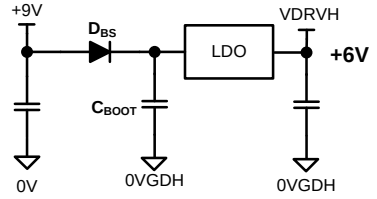
- GaN enables fast switching dv/dt >100kV/us:
  - Minimize Coupling capacitance C_{IO}
  - CM current via C_{IO} limits CMTI
- **Full Isolated gate drive:**
  - Best performance
  - Isolation power supply – Minimize inter-winding Capacitance
- **Bootstrap:**
  - Lower cost, simpler design
  - Post-regulation or voltage clamping is required after bootstrap



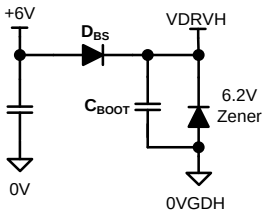
Note:
Watch for bootstrap HV diode power loss limit and recovery time for High-Frequency operation. Choose the HV diode with low C_j and fast recovery time. For switching frequency application > 500k-800kHz, isolated gate drive is recommended

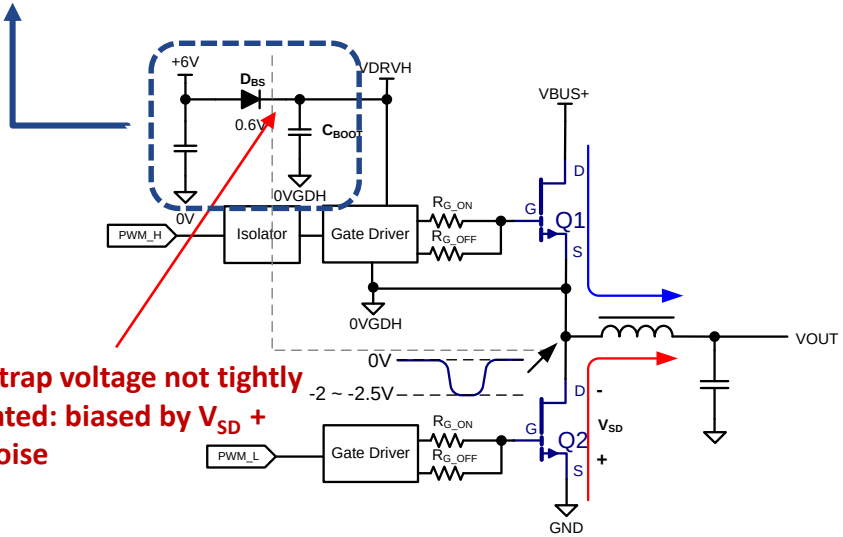
Bootstrap circuit design

Bootstrap with post-regulation



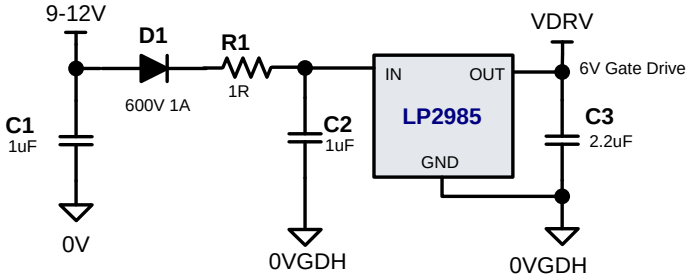
Using Zener for clamping

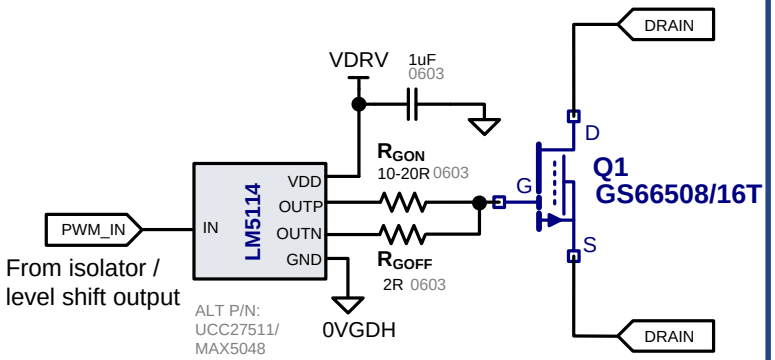




Bootstrap voltage not tightly regulated: biased by V_{SD} + V_{SW} noise

Bootstrap Design Example



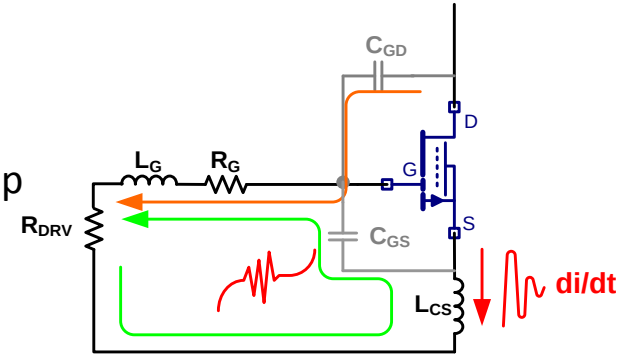


Preventing Oscillations

Gate drive stability – parasitic oscillation

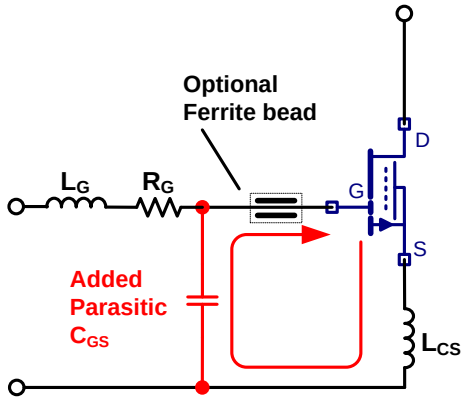
What causes the gate oscillation?

- Common Source Inductance (CSI) L_{CS} Feedback path from power loop to gate loop (di/dt)
- Capacitive coupling via miller capacitor C_{GD} (dv/dt)
- Uncontrolled oscillation if feedback phase shift is -180deg
- L_{CS} and power loop Inductance should be minimized



How to prevent parasitic oscillation

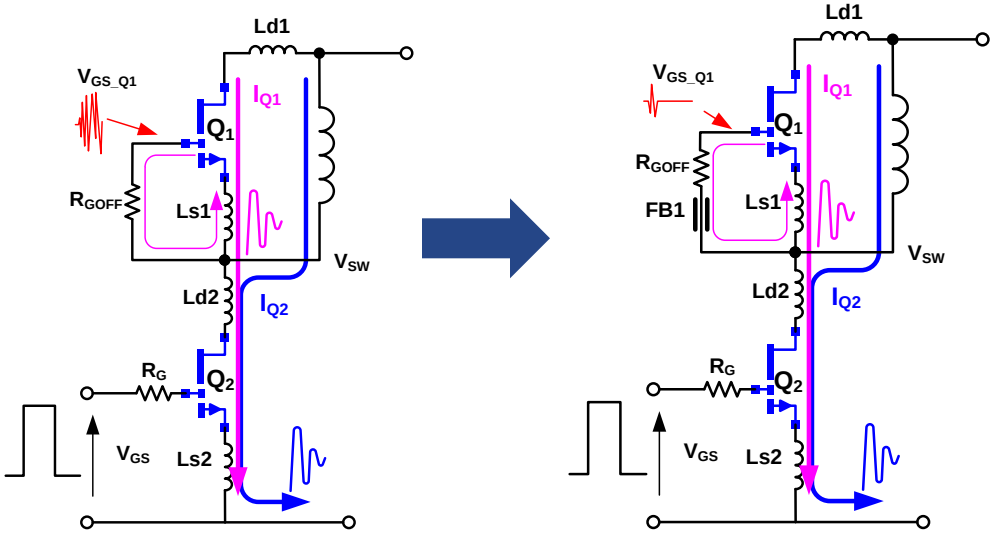
- Reduce $L_{CS,}$ L_G and minimize external C_{GD}
- Slow down turn-on to reduce dv/dt and gate ringing
- Reduce additional C_{GS} -> high frequency path for gate current ringing
- Add small ferrite bead in series with R_G if oscillation observed:
  - Damp high frequency current ringing
  - Use a small SMD ferrite bead (Z=10-20)



Preventing Oscillations – half bridge

Parasitic oscillation in half bridge

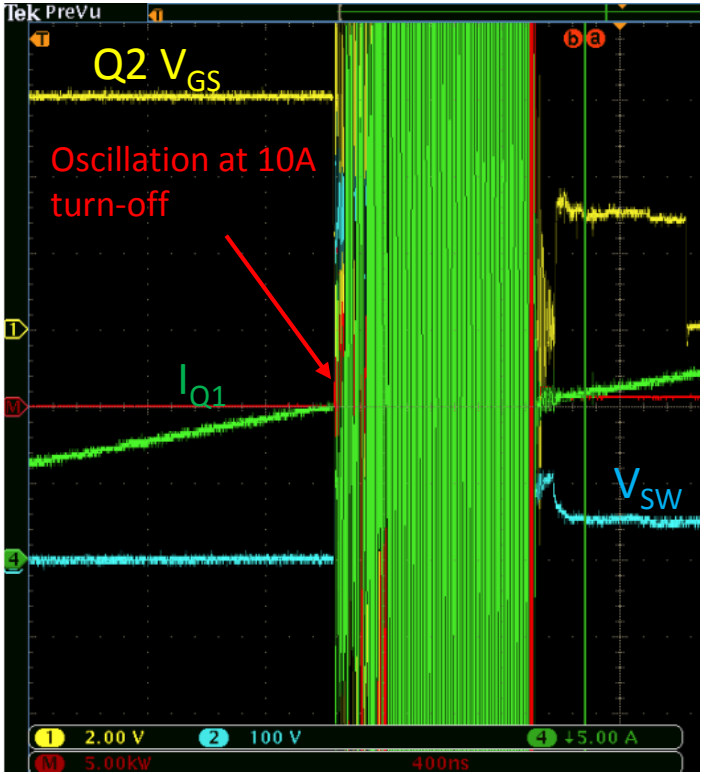
- Use double pulse tester as example: Q1 is synchronous and Q2 is active control device
- Q2 gate affects the Q1 gate stability with the presence of parasitic inductances
- Q2 switching noise couples to Q1 gate loop by parasitic inductance Ls1 (L*di/dt)
- Q1 Gate is OFF when Q2 is switched: Potential uncontrolled oscillation on half bridge if Q1 gate high frequency current ringing is not damped properly (Too low Z in turn-off drive path)
- **Adding drive pull-down impedance Z_{GATE} (Increasing R_{GOFF} and/or inserting a small ferrite bead) damps the gate current ringing and improves the half bridge switching stability**



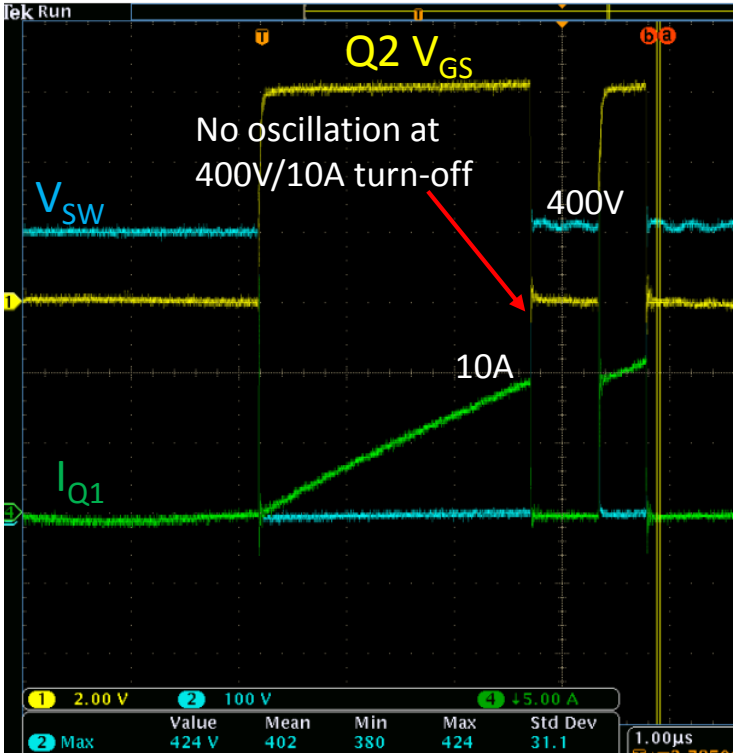
Ferrite bead can prevent oscillations

Parasitic oscillation in half bridge

GS66504B 400V/10A Turn-off gate oscillation
Q1: R_{GOFF}=3.3Ω; Q2: R_G=15Ω /3.3Ω



No oscillation observed at 400V/10A switching
Q1 R_{GOFF}=3.3Ω + **Ferrite bead**; Q2: R_G=15Ω /3.3Ω



Driver Selection

- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

Gate Driver selection

Select right gate driver for GaN E-HEMT

Non-isolated single gate driver:

Minimum requirement:

- Must operate at **5-6.5V** gate drive
- Low pull-down output impedance: **R_{OL} ≤ 2Ω**
- **2A** or higher peak drive current for robust turn-off
- Low inductance SMT package

Preferred:

- Separate pull-up/down drive output pins
- **≤ 1Ω** pull-down impedance
- Propagation delay < **20ns**
- Integrated LDO for regulated 5-6V gate drive
- High frequency capability (>1MHz)

Isolator / Isolated gate driver

CMTI rating:

- GaN switches fast: 50-100kV/us dv/dt at switching node is common
- High CMTI is required for 650V: 50kV/us is typical, 100-200kV/us preferred.

High F_{SW} and minimum dead time:

- Good delay matching between high and low sides:
  - **650V application w/ isolated driver: 50-100ns,** ≤ **50ns** preferred
  - 100V application w/o isolated: **<20ns** preferred.

Recommended gate drivers - 650V GaN E-HEMT

GaN Systems 650V E-HEMTs can be driven by many standard gate drivers

Non-isolated low side single gate drivers:

- **Recommend LM5114/UCC27511/MAX5048C**:
  - Separate source/sink outputs
  - Footprint compatible
  - Low T_{prod} and low pull-down resistance
- Other lab tested compatible gate drivers:
  - **FAN3122**
  - **FAN3224/FAN3225** (dual)
  - **MCP1407/TC4422/IXDN609SI/LTC4441**

Integrated isolated gate drivers

half bridge gate drivers (footprint compatible):

- SiLab **Si8273/4** (Use 4V UVLO for 6V drive, **Recommended for high CMTI rating 200kV/us**)
- SiLab **Si8233AD** (UVLO= 6V for 6.5V gate drive)
- Analog device **ADuM4223A** (UVLO = 4.1V)

Isolated single gate driver:

- **Recommended:** SiLab **Si8271** (4V UVLO for 6V drive, 200kV/us CMTI rating)
- SiLab **Si8261BAC** (6.3V UVLO for 6.5V gate drive)

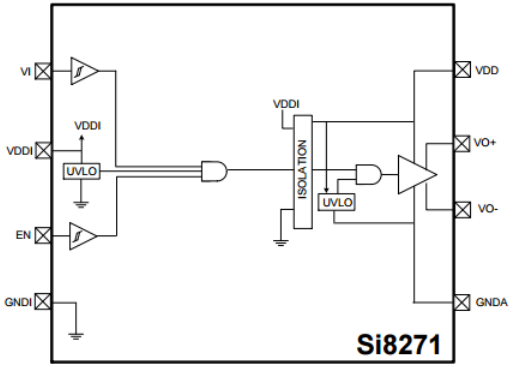
Isolators (use with low side gate drivers):

- SiLab **Si8610**: Recommended for High CMTI (lab tested 150V/ns) and low Tprod, requires 5V VCC
- New SiLab **Si862xxT** features >100kV/us CMTI rating
- Avago High CMR opto-coupler **ACPL-W483**: No 5V needed / Longer propagation delay and lower CMTI rating / 5kVrms reinforced insulation: for industrial application inverter, 3ph motor drive

SiLabs Si827x Series for 650V GaN E-HEMT

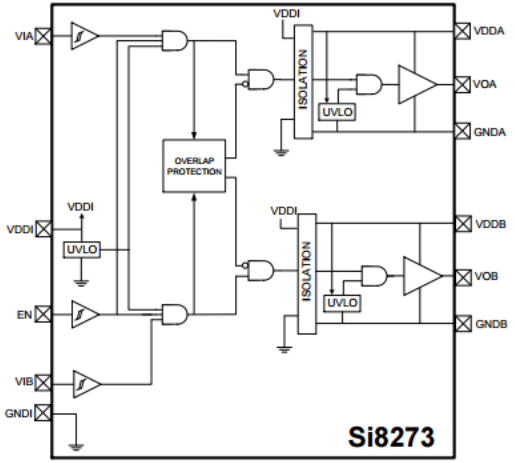
New Silicon Labs Si827x series isolated gate driver offers high CMTI dv/dt rating and low UVLO for GaN E-HEMTs:

- 4V UVLO for 5-6V optimum gate drive
- Separate Source/sink drive outputs (Si8271)
- 4A peak current
- High dv/dt immunity: **200kV/us** CMTI, **400kV/us** latch-up



Recommended P/N for GaN E-HEMT (4V UVLO):

- **Si8271BG-IS:** Single, split drive outputs
- **Si8273GB-IS1/IM:** High Side / Low Side
- **Si8274GB1-IS1/IM:** PWM with DT Adj.
- **Si8275GB-IS1/IM:** Dual



Recommended gate drivers - 100V GaN E-HEMT

Gate driver for 100V Application:

Single/dual gate driver:

- Recommend: **LM5114/FAN3122/FAN3225**
- Any standard MOSFET driver that supports 5-6V gate drive
- Secondary Synchronous Rectification

Half bridge gate driver:

- **For 48V Sync Buck, motor drive / inverter**
- No isolation required
- Dead time loss is critical: Minimize dead time
- TI **LM5113** (5V VCC, recommended for good propagation delay matching)
- Linear Tech **LTC4444-5** (Synchronous MOSFET driver, 5-6V VCC)

Compatible Controllers:

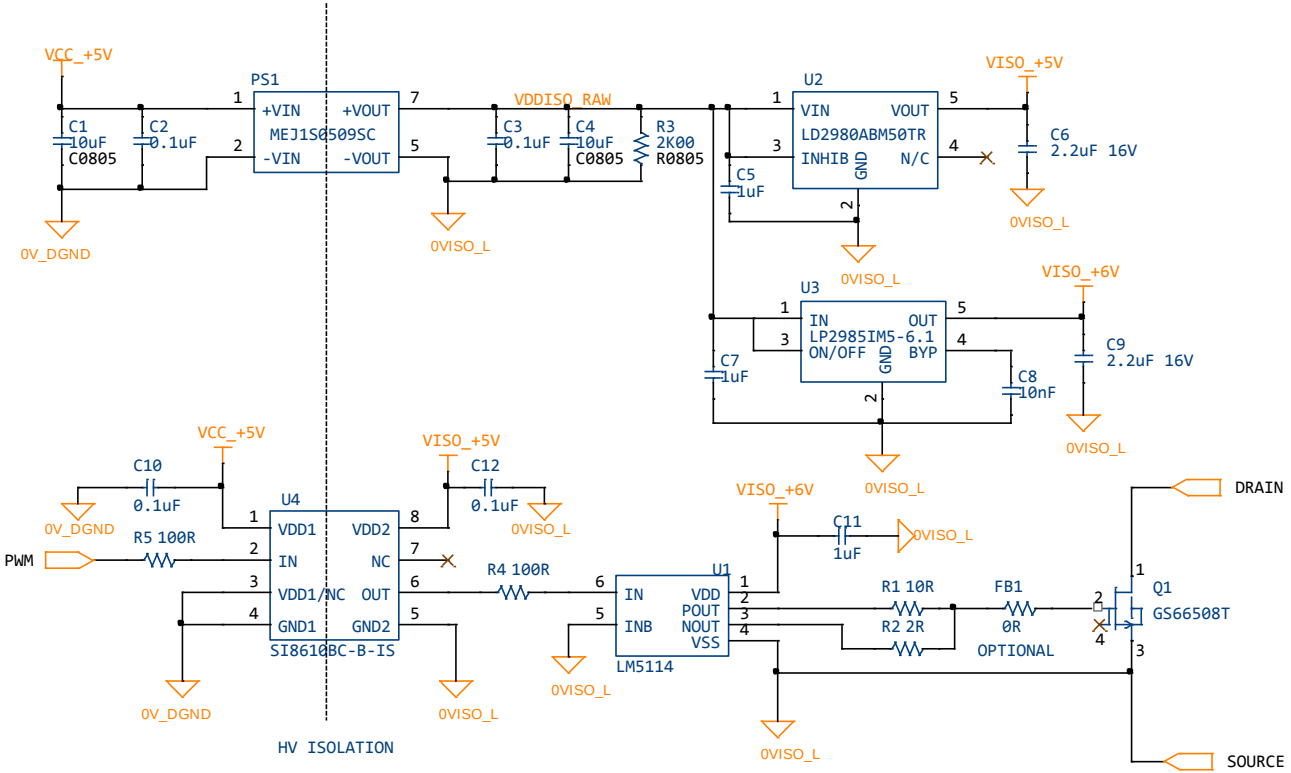
- **LTC3890**/**LTC3891** (60V Synchronous step-down controller, dual/single phase)
- **TPS40490** (5-60V Synchronous PWM Buck Controller)

Design Examples

- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

650V Gate Drive Design Example 1

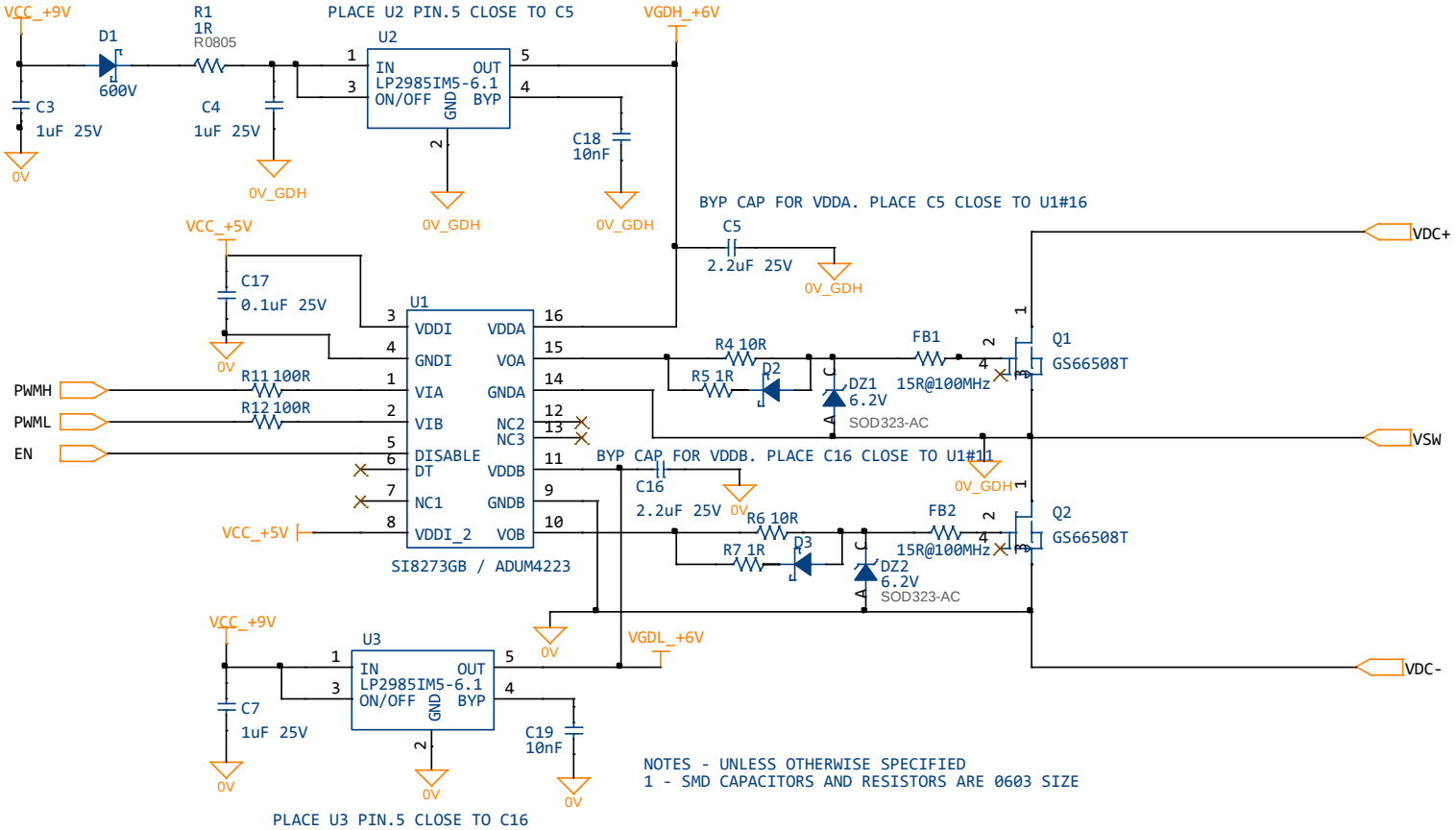
650V Half bridge fully isolated gate driver design reference (LM5114 + Si8610)



NOTE - UNLESS OTHWISE SPECIFIED
1 - ALL SMD CAPACITORS AND RESISTORS ARE 0603 SIZE
2 - SMD CAPACITORS ARE 25V RATED 10%

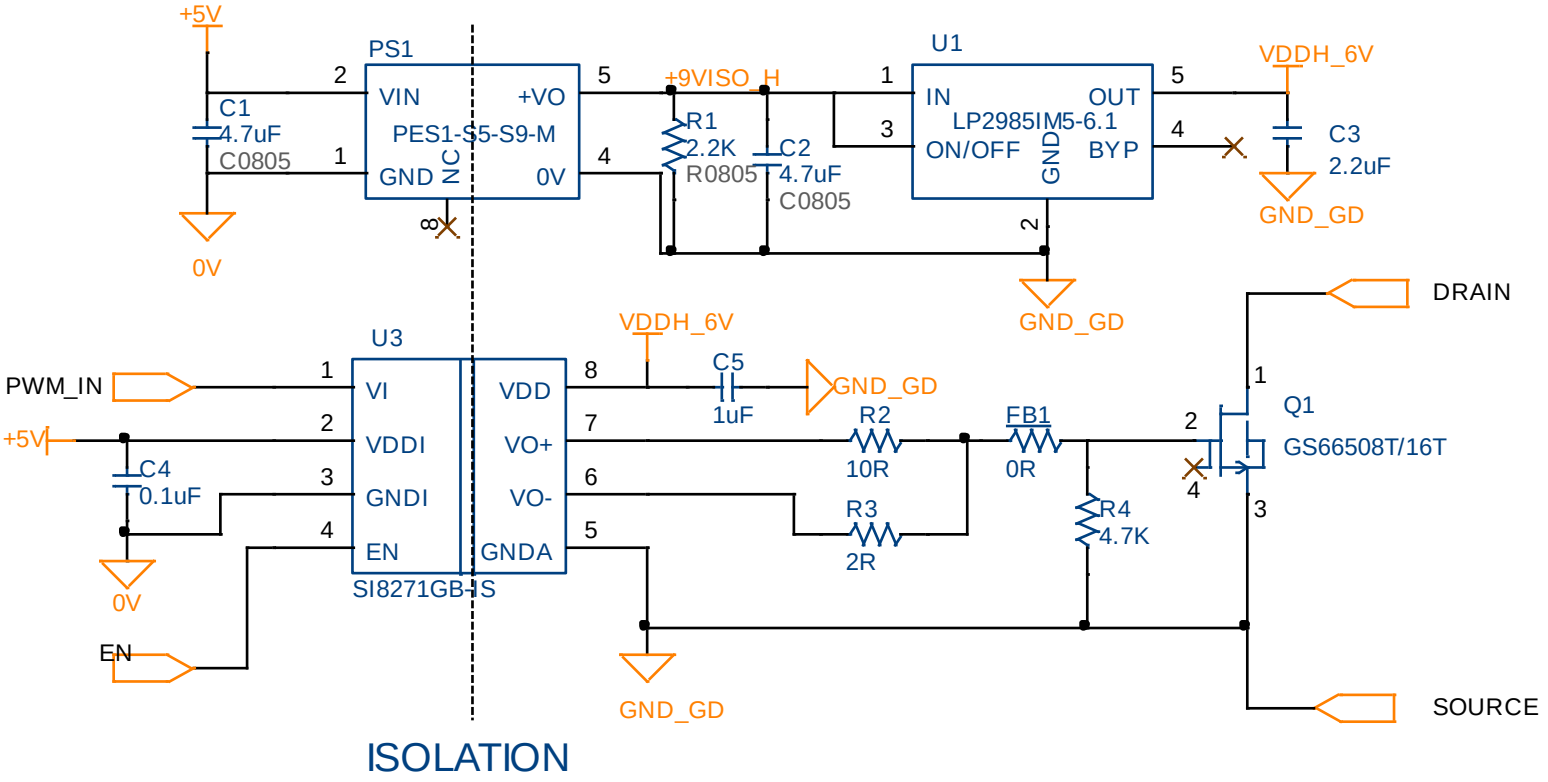
650V Gate Drive Design Example 2

650V Half bridge gate driver design using Si8273GB (footprint compatible with ADuM4223)



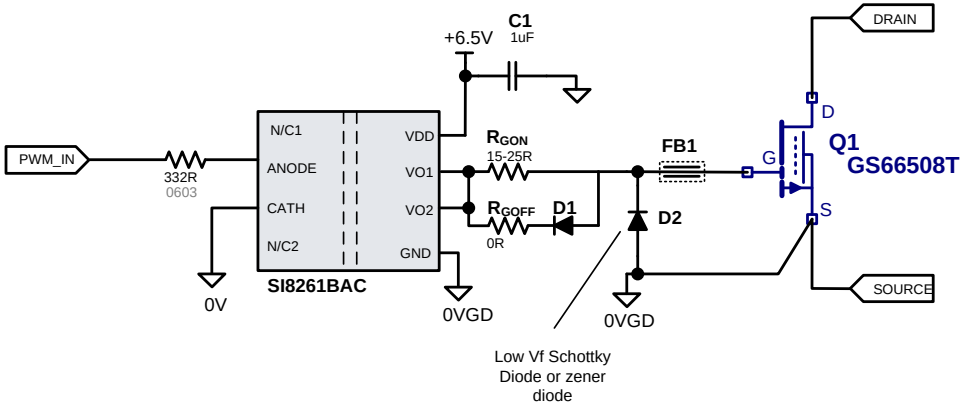
650V Gate Drive Design Example 3

650V Half bridge gate driver design (Si8271GB-IS w/ Isolated DC/DC)

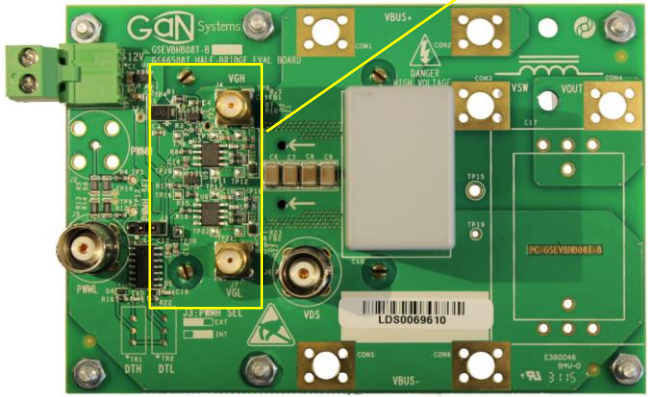


650V Gate Drive Design Example 4

650V Half bridge power stage design based on Si8261BAC (GS66508T Eval Board)



FB1: 15ohm@100MHz
D1: PMEG2010
D2: 6.8V 200mW Zener diode SOD323 (MMSZ5235BS-7-F)



Full schematics and Gerber files can be found at:
http://www.gansystems.com/gs66508t-evbhb.php

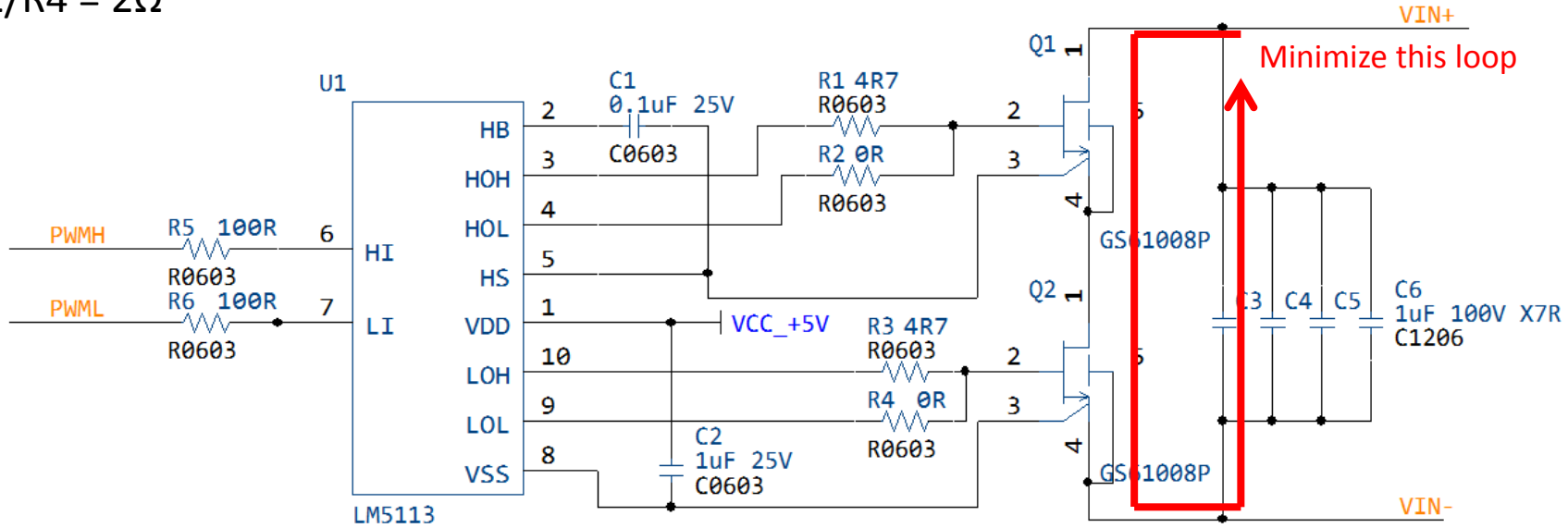
100V Gate Drive Example

LM5113-based half bridge power stage (GS61008P), VDRV=+5V

For half bridge-based application: Sync. Buck, motor drive/inverter

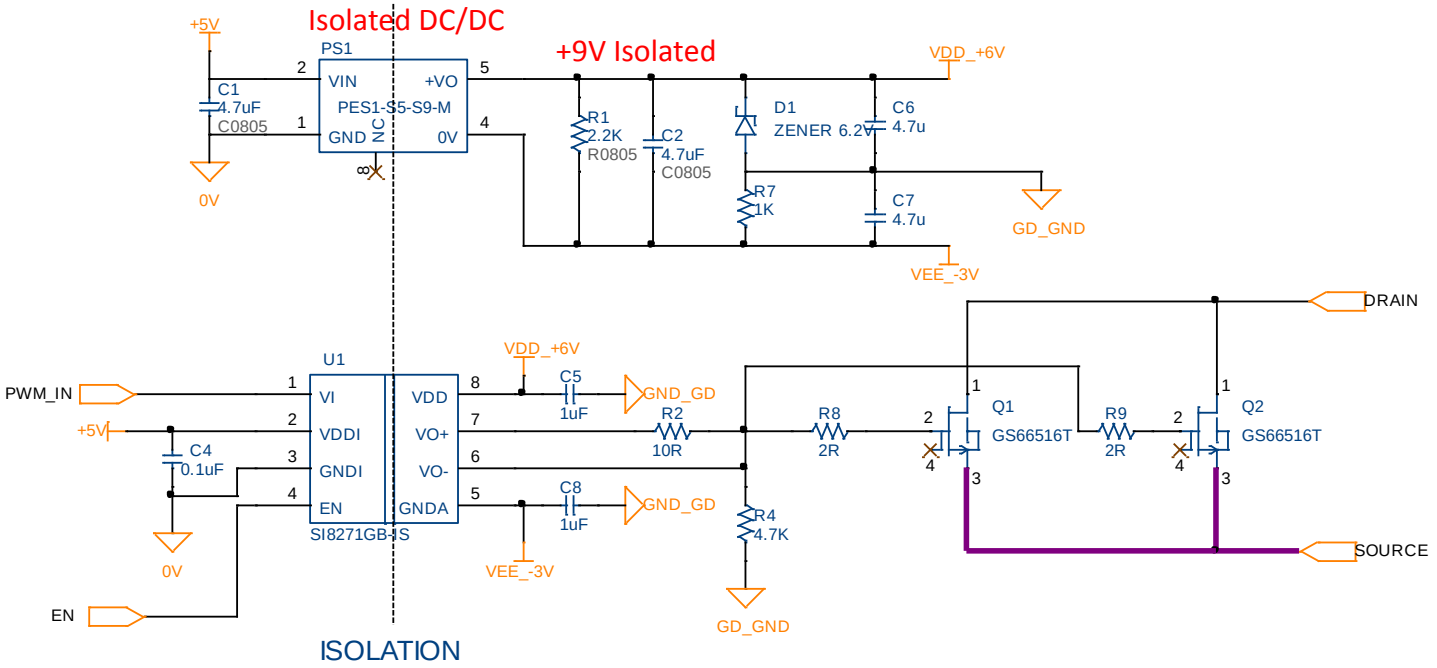
Recommended Gate resistor:

- R1/R3 = 4.7 -10Ω
- R2/R4 = 2Ω



Gate drive with negative gate bias

- For higher power and paralleled design, a small negative gate bias can be used to ensure safe turn-off
- Use a zener to create negative gate drive rail: +6/-3V

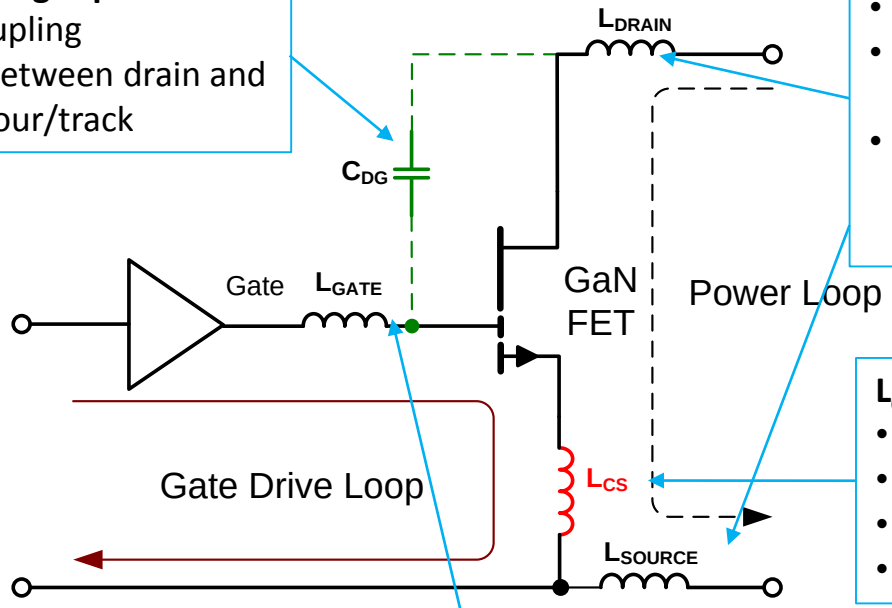


PCB Layout

- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

Impact of PCB Layout Parasitics

C_{DG}: drain-to-gate coupling capacitance
- Capacitive noise coupling
- Avoid overlapping between drain and gate drive copper pour/track



L_{DRAIN}/L_{SOURCE} : Power Loop Inductance:
- Drain voltage overshoot
- Turn-on/off drain voltage/current ringing
- Minimize power loop length and place decoupling Cap close to power device

L_{CS}: Common source Inductance:
- Gate ringing / oscillation
- Slow down switching
- Critical for gate drive stability
- Use kelvin connection to source

L_{GATE}: Gate loop inductance
- Gate signal over/undershoot
- Miller turn-on
- Place driver close to GaN FET to minimize gate loop

Layout best practice checklist

1. **Reduce common source inductance**
   - Reference gate return ground to the source pad using Kelvin connection. For GS6xxx8P and GS66508B package use “SS” pin.
   - Increase R_G or use ferrite bead on gate if gate oscillation is observed
2. **Optimize gate drive loop:**
   - Place driver close to GaN FET
   - Minimize the gate drive loop area and length
3. **Optimize power loop inductance:**
   - Use tight layout to minimize power loop length
   - Place decoupling capacitors as close as possible.
4. **Design for high dv/dt**
   - Minimize noise coupling due to PCB parasitic capacitance
   - Minimize overlapping between drain side power connection and gate drive signal track.
5. **Optimize thermal performance (B&P type package):**
   - Design for low thermal resistance using thermal vias and Cu. Pours

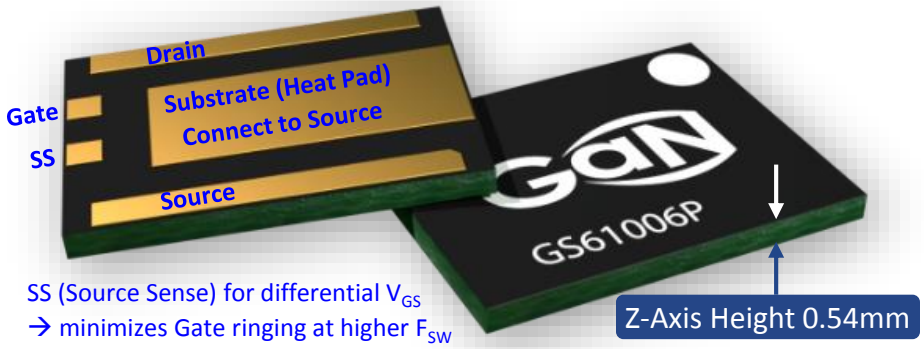
GaN*PX*™ Optimized for Switching, Thermals, & PCB Layout

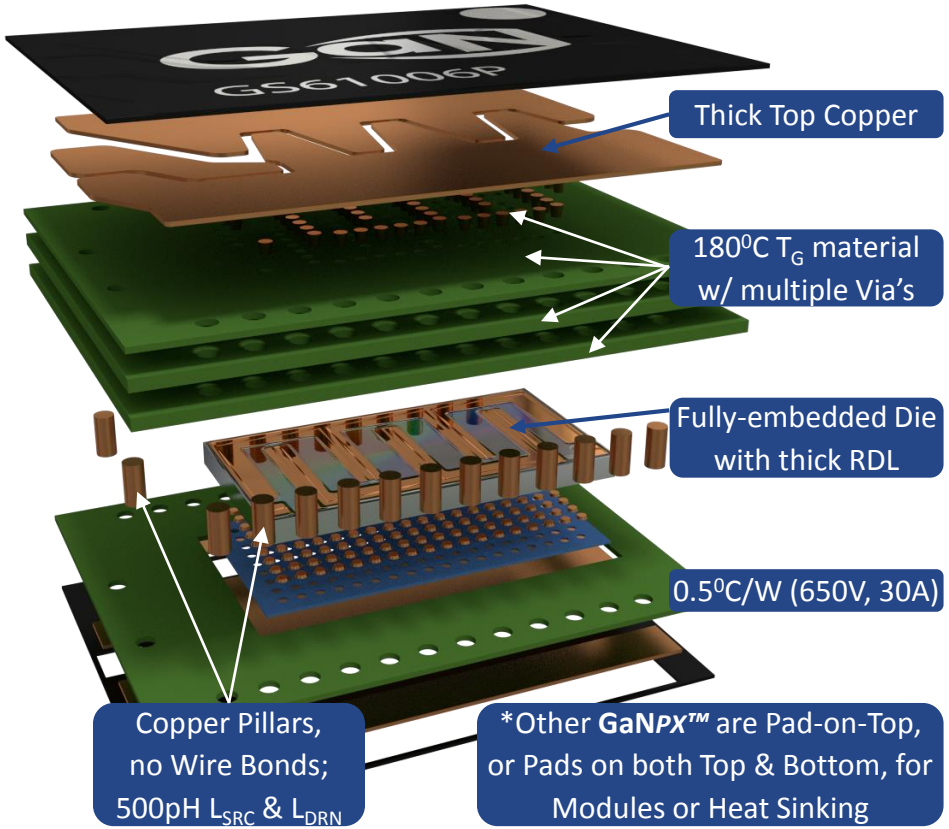
No Wire Bonds: ultra-low Inductance and much higher Manufacturing Reliability

Thick RDL & top Copper: extremely low R_{ON}

Embedded Package using high-T_G material

Overall design achieves optimized Thermals

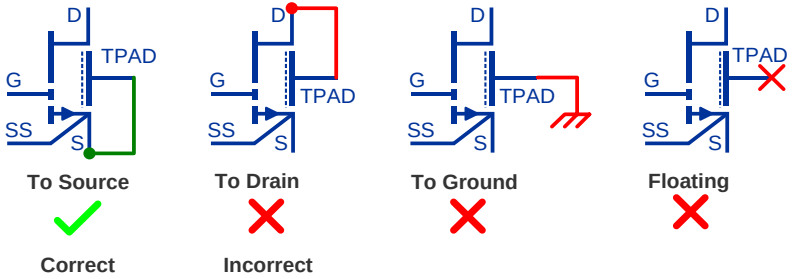




B & P Type GaN*PX* PCB Layout

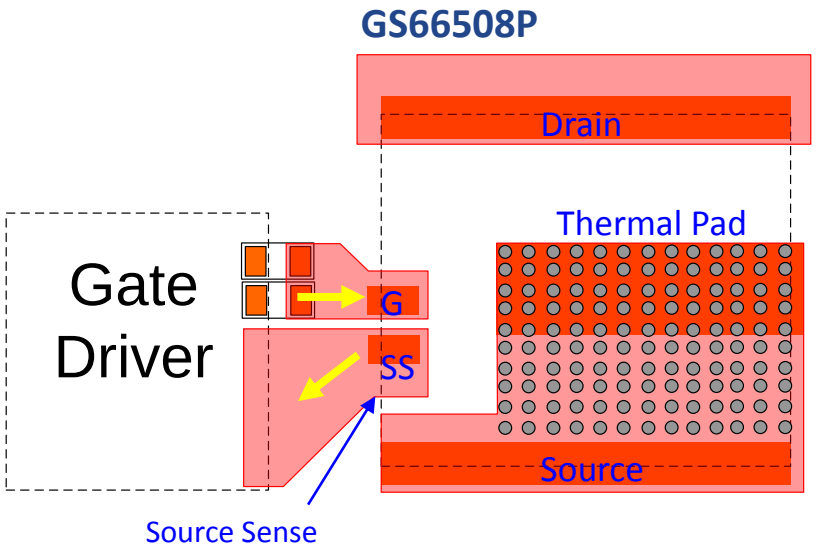
Bottom side **GaN*PX*™** “P” & “B” Packages

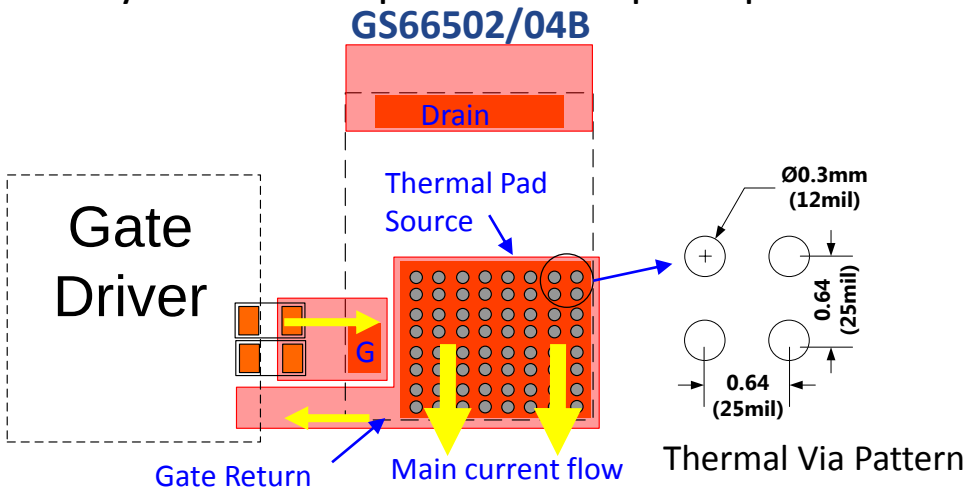
- B package: create kelvin source on PCB
- P package: use SS pin
- Thermal pad connect to Source
- Use thermal vias for PCB cooling



For P package:

Always connect thermal pad to Source for optimum performance

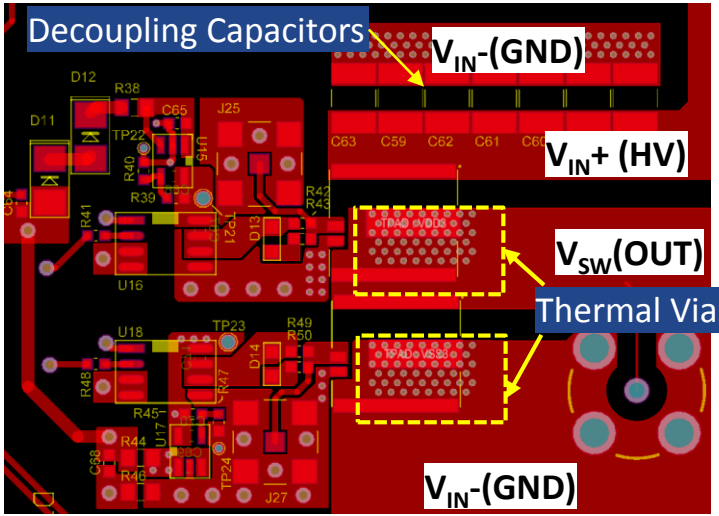




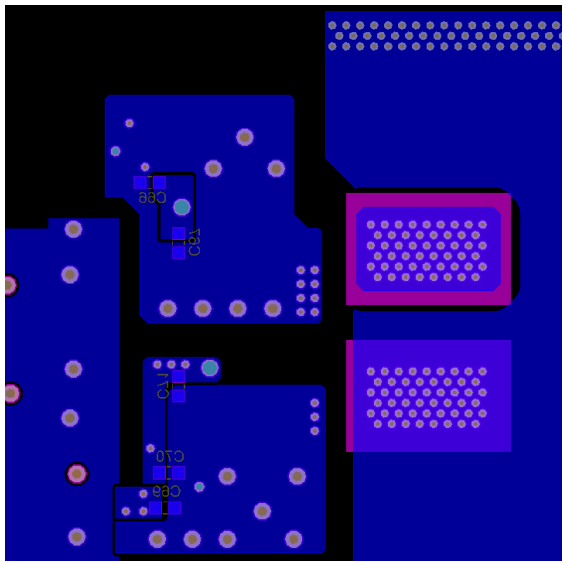
Half bridge Layout Examples 1

GS66508P Half bridge – (Si8261)

Component Side

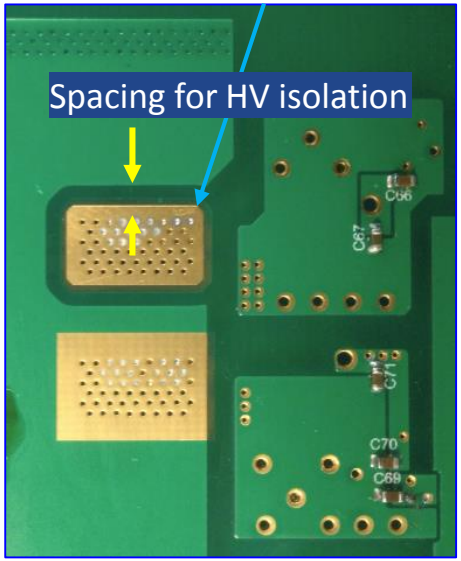


Bottom Side



Solder Mask pulled-back:

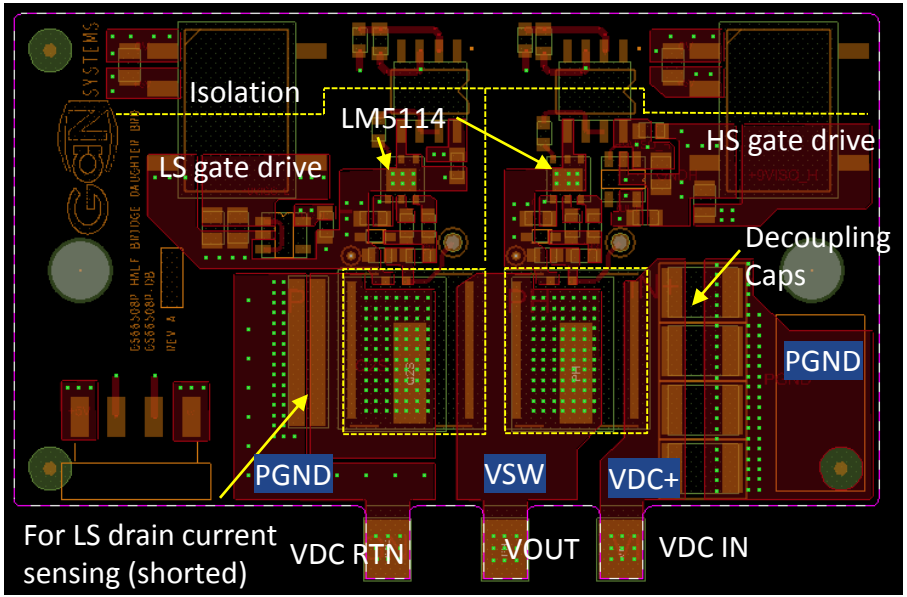
- Improves thermal performance
- Allows Heat Sink attachment



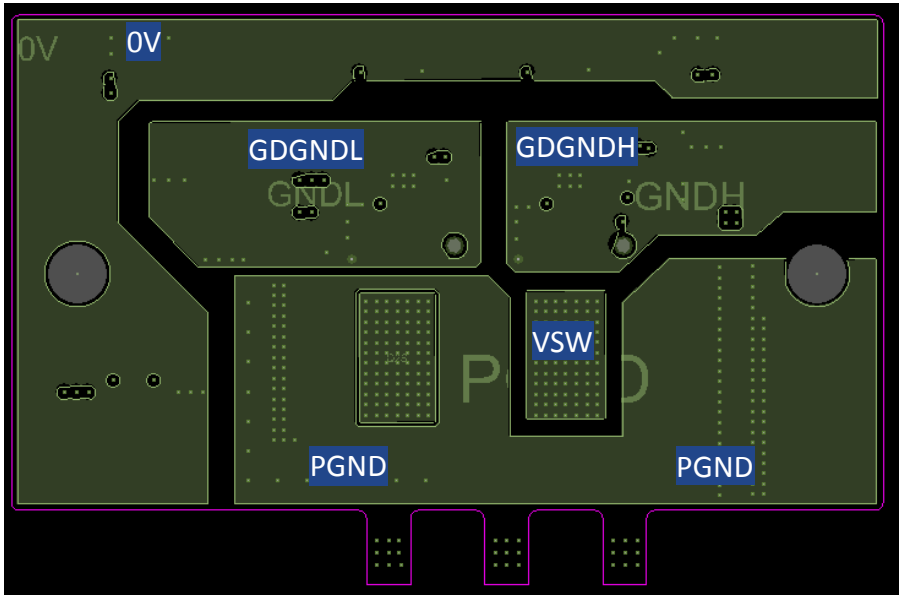
GS66508P Evaluation Board Layout Example

Half bridge Layout Examples 2

GS66508P Half bridge daughter board (isolated gate drive)



Top (component) layer

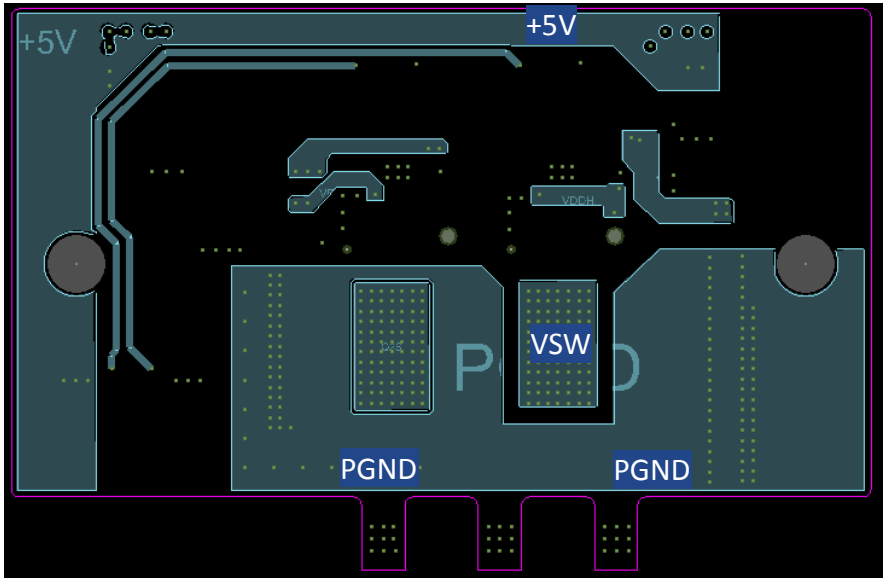


Internal Layer 1

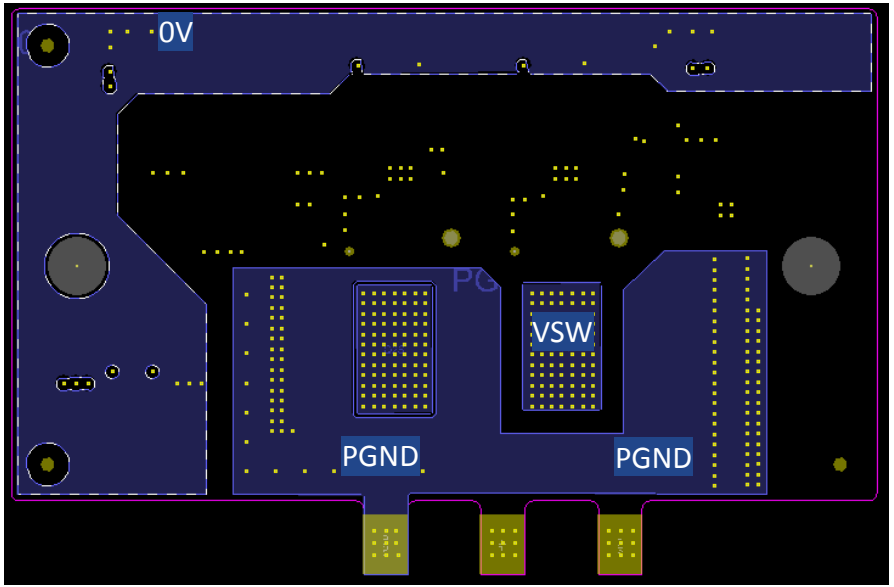
GS66508P Half Bridge Daughter Board Layout Example

Half bridge Layout Examples 2

GS66508P Half bridge daughter board

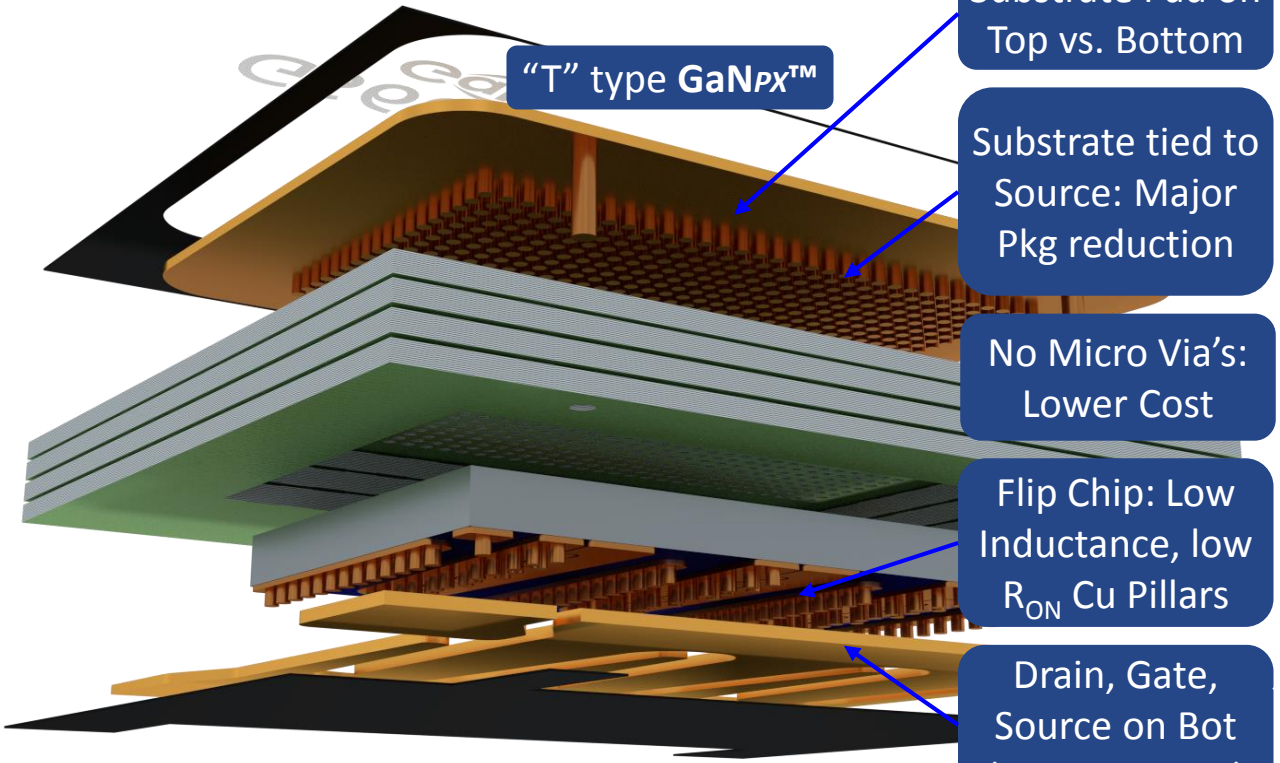


Internal layer 2



Bottom layer

GaN*PX* T-Type: Additional Optimization for Power Density



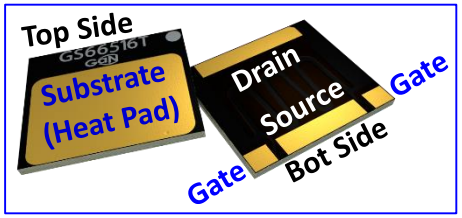
Substrate Pad on Top vs. Bottom

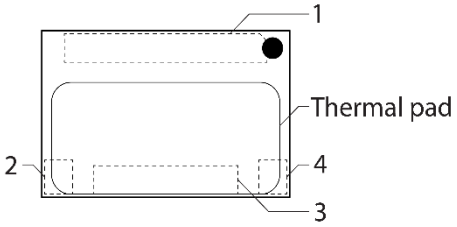
Substrate tied to Source: Major Pkg reduction

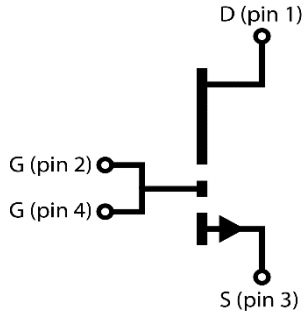
No Micro Via's: Lower Cost

Flip Chip: Low Inductance, low R_{ON} Cu Pillars

Drain, Gate, Source on Bot (**GaN*PX*™** SMD)





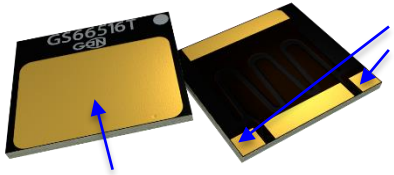


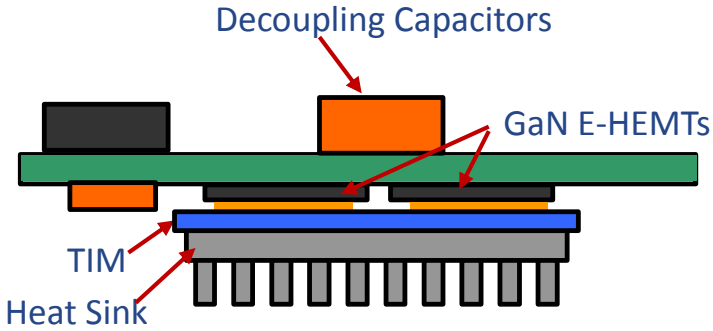
GaN*PX*™ "T" designed for higher-power Applications with Top-Side Heat-Sinking and lower Θ_{JA}

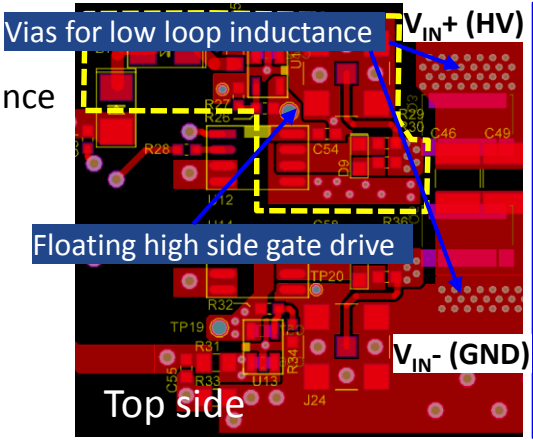
GaN*PX* T type PCB Layout

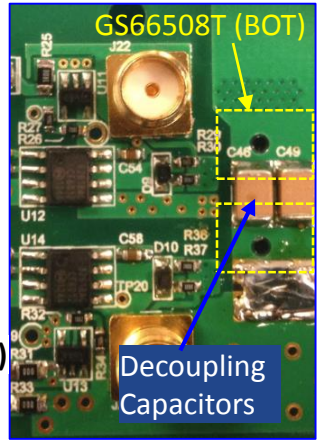
Top side cooled **GaN*PX*™** "T" series packages

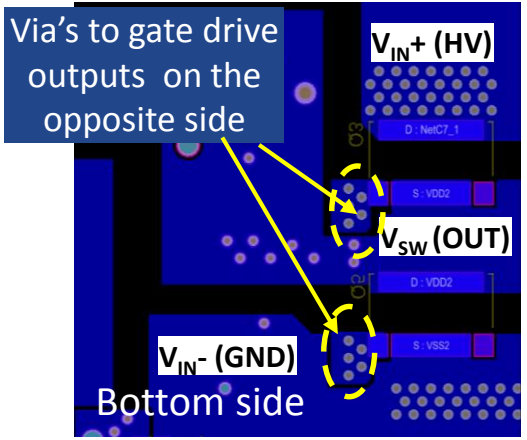
- low inductance package design with excellent thermal performance
- Dual gate (symmetric, internally connected) for easier layout
- Use the gate on driver side and keep the other floating, or
- Connect both gates for lower L_{gate} if layout allows







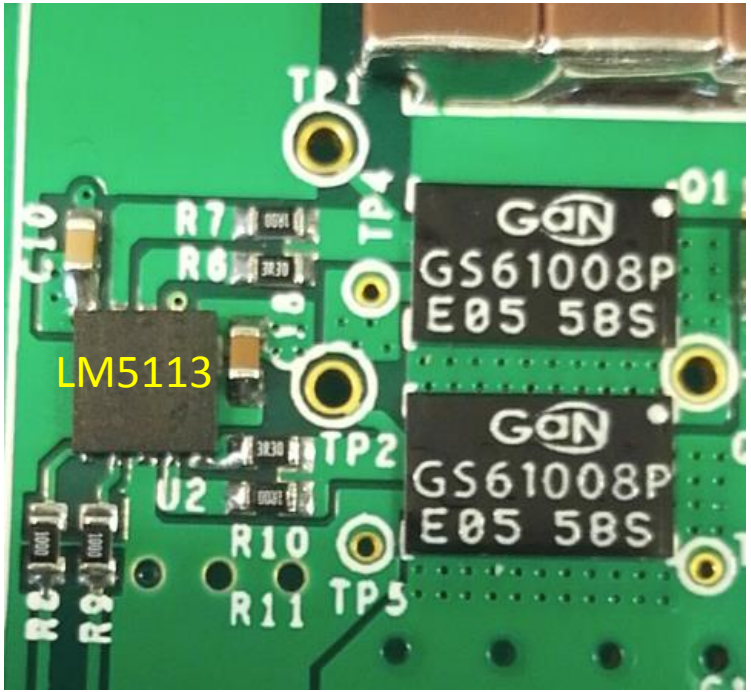


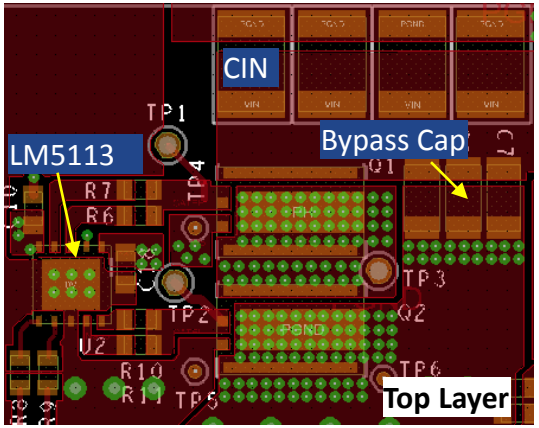


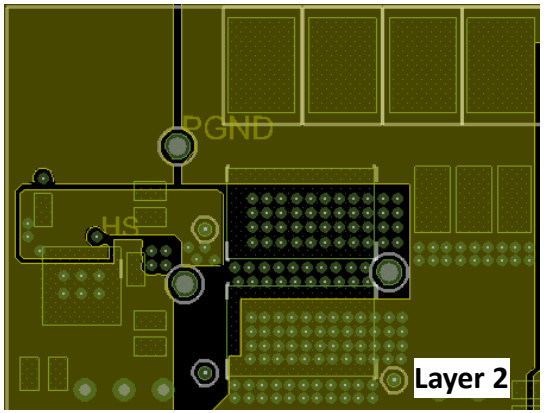
GS61008P 100V Half Bridge Layout Example

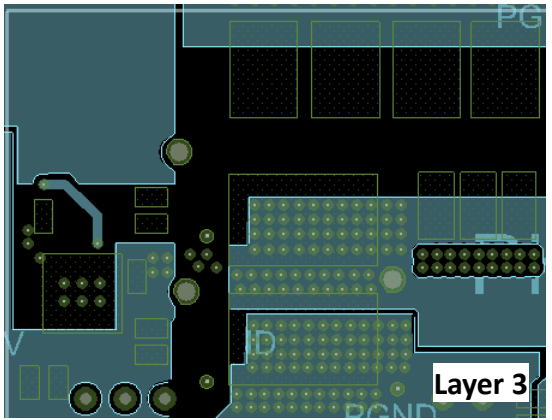
100V GS61008P Half bridge Layout

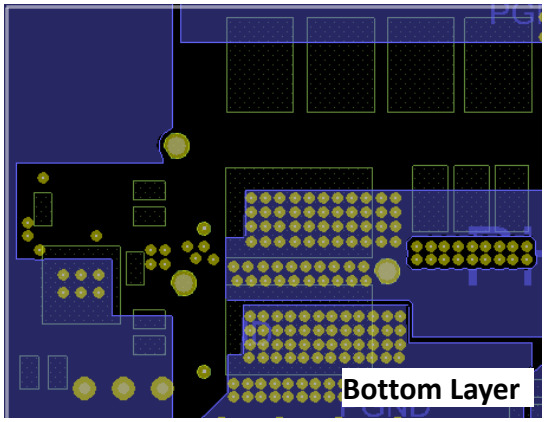
TI LM5133 half bridge gate driver





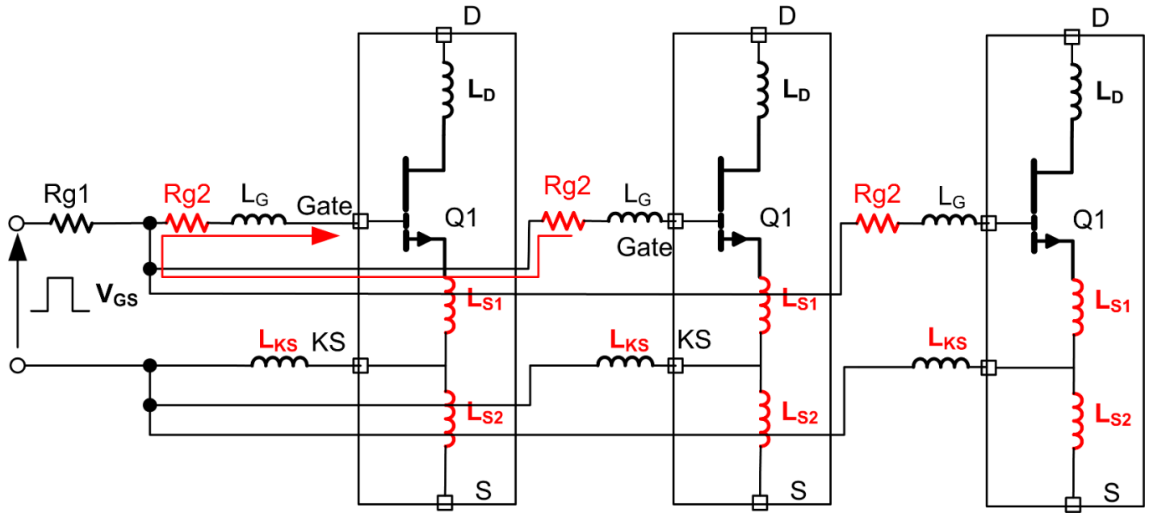






Optimum Gate drive layout for Paralleling

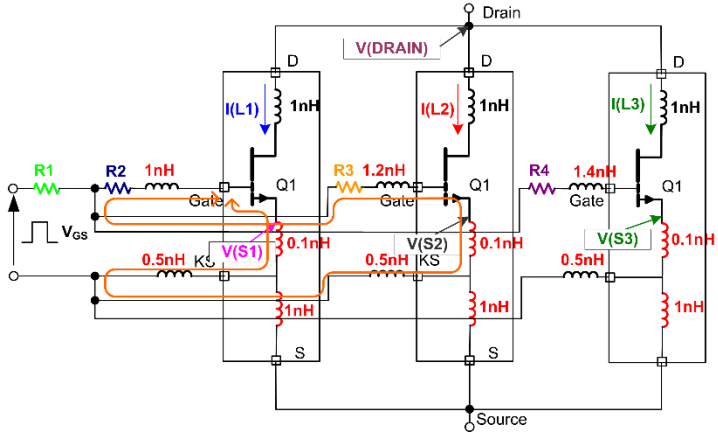
- GaNPx is easy to parallel thanks to its low package inductance
- Star connection and equal gate length if possible (minimize current imbalance caused by L_G)
- **Insert small distributed R_{G2} on each gate to minimize the gate current circulation and ringing among all paralleled devices.**
- Minimize Kelvin source connection inductance L_{KS} and equal gate return length if possible
- If needed, a small negative gate drive (+6/-3V) can be used to improve gate drive robustness



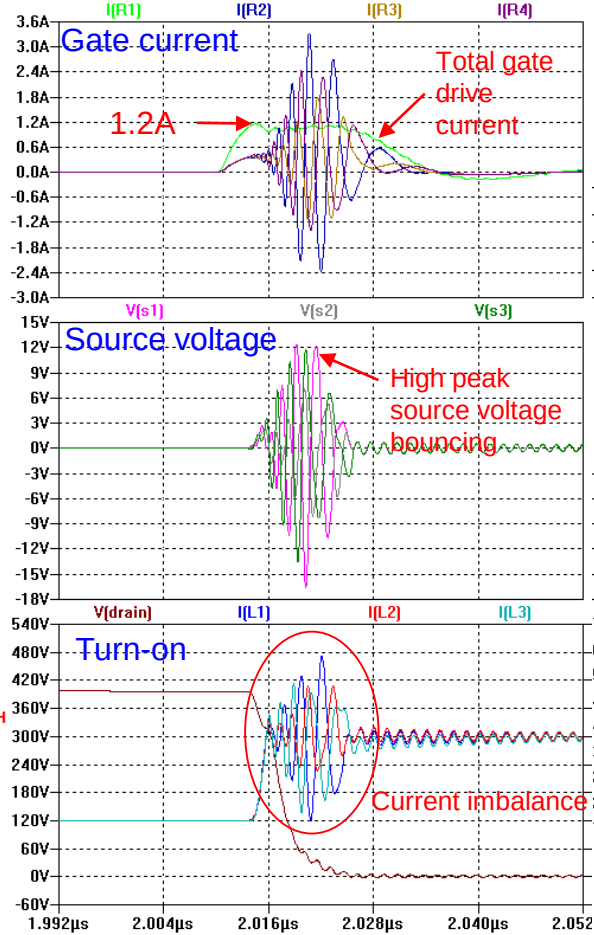
Effect of series Rg on each gate in paralleling operation

Centralized vs distributed Rg:

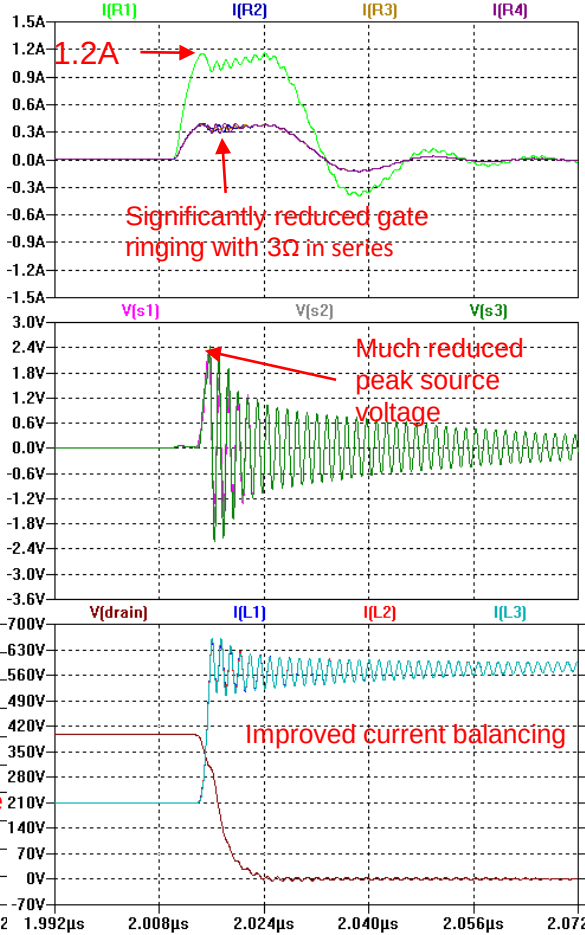
- Ltspice simulation shows that using series Rg on each device **significantly** reduces gate ringing and improve switching stability
- Gate ringing/oscillation is caused by high-frequency current ringing among gates triggered by imbalanced current across Lcs.
- R1 current show no ringing in both cases



Scenario #1: Centralized R1=**2Ω**, R2=R3=R4=0



Scenario #2: Series Rg: R1=0. R2=R3=R4=**3Ω**

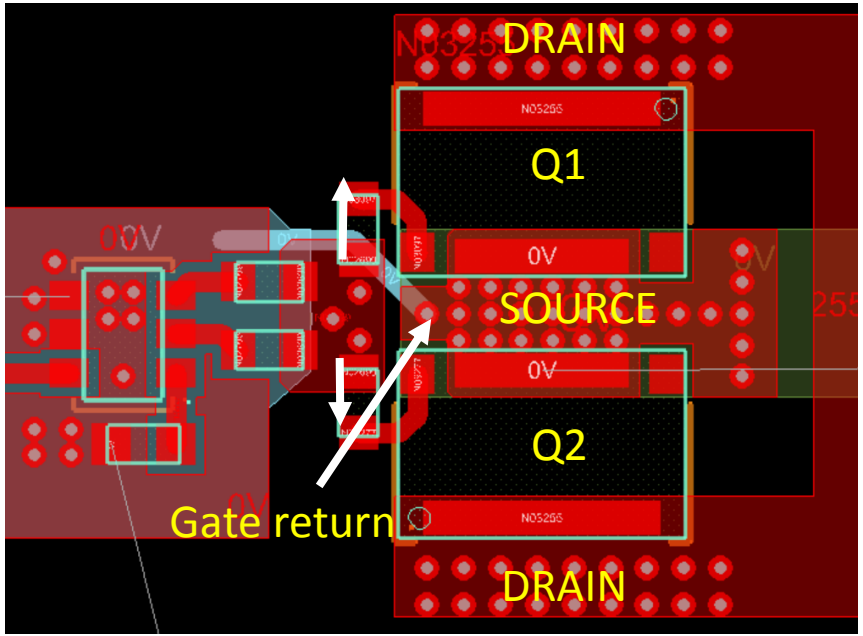


Paralleling for T package

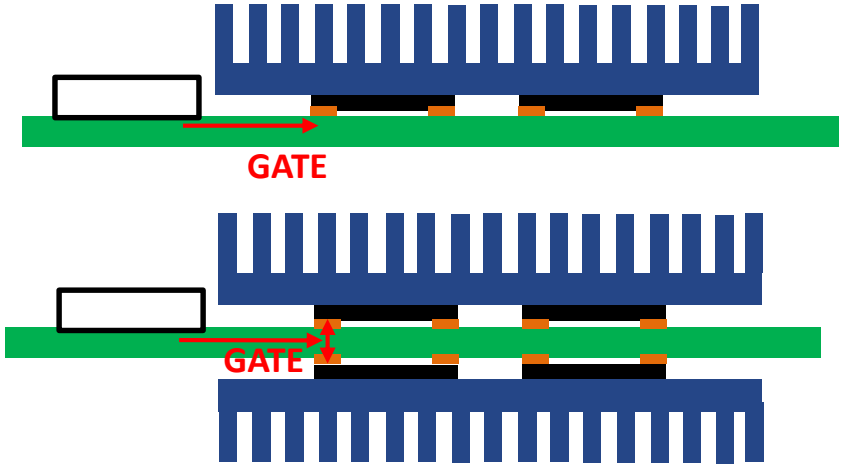
T type package is designed for easy paralleling

- Symmetric gate design allows short and equal gate length
- Easy dual side placement with optimum layout
- Use individual gate resistors and star connection for gate drive

An example showing symmetric gate design with GaNPx T



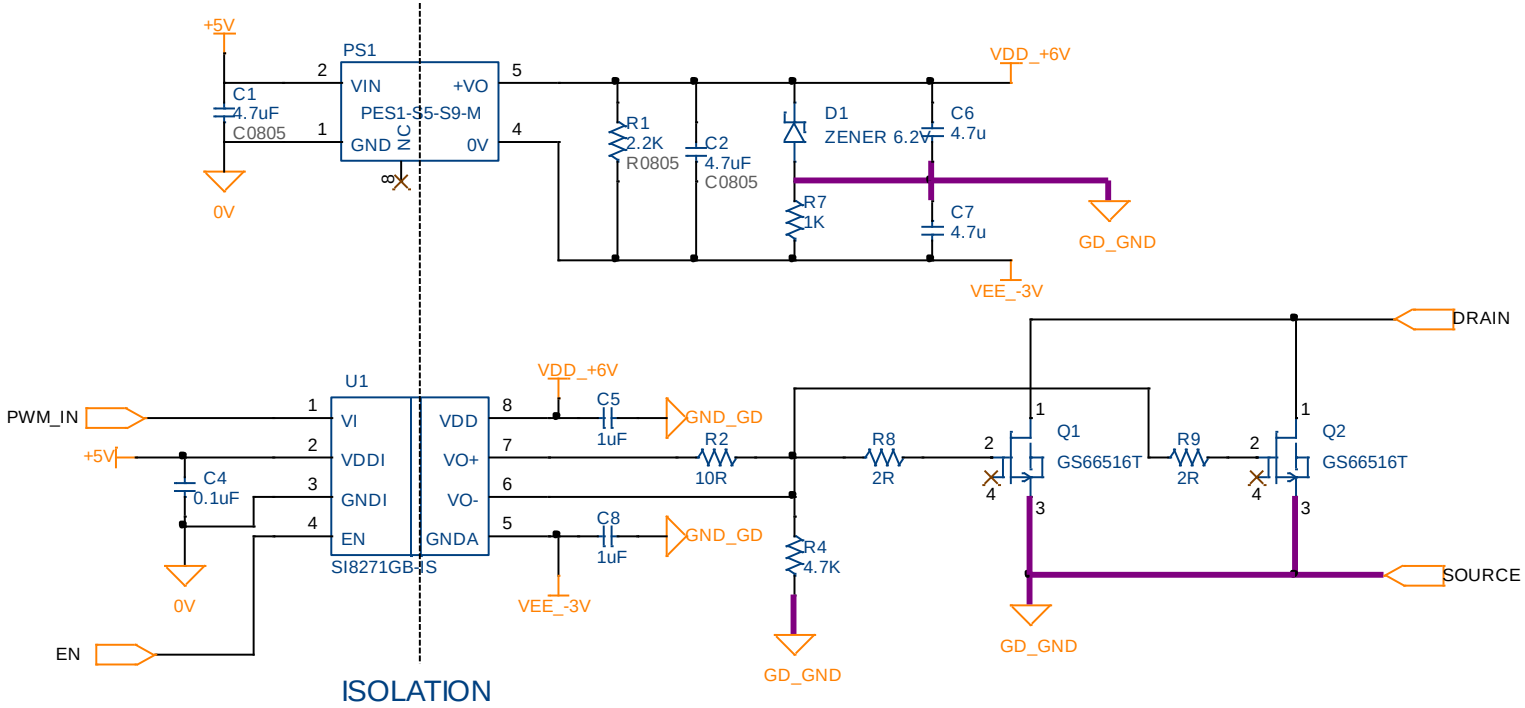
Device paralleling with dual side device placement and cooling



Gate drive example for paralleling

Gate drive design for paralleling GS66516T

- Use a small distributed R_G on each gate
- +6/-3V gate drive



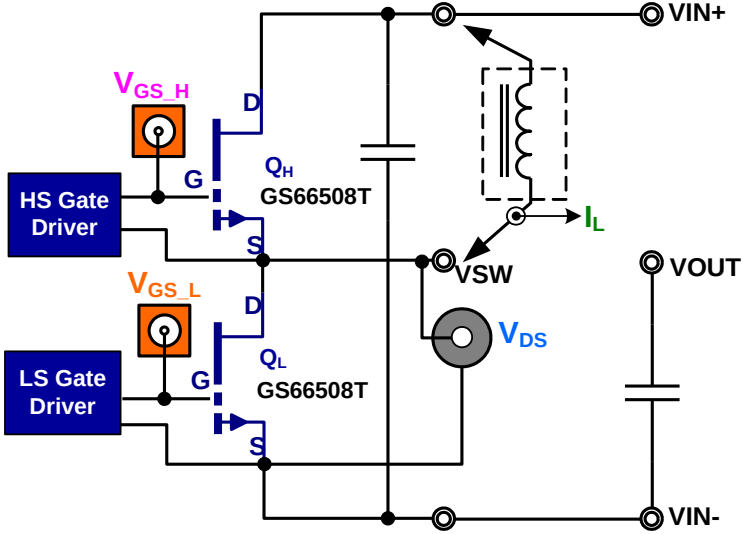
Switching Test Results

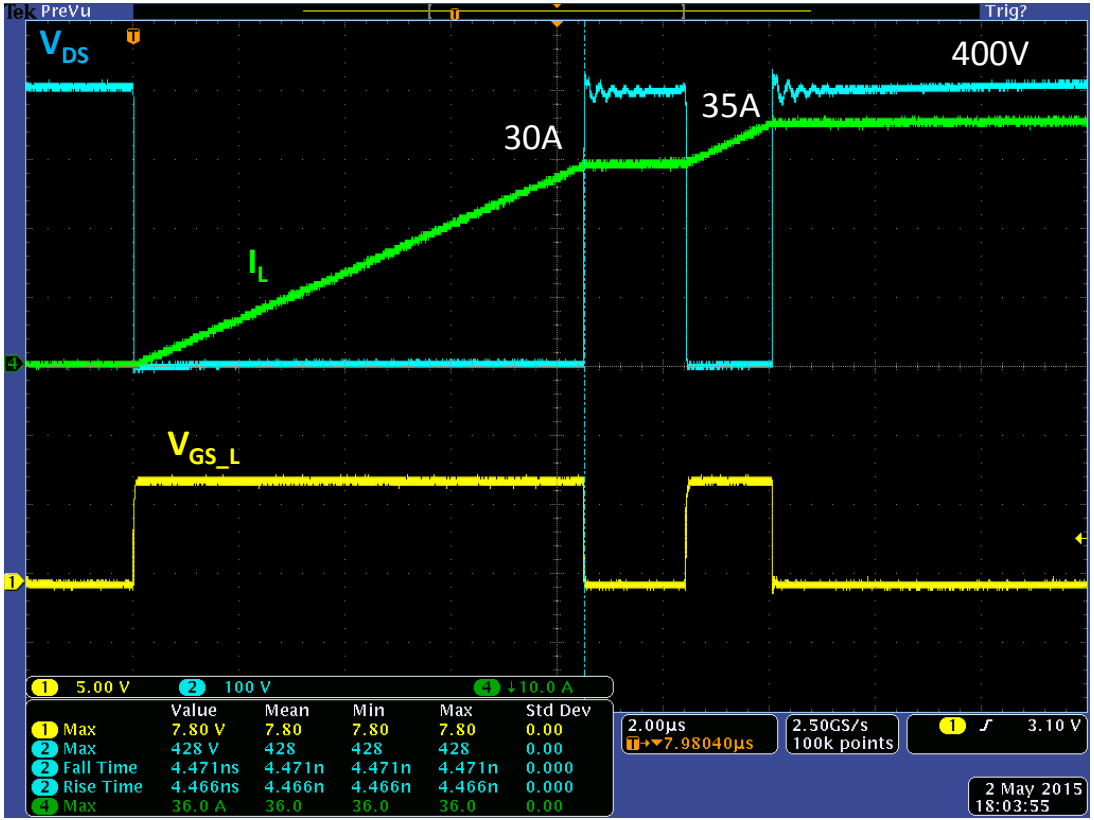
- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

Switching Tests - Double Pulse Test Waveforms

Double pulse Switching Test

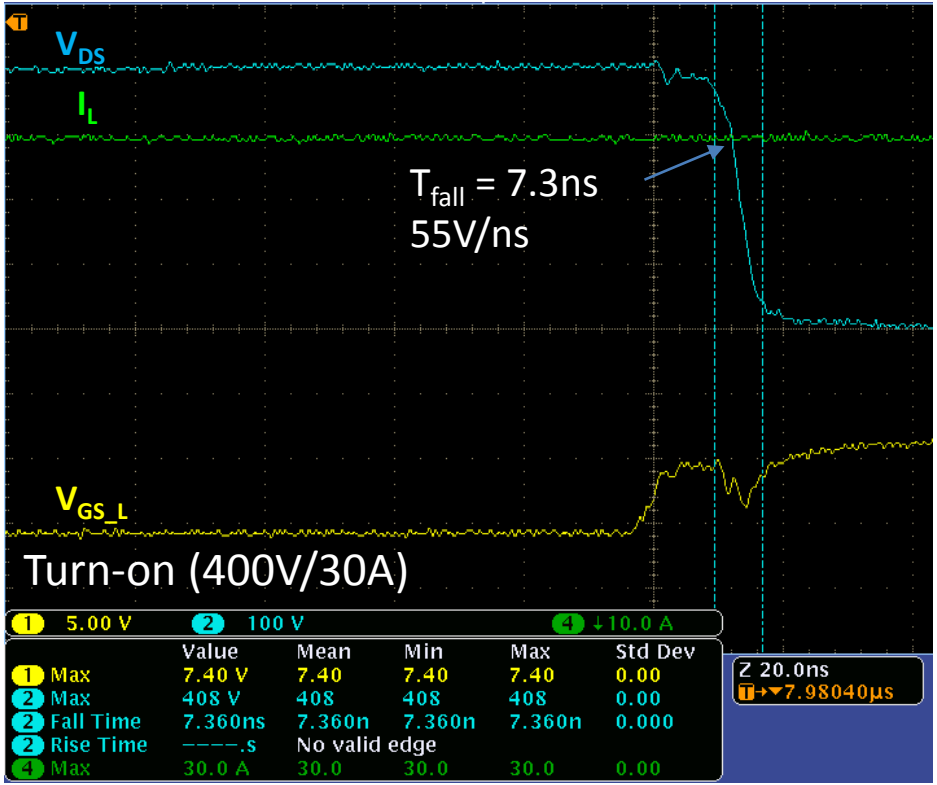
- **Gate Drive design:**
  - GS66508T in half bridge
  - Si8610 plus LM5114
  - Isolated Gate Drive supply
  - R_{ON} = 10Ω / R_{OFF} = 2Ω
- **Tested at 400V, 35A Hard-Switching**

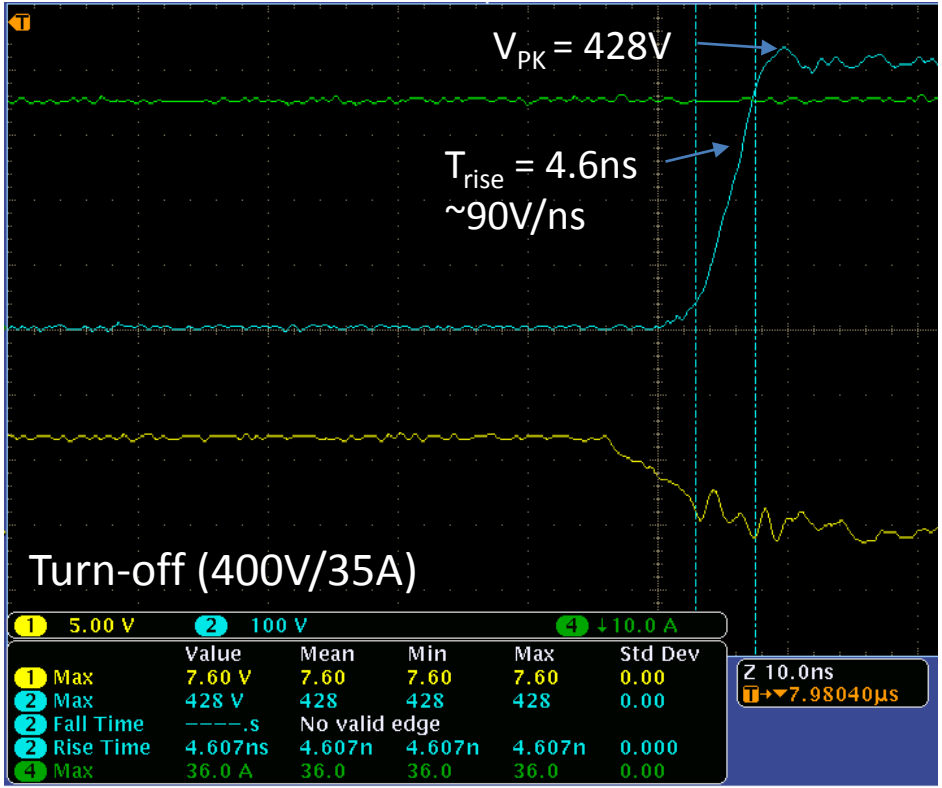




Turn-off and Turn-on waveforms

Low inductance GaNPx T package achieves minimum V_{DS} overshoot and V_{GS} ringing (No kelvin source)

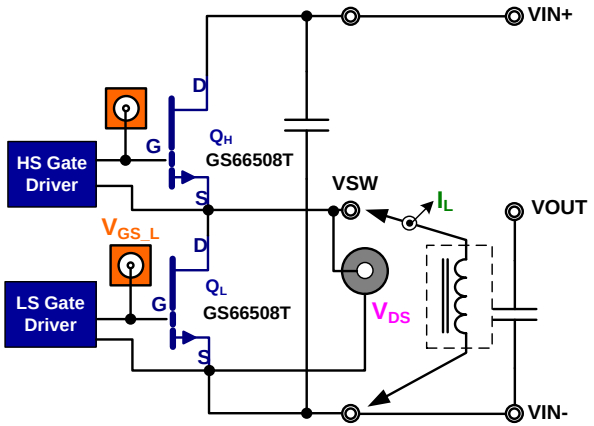


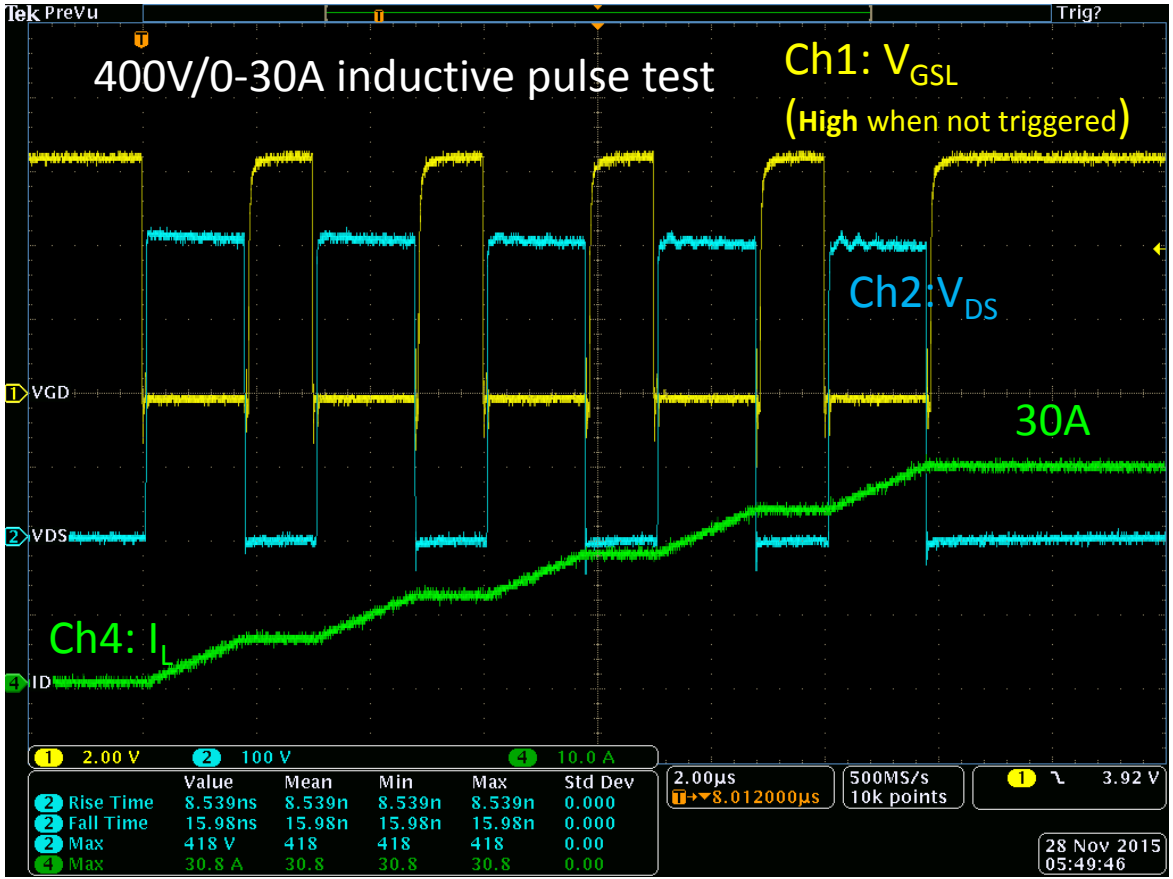


Gate drive waveforms

Gate Drive Switching Waveforms

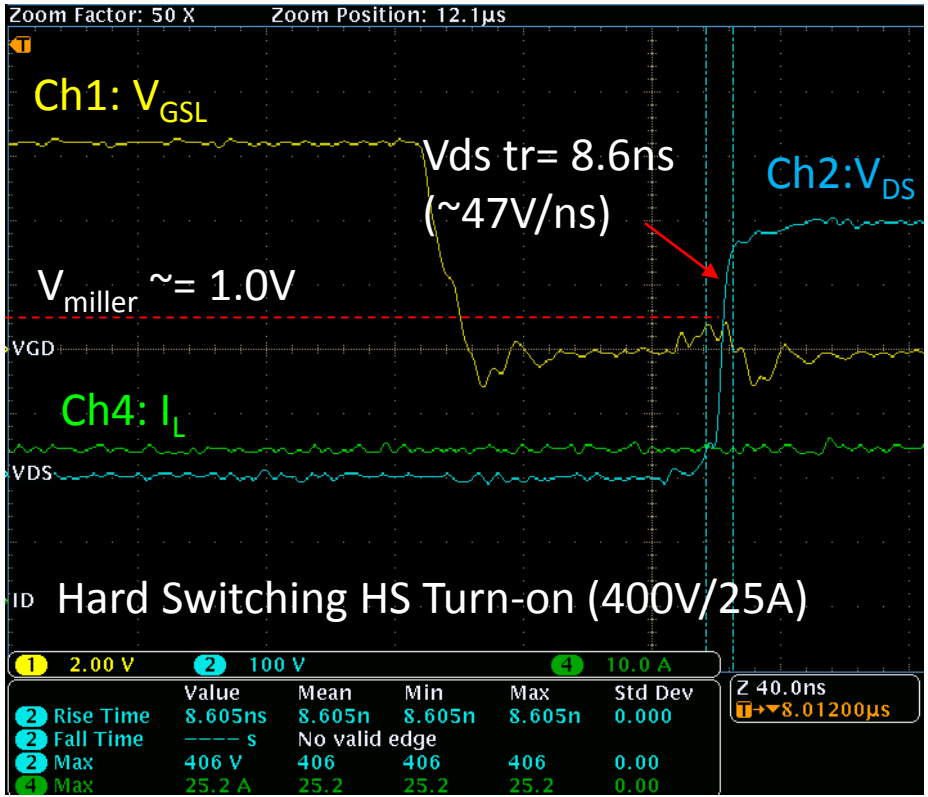
- Inductive load pulse testing to verify gate driver stability over the current range
- Si8261BAC Gate driver (EVAL BOARD)
- R_{ON}=25Ω / R_{OFF}=0Ω
- Use Ferrite bead 15R@100MHz
- No oscillation and minimum drain voltage overshoot

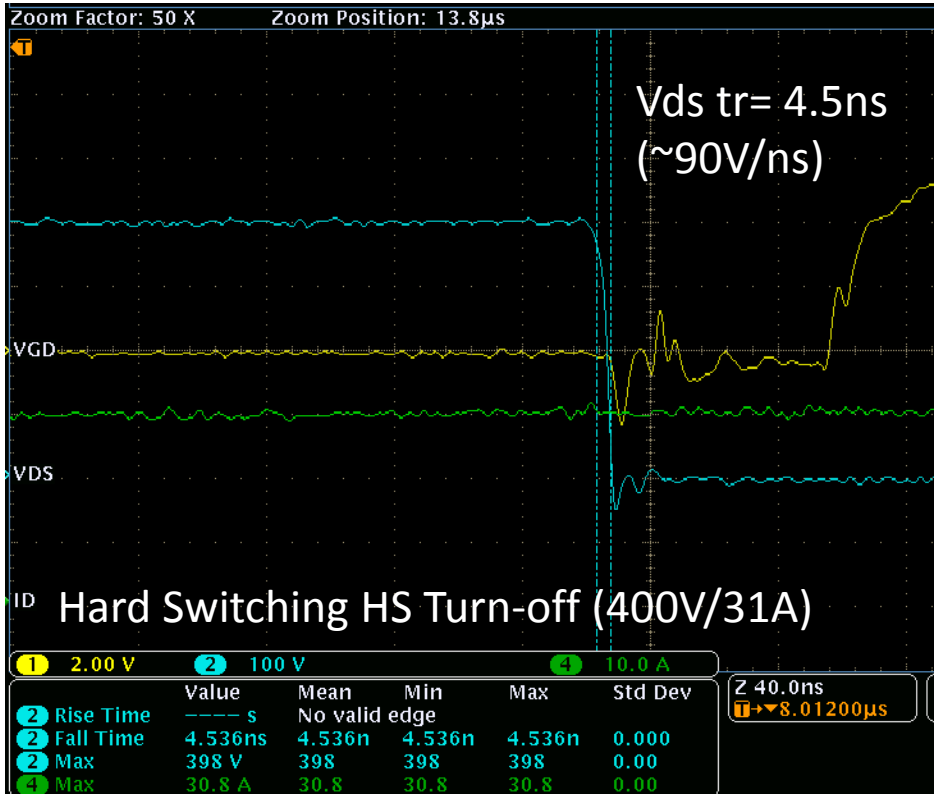




Clean waveforms – controlled Miller voltage

Clean turn-on and off switching waveforms with well controlled gate ringing and miller voltage

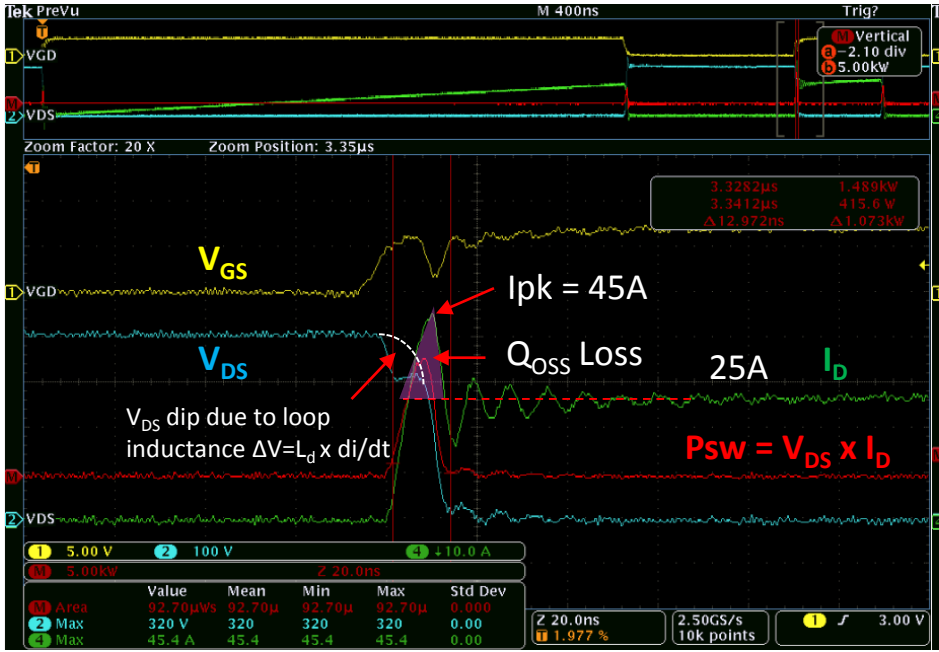


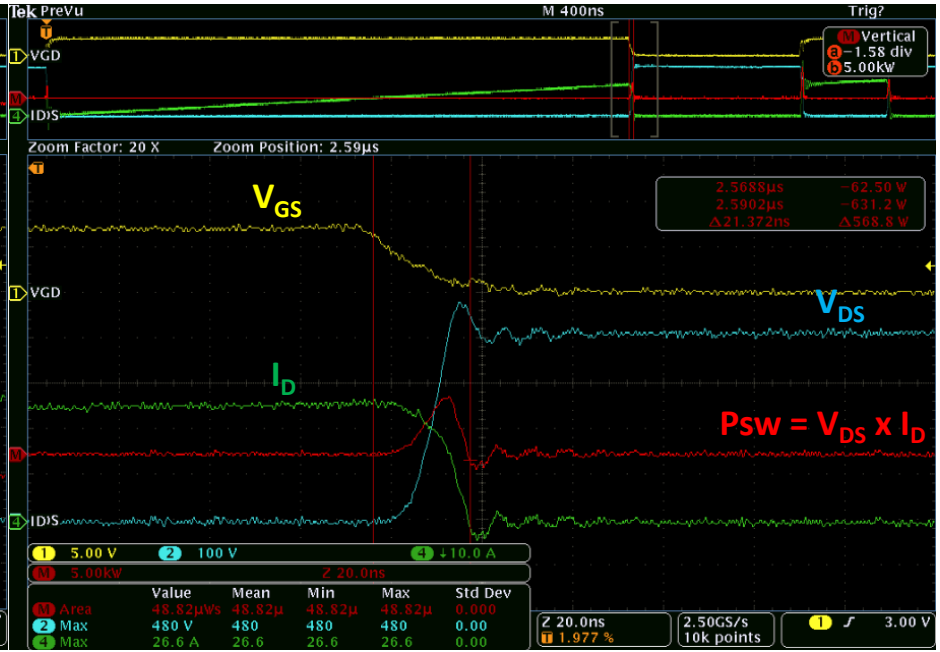


Measuring Eon and Eoff

GS66508P E_{ON}/E_{OFF} measurement waveforms (half bridge)

- Current shunt: T&M research SDN-414-10

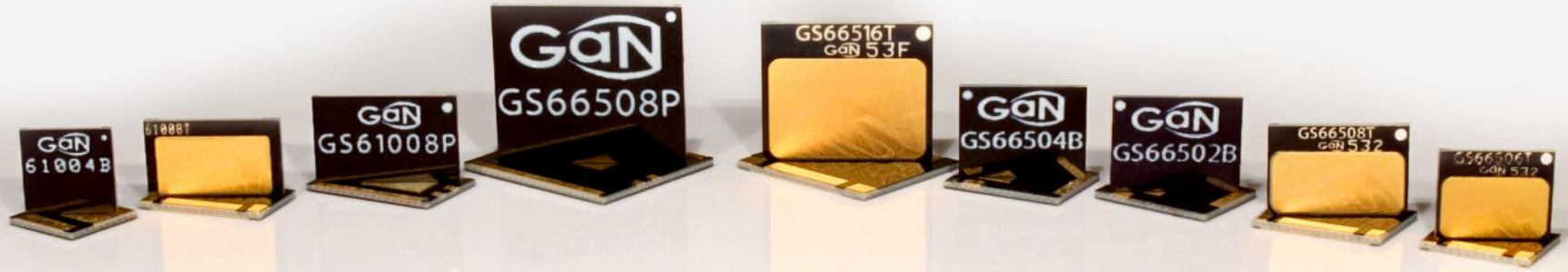




400V/25A Turn-on switching loss energy E_{ON} = **93**uJ
R_{GON}=10Ω

400V/25A Turn-off switching loss energy E_{OFF} = **49**uJ
R_{GOFF}=10Ω

Tomorrow's power today™



GaN Systems

www.gansystems.com • North America • Europe • Asia