WHITE PAPER

Cypress Semiconductor Corp.

F-RAM™ Technology Brief

Abstract

F-RAM (Ferroelectric Random Access Memory) is a nonvolatile memory that uses a ferroelectric capacitor to store data. It offers higher write speeds over flash/EEPROM.

This white paper provides a brief of the F-RAM Technology, its operation, benefits, and typical applications.

Introduction

Established semiconductor memory technologies are divided into two categories:

1. RAMs are random access memories, which have symmetric read and write access time.

2. Nonvolatile memories that have traditionally been ROM (read only memory) until the advent of floating-gate technology. Floating-gate technology produced electrically erasable memories such as flash and EEPROM. These products allow for in-system programming but read and write access times are dissimilar. In fact, the write access times can be several orders of magnitude greater than the read access times.

Ferroelectric random access memory or F-RAM is a true nonvolatile RAM because it combines the advantages of both RAM and nonvolatile memory. The write advantages over flash/EEPROM and nonvolatility make it quite suitable for storing data in the absence of power.

Ferroelectric Property

The ferroelectric property is a phenomena observed in a class of materials such as Lead Zirconate Titanate (PZT). PZT has perovskite crystal structure shown in Figure 1**.** The cation in the center has two equal and stable low-energy states. These states determine the position of the cation. If an electric field is applied in the proper direction, the cation will move in the direction of the field.

Applying an electric field across the crystal causes the low-energy state or position to be aligned in the direction of the field and, conversely, the high-energy state in the opposite position. The applied field will, therefore, cause the cation to move from the high-energy state to the low-energy state. This transition produces energy in the form of a charge generally referred to as switch charge (Qs). Therefore, applying an alternating electric field across the crystal will cause the cation to move from the top of the crystal to the bottom and back again. Each transition will produce a charge, Qs.

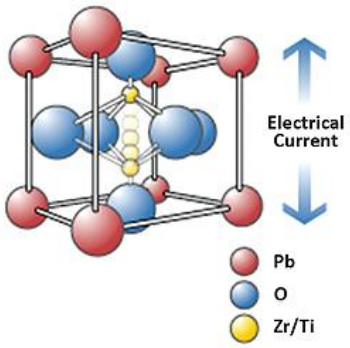

Figure 1. Ferroelectric PZT Perovskite Crystal

A common misconception is that ferroelectric crystals are ferromagnetic or have similar properties. The term “ferroelectric” refers to the similarity of the graph of the charge plotted as a function of the voltage to the hysteresis loop (BH curve) of ferromagnetic materials as shown in Figure 2. Ferroelectric materials switch in an electric field and are not affected by magnetic fields.

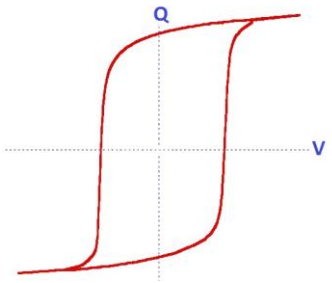

Figure 2. Ferroelectric Hysteresis Loop

The ferroelectric material has two states, the cation at the top, which is referred to as “up polarization”, and the cation at the bottom, which is referred to as “down polarization,” as shown in Figure 3. Therefore, with a viable sensing scheme, a binary memory can be produced.

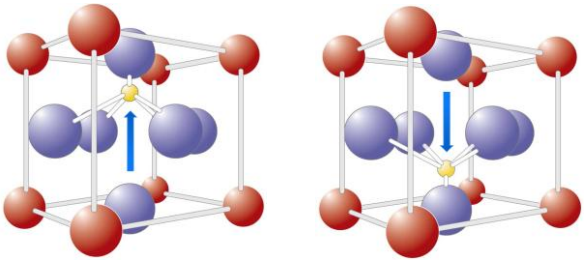

Figure 3. Two Polarization States

F-RAM Operation

The basic storage element is a ferroelectric capacitor. The capacitor can be polarized up or down by applying an electric field as shown in Figure 4.

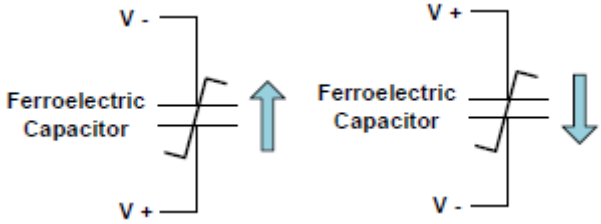

Figure 4. Ferroelectric Capacitor Polarization

The ferroelectric capacitor symbol indicates that the capacitance is variable and is not a traditional linear capacitor. If a ferroelectric capacitor is not switched when an electric field is applied (no change in polarization state), it behaves like a linear capacitor. If it is switched, there is an additional charge induced, therefore, the capacitance must increase. The ferroelectric capacitor is combined with an access transistor, a bit line, and a plate line to form the memory cell as shown in Figure 5.

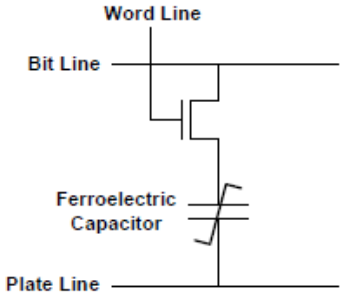

Figure 5. F-RAM Memory Cell

Read Operation

Figure 6.A shows the static state of the cell, which is Bit Line low, Plate Line low, and Word Line low. The access begins by applying a voltage to the Word Line and the Plate Line as given in Figure 6.B. This applies a field across the ferroelectric capacitor resulting in the ferroelectric capacitor switching. This switching is shown in Figure 6.C. The induced charge (Qs) is shared with the parasitic Bit Line capacitance (Cbit) and the switched ferroelectric capacitor (Cs). The voltage on the bit line, therefore, is proportional to the ratio of the capacitances, Cs/Cbit (Cs includes a small contribution from transistor and interconnect parasitics).

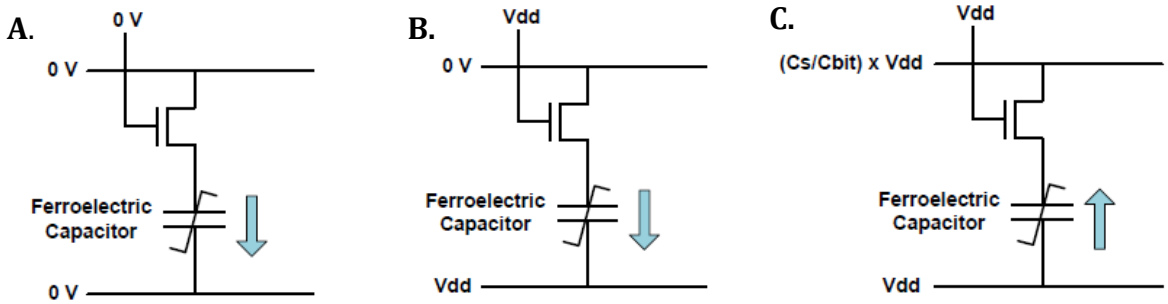

Figure 6. Memory Cell Access Sequence

If the polarization is up in the sequence shown in Figure 6, the capacitor will not switch and there will be no additional charge induced. The charge induced in the switched capacitor is at least two times greater than the charge available in the unswitched capacitor (Qu).

$$Qs \geq 2 \times Qu$$

Therefore, the switched capacitance (Cs) is at least twice the unswitched capacitance (Cu).

$$Cs \geq 2 \times Cu$$

Therefore, it follows that the Bit Line voltage for the switched case is at least twice the Bit Line voltage for the unswitched case.

The sensing scheme is very similar to the techniques used in DRAMs. The Bit Line voltage is compared to a reference voltage, which is above the unswitched value but below the switched value. The sense amp drives the Bit Lines to the rails and the output of the sense amp is either HIGH or LOW (1 or 0). The access is completed in less than 100 ns.

At the end of the access, the Bit Lines are set high for the switched case and set low for the unswitched case. The cycle is completed by bringing the Plate Line low, which restores the state of the switched capacitors and then the Bit Line is precharged to 0 V. The restore/precharge period is also very fast (less than 100 ns). The minimum achievable access/cycle times are primarily driven by

the capacitance of the memory cell. The time it takes to switch the ferroelectric capacitor is nearly instantaneous and, therefore, switching mechanism does not contribute to the overall cycle time.

A comparison of DRAM and F-RAM shows that the sensing scheme is similar because both sense the charge. The charge in a DRAM is stored in a linear capacitor that leaks and requires refresh. The charge in an F-RAM is stored as state in the crystal and is, therefore, nonvolatile and requires no refresh. Like DRAMs, F-RAMs have a cycle time, so the minimum time between back-to-back random addresses is equal to the cycle time, not the access time. Today, typical cycle times for F-RAM are between 90 ns and 140 ns.

Write Operation

A write operation is very similar to a read operation. The circuit applies an electric field in the desired direction across the ferroelectric capacitor.

F-RAM Benefits

Traditional writable nonvolatile memories derived from the floating gate technology use charge pumps to develop high voltages on-chip (10 V or more) to force carriers through the gate oxide. Therefore, there are long write delays, high write power, and the write operation is actually destructive to the memory cell. Floating gate devices are incapable of supporting writes that exceed 10^6 accesses. To put this in perspective, a data recorder using EEPROM to record data at 1 sample/s would wear out in less than 12 days. In comparison, the 3-V F-RAM products offer virtually unlimited endurance (10^{14} accesses).

The F-RAM is far superior to floating-gate devices in both write speed and power. For a typical serial EEPROM with a clock rate of 20 MHz, it would take 5 ms to write 256 bits (32-byte page buffer) and 1283.6 ms to write to the entire 64 Kb. For an equivalent F-RAM, it takes only 14 µs for 256 bits and just 3.25 ms to write to the entire 64 Kb. In addition, it requires 3900 µJ to write 64 Kb for the EEPROM, compared with 17 µJ to write 64 Kb to an F-RAM—a difference of more than 229 times.

In summary:

- Read Access Time = Write Access Time < 100 ns
- Read Energy = Write Energy
- High Write Endurance 10^{14}

Applications

1. **Automotive:** The need for F-RAM technology in the automotive market is growing. As electronic content mushrooms with the widespread use of microcontrollers and sensors, the need for data storage is growing in automotive subsystems. High-content features like Smart Airbags or sophisticated Seat Memory Systems are being introduced in high-end automobiles and are migrating into mass-market models over time. F-RAM is now established in high-end models across several applications. The key application areas where F-RAMs find use are Smart Airbags, Automatic Driver Assistance Systems (ADAS), Navigation and Infotainment Systems, Engine Control Units (ECU), Event Data Recorders (EDR), Powertrain Systems, and Battery Management Systems (BMS). Cypress offers high-quality automotive grade, AEC-Q100 qualified F-RAMs for this market in a wide variety of density options.

2. **Metering:** F-RAMs are the dominant memory type used in the market in power metering systems. High endurance, fast writes, and low energy consumption features contribute to the rapid adoption of F-RAMs in this space. The need for storing more data as devices get sophisticated is driving F-RAM adoption in the market. Common metering systems where F-RAMs play are smart electricity meters, water meters, and gas meters.

3. **Printers:** An F-RAM fits into the Business Printer market as the ideal fast, energy efficient, and high-endurance memory. The need for frequent data logging (page counts, settings) has made F-RAMs the default choice over EEPROMs or flash in this market.

4. **Industrial:** Industrial applications require long-term support with some applications needing 20-year support cycles. Cypress specializes in providing long-term support to customers in the Industrial space with Form-Fit-Function-compatible products with long lifecycles. The robustness of F-RAM makes it an ideal memory for battery-backed SRAM replacement (pin-for-pin compatible parallel interface options) and EEPROM replacements (pin-form-pin compatible serial interface 8-pin options).

5. **Wearable Electronics and Other Energy-Efficient Applications:** A major consideration for electronic wearable designs is reducing the total energy consumption while increasing the reliability. Designers must add functionalities while simultaneously reducing the system's power budget for a longer battery life. At the same time, embedded software is becoming larger and more complex, requiring more memory, thus further stressing the power budget. There are two principal advantages of Serial F-RAMs over EEPROMs and flash-based memories. Energy to write into F-RAMs is multiple orders of magnitude better than other nonvolatile memories. A second advantage can be obtained on the endurance front with near-infinite write cycles. F-RAMs are available in pin-for-pin compatible packages to EEPROMs and flash.

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