

# 54ACT16623, 74ACT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS152A – JANUARY 1991 – REVISED APRIL 1996

- **Members of the Texas Instruments Widebus™ Family**
- **Inputs are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

## description

The 'ACT16623 are 16-bit transceivers designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

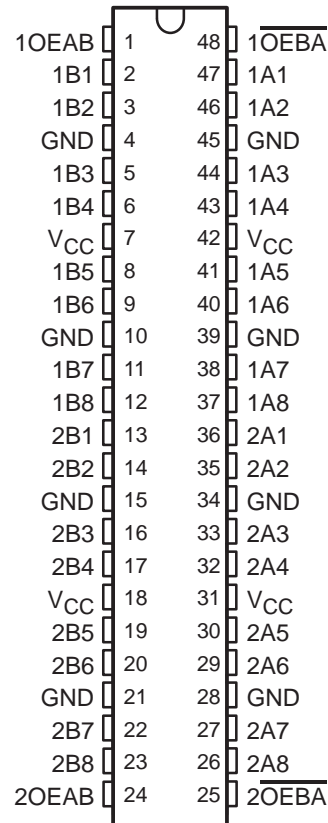
These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable (OEBA and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneously enabling OEBA and OEAB. Each output reinforces its input in this transceiver configuration. When both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74ACT16623 is packaged in TI's shrink small-outline package, which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16623 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16623 is characterized for operation from –40°C to 85°C.

54ACT16623 . . . WD PACKAGE  
75ACT16623 . . . DL PACKAGE  
(TOP VIEW)



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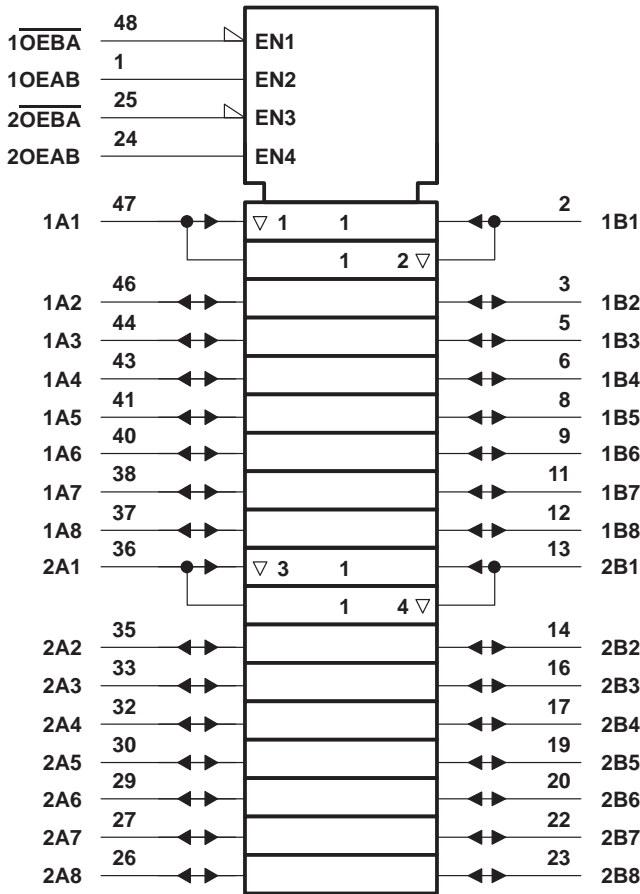
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FUNCTION TABLE

(each 8-bit section)

INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

logic symbol†

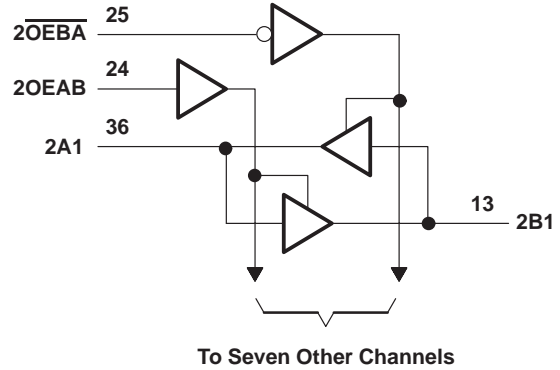
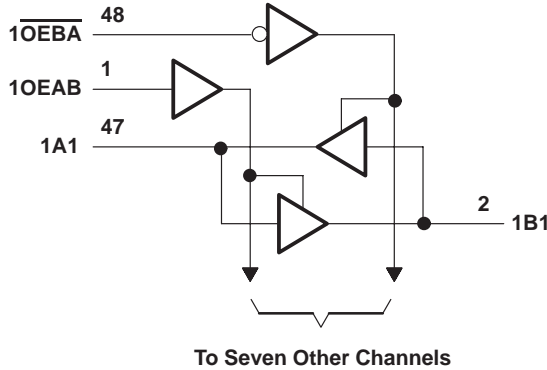


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±400 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

		54ACT16623			74ACT16623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage (see Note 4)	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$	High-level output current			–24			–24	mA
$I_{OL}$	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$	Operating free-air temperature	–55		125	–40		85	°C

- NOTES: 3. Unused inputs should be connected to  $V_{CC}$  through a pullup resistor of approximately 5 k $\Omega$  or greater.  
4. All  $V_{CC}$  and GND pins must be connected to the proper power supply.

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# 54ACT16623, 74ACT16623

## 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT16623		74ACT16623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = -50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I <sub>OH</sub> = -75 mA†	5.5 V				3.85		3.85		
V <sub>OL</sub>		I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I <sub>OL</sub> = 75 mA†	5.5 V					1.65		1.65	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	µA
I <sub>OZ</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5		±5	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80		80	µA
ΔI <sub>CC</sub> ‡		One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			0.9		1		1	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5						pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54ACT16623		74ACT16623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	4.2	7.3	9.5	4.2	10.4	4.2	10.4	ns
t <sub>PHL</sub>			3.1	7.3	9.5	3.1	10.3	3.1	10.3	
t <sub>PZH</sub>	$\overline{\text{OEBA}}$	A	2.7	6.8	8.8	2.7	9.5	2.7	9.5	ns
t <sub>PZL</sub>			3.5	8.2	10.2	3.5	11.1	3.5	11.1	
t <sub>PHZ</sub>	$\overline{\text{OEBA}}$	A	6	9.6	11.3	6	12	6	12	ns
t <sub>PLZ</sub>			5.3	8.6	10.3	5.3	10.7	5.3	10.7	
t <sub>PZH</sub>	OEAB	B	4.1	6.9	8.7	4.1	9.3	4.1	9.3	ns
t <sub>PZL</sub>			5.1	7.9	9.7	5.1	10.6	5.1	10.6	
t <sub>PHZ</sub>	OEAB	B	5.1	8.2	10.2	5.1	10.4	5.1	10.4	ns
t <sub>PLZ</sub>			4.4	7.4	9.3	4.4	9.5	4.4	9.5	

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

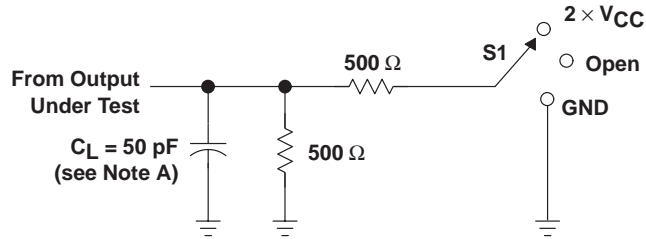
PARAMETER			TEST CONDITIONS		TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	C <sub>L</sub> = 50 pF, f = 1 MHz		56	pF
		Outputs disabled			11	

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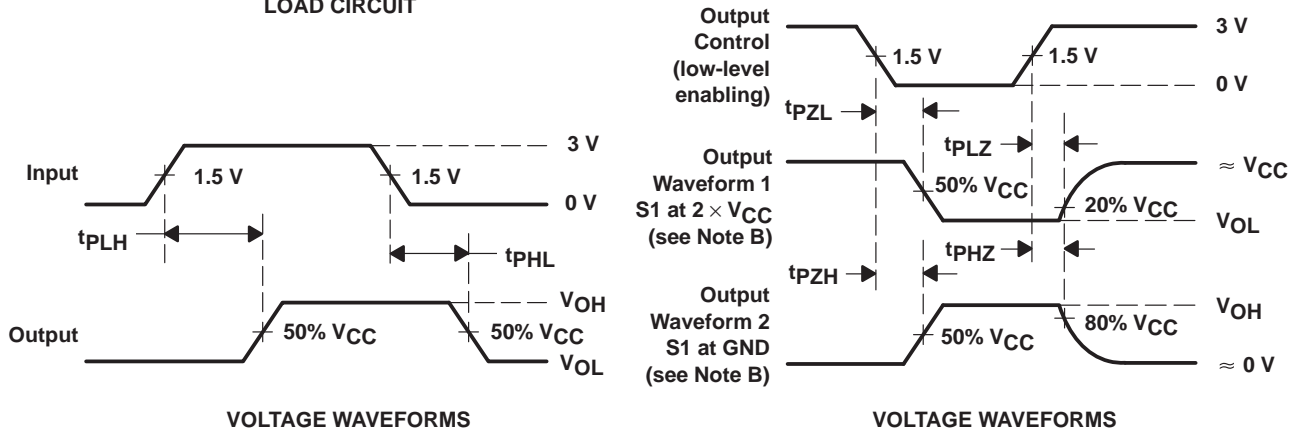
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## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT16623DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16623DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16623DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16623DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16623DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16623DLR	SSOP	DL	48	1000	346.0	346.0	49.0



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