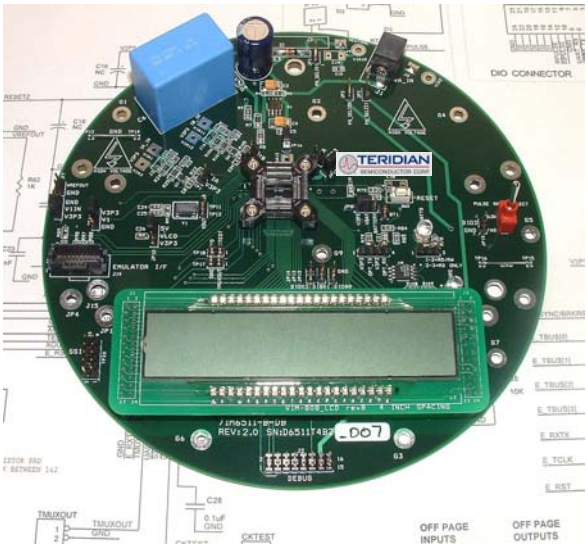
71M6511/71M6511H Demo Board

USER'S MANUAL



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Revision 5.4

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71M6511

Single-Phase Energy Meter IC

DEMO BOARD

USER'S MANUAL

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1 GETTING STARTED

1.1 GENERAL

The TERIDIAN Semiconductor Corporation (TSC) 71M6511 Demo Board is an energy meter IC demonstration board for evaluating the 71M6511/6511H device for single-phase electronic energy metering applications. It incorporates a 71M6511 or 71M6511H integrated circuit, peripheral circuitry such as a serial EEPROM, emulator port, and on board power supply as well as a companion Debug Board that allows a connection to a PC through a RS232 port. The Demo Board allows the evaluation of the 71M6511 energy meter chip for measurement accuracy and overall system use.

The board is pre-programmed with a Demo Program (file name 6511_demo.hex) in the FLASH memory of the 71M6511/6511H IC. This embedded application was developed to exercise all low-level functions to directly manage the peripherals, flash programming, and CPU (clock, timing, power savings, etc.).

The 71M6511/6511H IC on the Demo Board is pre-programmed with default calibration factors.

1.2 SAFETY AND ESD NOTES

Connecting live voltages to the Demo Board system will result in potentially hazardous voltages on the Demo Board.

BEFORE OPERATING THE DEMO BOARD, THE JUMPERS ON JP2 AND JP3 (IF INSTALLED) SHOULD BE REMOVED! IT IS RECOMMENDED TO OPERATE THE DEBUG BOARD WITH ITS OWN POWER SUPPLY.

THE DEMO SYSTEM IS ESD SENSITIVE! ESD PRECAUTIONS SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD!

EXTREME CAUTION SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD ONCE IT IS CONNECTED TO LIVE VOLTAGES!

1.3 DEMO KIT CONTENTS

- 71M6511 Demo board containing 71M6511 or 71M6511H IC with preloaded Demo Program (4-layer, round, Demo Board or 2-layer, rectangular Demo Board with capacitive or transformer power supply)
- Debug Board
- Two 5VDC/1,000mA universal wall transformers w/ 2.5mm plug (Switchcraft 712A)
- Serial cable, DB9, Male/Female, 2m length (Digi-Key AE1020-ND)
- CD-ROM containing documentation (data sheet, board schematics, BOM, layout), Demo Code, and utilities

1.4 DEMO BOARD VERSIONS

Three versions of the Demo Board are available, as shown in Figure 1-1:

- 4-layer Demo Board with round PCB, for demonstration of 4-layer designs (identification number D6511T4B2).
- 2-layer Demo Board with rectangular PCB, with capacitive power supply, for demonstration of economical 2-layer designs (identification number D6511T4A7).
- 2-layer Demo Board with rectangular PCB, with transformer power supply, for demonstration of economical 2-layer designs (identification number D6511BT4A4).

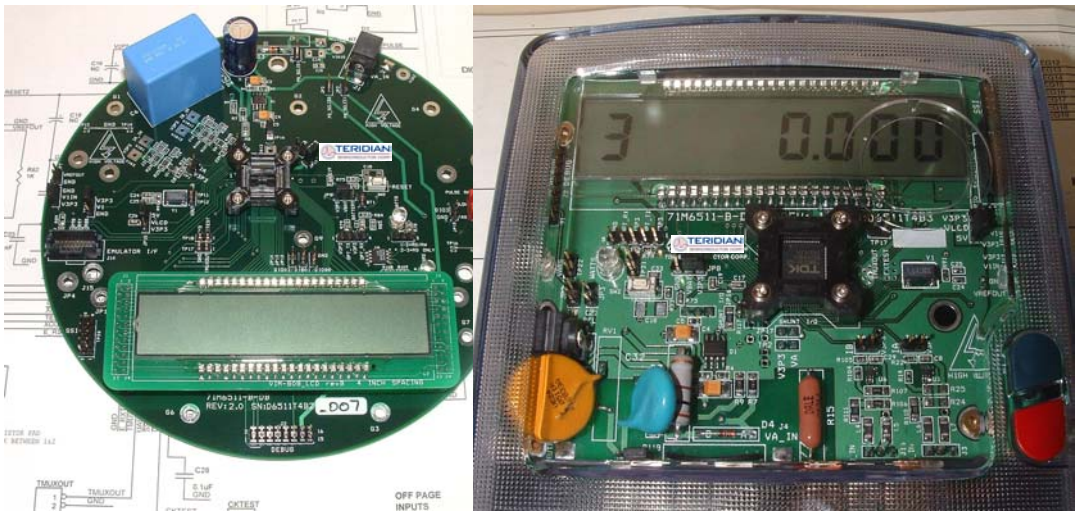


Figure 1-1: Demo Board Versions. 4-layer (left), 2-layer (right)

1.5 COMPATIBILITY

This manual applies to the following hardware and software revisions:

- 71M6511 or 71M6511H chip revision B03
- Demo Kit firmware revision 3.04 and 3.05, or later
- 4-layer Demo Board revision D6511T4B
- 2-layer Demo Board D6511BT4A4 or D6511T4A7

1.6 SUGGESTED EQUIPMENT AND TEST TOOLS NOT INCLUDED

For functional demonstration:

- PC w/ MS-Windows® versions XP or 2000, equipped with RS232 port (COM port) via DB9 connector

For software development (MPU code):

- Signum ICE (In Circuit Emulator): ADM-51

  http://signum.temp.veriohosting.com/Signum.htm

- Keil 8051 "C" Compiler kit: CA51

  http://www.keil.com/c51/ca51kit.htm, http://www.keil.com/product/sales.htm

For calibration and accuracy tests:

- Calibration system (see section 2.2 for details)

1.7 DEMO BOARD TEST SETUP

Figure 1-2 and Figure 1-3 show the basic connections of the Demo Boards plus Debug Boards with the external equipment for desktop testing, i.e. without live power applied. For desktop testing, both the Demo and Debug board may be powered with just the 5VDC power supplies.

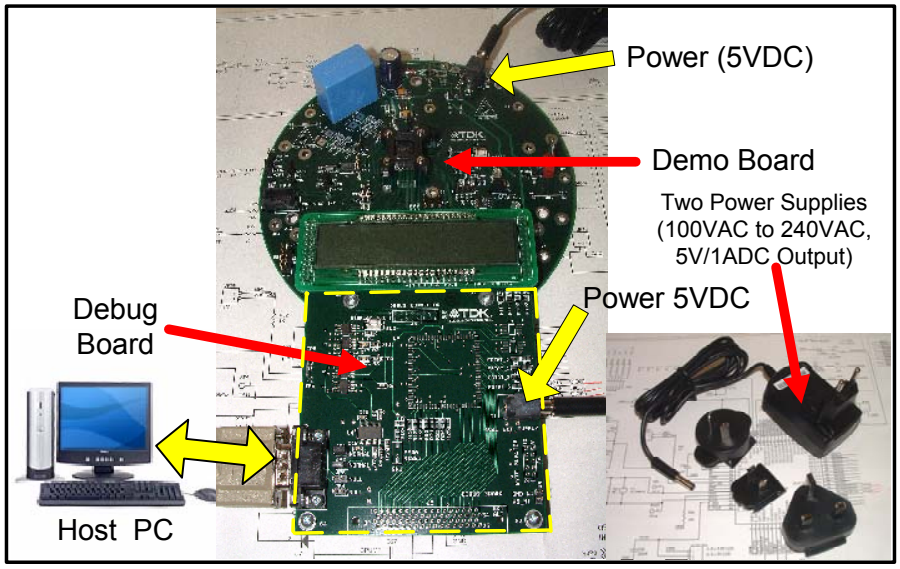


Figure 1-2: 4-Layer Demo Board: Basic Connections

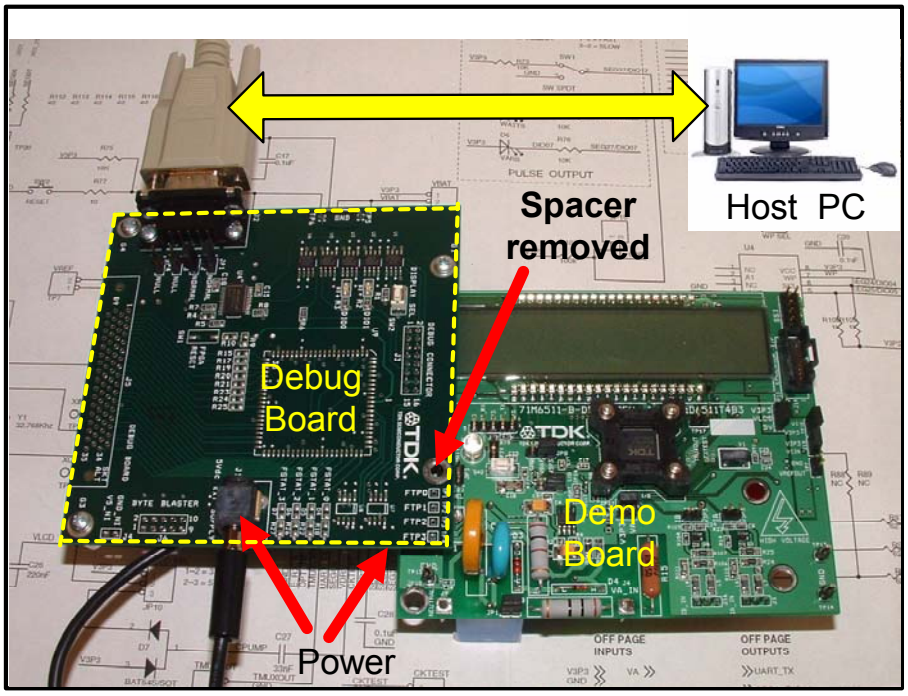


Figure 1-3: 2-Layer Demo Board: Basic Connections

The Debug Board can be plugged into J2 of the Demo Board. For the 2-Layer Demo Board, one spacer of the Debug Board should be removed, as shown in Figure 1-3. Alternatively, both boards can be connected using a flat ribbon cable, as shown in Figure 1-4. The male-to-female flat ribbon cable is not supplied with the Demo Kit (use Digi-Key P/N A3AKA-1606M-ND or similar).

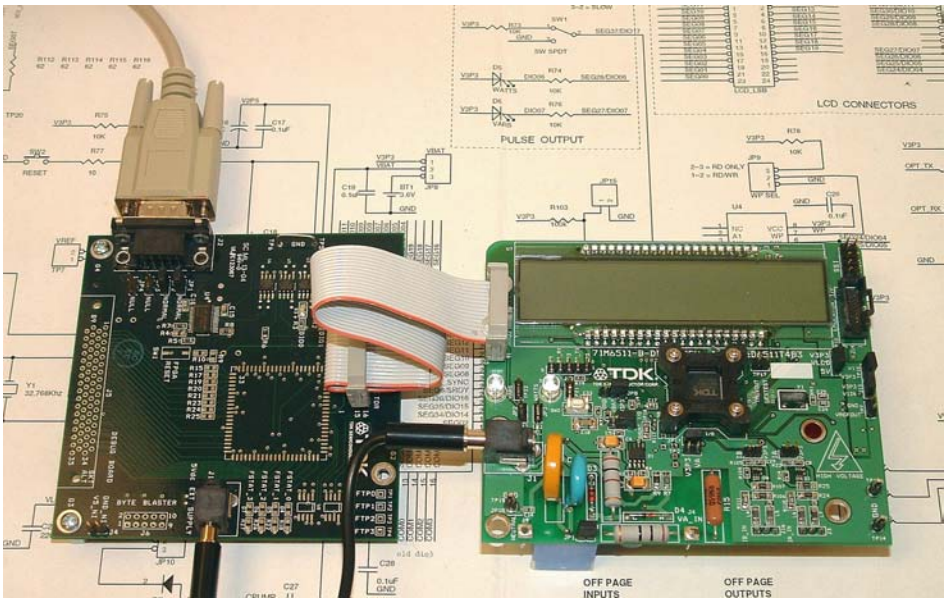


Figure 1-4: 2-Layer Demo Board: Ribbon Cable Connections

The 71M6511 Demo Board block diagram is shown in Figure 1-5. The demo setup consists of a stand-alone meter Demo Board and an optional Debug Board. The Demo Board contains all circuits necessary for operation as a meter, including display, calibration LED, and internal power supply. The Debug Board, when using a separate power supply, is optically isolated from the meter and interfaces to a PC through a 9-pin serial port.

Connections to the external signals to be measured, i.e. scaled AC voltages and current signals derived from shunt resistors or current transformers, are provided on the rear side of the Demo Board.

It is recommended to set up the Demo Board with no live AC voltage connected, and to connect live AC voltages only after the user is familiar with the demo system.

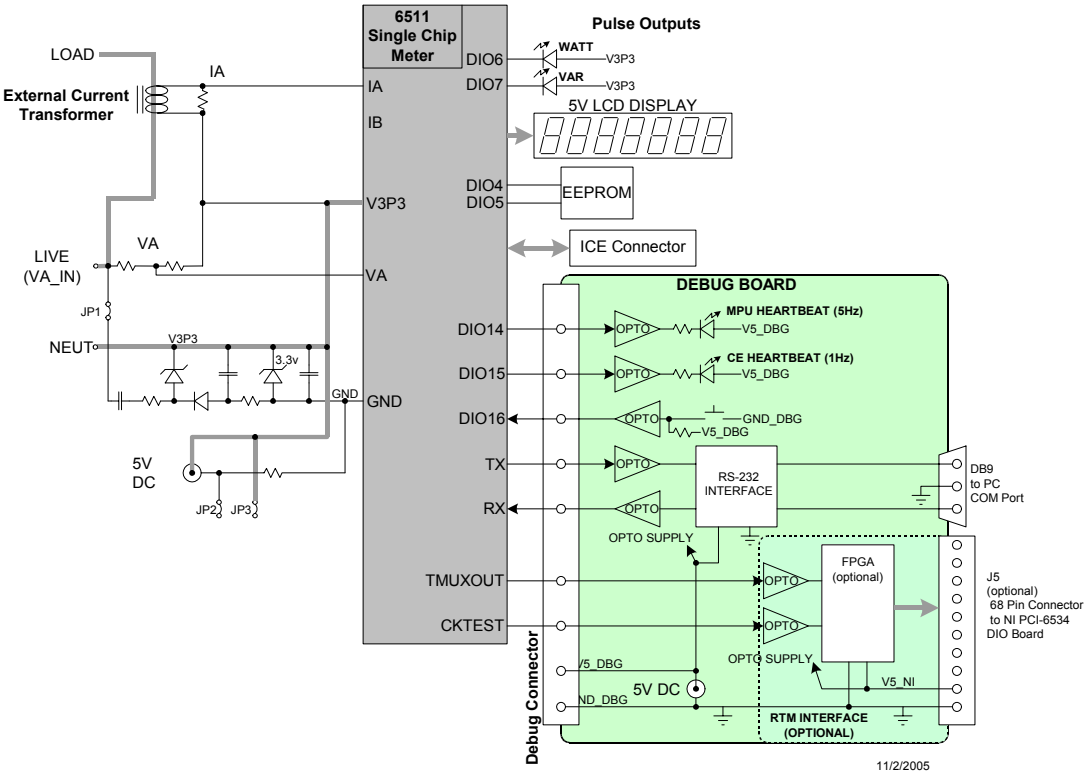


Figure 1-5: The TERIDIAN 6511 Demo Board with Debug Board Block Diagram (CT Configuration)

All input signals are referenced to the V3P3 (3.3V power supply to the chip).

1.7.1 POWER SUPPLY SETUP

There are several choices for meter power supply:

- Internal (using the AC line voltage). The internal power supply is only suitable when the line voltage exceeds 220V RMS.
- External 5VDC connector (J1) on the Demo Board
- External 5VDC connector (J1) on the Debug Board.

The three power supply jumpers, JP1, JP2, and JP3 (JP2/JP3 is only provided on the D6511T4B2 Demo Board), must be consistent with the power supply choice. JP1 connects the AC line voltage to the internal power supply. This jumper should usually be left in place. **JP2 and JP3 should be left open (unconnected).**

1.7.2 CABLE FOR SERIAL CONNECTION (DEBUG BOARD)

For connection of the DB9 serial port to a PC, either a straight or a so-called "null-modem" cable may be used. JP1 and JP2 on the Debug Board are plugged in for the straight cable, and JP3/JP4 are empty. The jumper configuration is reversed for the null-modem cable, as shown in Table 1-1.

Cable Configuration	Mode	Jumpers on Debug Board			
		JP1	JP2	JP3	JP4
Straight Cable	**Default**	Installed	Installed	--	--
Null-Modem Cable	Alternative	--	--	Installed	Installed

Table 1-1: Jumper settings on the Debug Board

JP1 through JP4 can also be used to alter the connection when the PC is not configured as a DCE device. Table 1-2 shows the connections necessary for the straight DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	2
3	RX	3
5	Signal Ground	5

Table 1-2: Straight Cable Connections

Table 1-3 shows the connections necessary for the null-modem DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	3
3	RX	2
5	Signal Ground	5

Table 1-3: Null-Modem Cable Connections

1.7.3 CHECKING OPERATION

A few seconds after power up, the LCD display on the Demo Board should briefly display the following welcome text:

		H	E	L	L	0	

After the welcome text, the Demo Board should display the following information:

3.				0.	0	0	1

The decimal dot in the leftmost segment will be blinking, indicating activity of the MPU inside the 71M6511.

1.7.4 SERIAL CONNECTION SETUP

After connecting the DB9 serial port to a PC, start the HyperTerminal application and create a session using the following parameters:

Port Speed: 9600 baud

Data Bits: 8

Parity: None

Stop Bits: 1

Flow Control: XON/XOFF

HyperTerminal can be found by selecting Programs →Accessories → Communications from the Windows© start menu.

The connection parameters are configured by selecting File → Properties and then by pressing the Configure button. Port speed and flow control are configured under the General tab (Figure 1-7, left), bit settings are configured by pressing the Configure button (Figure 1-7, right), as shown below. A setup file (file name "Demo Board Connection.ht") for HyperTerminal that can be loaded with File → Open is also provided with the tools and utilities on the supplied CD-ROM.

Port parameters can only be adjusted when the connection is not active. The disconnect button, as shown in Figure 1-6 must be clicked in order to disconnect the port.

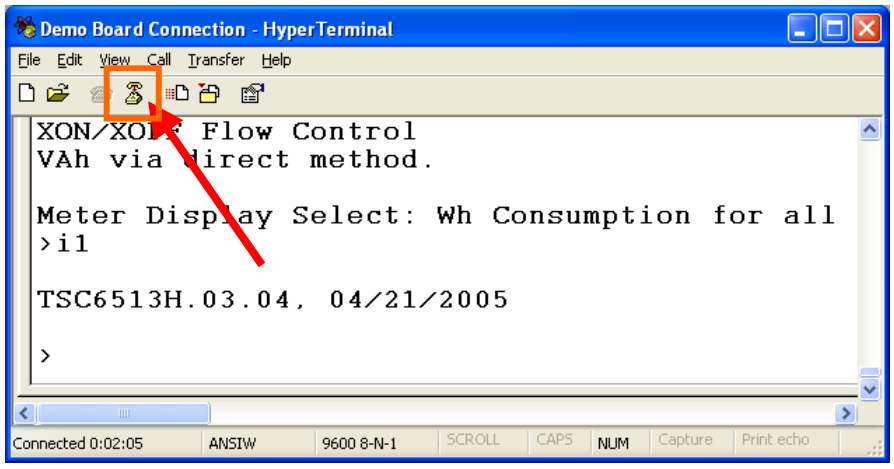


Figure 1-6: Hyperterminal Sample Window with Disconnect Button

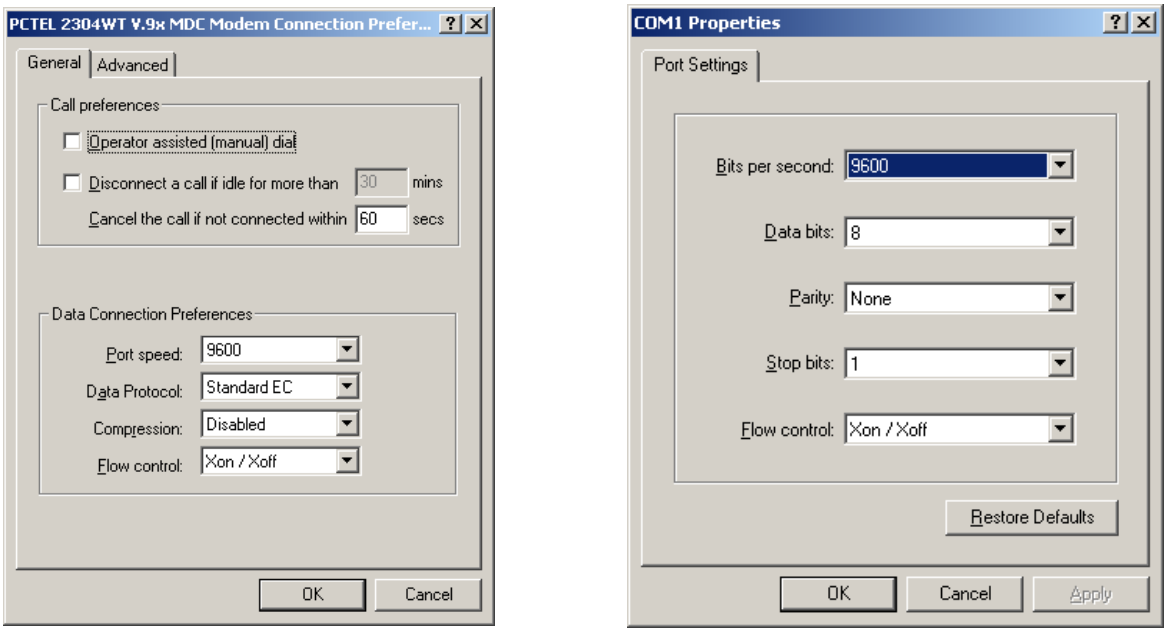


Figure 1-7: Port Speed/Handshake Setup (left) and Port Bit Setup (right)

Once, communication to the Demo Board is established, press <CR> and the Demo Program prompt, >, should appear. Type **>?** to see the Demo Program help menu. Type **>i1** to verify that the Demo Program version is revision 3.04 or later.

1.8 USING THE DEMO BOARD

The 71M6511/6511H Demo Board is a ready-to-use meter prepared for use with an external current transformer.

Using the Demo Board involves communicating with the Demo Code via the command line interface (CLI). The CLI allows all sorts of manipulations to the metering parameters, access to the EEPROM, initiation of auto-cal sequences, selection of the displayed parameters, changing calibration factors and many more operations.

Before evaluating the 71M6511/6511H on the Demo Board, users should get familiar with the commands and responses of the CLI. A complete description of the CLI is provided in section 1.8.1.

1.8.1 SERIAL COMMAND LANGUAGE

The Demo Code residing in the flash memory of the 71M6511/6511H provides a convenient way of examining and modifying key meter parameters. Once the Demo Board is connected to a PC or terminal per the instructions given in Section 1.7.2 and 1.7.4, typing '?' will bring up the list of commands shown in Figure 1-8.

```
>?

??       : Command Line Interpreter On-line help
Usage: ?<char> or ?? to get this help page
Where <char> is an uppercase letter of the command.
The following commands/<char> are available:
  ,  - Repeat last command    : /  - Ignore rest of line
  C  - Compute Engine Control : EE - EEprom Control
  I  - Information message    : M  - Meter Display Control
  P  - Profile of Meter
  R  - SFR Control            : RT - RTC Control
  T  - Trim Controls          : Z  - Reset
  ]  - Access CE Data RAM     : )  - Access MPU Data RAM

For Example: ?C to get help on Compute Engine Control.
>
```

Figure 1-8: Command Line Interface Help Display

The tables below describe the commands in detail.

Demo Code revision 3.05 offers more commands than revision 3.04. Commands only available on 3.05 are marked in the tables presented in this chapter.

Commands to Display Help on the CLI Commands:

?	**HELP**	
Description:	Command help available for each of the options below.	
Command combinations:	?	Command line interpreter help menu.
	?]	Display help on access CE data RAM
	?)	Display help on access MPU RAM
	?,	Display help on repeat last command
	?/	Display help on ignore rest of line
	?C	Display help on compute engine control and calibration. **In 3.05, pulse counter functions are offered.**
	?EE	Display help on EEPROM control
	?I	Display help on information message
	?M	Display help on meter display control
	?P	Display help on profile of meter
	?R	Display help on SFR control
	?RT	Display help on RTC control
	?T	Display help on trim control
	?W	**Display help on the wait/reset command – 3.05 only**
	?Z	Display help on reset
Examples:	??	Display the command line interpreter help menu.
	?C	Displays compute engine control help.

Commands for CE Data Access:

]	CE DATA ACCESS	
Description:	Allows user to read from and write to CE data space.	
Usage:	] [Starting CE Data Address] [option]…[option]	
Command combinations:	]???	Read consecutive 16-bit words in Decimal
	]$$$	Read consecutive 16-bit words in Hex
	]=n=n	Write consecutive memory values
	]U	Update default version of CE Data in flash memory
Example:	]40$$$	Reads CE data words 0x40, 0x41 and 0x42.
	]7E=12345678=9876ABCD	Writes two words starting @ 0x7E

CE data space is the address range for the CE DRAM (0x1000 to 0x13FF). All CE data words are in 4-byte (32-bit) format. The offset of 0x1000 does not have to be entered when using the] command, thus typing]A? will access the 32-bit word located at the byte address 0x1000 + 4 * A = 0x1028.

Commands for MPU/XDATA Access:

)	MPU DATA ACCESS	
Description:	Allows user to read from and write to MPU data space.	
Usage:	) [Starting MPU Data Address] [option]…[option]	
Command combinations:	)???	Read three consecutive 32-bit words in Decimal
	)$$$	Read three consecutive 32-bit words in Hex
	)a=n=m	Write the values n and m to two consecutive addresses starting at a
Example:	)08$$$$	Reads data words 0x08, 0x0C, 0x10, 0x14
	)04=12345678=9876ABCD	Writes two words starting @ 0x04

MPU or XDATA space is the address range for the MPU XRAM (0x0000 to 0x7FFF). All MPU data words are in 4-byte (32-bit) format. Typing]A? will access the 32-bit word located at the byte address 4 * A = 0x28. The energy accumulation registers of the Demo Code can be accessed by typing two Dollar signs ("$$"), typing question marks will display negative decimal values if the most significant bit is set.

RAM access is limited to the lower 1KB address range. Read and write operations will "wrap around" at higher addresses, i.e.)200? will yield the same result as)0?

Commands for DIO RAM (Configuration RAM) and SFR Control:

R	DIO AND SFR CONTROL	
Description:	Allows the user to read from and write to DIO RAM and special function registers (SFRs).	
Usage:	R [option] [register] … [option]	
Command combinations:	RIx…	Select I/O RAM location x (0x2000 offset is automatically added)
	Rx…	Select internal SFR at address x
	R???...	Read consecutive registers in Decimal
	R$$$...	Read consecutive registers in Hex
	Ra=n=m…	Set values of consecutive registers to n and m starting at address a
Example:	RI0$$$	Read CE0, CE1 and CE2 registers

DIO or Configuration RAM space is the address range 0x2000 to 0x20FF. This RAM contains registers used for configuring basic hardware and functional properties of the 71M6511/6511H and is organized in bytes (8 bits). The 0x2000 offset is automatically added when the command RI is typed.

The SFRs (special function registers) are located in internal RAM of the 80515 core, starting at address 0x80.

Commands for EEPROM Control:

EE	EEPROM CONTROL	
Description:	Allows user to enable read and write to EEPROM.	
Usage:	EE [option] [arguments]	
Command combinations:	EECn	EEPROM Access (1 → Enable, 0 → Disable)
	EERa.b	Read EEPROM at address 'a' for 'b' bytes.
	EESabc..xyz	Write characters to buffer (sets Write length)
	EETa	Transmit buffer to EEPROM at address 'a'.
	EEWa.b...z	Write values to buffer
Example:	EEShello; EET$0210	Writes 'hello' starting at EEPROM address 0x210.

Due to buffer size restrictions, the maximum number of bytes handled by the EEPROM command is 0x40.

Auxiliary Commands:

Typing a comma (",") repeats the command issued from the previous command line. This is very helpful when examining the value at a certain address over time, such as the CE DRAM address for the temperature (0x40).

The slash ("/") is useful to separate comments from commands when sending macro text files via the serial interface. All characters in a line after the slash are ignored.

Commands controlling the CE, TMUX and the RTM:

C	**COMPUTE ENGINE CONTROL**	
Description:	Allows the user to enable and configure the compute engine.	
Usage:	C [option] [argument]	
Command combinations:	CEn	Compute Engine Enable (1 → Enable, 0 → Disable)
	CTn	Select input n for TMUX output pin
	CREn	RTM output control (1 → Enable, 0 → Disable)
	CRSa.b.c.d	Selects CE addresses for RTM output
Example:	CE0	Disables CE, followed by "CE OFF" display on LCD. The Demo Code will reset if the WD timer is enabled.
	CT3	Selects the VBIAS signal for the TMUX output pin

Commands controlling the Auto-Calibration Function:

CL	**AUTO-CALIBRATION CONTROL**	
Description:	Allows the user to initiate auto-calibration and to store calibration values.	
Usage:	CL [option]	
Command combinations:	CLB	Begin auto-calibration. Prior to auto-calibration, the calibration coefficients are automatically restored from flash memory. If the coefficients are not unity gain (0x4000), auto-calibration will yield poor results.
	CLS	Save calibration coefficients to EEPROM starting at address 0x0004
	CLR	Restore calibration coefficients from EEPROM
	CLD	Restore coefficients from flash memory
Example:	CLB	Starts auto-calibration

Before starting the auto-calibration process, target values for voltage and current must be entered in I/O RAM prior to calibration (V at 0x2029, I at 0x202A, duration in accumulation intervals at 0x2028), and the target voltage and current must be applied constantly during calibration. No phase adjustment will be performed. Coefficients can be saved to EEPROM using the CLS command.

Commands controlling the Pulse Counter Function (Demo Code Revision 3.05 only)

CP	PULSE-COUNT CONTROL	
Description:	Allows the user to control the pulse count functions.	
Usage:	CP [option]	
Command combinations:	CPA	Start pulse counting for time period defined with the CPD command. Pulse counts will display with commands M15.2, M16.2
	CPC	Clear the absolute pulse count displays (shown with commands M15.1, M16.1)
	CPDn	Set time window for pulse counters to n seconds, n is interpreted as a decimal number.
Example:	CPD60	Set time window to 60 seconds.

Pulse counts accumulated over a time window defined by the CPD command will be displayed by M15.2 or M16.2 **after** the defined time has expired.

Commands M15.1 and M16.1 will display the **absolute** pulse count for the W and VAR outputs. These displays are reset to zero with the CPC command (or the XRAM write)1=2). Commands M15.2 and M16.2 will display the number of pulses counted during the interval defined by the CPD command. These displays are reset only after a new reading, as initiated by the CPA command.

Commands for Identification and Information:

I	INFORMATION MESSAGES	
Description:	Allows user to read and write information messages.	
Usage:	I [option] [argument]	
Command combinations:	I0	Displays complete version information
	I1	Displays Demo Code version string
	I1=abcdef	Change Demo Code version string
	I2	Displays Copyright string
	I3	CE Version string
	I3=abcdef	Change CE Code version string
Example:	I1	Returns Demo Code version

The I commands are mainly used to identify the revisions of Demo Code and the contained CE code.

P	PROFILE OF METER	
Description:	Returns current meter configuration profile	
Usage:	P	

The profile of the meter is a summary of the important settings of the I/O RAM registers.

Commands for Controlling the Metering Values Shown on the LCD Display:

M	**METER DISPLAY CONTROL (LCD)**	
Description:	Allows user to select internal variables to be displayed.	
Usage:	M [option]. [option]	
Command combinations:	M	Displays "HELLO" message
	M0	Disables display updates
	M1	Temperature (C° delta from nominal)
	M2	Frequency (Hz)
	M3. [phase]	Wh Total Consumption (display wraps around at 999.999)
	M4. [phase]	Wh Total Inverse Consumption (display wraps around at 999.999)
	M5. [phase]	VARh Total Consumption (display wraps around at 999.999)
	M6. [phase]	VAh Total Inverse Consumption (display wraps around at 999.999)
	M7. [phase]	VAh Total (display wraps around at 999.999)
	M8	Operating Time (in hours)
	M9	Real Time Clock
	M10	Calendar Date
	M11. [phase]	V/I Angle at Phase (degrees)
	M12. 1	Main edge count (accumulated)
	M12. 2	CE main edge count for the last accumulation interval
	M13.1	Absolute count for W pulses. Reset with CPC command. **Demo Code revision 3.05 only.**
	M13.2	Count for W pulses in time window defined by the CPD command. **Demo Code revision 3.05 only.**
	M14.1	Absolute count for VAR pulses. Reset with CPC command. **Demo Code revision 3.05 only.**
	M15.2	Count for W pulses in time window defined by the CPD command. **Demo Code revision 3.05 only.**
Example:	M3.1	Displays Wh total consumption of phase A.

Displays for total consumption wrap around at 999.999Wh (or VARh, VAh) due to the limited number of available display digits. Internal registers (counters) of the Demo Code are 64 bits wide and do not wrap around.

When entering the phase parameter, use 1 for phase A, 2 for phase B, and 0 for all phases.

Commands for Controlling the RMS Values Shown on the LCD Display:

MR	**METER RMS DISPLAY CONTROL (LCD)**	
Description:	Allows user to select meter RMS display for voltage or current.	
Usage:	MR [option]. [option]	
Command combinations:	MR1. [phase]	Displays instantaneous RMS current
	MR2. [phase]	Displays instantaneous RMS voltage
Example:	MR1.1	Displays phase A RMS current.

No error message is issued when an invalid parameter is entered, e.g. MR1.8.

Commands for Controlling the MPU Power Save Mode:

PS	**POWER SAVE MODE**	
Description:	Enters power save mode	Disables CE, ADC, CKOUT, ECK, RTM, SSI, TMUX VREF, and serial port, sets MPU clock to 38.4KHz.
Usage:	PS	

Return to normal mode is achieved by resetting the MPU (Z command).

Commands for Controlling the RTC:

RT	**REAL TIME CLOCK CONTROL**	
Description:	Allows the user to read and set the real time clock.	
Usage:	RT [option] [value] … [value]	
Command combinations:	RTDy.m.d.w: Day of week	(year, month, day, weekday [1 = Sunday])
	RTR	Read Real Time Clock.
	RTTh.m.s	Time of day: (hr, min, sec).
	RTAs.t	Real Time Adjust: (start, trim). Allows trimming of the RTC. If s > 0, the speed of the clock will be adjusted by 't' parts per billion (PPB). If the CE is on, the value entered with 't' will be changing with temperature, based on Y_CAL, Y_CAL_DEG1 and Y_CAL_DEG2 .
Example:	RTD05.03.17.5	Programs the RTC to Thursday, 3/17/2005
	RTA1.+1234	Speeds up the RTC by 1234 PPB.

The "Military Time Format" is used for the RTC, i.e. 15:00 is 3:00 PM.

Commands for Accessing the Trim Control Registers:

T	TRIM CONTROL	
Description:	Allows user to read trim and fuse values.	
Usage:	T [option]	
Command combinations:	T4	Read fuse 4.
	T5	Read fuse 5.
	T6	Read fuse 6.
Example:	NONE	

These commands are only accessible for the 6511H (0.1%) parts. When used on a 71M6511 (0.5%) part, the results will be displayed as zero.

Reset Commands:

W, Z	RESET	
Description:	Soft Reset and watchdog control	
Usage:	W, Z	
Commands:	W	Halts the Demo Code program, thus suppressing the triggering of the hardware watchdog timer. This will cause a reset, if the watchdog timer is enabled. **Demo Code revision 3.05 only.**
	Z	Soft reset. This command acts like a hardware reset. The energy accumulators in XRAM will retain their values.

1.8.2 USING THE DEMO BOARD FOR ENERGY MEASUREMENTS

The 71M6511/6511H Demo Board was designed for current transformer (CT), current shunt, or current shunt/CT combinations. The demo code is designed to support both operating modes. **The Demo Boards are normally shipped in CT configuration**.

1.8.3 USING THE DEMO BOARD IN CT MODE

The Demo Board may immediately be used with current transformers having 2,000:1 winding ratio and is programmed for a Kh factor of 1.0 and (see Section 1.8.4 for adjusting the Demo Board for transformers with different turns ratio).

Once voltage is applied and load current is flowing, the red LED D5 (controlled by pin DIO6) will pulse each time an energy sum of 1.0 Wh is collected. The LCD display will show the accumulated imported energy in Wh when set to display mode 3 (command **>M3** via the serial interface). If no energy is displayed, reversed polarity of the current channel may be the reason. The command **>M4** will display the exported energy.

Similarly, the red LED D6 (controlled by pin DIO7) will pulse each time a reactive energy sum of 1.0 VARh is collected. The LCD display will show the accumulated energy in VARh when set to display mode 5 (command **>M5** via the serial interface).

1.8.4 ADJUSTING THE DEMO BOARD TO DIFFERENT CURRENT TRANSFORMERS

The Demo Board is prepared for use with 2000:1 current transformers (CTs). This means that for the unmodified Demo Board, 208A on the primary side at 2000:1 ratio result in 104mA on the secondary side, causing 177mV at the 1.7Ω resistor pairs R24/R25, R36/R37, R56/R57 (2 x 3.4Ω in parallel).

In general, when *IMAX* is applied to the primary side of the CT, the voltage V_{in} at the IA or IB input of the 71M6511 IC is determined by the following formula:

$V_{in} = R * I = R * IMAX/N$
where N = transformer winding ratio, R = resistor on the secondary side

If, for example, *IMAX* = 208A are applied to a CT with a 2500:1 ratio, only 83.2mA will be generated on the secondary side, causing only 141mV. The steps required to adapt a 71M6511 Demo Board to a transformer with a winding ratio of 2500:1 are outlined below:

1) The formula R_x = 177mV/(IMAX/N) is applied to calculate the new resistor R_x. We calculate Rx to 2.115Ω

2) **Changing the resistors R24/R25, R106/R107 to a combined resistance of 2.115Ω** (for each pair) will cause the desired voltage drop of 177mV appearing at the IA, or IB inputs of the 71M6511 IC.

3) *WRATE* should be adjusted to achieve the desired Kh factor, as described in 1.8.2.

Simply scaling *IMAX* is not recommended, since peak voltages at the 71M6511 inputs should always be in the range of 0 through ±250mV (equivalent to 177mV rms). If a CT with a much lower winding ratio than 1:2,000 is used, higher secondary currents will result, causing excessive voltages at the 71M6511 inputs. Conversely, CTs with much higher ratio will tend to decrease the useable signal voltage range at the 71M6511 inputs and may thus decrease resolution.

1.8.5 ADJUSTING THE KH FACTOR FOR THE DEMO BOARD

The 71M6511/6511H Demo Board is shipped with a pre-programmed scaling factor Kh of 1.0, i.e. 1Wh per pulse. In order to be used with a calibrated load or a meter calibration system, the board should be connected to the AC power source using the spade terminals on the bottom of the board. The current transformers should be connected to the dual-pin headers on the bottom of the board.

The Kh value can be derived by reading the values for IMAX and VMAX (i.e. the RMS current and voltage values that correspond to the 250mV maximum input signal to the IC), and inserting them in the following equation for Kh:

$$\mathbf{Kh = \mathit{IMAX} * \mathit{VMAX} * 47.1132 / (In\_8 * \mathit{WRATE} * N_{ACC} * X) = 0.99967\ Wh/pulse.}$$

Where *IMAX* is the current scaling factor, *VMAX* is the voltage scaling factor, *In_8* is the current shunt gain factor, *WRATE* is the CE variable controlling Kh, N_{ACC} is the product of the I/O RAM variables *PRE_SAMPS* and *SUM_CYCLES*, and X is the pulse frequency factor derived from the CE variables *PULSE_SLOW* and *PULSE_FAST*.

The small deviation between the adjusted Kh of 0.99967 and the ideal Kh of 1.0 is covered by calibration. The default values used for the 71M6511/6511H Demo Board are:

WRATE:	1556	
IMAX:	208	
VMAX:	600	
In_8:	1	(controlled by *IA_SHUNT* = -15)
N_{ACC}:	2520	
X:	1.5	

Explanation of factors used in the Kh calculation:

WRATE: The factor input by the user to determine Kh

IMAX: The current input scaling factor, i.e. the input current generating 177mVrms at the IA/IB input pins of the 71M6511. 177mV rms is equivalent to 250mV peak.

VMAX: The voltage input scaling factor, i.e. the voltage generating 177mVrms at the VA input pins of the 71M6511

In_8: The setting for the additional ADC gain (8 or 1) determined by the CE register *IA_SHUNT*

N_{ACC}: The number of samples per accumulation interval, i.e. *PRE_SAMPS* *SUM_CYCLES*

X: The pulse rate control factor determined by the CE registers *PULSE_SLOW* and *PULSE_FAST*

Almost any desired Kh factor can be selected for the Demo Board by resolving the formula for WRATE:

$$\mathbf{\mathit{WRATE} = (IMAX * VMAX * 47.1132) / (Kh * In\_8 * N_{ACC} * X)}$$

For the Kh of 1.0Wh, the value 1556 (decimal) should be entered for WRATE at location 2D (using the CLI command **>]2D=+1556**).

1.8.6 USING THE DEMO BOARD IN CURRENT SHUNT MODE

With a few quick modifications, the 71M6511/6511H Demo Board can be adapted to operate with a current shunt/CT combination or a single shunt. **Modifications are shown for the 2-Layer Demo Board. Component references and configuration are slightly different for the 4-Layer Demo Board. Check the schematic and PCB layout given for the 4-Layer Demo Board when applying the modifications.**

Figure 1-9 shows the connections necessary for this operation mode. The voltage drop across the shunt resistor is fed into the IA input of the 71M6511/6511H, with V3P3 being the reference. The voltage between LIVE and NEUTRAL is divided by the resistor divider associated with the voltage input and supplied to the VA input of the chip. The division ratio is so that the voltage at VA is within ±250mV of V3P3. The power supply generates the 3.3VDC from the voltage between the shunt and the load, with "ground" being only 3.3V lower than the voltage at the load.

In this configuration, the whole Demo Board will be at line voltage! Touching the board or any components must be avoided!

The routing of the input sensing traces for the reference V3P3 at the voltage and shunt inputs is very critical.

Current shunts used in energy meters are usually of very low resistance, typically 100µΩ to 400µΩ. This is because self-heating of the resistor that could lead to non-linear behavior must be avoided. A current shunt of 200µΩ operated at 40A (at a power of 320mW) will only generate 8mV, far below the maximum range of 176mV for the current inputs of the 71M6511/6511H.

The 71M6511/6511H has an optional digital gain stage that can be used to increase low signals, as generated by current shunts, by eight.

In order to operate the 71M6511/6511H Demo Board (D6511BT4A4, D6511BT4A5, D6511BT4A7 or later) with a current shunt sensor, the following measures must be taken:

a) Remove the jumpers on JP16 and JP17.

b) Remove R24 and R25 if IA_IN is the input channel for the current shunt or remove R106 and R107 if IB_IN is the input channel for the current shunt.

c) Add a 10kΩ resistor at R24 if IA_IN is the input channel for the current shunt or add a 10kΩ resistor at R106 if IB_IN is the input channel for the current shunt. This resistor will provide noise termination and will suppress unwanted readings.

d) The LIVE line must be connected to the spade terminal J4 (bottom of the board).

e) The blue and white pair of wires from the shunt resistor must be connected to contacts 1 and 2 on J3, as shown in **Error! Reference source not found.**, if IA_IN is the input channel or contacts 1 and 2 on J16 if IB_IN is the input channel.

f) Connect the green wire to pin1 of JP16 (pin closest to the regulator output, power supply pin) and the red wire to pin 2 of JP17 (resistor divider output). Both wires are joined at the shunt.

g) Through the serial terminal (command line interface), the Demo Program can be set to run in current shunt mode. This is done by issuing the commands **`>]2A=1`** if IA_IN is connected to the shunt or **`>]2B=1`** for IB_IN connected to the shunt. This will cause the Demo Program to select the proper input channels and to apply the gain of 8 to the shunt input channel from the ADC output before processing for power measurement.

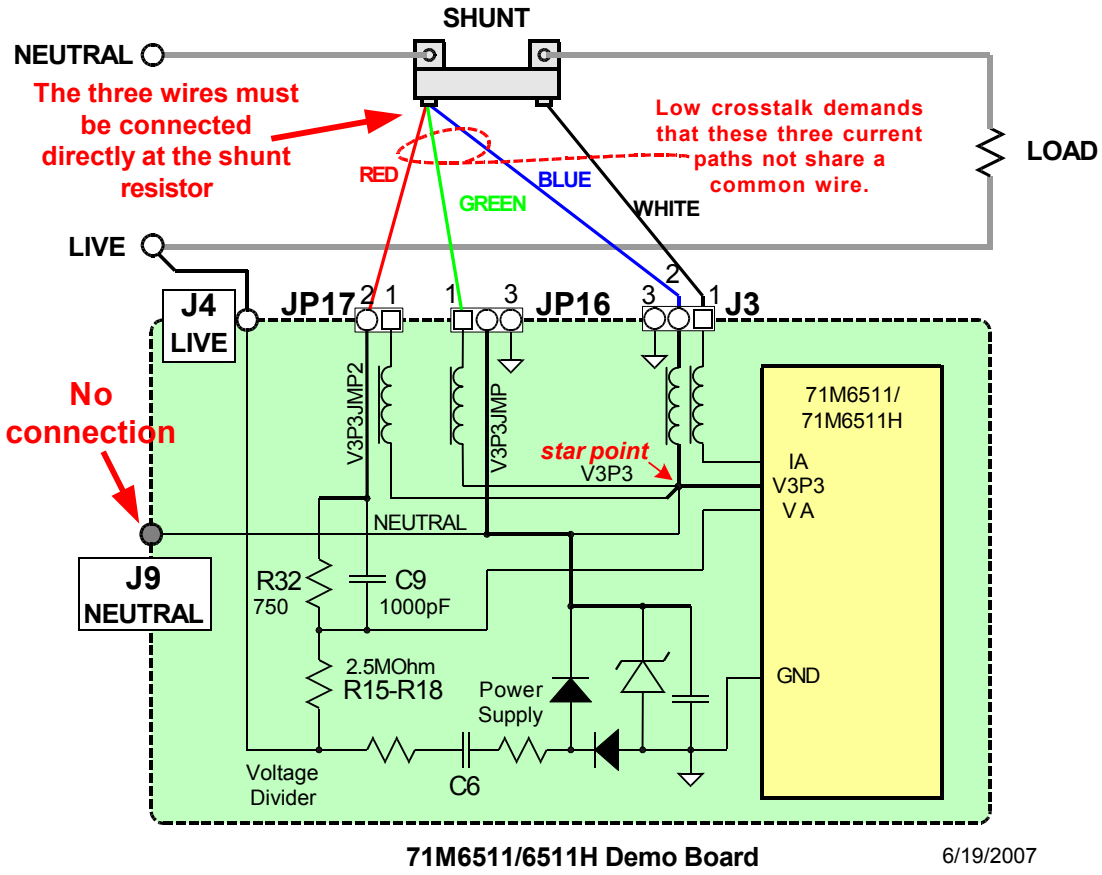


Figure 1-9: Current Shunt Operation Mode (Shown for the D6511T4A7 2-layer PCB)

The *IMAX* variable has to re-calculated for current shunt mode using the formula:

$$IMAX = 177mV/R_{shunt}$$

The new value for IMAX (XRAM address 0x0A) should be entered, using the command line interface, as follows (example shown assuming $R_{shunt} = 400\mu\Omega$, with resulting IMAX = 440):

```
>)A=+4400
```

Note: IMAX values have a LSB resolution of 0.1A, VMAX values have a LSB resolution of 0.1V

Note: Since IMAX has been changed, WRATE has to be recalculated to maintain the desired Kh.

If desired, the Demo Code can be set to run with increased gain (8 instead of 1) of the current channels, as sometimes required in current shunt mode due to low currents and low shunt resistances. This can be done via the command line interface by the commands

`>]2A=+15`	setting IA_8 to 8 by controlling IA_SHUNT at address 0x2A, if IA_IN is connected to the shunt, or
`>]2B=+15`	setting IB_8 to 8 by controlling IB_SHUNT at address 0x2B if IB_IN is connected to the shunt.

Typically, only one shunt resistor is used in a meter. Isolation requires a transformer for the second shunt resistor when using two shunts in a meter.

The Demo Code will compensate for the increased gain, i.e. the energy and current readings do not have to be scaled.

A top-level schematic of the board connected to a shunt resistor is shown in Figure 1-10.

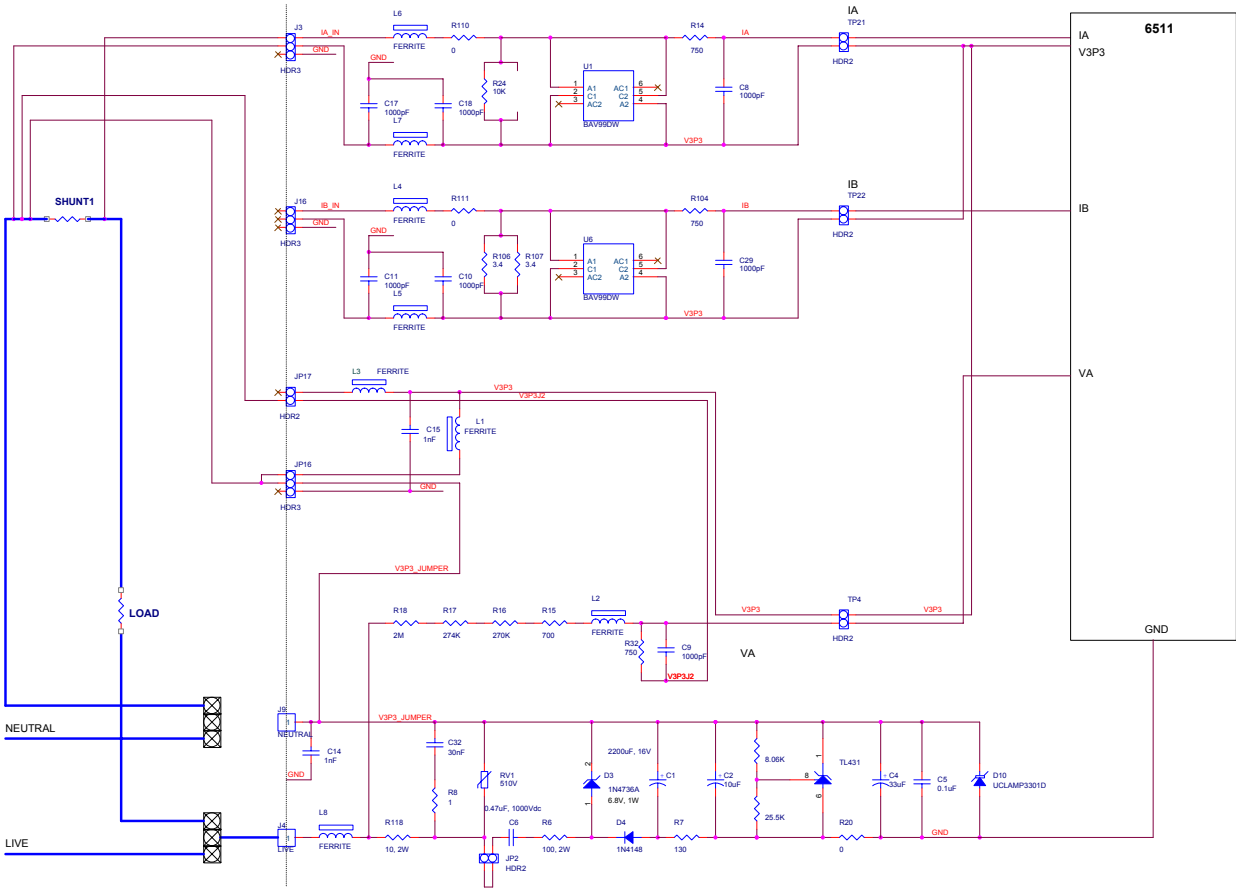


Figure 1-10: Current Shunt Top-Level Schematics (Shown for the 2-Layer Board)

1.8.7 ADJUSTING THE DEMO BOARD TO DIFFERENT VOLTAGE DIVIDERS

The 6511 Demo Board comes equipped with its own network of resistor dividers for voltage measurement mounted on the PCB. The resistor values (for the 4-layer Demo Board) are 2.5477MΩ (R15-R21, R26-R31 combined) and 750Ω (R32), resulting in a ratio of 1:3,393.933. This means that *VMAX* equals 176.78mV*3,393.933 = 600V. A large value for *VMAX* has been selected in order to have headroom for overvoltages. This choice need not be of concern, since the ADC in the 71M6511 has enough resolution, even when operating at 120Vrms or 240Vrms.

If a **different set of voltage dividers** or an external voltage transformer is to be used, scaling techniques similar to those applied for the current transformer should be used.

In the following example we assume that the line voltage is not applied to the resistor divider for VA formed by R15-R21, R26-R31, and R32, but to a voltage transformer with a ratio N of 20:1, followed by a simple resistor divider. We also assume that we want to maintain the value for *VMAX* at 600V to provide headroom for large voltage excursions.

When applying VMAX at the primary side of the transformer, the secondary voltage V_s is:

V_s = VMAX / N

V_s is scaled by the resistor divider ratio R_R. When the input voltage to the voltage channel of the 71M6511 is the desired 177mV, V_s is then given by:

$V_s = R_R * 177mV$

Resolving for R_R, we get:

R_R = (VMAX / N) / 177mV = (600V / 30) / 177mV = 170.45

This divider ratio can be implemented, for example, with a combination of one 16.95kΩ and one 100Ω resistor.

1.9 CALIBRATION PARAMETERS

1.9.1 GENERAL CALIBRATION PROCEDURE

Any calibration method can be used with the 71M6511/6511H chips. This Demo Board User's Manual presents calibration methods with three or five measurements as recommended methods, because they work with most manual calibration systems based on counting "pulses" (emitted by LEDs on the meter).

Naturally, a meter in mass production will be equipped with special calibration code offering capabilities beyond those of the Demo Code. It is basically possible to calibrate using voltage and current readings, with or without pulses involved. For this purpose, the MPU Demo Code can be modified to display averaged voltage and current values (as opposed to momentary values). Also, automated calibration equipment can communicate with the Demo Boards via the serial interface and extract voltage and current readings. This is possible even with the unmodified Demo Code.

A complete calibration procedure is given in Section 2.1 (Application Information).

Regardless of the calibration procedure used, parameters (calibration constants) will result that will have to be applied to the 71M6511/6511H chip in order to make the chip apply the modified gains and phase shifts necessary for accurate operation. Table 1-4 shows the names of the calibration constants, their function, and their location in the CE RAM.

Again, the command line interface can be used to store the calibration constants in their respective CE RAM addresses. For example, the command

>]8=+16302

stores the decimal value 16302 in the CE RAM location controlling the gain of the current channel (*CAL_IA*).

The command

>]9=4005

stores the hexadecimal value 0x4005 (decimal 16389) in the CE RAM location controlling the gain of the voltage channel (*CAL_VA*).

Constant	CE Address (hex)	Description
CAL_VA *RESERVED* *RESERVED*	0x09 0x0B 0x0D	Adjusts the gain of the voltage channel. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%.
CAL_I0 *CAL_I1* *RESERVED*	0x08 0x0A 0x0C	Adjusts the gain of the current channels. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%.
PHADJ_0 *PHADJ_1*[1] *RESERVED*	0x0E 0x0F 0x10	This constant controls the CT phase compensation. No compensation occurs when PHADJ=0. As PHADJ is increased, more compensation is introduced. **Note: PHASDJ_1[1] applies to 3W/1-phase systems.**
TEMP_NOM	0x11	*TEMP_RAWX* reading

Table 1-4: CE RAM Locations for Calibration Constants

1.9.2 CALIBRATION MACRO FILE

Once, calibration parameters (calibration constants) have been determined, instead of manually typing them in using the command line interface, macro files may be used to simplify this procedure.

The macro file in Figure 1-11 contains a sequence of the serial interface commands that implements changes to the calibration parameters (CE address locations 0x08 to 0x10). It is a simple text file and can be created with Notepad or an equivalent ASCII editor program.

The file is executed with the following command of the HyperTerminal program:

Transfer->Send Text File.

```
]8=+16022/      CAL_IA (gain=CAL_IA/16384)
]9=+16381/      CAL_VA (gain=CAL_VA/16384)
]a=+16019/      CAL_IB (gain=CAL_IB/16384)
]e=+115/        PHADJ_A (default 0)
]f=+113/        PHADJ_B (default 0)
ce1
```

Figure 1-11: Typical Calibration Macro file

It is possible to send the calibration macro file to the 71M6511/71M6511H for "temporary" calibration. This will temporarily change the CE data values. Upon power up, these values are refreshed back to the default values stored in flash memory. Thus, until the flash memory is updated, the macro file must be loaded each time the part is powered up. The macro file is run by first issuing the CE0 command to turn off the compute engine and then sending the file with the *transfer → send text file* procedure.

Note: Use the *Transfer → Send Text File* command!

1.9.3 UPDATING THE 6511_DEMO.HEX FILE

The io_merge program updates the 6511_demo.hex file with the values contained in the macro file. This program is executed from a DOS command line window. Executing the io_merge program with no arguments will display the syntax description. To merge macro.txt and old_6511_demo.hex into new_6511_demo.hex, use the command:

```
io_merge old_6511_demo.hex macro.txt new_6511_demo.hex
```

The new hex file can be written to the 71M6511/71M6511H through the ICE port using an in-circuit emulator. This step makes the calibration to the meter permanent.

1.9.4 UPDATING CALIBRATION DATA IN FLASH MEMORY WITHOUT USING THE ICE

It is possible to make data permanent that had been entered temporarily into the CE RAM. The transfer to flash memory is done using the following serial interface command:

```
>]U
```

Thus, after transferring calibration data with manual serial interface commands or with a macro file, all that has to be done is invoking the U command.

Similarly, calibration data can also stored in EEPROM using the CLS command.

After reset, calibration data is copied from the EEPROM, if present. Otherwise, calibration data is copied from the flash memory. Writing 0xFF into the first few bytes of the EEPROM deactivates any calibration data previously stored to the EEPROM.

1.9.5 AUTOMATIC GAINS CALIBRATION

Starting with Demo Code revision 3.04, it is possible to perform a simple automatic calibration. This calibration is performed for resistive loads only and will not correct phase angle. The steps required for the calibration are:

1. Enter operating values for voltage and current in I/O RAM. The voltage is entered at address 0x2029 (e.g. with the command **)29=+2400** for 240V), the current is entered at 0x202A (e.g. with the command **)2A=+300** for 30A) and the duration measured in accumulation intervals is entered at 0x2028.
2. The operating voltage and current defined in step 1 must be applied to the meter (Demo Board).
3. The CLB (Begin Calibration) command is then entered via the serial interface. The operating voltage and current must be maintained accurately while the calibration is being performed.
4. The calibration procedure will automatically reset CE addresses 08, 09, 0x0A, 0x0B, 0x0C, and 0x0D to nominal values (0x4000), and 0x0E, 0x0F and 0x10 to zero prior to starting the calibration. Automatic calibration also reads the chip temperature and enters it in CE location 0x11 for proper temperature compensation.
5. Completion of the automatic calibration will be signaled by the LCD showing the "HELLO" message. Enter M3 or another serial interface command to bring the display back to normal.
6. CE addresses 0x08 and 0x09 will now show values other than 0x4000. These values can be stored in EEPROM by issuing the CLS command.

Note: Current transformers of a given type usually have very similar phase angle for identical operating conditions. If the phase angle is accurately determined for one current transformer, the corresponding phase adjustment coefficient PHADJ_X can be entered for all calibrated units.

1.9.6 LOADING THE 6511_DEMO.HEX FILE INTO THE DEMO BOARD

Hardware Interface for Programming: The 71M6511/6511H IC provides an interface for loading code into the internal flash memory. This interface consists of the following signals:

E_RXTX (data)

E_TCLK (clock)

E_RST (reset)

These signals, along with V3P3 and GND are available on the emulator header J14. Production meters may be equipped with much simpler programming connectors, e.g. a 5x1 header.

Programming of the flash memory requires either the ADM51 in-circuit emulator by Signum Systems (http//www.signumsystems.com) or the Flash Download Board Module (FDBM) provided by TERIDIAN Semiconductor.

In-Circuit Emulator: If firmware exists in the 71M6511/6511H flash memory, the memory has to be erased before loading a new file into memory. In order to erase the flash memory, the RESET button of the emulator software has to be clicked followed by the ERASE button (Figure 1-12).

Once the flash memory is erased, the new file can be loaded using the Load command in the File menu. The dialog box shown in Figure 1-13 makes it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button loads the file into the flash memory of the IC.

At this point, the emulator probe (cable) can be removed. Once the 71M6511/6511H IC is reset using the reset button on the Demo Board, the new code starts executing.

Flash Download Board Module (FDBM): Follow the instructions given in the User Manual for the FDBM.

The hardware watchdog timer must be disabled during all programming operations.

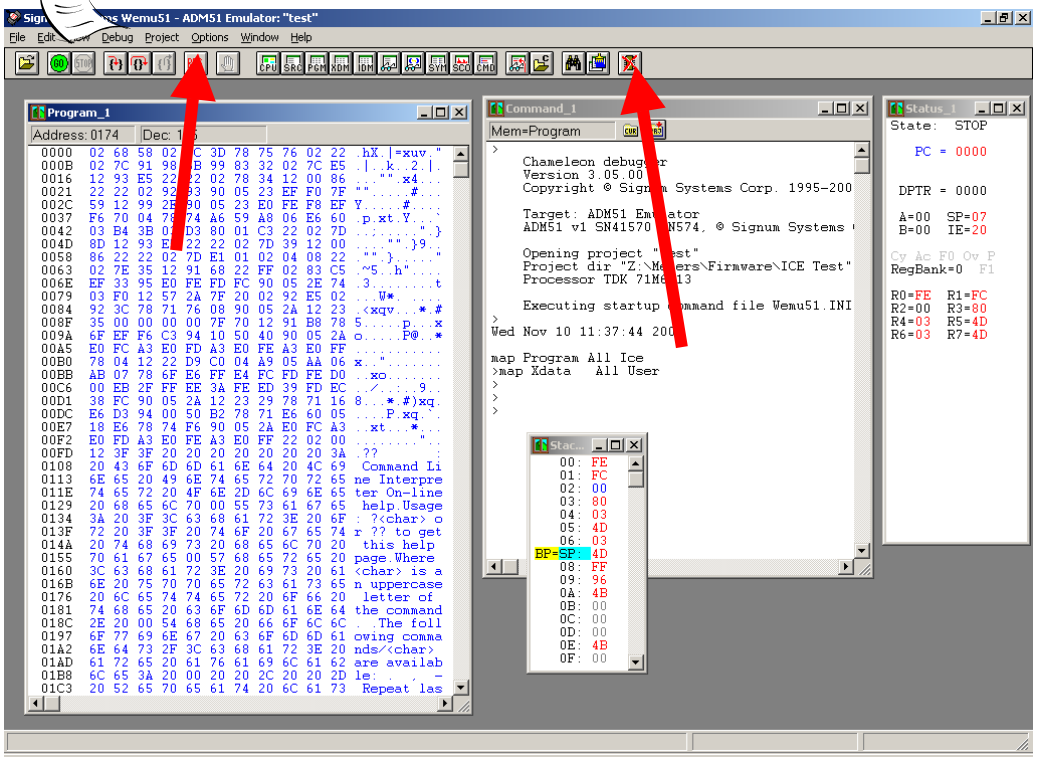


Figure 1-12: Emulator Window Showing Reset and Erase Buttons

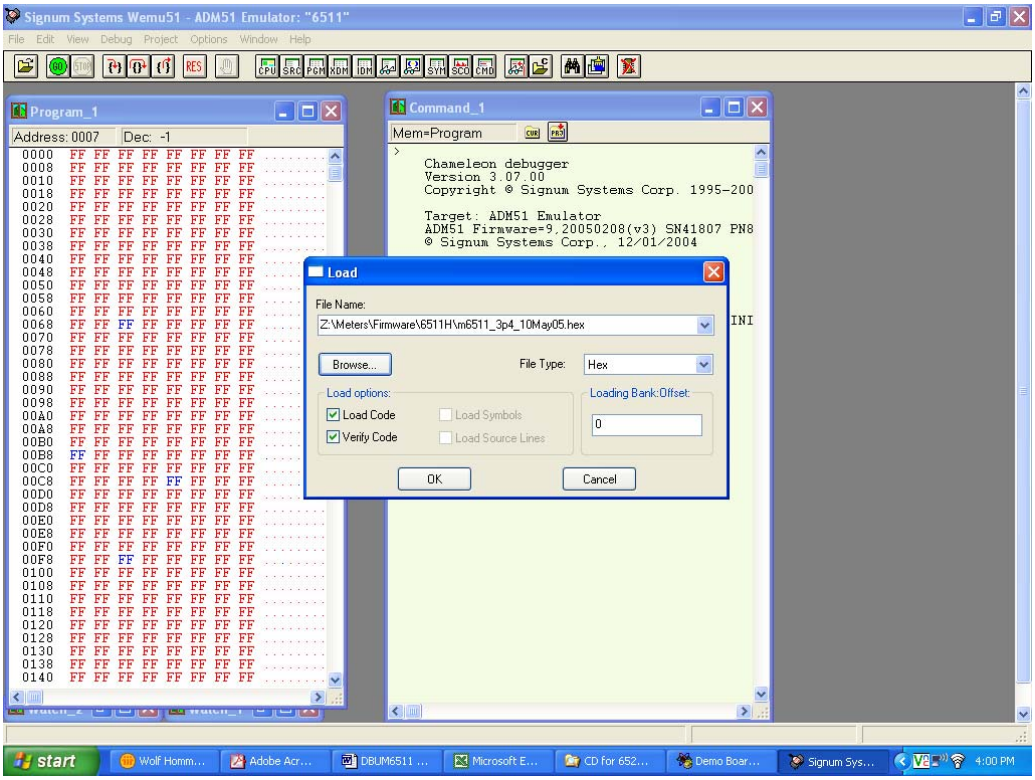


Figure 1-13: Emulator Window Showing Erased Flash Memory and File Load Menu

1.9.7 THE PROGRAMMING INTERFACE OF THE 71M6511/6511H

Flash Downloader/ICE Interface Signals

The signals listed in Table 1-5 are necessary for communication between the Flash Downloader or ICE and the 71M6511/6511H.

Signal	Direction	Function
E_TCLK	Output from 71M6511/6511H	Data clock
E_RXTX	Bi-directional	Data input/output
E_RST	Bi-directional	Flash Downloader Reset (active low)

Table 1-5: Flash Programming Interface Signals

The E_RST signal should only be driven by the Flash Downloader when enabling these interface signals. The Flash Downloader must release E_RST at all other times.

1.10 DEMO CODE

1.10.1 DEMO CODE DESCRIPTION

The Demo Board is shipped preloaded with Demo Code revision 3.0.4 or later in the 71M6511 or 71M6511H chip. The code revision can easily be verified by entering the command >**i1** via the serial interface (see section 1.8.1). Check with your local TERIDIAN representative or FAE for the latest revision.

Some Demo Boards are shipped with Demo Code revision 3.03. These boards can be updated to revision 3.04 or later using either an in-circuit emulator (ICE) or the Flash Download Board Module (FDBM), as described in section 1.9.6.

The Demo Code is useful due to the following features:

- It provides basic metering functions such as pulse generation, display of accumulated energy, frequency, date/time, and enables the user to evaluate the parameters of the metering IC such as accuracy, harmonic performance, etc.
- It maintains and provides access to basic household functions such as real-time clock (RTC).
- It provides access to control and display functions via the serial interface, enabling the user to view and modify a variety of meter parameters such as Kh, calibration coefficients, temperature compensation etc.
- It provides libraries for access of low-level IC functions to serve as building blocks for code development.

A detailed description of the Demo Code can be found in the Software User's Guide (SUG). In addition, the comments contained in the library provided with the Demo Kit can serve as useful documentation.

The Software User's Guide contains the following information:

- Design guide
- Design reference for routines
- Tool Installation Guide
- List of library functions
- 80515 MPU Reference (hardware, instruction set, memory, registers)
- Description of serial interface commands

1.10.2 DEMO CODE MPU PARAMETERS

In the Demo Code, certain MPU XRAM parameters have been given fixed addresses in order to permit easy external access. These variables can be read via the serial interface, as described in section 1.8.1, with the **)n$** command and written with the **)n=xx** command where n is the word address. Note that accumulation variables are 64 bits long and are accessed with **)n$$** (read) and **)n=hh=ll** (write) in the case of accumulation variables.

MPU INPUT PARAMETERS

All MPU Input Parameters are loaded by the MPU at startup and should not need adjustment during meter calibration.

MPU Input Parameters for Metering

XDATA Word Address	Default Value	Name	Description
0x00	8311	*WCREEP_THR*	For each element, if *WSUM_X* or *VARSUM_X* of that element exceeds W*CREEP_THR*, the sample values for that element are not zeroed. Otherwise, the accumulators for Wh, VARh, and VAh are not updated and the instantaneous value of IRMS for that element is zeroed. LSB = $6.6952*10^{-13}$ VMAX IMAX Wh The default value 8310 is equivalent to 2.5Wh/h. **Demo Code revision 3.05:** *WCREEP_THR* applies to phase A only.
0x01	0	*CONFIG*	Bit 0: Sets VA calculation mode. 0: $V_{RMS}*A_{RMS}$ 1: $\sqrt{W^2 + VAR^2}$ Bit 1: Clears accumulators for Wh, VARh, VAh. This bit need not be reset.
0x02	0	*PK_VTHR*	Demo Code revision 3.04: Not implemented.
	191181742		**Demo Code revision 3.05:** When the voltage exceeds this value, bit 5 in the MPU status word is set, and the MPU might choose to log a warning. Event logs are not implemented in Demo Code. LSB = $6.6952*10^{-13}*VMAX^2\ V^2h_{RMS}$ The default value of 191181742 is equivalent to $407.3V_{RMS}$ if VMAX = 600V and a 1-second accumulation interval is used.
0x03	0	*PK_ITHR*	Demo Code revision 3.04: Not implemented.
	24856631		**Demo Code revision 3.05:** When the current exceeds this value, bit 6 in the MPU status word is set, and the MPU might choose to log a warning. Event logs are not implemented in Demo Code. LSB = $6.6952*10^{-13}*IMAX^2\ V^2h_{RMS}$ The default value of 24856631 is equivalent to $50.9A_{RMS}$ if IMAX = 208A and a 1-second accumulation interval is used.
0x09	6000	*VMAX*	The nominal external RMS voltage that corresponds to 250mV peak at the ADC input. The meter uses this value to convert internal quantities to external. LSB=0.1V
0x0A	2080	*IMAX*	The nominal external RMS current that corresponds to 250mV peak at the ADC input. The meter uses this value to convert internal quantities to external. LSB=0.1A

0x13	61	*ICREEP_THR*	For each element, if *ISQSUM* of that element exceeds I*CREEP_THR*, the sample values for that element are not zeroed. Otherwise, the accumulators for Wh, VARh, and VAh are not updated and the instantaneous value of IRMS for that element is zeroed. LSB = $6.6952*10^{-13}$ MAX^2 Wh The default value 61 is equivalent to 80mA. **Demo Code revision 3.05:** *WCREEP_THR* applies to phase A only.

Table 1-6: MPU Input Parameters for Metering

MPU Input Parameters for Temperature Compensation

XDATA Word Address	Default Value	Name	Description
4	0	*Y_CAL*	Implement RTC trim. $CORRECTION(ppm) = \frac{Y\_CAL}{10} + T \cdot \frac{Y\_CALC}{100} + T^2 \cdot \frac{Y\_CALC2}{1000}$
5	0	*Y_CALC*	
6	0	*Y_CALC2*	
B	0	*PPMC*	PPM/C*26.84. Linear temperature compensation. A positive value will cause the meter to run faster when hot. This is applied to both V and I and will therefore have a double effect on products. Default is 0.
C	0	*PPMC2*	PPM/C^2*1374. Square law compensation. A positive value will cause the meter to run faster when hot. This is applied to both V and I and will therefore have a double effect on products. Default is 0.
D	9585	*DEGSCALE*	Scale factor for TEMP_X. TEMP_X=*DEGSCALE*$*2^{-22}*$(TEMP_RAW_X-TEMP_NOM).

Table 1-7: MPU Input Parameters for Temperature Compensation

MPU Input Parameters for Pulse Generation

XDATA Word Address	Default Value	Name	Description
7	1	*PULSEW_SRC*	This address contains a number that points to the selected pulse source. Selectable pulse sources are listed in Table 1-9.
8	5	*PULSER_SRC*	This address contains a number that points to the selected pulse source. Selectable pulse sources are listed in Table 1-9.

Table 1-8: MPU Parameters for Pulse Source Selection

Any of the values listed in Table 1-9 can be selected for as a source for PULSEW and PULSER. The designation "source_I" refers to values imported by the consumer, "source_E" refers to energy exported by the consumer (energy generation).

Number	Pulse Source	Description
0	Reserved	
1	***WASUM***	***default for PULSEW_SRC***
2	*WBSUM*	
3	Reserved	
4	Reserved	
5	***VAR0SUM***	***default for PULSER_SRC***
6	*VAR1SUM*	
7	Reserved	
8	*IASQSUM*	
9	*IBSQSUM*	
10	Reserved	
11	Reserved	
12	*VASQSUM*	
13	Reserved	
14	Reserved	
15	Reserved	
16	*VAASUM*	
17	*VABSUM*	

Number	Pulse Source	Description
18	Reserved	
19	Reserved	
20	*WASUM_I*	Imported real energy on element A
21	*WBSUM_I*	Imported real energy on element B
22	Reserved	
23	Reserved	
24	*VARASUM_I*	Imported reactive energy on element A
25	*VARBSUM_I*	Imported reactive energy on element B
26	Reserved	
27	Reserved	
28	*WASUM_E*	Exported real energy on element A
29	*WBSUM_E*	Exported real energy on element B
30	Reserved	
31	Reserved	
32	*VARASUM_E*	Exported reactive energy on element A
33	*VARBSUM_E*	Exported reactive energy on element B
34	Reserved	

Table 1-9: Selectable Pulse Sources

MPU INSTANTANEOUS OUTPUT VARIABLES

The Demo Code processes CE outputs after each accumulation interval. It calculates instantaneous values such as VRMS, IRMS, W and VA as well as accumulated values such as Wh, VARh, and VAh. Table 1-10 lists the calculated instantaneous values.

XRAM Word Address	Name	Description
0x14 0x15 0x16	Vrms_A reserved reserved	Vrms: $LSB = \frac{3.7610 \cdot 10^{-8} VMAX}{\sqrt{Nacc}}$
0x17 0x18 0x19	Irms_A Irms_B reserved	Irms from element 0, 1, 2. $LSB = \frac{3.7610 \cdot 10^{-8} IMAX\ In8}{\sqrt{Nacc}}$
0x1A 0x1B 0x1C	IPhase_A reserved reserved	Phase between voltage and current. The number of degrees I lags V. LSB=0.001°, range: 0…+360
0x1D	Frequency	Frequency of the voltage signal selected by the CE input. If the selected voltage is below the sag threshold, Frequency = 0. LSB $\equiv \frac{F_S}{2^{32}} \approx 0.587 \cdot 10^{-6}$ Hz
0x1E	Delta_T	Deviation from Calibration temperature. LSB = 0.1 ^{0}C.
0x1F 0x20	reserved reserved	
0x21	Status	MPU Status Word
0x22	OperatingTime	Total operating time. LSB = 0.01h = 36s
0x23	Reserved	

Table 1-10: MPU Instantaneous Output Variables

MPU STATUS WORD

The MPU maintains the status of certain meter and I/O related variables in the Status Word. The Status Word is located at address 0x21. The bit assignments are listed in Table 1-11.

Status Word Bit	Name	DESCRIPTION
0	Reserved	
1	SAGA	Reserved for sag flag phase A – not implemented[1]
2	Reserved	Reserved
3	Reserved	Reserved
4	F0	Reconstructed line signal flag
5	MAXV	Overvoltage. 1 when overvoltage is detected.
6	MAXI	Overcurrent. 1 when overcurrent is detected.
7	ONE_SEC	Reserved
8	VXEDGE	Reserved
9	Reserved	
10	Reserved	
11	XFER	Reserved
12	CREEP	Creep bit. This bit is 1 when creep is detected. The creep bit is only set when a creep condition is active in both phases.
13-31	Reserved	

Note: [1]: Not implemented in Demo Code revision 3.04

Table 1-11: MPU Status Word Bit Assignment

MPU ACCUMULATION OUTPUT VARIABLES

Accumulation values are accumulated from XFER cycle to XFER cycle (see Table 1-12). They are all in 64-bit format. The 6511 has an LSB of $6.6925*10^{-13}*VMAX*IMAX*In\_8$ Wh. Thus, the accumulators will hold at least 136 years of data when XFER rate is 1Hz.

The CLI commands with two Dollar signs e.g. **)39$$** should be used to read the variables. When using the commands with two question marks, e.g. **)39??**, negative decimal values will be displayed when the most significant bit is set.

XDATA Word Address	Name	Description
0x2F	Reserved	
0x31	Reserved	
0x33	Reserved	
0x35	Reserved	
0x37	Reserved	
0x39	*Wh_A*	Total Watt hours consumed through phase A[1)]
0x3B	*Whe_A*	Total Watt hours generated (inverse consumed) through phase A[1)]
0x3D	*VARh_A*	Total VAR hours consumed through phase A[2)]
0x3F	*VARhe_A*	Total VAR hours generated (inverse consumed) through phase A[2)]
0x41	*VAh_A*	Total VA hours in phase A[3)]
0x43	*Wh_B*	Total Watt hours consumed through phase B[1)]
0x45	*Whe_B*	Total Watt hours generated (inverse consumed) through phase B[1)]
0x47	*VARh_B*	Total VAR hours consumed through phase B[2)]
0x49	*VARhe_B*	Total VAR hours generated (inverse consumed) through phase B[2)]
0x4B	*VAh_B*	Total VA hours in phase B[3)]
0x4D	Reserved	
0x4F	Reserved	
0x51	Reserved	
0x53	Reserved	
0x55	Reserved	

Table 1-12: MPU Accumulation Output Variables

Notes:

[1)]: If *EQU* = 0, Wh_A = real component of IA*VA and Wh_B = real component of IB*VA.
If *EQU* = 1, Wh_A = real component of VA * (IA – IB)/2 and Wh_B = real component of VA*IB.
[2)]: If *EQU* = 0, VARh_A = reactive component of IA*VA and VARh_B = reactive component of IB*VA.
If *EQU* = 1, VARh_A = VA * (IA – IB)/2 and Wh_B = VA*IB.
[3)]: If *EQU* = 0, VAh_A = apparent energy based on IA*VA and VAh_B = apparent energy based on IB*VA.
If *EQU* = 1, VAh_A = apparent energy based on VA * (IA – IB)/2 and VAh_B = apparent energy based on VA*IB.

MPU VARIABLES INDEPENDENTLY CONTROLLING THE SECOND CURRENT CHANNEL

The 6511 Demo Code revision 3.05 offers independent scaling and creep suppression parameters for the second current channel (phase B). This is useful for meter configurations where different sensors are used for the primary and secondary channel. An example for this would be a meter using a CT for phase A and an additional resistive shunt for phase B to counter tampering. In most cases, the input voltage at the IA and IB inputs generated by the current flowing through both sensors will not be identical due to the differing characteristics of the sensors. In order to enable comparative measurements and true application of tariffs, Demo Code revision 3.05 offers a set of variables used to scale the IB channel (phase B).

The variables added in 6511 Demo Code revision 3.05 are shown in Table 1-13.

Note that the values for *IMAX*, *ICREEP2*, and *WCREEP2* are closely coupled: When entering a different value for *IMAX2*, *ICREEP2* and *WCREEP2* should be changed accordingly, if the accuracy of the creep detection is of interest.

XRAM Word Address	Default Value	Name	Description
0x2B	2080	*IMAX2*	The nominal external RMS current that corresponds to 250mV peak at the IB input. The meter uses this value to convert internal quantities to external. LSB=0.1A
0x2C	61	*ICREEP2*	If the squared current (ISQSUM from the CE) of phase B is below *ICREEP2*, the sample values for phase B are zeroed. In that case, the accumulators for Wh, VARh, and VAh are not updated and the instantaneous value of IRMS for phase B is zeroed. The default value corresponds to $0.00636A^2$ (80mA), if the default setting for *IMAX2* is used. LSB = $6.6952*10^{-13}$ $IMAX^2$ Wh
0x2D	8311	*WCREEP2*	If *WSUM_2* or *VARSUM_2* are below *WCREEP2*, the sample values for phase B are zeroed. In that case, the accumulators for Wh, VARh, and VAh are not updated and the instantaneous value of IRMS for phase B is zeroed. The default value corresponds to 2.5W, if the default settings for *VMAX* and *IMAX2* are used. LSB = $6.6952*10^{-13}$ *VMAX IMAX2* Wh

Table 1-13: MPU Variables Related to Phase B (6511, Revision 3.05 only)

1.10.3 USEFUL CLI COMMANDS INVOLVING THE MPU AND CE

Table 1-14 shows a few essential commands involving MPU data memory.

Command	Description
>)1=2	Clears the accumulators for Wh, VARh, and VAh by setting bit 1 of the *CONFIG* register.
>)7=1	Switches the Wh pulse source to W0SUM
>)7=2	Switches the Wh pulse source to W1SUM (e.g. when testing with single phase CT applied to phase B)
>)A=+2080	Applies the value corresponding to 208A to the IMAX register
>)9=+6000	Applies the value corresponding to 600V to the VMAX register
>)22?	Displays the operating time since the last power up (in 1/100 of hours)
>)39$$	Displays the total accumulated Wh energy for phase A (two $$ used for full 64-bit hexa-decimal display)
>MR2.1	Displays the current RMS voltage in phase A
>MR1.2	Displays the current RMS current in phase B
]U	Stores the current CE RAM variables in flash memory. The stored variables will be applied by the MPU at the next reset or power-up.

Table 1-14: CLI Commands for MPU Data Memory

2

2 APPLICATION INFORMATION

2.1 CALIBRATION THEORY

A typical meter has phase and gain errors as shown by ϕ_S, A_{XI}, and A_{XV} in Figure 2-1. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 2-1 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

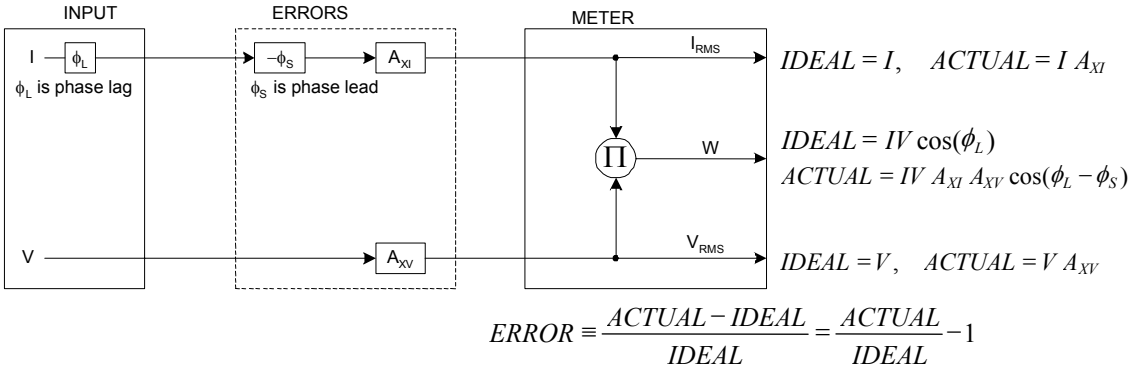


Figure 2-1: Watt Meter with Gain and Phase Errors.

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.

2.1.1 CALIBRATION WITH THREE MEASUREMENTS

The simplest calibration method is to make three measurements. Typically, a voltage measurement and two Watt-hour (Wh) measurements are made. A voltage display can be obtained for test purposes via the command >**MR2.1** in the serial interface.

Let's say the voltage measurement has the error E_V and the two Wh measurements have errors E_0 and E_{60}, where E_0 is measured with $\phi_L = 0$ and E_{60} is measured with $\phi_L = 60$. These values should be simple ratios—not percentage values. They should be zero when the meter is accurate and negative when the meter runs slow. The fundamental frequency is f_0. T is equal to $1/f_S$, where f_S is the sample frequency (2560.62Hz). Set all calibration factors to nominal: *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

From the voltage measurement, we determine that

1.➔ $$A_{XV} = E_V + 1$$

We use the other two measurements to determine ϕ_S and A_{XI}.

2. $$E_0 = \frac{IV\ A_{XV}\ A_{XI}\cos(0-\phi_S)}{IV\cos(0)} - 1 = A_{XV}\ A_{XI}\cos(\phi_S) - 1$$

2a. $$A_{XV}A_{XI} = \frac{E_0 + 1}{\cos(\phi_S)}$$

3. $$E_{60} = \frac{IV\ A_{XV}\ A_{XI}\cos(60-\phi_S)}{IV\cos(60)} - 1 = A_{XV}\ A_{XI}\frac{\cos(60-\phi_S)}{\cos(60)} - 1$$

3a. $$E_{60} = \frac{A_{XV}A_{XI}\left[\cos(60)\cos(\phi_S) + \sin(60)\sin(\phi_S)\right]}{\cos(60)} - 1$$

$$= A_{XV}A_{XI}\cos(\phi_S) + A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$$

Combining 2a and 3a:

4. $$E_{60} = E_0 + (E_0 + 1)\tan(60)\tan(\phi_S)$$

5. $$\tan(\phi_S) = \frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}$$

6.➔ $$\phi_S = \tan^{-1}\left(\frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}\right)$$

and from 2a:

7.➔ $$A_{XI} = \frac{E_0 + 1}{A_{XV}\cos(\phi_S)}$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1 + \frac{2^{-20} PHADJ(2 + 2^{-20} PHADJ - 2(1 - 2^{-9})\cos(2\pi f_0 T))}{1 - 2(1 - 2^{-9})\cos(2\pi f_0 T) + (1 - 2^{-9})^2}}}$$

2.1.2 CALIBRATION WITH FIVE MEASUREMENTS

The five measurement method provides more orthogonality between the gain and phase error derivations. This method involves measuring E_V, E_0, E_{180}, E_{60}, and E_{300}. Again, set all calibration factors to nominal, i.e. *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

First, calculate A_{XV} from E_V:

1.➔ $$A_{XV} = E_V + 1$$

Calculate A_{XI} from E_0 and E_{180}:

2. $$E_0 = \frac{IV\ A_{XV}\ A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\ A_{XI} \cos(\phi_S) - 1$$

3. $$E_{180} = \frac{IV\ A_{XV}\ A_{XI} \cos(180 - \phi_S)}{IV \cos(180)} - 1 = A_{XV}\ A_{XI} \cos(\phi_S) - 1$$

4. $$E_0 + E_{180} = 2A_{XV} A_{XI} \cos(\phi_S) - 2$$

5. $$A_{XV} A_{XI} = \frac{E_0 + E_{180} + 2}{2\cos(\phi_S)}$$

6.➔ $$A_{XI} = \frac{(E_0 + E_{180})/2 + 1}{A_{XV} \cos(\phi_S)}$$

Use above results along with E_{60} and E_{300} to calculate ϕ_S.

7. $$E_{60} = \frac{IV\ A_{XV}\ A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1$$

$$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60) \sin(\phi_S) - 1$$

8. $$E_{300} = \frac{IV\ A_{XV}\ A_{XI} \cos(-60 - \phi_S)}{IV \cos(-60)} - 1$$

$$= A_{XV} A_{XI} \cos(\phi_S) - A_{XV} A_{XI} \tan(60) \sin(\phi_S) - 1$$

Subtract 8 from 7

9. $$E_{60} - E_{300} = 2A_{XV} A_{XI} \tan(60) \sin(\phi_S)$$

use equation 5:

10. $$E_{60} - E_{300} = \frac{E_0 + E_{180} + 2}{\cos(\phi_S)} \tan(60) \sin(\phi_S)$$

11. $$E_{60} - E_{300} = (E_0 + E_{180} + 2) \tan(60) \tan(\phi_S)$$

12.➔ $$\phi_S = \tan^{-1}\left(\frac{(E_{60} - E_{300})}{\tan(60)(E_0 + E_{180} + 2)} \right)$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1 - 2^{-9})^2 - 2(1 - 2^{-9})\cos(2\pi f_0 T)\right]}{(1 - 2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1 - 2^{-9})\cos(2\pi f_0 T)\right]} \right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1 + \frac{2^{-20} PHADJ(2 + 2^{-20} PHADJ - 2(1 - 2^{-9})\cos(2\pi f_0 T))}{1 - 2(1 - 2^{-9})\cos(2\pi f_0 T) + (1 - 2^{-9})^2}}}$$

2.2 CALIBRATION PROCEDURES

Calibration requires that a calibration system is used, i.e. equipment that applies accurate voltage, load current and load angle to the unit being calibrated, while measuring the response from the unit being calibrated in a repeatable way. By repeatable we mean that the calibration system is synchronized to the meter being calibrated. Best results are achieved when the first pulse from the meter opens the measurement window of the calibration system. This mode of operation is opposed to a calibrator that opens the measurement window at random time and that therefore may or may not catch certain pulses emitted by the meter.

It is essential for a valid meter calibration to have the voltage stabilized a few seconds before the current is applied. This enables the Demo Code to initialize the 71M6511/6511H and to stabilize the PLLs and filters in the CE. This method of operation is consistent with meter applications in the field as well as with metering standards.

Each meter phase must be calibrated individually. The procedures below show how to calibrate a meter phase with either three or five measurements. The PHADJ equations apply only when a current transformer is used for the phase in question. Note that positive load angles correspond to lagging current (see Figure 2-2).

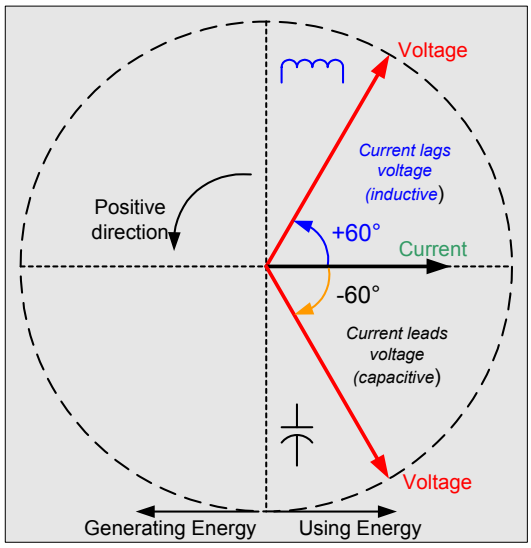


Figure 2-2: Phase Angle Definitions

The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6511/6511H chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 71M6511/6511H, is scaled to be less than 250mV (peak).

2.2.1 CALIBRATION PROCEDURE WITH THREE MEASUREMENTS

The calibration procedure is as follows:

1) All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.

2) An RMS voltage V_{ideal} consistent with the meter's nominal voltage is applied, and the RMS reading V_{actual} of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$

3) Apply the nominal load current at phase angles 0° and 60°, measure the Wh energy and record the errors E_0 and E_{60}.

4) Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.1 or using the spreadsheet presented in section 2.2.3.

5) Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.

6) Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.

7) Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the flash memory of the meter. If the calibration is performed on a TERIDIAN Demo Board, the methods shown in sections 1.9.3 and 1.9.3 can be used.

8) For added temperature compensation, read the value in CE RAM location 0x54 and write it to CE RAM location 0x11. If Demo Code 3.05 or later is used, this will automatically calculate the correction coefficients PPMC and PPMC2 from the nominal temperature entered in CE location 0x11 and from the characterization data contained in the on-chip fuses.

2.2.2 CALIBRATION PROCEDURE WITH FIVE MEASUREMENTS

The calibration procedure is as follows:

1) All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.

2) An RMS voltage V_{ideal} consistent with the meter's nominal voltage is applied, and the RMS reading V_{actual} of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$

3) Apply the nominal load current at phase angles 0°, 60°, 180° and –60° (-300°). Measure the Wh energy each time and record the errors E_0, E_{60}, E_{180}, and E_{300}.

4) Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.2 or using the spreadsheet presented in section 2.2.3.

5) Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.

6) Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.

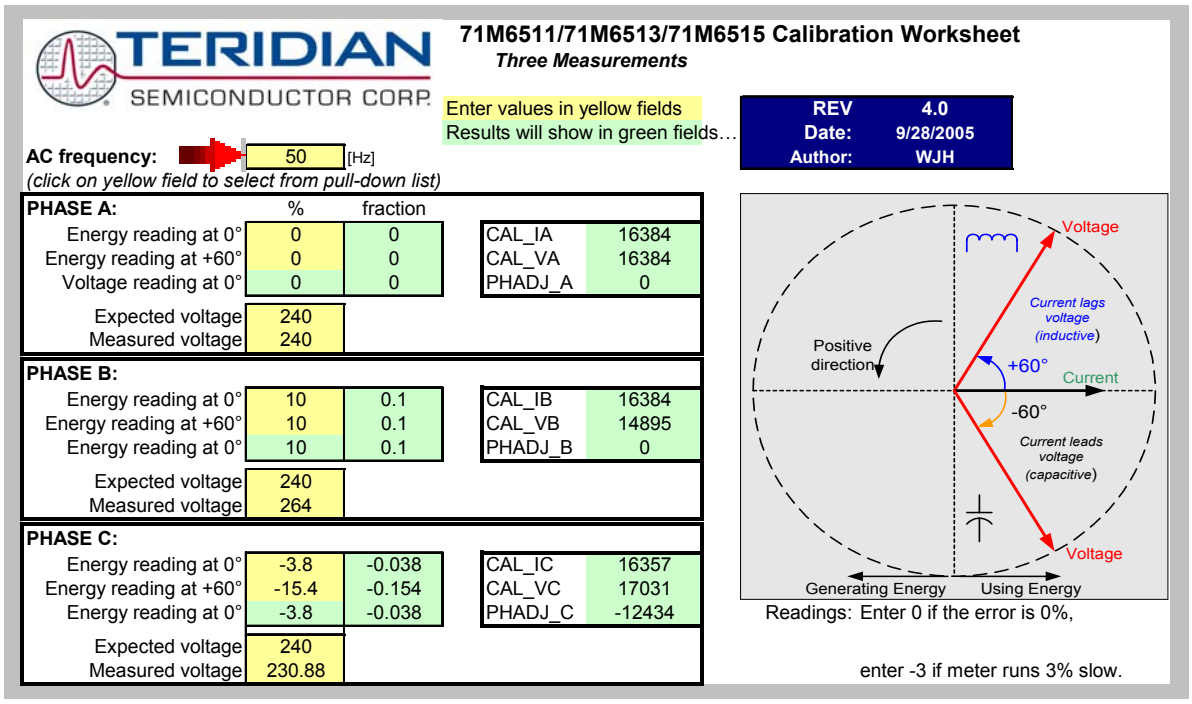
7) Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the flash memory of the meter. If the calibration is performed on a TERIDIAN Demo Board, the methods shown in sections 1.9.3 and 1.9.3 can be used.

8) For added temperature compensation, read the value in CE RAM location 0x54 and write it to CE RAM location 0x11. If Demo Code 3.05 or later is used, this will automatically calculate the correction coefficients PPMC and PPMC2 from the nominal temperature entered in CE location 0x11 and from the characterization data contained in the on-chip fuses.

2.2.3 CALIBRATION SPREADSHEETS

Calibration spreadsheets are available from TERIDIAN Semiconductor. They are also included in the CD-ROM shipped with any Demo Kit. Figure 2-3 shows the spreadsheet for three measurements with three phases in use (only one phase needs to be used for the 71M6511/6511H chip).

Figure 2-3 shows the spreadsheet for five measurements with three phases (only one phase needs to be used for the 71M6511/6511H chip).



TERIDIAN SEMICONDUCTOR CORP.

71M6511/71M6513/71M6515 Calibration Worksheet

Three Measurements

Enter values in yellow fields
Results will show in green fields…

REV	4.0
Date:	9/28/2005
Author:	WJH

AC frequency: 50 [Hz]
(click on yellow field to select from pull-down list)

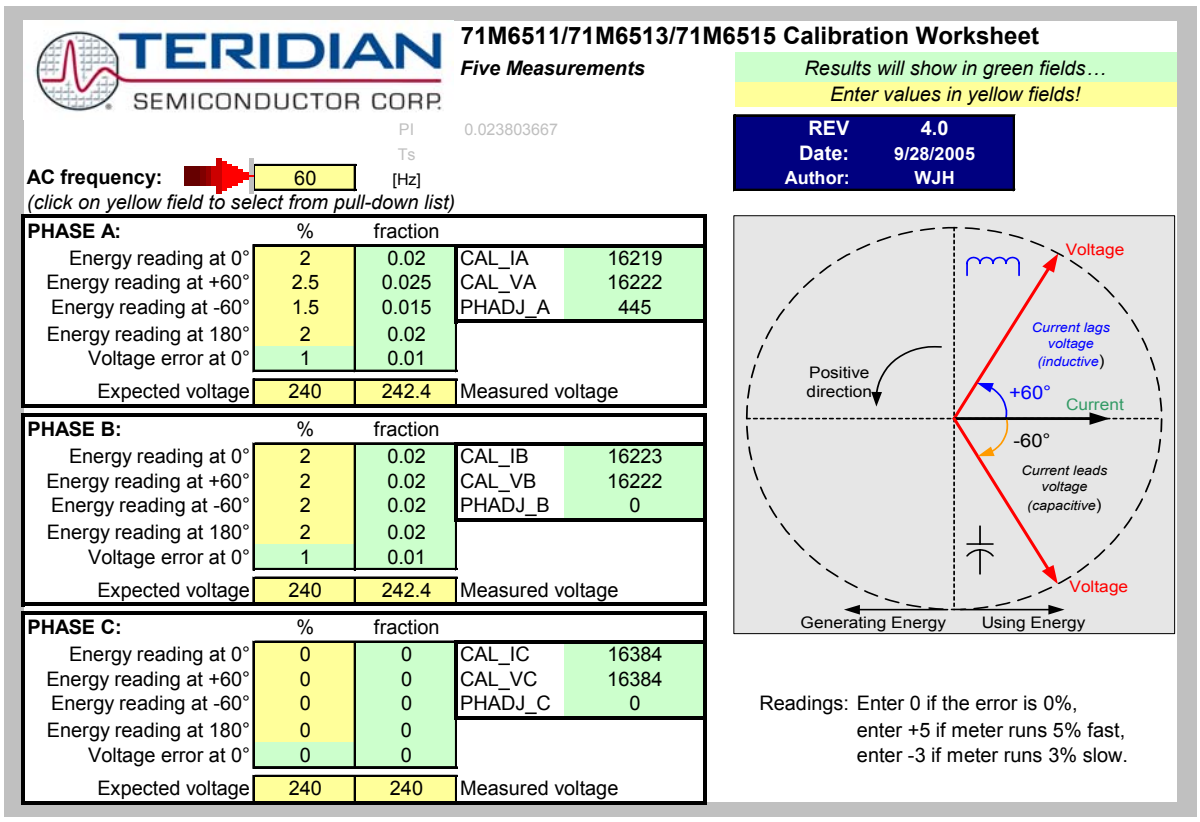
PHASE A:	%	fraction		
Energy reading at 0°	0	0	CAL_IA	16384
Energy reading at +60°	0	0	CAL_VA	16384
Voltage reading at 0°	0	0	PHADJ_A	0
Expected voltage	240			
Measured voltage	240			

PHASE B:				
Energy reading at 0°	10	0.1	CAL_IB	16384
Energy reading at +60°	10	0.1	CAL_VB	14895
Energy reading at 0°	10	0.1	PHADJ_B	0
Expected voltage	240			
Measured voltage	264			

PHASE C:				
Energy reading at 0°	-3.8	-0.038	CAL_IC	16357
Energy reading at +60°	-15.4	-0.154	CAL_VC	17031
Energy reading at 0°	-3.8	-0.038	PHADJ_C	-12434
Expected voltage	240			
Measured voltage	230.88			

Readings: Enter 0 if the error is 0%,
enter -3 if meter runs 3% slow.

Figure 2-3: Calibration Spreadsheet for Three Measurements



TERIDIAN SEMICONDUCTOR CORP.

71M6511/71M6513/71M6515 Calibration Worksheet

Five Measurements

Results will show in green fields…
Enter values in yellow fields!

PI 0.023803667
Ts

REV	4.0
Date:	9/28/2005
Author:	WJH

AC frequency: 60 [Hz]
(click on yellow field to select from pull-down list)

PHASE A:	%	fraction		
Energy reading at 0°	2	0.02	CAL_IA	16219
Energy reading at +60°	2.5	0.025	CAL_VA	16222
Energy reading at -60°	1.5	0.015	PHADJ_A	445
Energy reading at 180°	2	0.02		
Voltage error at 0°	1	0.01		
Expected voltage	240	242.4	Measured voltage	

PHASE B:	%	fraction		
Energy reading at 0°	2	0.02	CAL_IB	16223
Energy reading at +60°	2	0.02	CAL_VB	16222
Energy reading at -60°	2	0.02	PHADJ_B	0
Energy reading at 180°	2	0.02		
Voltage error at 0°	1	0.01		
Expected voltage	240	242.4	Measured voltage	

PHASE C:	%	fraction		
Energy reading at 0°	0	0	CAL_IC	16384
Energy reading at +60°	0	0	CAL_VC	16384
Energy reading at -60°	0	0	PHADJ_C	0
Energy reading at 180°	0	0		
Voltage error at 0°	0	0		
Expected voltage	240	240	Measured voltage	

Readings: Enter 0 if the error is 0%,
enter +5 if meter runs 5% fast,
enter -3 if meter runs 3% slow.

Figure 2-4: Calibration Spreadsheet for Five Measurements

2.2.4 COMPENSATING FOR NON-LINEARITIES

Nonlinearity is most noticeable at low currents, as shown in Figure 2-5, and can result from input noise and truncation. Nonlinearities can be eliminated using the *QUANT* variable.

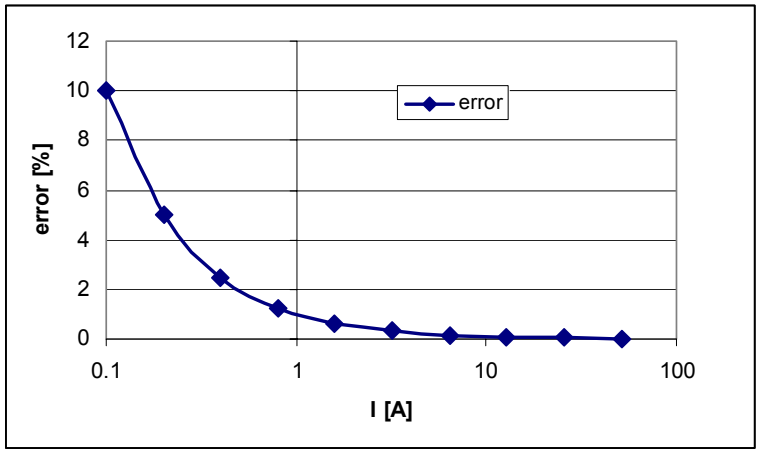


Figure 2-5: Non-Linearity Caused by Quantification Noise

The error can be seen as the presence of a virtual constant noise current. While 10mA hardly contribute any error at currents of 10A and above, the noise becomes dominant at small currents.

The value to be used for QUANT can be determined by the following formula:

$$QUANT = -\frac{\frac{error}{100} V \cdot I}{VMAX \cdot IMAX \cdot LSB}$$

Where error = observed error at a given RMS voltage (V) and RMS current (I),
VMAX = voltage scaling factor, as described in section 1.8,
IMAX = current scaling factor, as described in section 1.8,
LSB = QUANT LSB value = $7.4162*10^{-10}$W

Example: Assuming an observed error as in Figure 2-5, we determine the error at 1A RMS to be +1%. If VMAX is 600V and IMAX = 208A, and if the measurement was taken at 240V RMS, we determine QUANT as follows:

$$QUANT = -\frac{\frac{1 \cdot 240 \cdot 1}{100}}{600 \cdot 208 \cdot 7.4162 \cdot 10^{-10}} = -11339$$

QUANT is to be written to the CE location 0x2F. It does not matter which current value is chosen as long as the corresponding error value is significant (5% error at 0.2A used in the above equation will produce the same result for *QUANT*).

Input noise and truncation can cause similar errors in the VAR calculation that can be eliminated using the *QUANT_VAR* variable. *QUANT_VAR* is determined using the same formula as *QUANT*.

2.2.5 CALIBRATING METERS WITH COMBINED CT AND SHUNT RESISTOR

In many cases it is desirable to discourage tampering by using two current sensors. Simple tampering methods based on connecting the low side of the load to earth ground (neutral) can be detected by adding a second current sensor in the neutral path, as shown in Figure 2-6.

In this configuration, the shunt resistor is connected to the IA channel while the current transformer is connected to the IB channel of the 71M6511.

Calibrating this arrangement requires a few extra steps above the regular calibration. The calibration procedure applies to the sensor arrangement described above (SHUNT = IA, CT = IB) and Demo Code 3.04.

Preparation:

1. Set the meter equation field of the configuration RAM for *EQU* to zero using the command:

   RI0=10 // *EQU* = 0; *CE_EN* =1; *TMUX* = 0;

2. For the sake of calculation, individual *WRATE* parameters for Pulse generation, i.e. *WRATE_SHUNT* and *WRATE_CT* will be used.

3. It is also necessary to compute and estimate *IMAX_SHUNT* and *IMAX_CT* parameters for meter billing purposes.

4. Using *IMAX_SHUNT* and *VMAX*, the energy calculations for channel A should be performed.

5. The energy calculations for channel B should be performed using *IMAX_CT* and *VMAX*.

6. The LSB values for measurements for *W0SUM, W1SUM, VAR0SUM, VAR1SUM, I0SQSUM, I1SQSUM, and V0SQSUM* should be modified to compute the correct energy values. That is, *IMAX_SHUNT* and *IMAX_CT* should be applied separately to individual channels based on the sensor connections.

7. Before starting a calibration, all calibration factors must be in their default state, i.e. *CAL_IA* (0x08), *CAL_VA* (0x09), *CAL_IB* (0x0A) must be +16384. *PHADJ_A* (0x0E) and *PHADJ_B* (0x0F) should be zero.

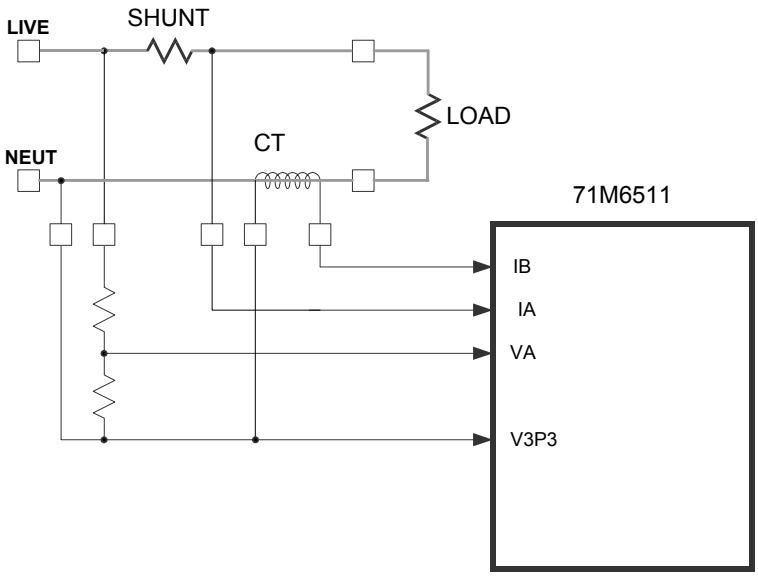


Figure 2-6: 71M6511 with Shunt and CT

The calibration procedure, using Demo Code revision 3.04, is as follows:

Calibrating for Shunt Resistor (Channel A):

1. Calculate *IMAX* for the shunt resistor (*IMAX_SHUNT*). This can be done by using the following formula:

   IMAX_SHUNT = Vi_{MAX}/R_{SH}

   The Vi_{MAX} value is the maximum analog input voltage for the channel, typically 177mV (RMS), and R_{SH} is the resistance value of the shunt resistor.
   The value obtained for *IMAX_SHUNT* is stored at the MPU address 0x0A, using the CLI command
)A= *IMAX_SHUNT*

2. Compute *WRATE_SHUNT* based on *IMAX_SHUNT* and *VMAX* and the formula given in 1.8.2:

   WRATE_SHUNT = (*IMAX_SHUNT* * VMAX * 47.1132) / (Kh * In_8 * N_{ACC} * X)

   Use *VMAX* = 600V (RMS) for the 6511 Demo Board if the resistor divider for VA has not been changed.

3. Update the *WRATE* register (at CE address 0x2D) with *WRATE_SHUNT*, using the command **]2D=** *WRATE_SHUNT.*

4. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

5. Apply the error values to the calibration spreadsheet (revision 2.0 or later) and determine the calibration factors for channel A, i.e. *CAL_IA*, *CAL_VA*, and *PHADJ_A*.

6. Update the CE registers 0x08, 0x09 and 0x0E of the compute engine with the calibration factors obtained from the spreadsheet, using the commands **]8=***CAL_IA*, **]9=***CAL_VA*, and **]E=***PHADJ_A*.

7. Retest for accuracy at several currents and phase angles.

At this point, channel A is calibrated. WSUM will be based on the voltage applied to the meter and the current flowing through the shunt resistor. The pulses generated will be based on the parameters entered for channel A.

Calibration for CT (Channel B):

1. Compute *IMAX* for the CT channel (*IMAX_CT*), based on the CT turns ratio N and the termination resistor value R_T using the formula:

   IMAX_CT = 177mV* N / R_T

   This value is used in the following step as *IMAX_CT*.

2. Compute *WRATE_CT* based on the values obtained for *IMAX_CT* and the formula given in 1.8.2:

   WRATE_CT = (*IMAX_CT* * VMAX * 47.1132) / (Kh * In_8 * N_{ACC} * X)

3. Update the *WRATE* register (CE address 0x2D) with *WRATE_CT*, using the command **]2D=** *WRATE_CT.*

4. Enter the command **>)7=2**. Configure *W1SUM* as external pulse source since the CT is connected to Channel 1 for VA*IB.

5. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

6. Apply these values to the calibration spread sheet (revision 4.0 or later) and derive the calibration factor *PHADJ_B*.

7. Update only the CE address 0x0F with the value for *PHADJ_B* using the command **]F=** *PHADJ_B.*

8. Adjust *CAL_IB* for the total error found in the accuracy test using the formula

   CAL_IB = 16384 * (1 - error/100)

   That is, if the chip reports an error of -2.5%, *CAL_IB* should be adjusted to a value of

   (16384 * (1 - (-2.5/100)).

9. Since *CAL_VA* and CAL_IA have already been adjusted for channel A, these registers should not be updated.

10. Retest for accuracy at several currents and phase angles.

After completing the calibration, the energy values W0SUM, based on VA*IA and W1SUM, based on VA*IB are accessible to the MPU firmware. The pulse rate is controlled by W1SUM and determined by the parameters selected for the CT channel (VA, IB). Differences between W0SUM and W1SUM, indicating tampering, can be detected by the MPU for each accumulation interval.

The user has to customize the Demo Code to utilize the values obtained from the VA, IA, and IB channels for proper calculation of tariffs.

Table 2-1 summarizes the important parameters used in the calibration procedure.

Channel, Sensor	Formulae	I Measurement Using	Parameters	W Pulse Generation	VAR Pulse Generation
A, Shunt Resistor	WASUM = VA*IA VARASUM = VA*IA	IMAX_SHUNT	IMAX = IMAX_SHUNT WRATE = WRATE_SHUNT	WASUM	VARASUM
B, CT	WBSUM = VA*IB VARBSUM = VA*IB	IMAX_SHUNT	IMAX = IMAX_CT WRATE = WRATE_CT	WBSUM	VARBSUM

Table 2-1: Calibration Summary

In Demo Code revision 3.05, the calibration procedure is simplified since separate IMAX parameters for both channels are available. The calibration procedure, is as follows:

Calibrating for Shunt Resistor (Channel A):

1. Calculate *IMAX* for the shunt resistor (*IMAX_SHUNT*). This can be done by using the following formula:

   IMAX_SHUNT = Vi_{MAX}/R_{SH}

   The Vi_{MAX} value is the maximum analog input voltage for the channel, typically 177mV (RMS), and R_{SH} is the resistance value of the shunt resistor.
   The value obtained for *IMAX_SHUNT* is stored at the MPU address 0x0A, using the CLI command
)A= *IMAX_SHUNT*

2. Compute *WRATE_SHUNT* based on *IMAX_SHUNT* and *VMAX* and the formula given in 1.8.2:

   WRATE_SHUNT = (*IMAX_SHUNT* * VMAX * 47.1132) / (Kh * In_8 * N_{ACC} * X)

   Use *VMAX* = 600V (RMS) for the 6511 Demo Board if the resistor divider for VA has not been changed.

3. Update the *WRATE* register (at CE address 0x2D) with *WRATE_SHUNT*, using the command
   ]2D= *WRATE_SHUNT.*

4. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

5. Apply the error values to the calibration spreadsheet (revision 4.0 or later) and determine the calibration factors for channel A, i.e. *CAL_IA*, *CAL_VA*, and *PHADJ_A*.

6. Update the CE registers 0x08, 0x09 and 0x0E of the compute engine with the calibration factors obtained from the spreadsheet, using the commands]8=*CAL_IA*,]9=*CAL_VA*, and]E=*PHADJ_A*.

7. Retest for accuracy at several currents and phase angles.

At this point, channel A is calibrated. WSUM will be based on the voltage applied to the meter and the current flowing through the shunt resistor. The pulses generated will be based on the parameters entered for channel A.

Calibration for CT (Channel B):

1. Compute *IMAX* for the CT channel (*IMAX_CT*), based on the CT turns ratio N and the termination resistor value R_T using the formula:

   IMAX_CT = 177mV* N / R_T

   Store the value obtained for *IMAX_CT* at the MPU address 0x2B (IMAX2), using the CLI command)2B= *IMAX_CT*. This value is used in the following step as *IMAX_CT*.

2. Compute *WRATE_CT* based on the values obtained for *IMAX_CT* and the formula given in 1.8.2:

   WRATE_CT = (*IMAX_CT* * VMAX * 47.1132) / (Kh * In_8 * N_{ACC} * X)

3. Update the *WRATE* register (CE address 0x2D) with *WRATE_CT*, using the command]2D= *WRATE_CT*.

4. Enter the command >)7=2 to configure *W1SUM* as the external pulse source, since the CT is connected to Channel 1 for VA*IB.

5. Test channel B for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

6. Apply the error values to the calibration spread sheet (revision 4.0 or later) and derive the calibration factor *PHADJ_B*.

7. Update only the CE address 0x0F with the value for *PHADJ_B* using the command]F= *PHADJ_B*.

8. Adjust *CAL_IB* for the total error found in the accuracy test using the formula

   CAL_IB = 16384 * (1 - error/100)

9. Since *CAL_VA* and *CAL_IA* have already been adjusted for channel A, these registers should not be updated.

10. Retest channel B for accuracy at several currents and phase angles.

After completing the calibration, the energy values W0SUM, based on VA*IA and W1SUM, based on VA*IB are accessible to the MPU firmware. The pulse rate is controlled by W1SUM and determined by the parameters selected for the CT channel (VA, IB). Differences between W0SUM and W1SUM, indicating tampering, can be detected by the MPU for each accumulation interval.

The user has to customize the Demo Code to utilize the values obtained from the VA, IA, and IB channels for proper calculation of tariffs.

Table 2-2 summarizes the important parameters used in the calibration procedure.

Channel, Sensor	Formulae	I Measurement Using	Parameters	W Pulse Generation	VAR Pulse Generation
A, Shunt Resistor	WASUM = VA*IA VARASUM = VA*IA	IMAX_SHUNT	IMAX = IMAX_SHUNT WRATE = WRATE_SHUNT	WASUM	VARASUM
B, CT	WBSUM = VA*IB VARBSUM = VA*IB	IMAX_CT	IMAX = IMAX_CT WRATE = WRATE_CT	WBSUM	VARBSUM

Table 2-2: Calibration Summary

Due to Demo Code revision 3.05 offering separate IMAX parameters for channels A and B it is possible to define individual creep settings for each channel (see section 1.10.2 for details).

2.3 POWER SAVING MEASURES

In many cases, especially when operating the TERIDIAN 71M6511/71M6511H from a battery, it is desirable to reduce the power consumed by the chip to a minimum. This can be achieved with the measures listed in Table 2-3.

Power Saving Measure	Software Control	Typical Savings
Disable the CE	*CE_EN* = 0	0.16mA
Disable the ADC	*ADC_DIS* = 1	1.8mA
Disable clock test output CKTEST	*CKOUTDIS* = 1	0.6mA
Disable emulator clock	*ECK_DIS* = 1	0.1mA
Set flash read pulse timing to 33 ns	*FLASH66Z* =1	0.04mA
Disable the LCD voltage boost circuitry	*LCD_BSTEN* = 0	0.9mA
Disable RTM outputs	*RTM_EN* = 0	0.01mA
Disable SSI output	*SSI_EN* = 0	
Select DGND for the multiplexer input	*TMUX*[3:0] = 0	
Disable reference voltage output	*VREF_DIS* = 1	
Reduce the clock for the MPU	*MPU_DIV* = 5	0.4mA/MHz

Table 2-3: Power Saving Measures

2.4 SCHEMATIC INFORMATION

In this section, hints on proper schematic design are provided that will help designing circuits that are functional and sufficiently immune to EMI (electromagnetic interference).

2.4.1 COMPONENTS FOR THE V1 PIN

The V1 pin of the 71M6511/6511H can never be left unconnected.

A voltage divider should be used to establish that V1 is in a safe range when the meter is in mission mode (V1 must be lower than 2.9V in all cases in order to keep the hardware watchdog timer enabled). For proper debugging or loading code into the 71M6513 mounted on a PCB, it is necessary to have a provision like the header JP1 shown above R1 in Figure 2-7. A shorting jumper on this header pulls V1 up to V3P3 disabling the hardware watchdog timer.

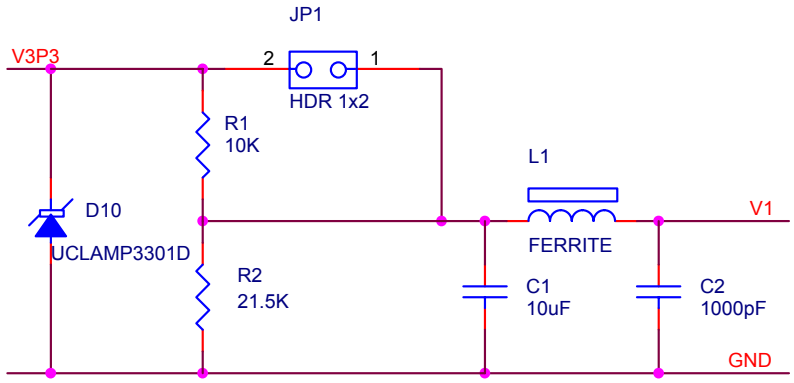


Figure 2-7: Voltage Divider for V1

On the 6511 Demo Boards this feature is implemented with resistors R83/R86, capacitor C34 (2-Layer Demo Board only) and TP10. See the board schematics in the Appendix for details.

2.4.2 RESET CIRCUIT

Even though a functional meter will not necessarily need a reset switch, the 71M6511 Demo Boards provide a reset pushbutton that can be used when prototyping and debugging software. When a circuit is used in an EMI environment, the RESETZ pin should be supported by the external components shown in Figure 2-8. R_1 should be in the range of 200Ω, R_2 should be around 10Ω. The capacitor C_1 should be 1nF. R1 and C1 should be mounted as close as possible to the IC. In cases where the trace from the pushbutton switch to the RESETZ pin poses a problem, R_2 can be removed.

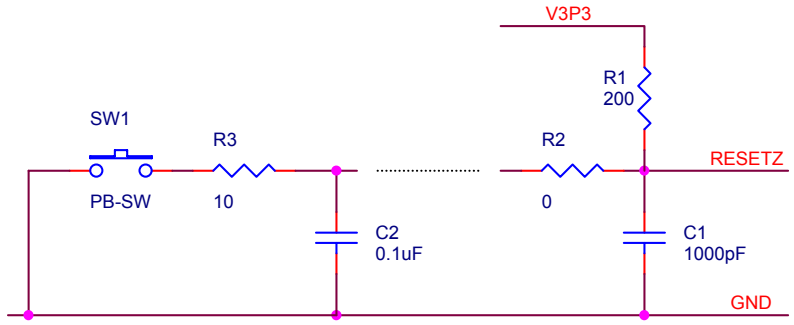


Figure 2-8: External Components for RESETZ

2.4.3 OSCILLATOR

The oscillator of the 71M6511 drives a standard 32.768kHz watch crystal (see Figure 2-9). Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the 71M6511 has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT pin.

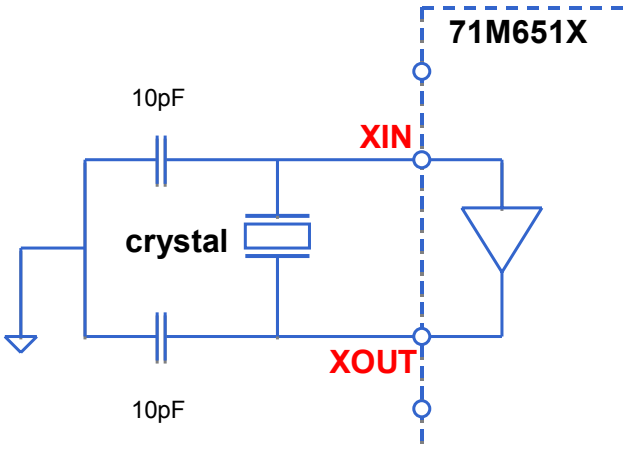


Figure 2-9: Oscillator Circuit

It is not necessary to place an external resistor across the crystal, i.e. R91 on the 4-Layer Demo Board must not be populated.

Capacitor values for the crystal must be <15pF.

2.4.4 EEPROM

EEPROMs should be connected to the pins DIO4 and DIO5 (see Figure 2-10). These pins can be switched from regular DIO to implement an I2C interface by setting the I/O RAM register DIO_EEX (0x2008[4]) to 1. Pull-up resistors of 3kΩ must be provided for both the SCL and SDA signals.

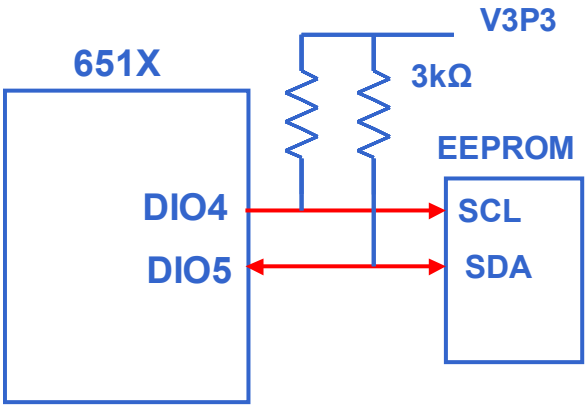


Figure 2-10: EEPROM Circuit

2.4.5 LCD

The 71M6511 has an on-chip LCD controller capable of controlling static or multiplexed LCDs. Figure 2-11 shows the basic connection for LCDs. Note that the LCD module itself has no power connection.

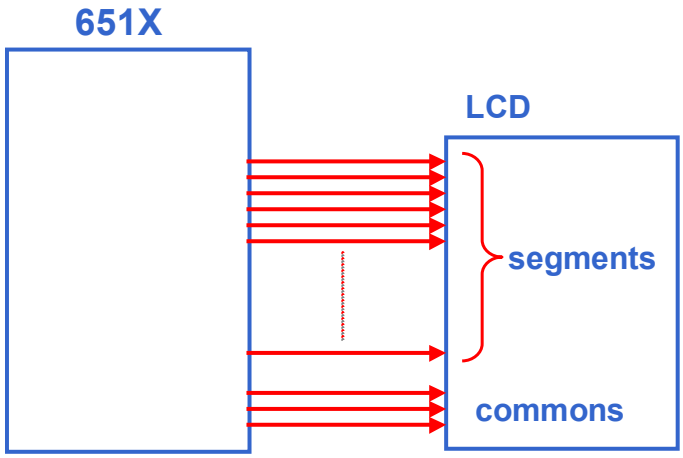


Figure 2-11: LCD Connections

Figure 2-12 shows how 5V LCDs can be operated even when a 5V supply is not available. Setting the I/O RAM register *LCD_BSTEN* to 1 starts the on-chip boost circuitry that will output an AC frequency on the VDRV pin. Using a small coupling capacitor, two general-purpose diodes and a reservoir capacitor, a 5VDC voltage is generated which can be fed back into the VLCD pin of the 71M6511. The LCD drivers are enabled with the I/O register *LCD_ON*; I/O register *LCD_FS* is used to adjust contrast, and *LCD_MODE* selects the operation mode (LCD type).

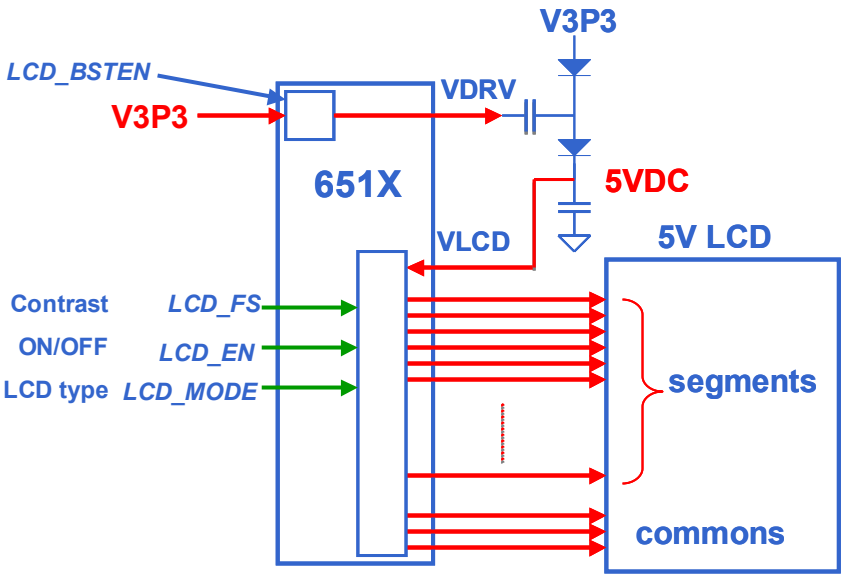


Figure 2-12: LCD Boost and LCD Control Registers

2.4.6 OPTICAL INTERFACE

The 71M6511 IC is equipped with two pins supporting the optical interface: OPT_TX and OPT_RX. The OPT_TX pin can be used to drive a visual or IR light LED with up to 20mA, a series resistor (R_2 in Figure 2-13) helps limiting the current). The OPT_RX pin can be connected to the collector of a photo-transistor, as shown in Figure 2-13.

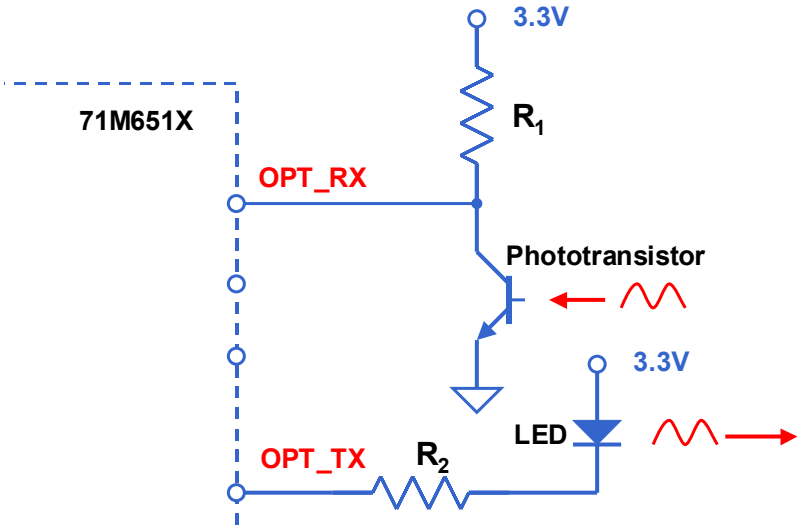


Figure 2-13: Optical Interface Block Diagram

On the 4-Layer Demo Boards, the current limiting resistor R79 is provided in between the OPT_TX pin of the chip and pin 2 of J12 (Figure 2-14). C21 on these boards should be shorted to create a DC path from the collector of the photo-transistor to the OPT_RX pin.

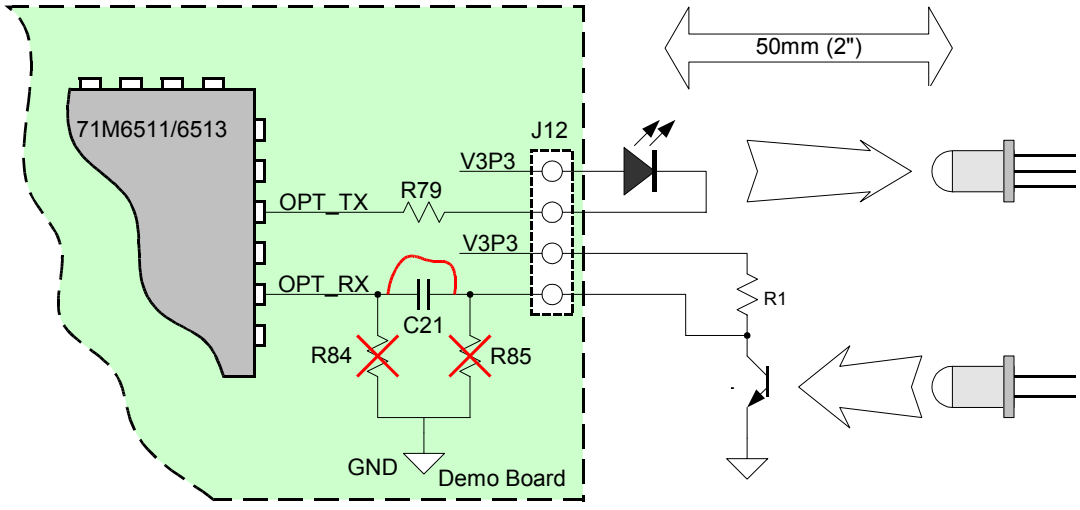


Figure 2-14: Optical Port Circuitry on the 4-Layer Demo Board

The IR diode should be connected between terminal 2 of header J12 on the Demo Board (cathode) and the V3P3 voltage (anode), which is accessible at terminal 1 of header J12 (see Figure 2-14). The value of R79 may be increased or decreased in order to vary the diode current. R84 and R85 should be removed when operating the photo-transistor in the configuration shown.

J12 on the 2-Layer Demo Boards has all the provisions for connecting the IR LED and photo-transistor (see Figure 2-15). Depending on the required LED current, R79 may have to be scaled. Similarly, R84 may be scaled or removed, depending on the current generated by the photo-transistor.

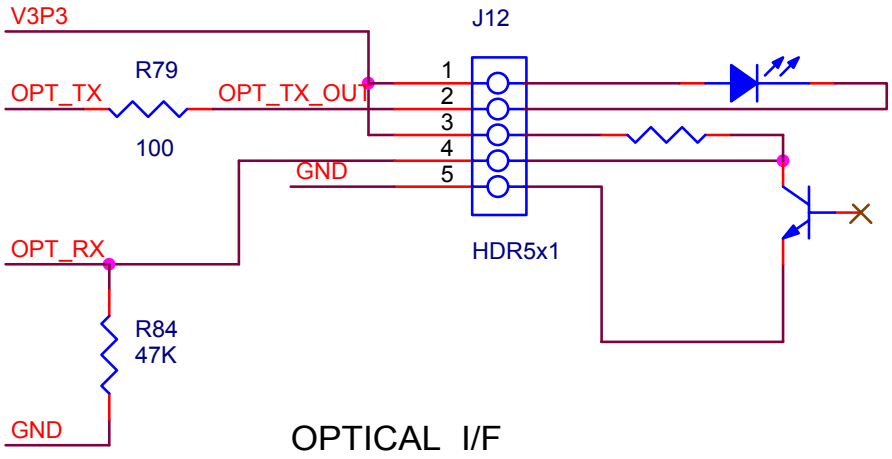


Figure 2-15: Optical Port Circuitry on the 2-Layer Demo Board

2.4.7 CONNECTING THE RX PIN

Due to unique circuitry on the RX input, its behavior is slightly different from the other digital inputs of the 651X family of metering ICs.

The Rx pin (serial port receive pin) of the 71M6511/6511H is internally clamped to the V3P3 supply as shown in Figure 2-16. This means, the voltage of signals applied to this pin will be clamped to V3P3D + 0.6V, i.e. nominally 3.9V. Note that this clamp voltage exceeds the 3.6V Absolute Maximum Rating of the RX input.

Inputs above 1.6V (V_{IL}) are guaranteed to be recognized as logic 1. Inputs below 0.8V (V_{IL}) are guaranteed to be recognized as logic 0. Input voltages between 0.8V and 1.6V must be avoided.

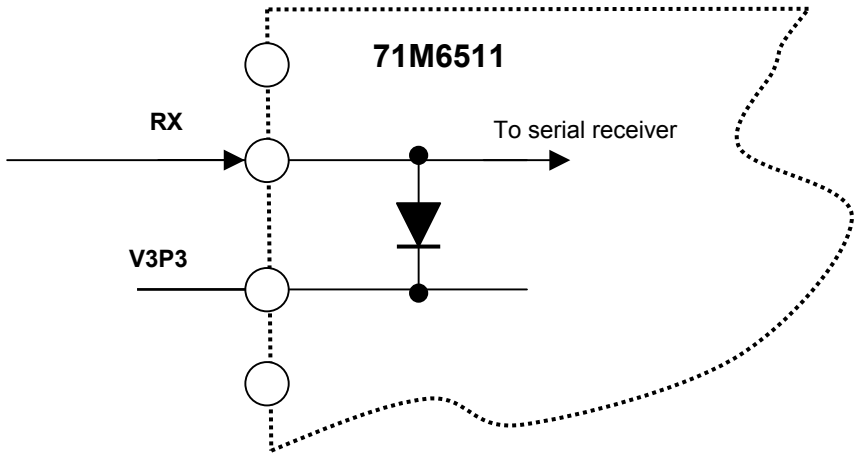


Figure 2-16: Internal Diode Clamp on the RX Pin

If inputs higher than 3.6V are expected at the RX pin, e.g. when interfacing to 5V-based driving circuitry such as RS-232 transceivers/receivers, TTL or CMOS logic, a resistor attenuator should be used in order to restrict the RX input voltage.

Figure 2-17 shows the recommended resistor network consisting of R1 (17kΩ) and R2 (33kΩ). This network scales the input voltage V_{IN} of 5.5V to 3.6V, and an input voltage of 2.5V will be scaled to 1.6V. For the low voltage level, V_{IN} voltages below 1.2V will be scaled to 0.8V. The maximum current at 5.5V input voltage is 5.5V/(50kΩ) + I_{IH} = 110µA + 1µA = 111µA.

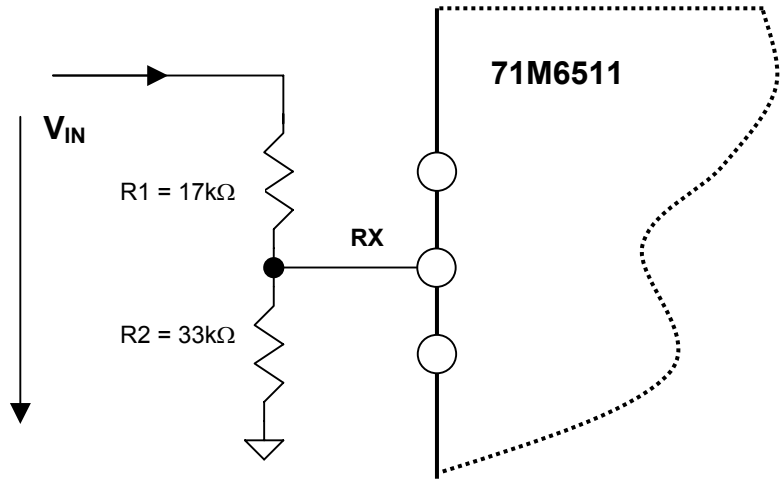


Figure 2-17: Resistor Network for RX

2.5 TESTING THE DEMO BOARD

This section will explain how the 71M6511/6511H IC and the peripherals can be tested. Hints given in this section will help evaluating the features of the Demo Board and understanding the IC and its peripherals.

2.5.1 FUNCTIONAL METER TEST

This is the test that every Demo Board has to pass before being integrated into a Demo Kit. Before going into the functional meter test, the Demo Board has already passed a series of bench-top tests, but the functional meter test is the first test that applies realistic high voltages (and current signals from current transformers) to the Demo Board.

Figure 2-18 shows a meter connected to a typical calibration system. The calibrator supplies calibrated voltage and current signals to the meter. It should be noted that the current flows through the CT or CTs that are not part of the Demo Board. The Demo Board rather receives the voltage output signals fro the CT. An optical pickup senses the pulses emitted by the meter and reports them to the calibrator. Some calibration systems have electrical pickups. The calibrator measures the time between the pulses and compares it to the expected time, based on the meter Kh and the applied power.

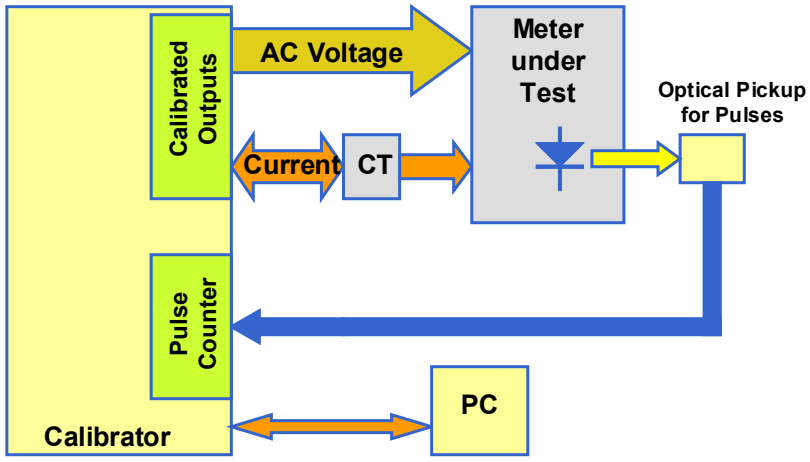


Figure 2-18: Meter with Calibration System

TERIDIAN Demo Boards are not calibrated prior to shipping. However, the Demo Board pulse outputs are tested and compared to the expected pulse output. Figure 2-19 shows the screen on the controlling PC for a typical Demo Board. The number in the red field under "As Found" represents the error measured for phase A, while the number in the red field under "As Left" represents the error measured for phase B. Both numbers are given in percent. This means that for the measured Demo Board, the sum of all errors resulting from tolerances of PCB components, CTs, and 71M6511/6511H tolerances was –2.8% and –3.8%, a range that can easily be compensated by calibration.

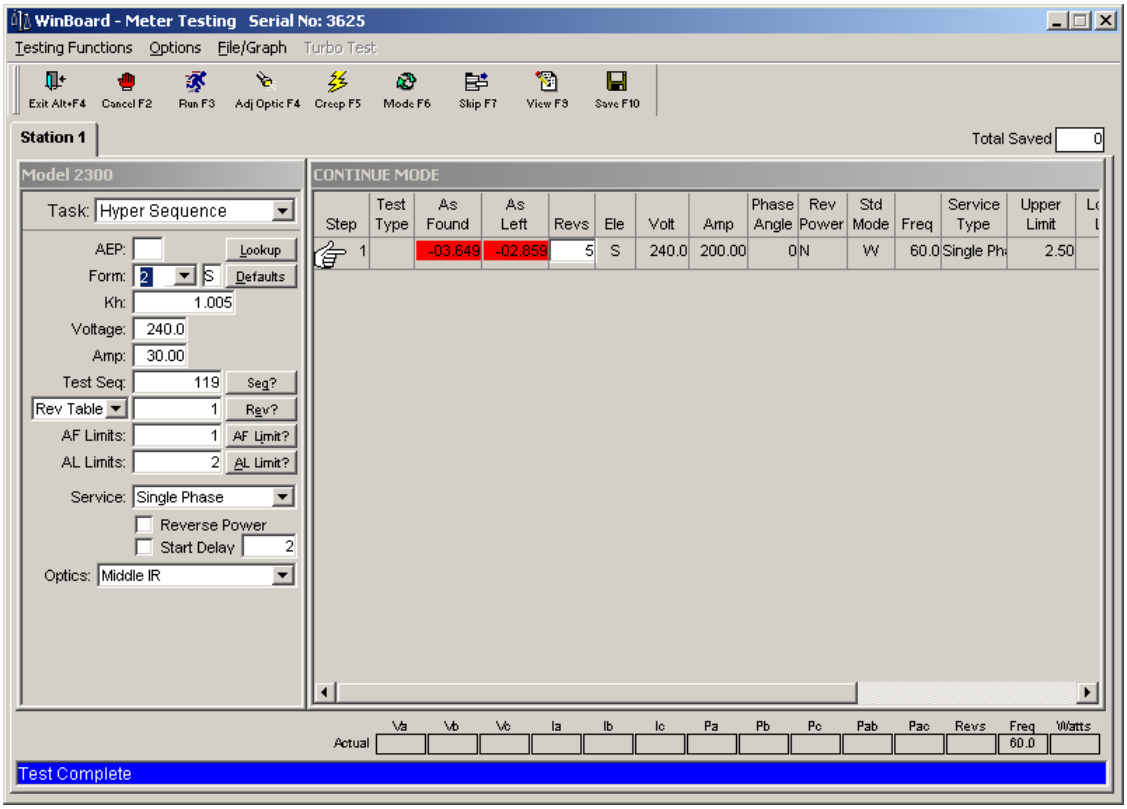


Figure 2-19: Calibration System Screen

2.5.2 EEPROM

Testing the EEPROM provided on the Demo Board is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To write a string of text characters to the EEPROM and read it back, we apply the following sequence of CLI commands:

>EEC1 Enables the EEPROM

>EESthis is a test Writes text to the buffer

>EET80 Writes buffer to address 80

Written to EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….

Response from Demo Code

>EER80.E Reads text from the buffer

Read from EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….

Response from Demo Code

>EEC0 Disables the EEPROM

2.5.3 RTC

Testing the RTC inside the 71M6511/6511H IC is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To set the RTC and check the time and date, we apply the following sequence of CLI commands:

>M10	LCD display to show calendar date
>RTD05.09.27.3	Sets the date to 9/27/2005 (Tuesday)
>M9	LCD display to show time of day
>RTT10.45.00	Sets the time to 10:45:00. AM/PM distinction: 1:22:33PM = 13:22:33

2.5.4 HARDWARE WATCHDOG TIMER

The hardware watchdog timer of the 71M6511/6511H is disabled when the voltage at the V1 pin is at 3.3V (V3P3). On the Demo Boards, this is done by plugging in a jumper at TP10 between the V1 and V3P3 pins.

Programming the flash memory or emulation using the ADM51 In-Circuit-Emulator can only be done when a jumper is plugged in at TP10 between V1 and V3P3.

Conversely, removing the jumper at TP10 will enable the hardware watchdog timer.

2.5.5 LCD

Various tests of the LCD interface can be performed with the Demo Board, using the serial command line interface (CLI):

The display outputs are enabled by setting the *LCD_EN* register to 1.

Register Name	Address [bits]	R/W	Description
LCD_EN	2021[5]	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs.

To access the *LCD_EN* register, we apply the following CLI commands:

>RI21$	Reads the hex value of register 0x2021
>25	Response from Demo Code indicating the bit 5 is set
>RI21=5	Writes the hex value 0x05 to register 0x2021 causing the display to be switched off
>RI21=25	Sets the *LCD_EN* register back to normal

The 71M6511/6511H provides a charge pump capable of boosting the 3.3VDC supply voltage up to 5.0VDC. The boost circuit is enabled with the *LCD_BSTEN* register. The 6511 Demo Boards have the boost circuit enabled by default.

Register Name	Address [bits]	R/W	Description
LCD_BSTEN	2020[7]	R/W	Enables the LCD voltage boost circuit.

To disable the LCD voltage boost circuit, we apply the following CLI commands:

>RI20$ Reads the hex value of register 0x2020

>8E Response from Demo Code indicating the bit 7 is set

>RI20=E Writes the hex value 0x0E to register 0x2020 causing the LCD boost to be switched off

>RI20=8E Enables the LCD boost circuit

The *LCD_CLK* register determines the frequency at which the COM pins change states. A slower clock means lower power consumption, but if the clock is too slow, visible flicker can occur. The default clock frequency for the 71M6511/6511H Demo Boards is 150Hz (*LCD_CLK* = 01).

Register Name	Address [bits]	R/W	Description
LCD_CLK[1:0]	2021[1:0]	R/W	Sets the LCD clock frequency, i.e. the frequency at which SEG and COM pins change states. f_w = CKADC/128 = 38,400 00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$

To change the LCD clock frequency, we apply the following CLI commands:

>RI21$ Reads the hex value of register 0x2021

>25 Response from Demo Code indicating the bit 0 is set and bit 1 is cleared.

>RI21=24 Writes the hex value 0x24 to register 0x2021 clearing bit 0 – LCD flicker is visible now

>RI21=25 Writes the original value back to *LCD_CLK*

2.6 TERIDIAN APPLICATION NOTES

Please contact your local TERIDIAN sales representative for TERIDIAN Application Notes. Available application notes are listed below.

Number	Title
AN_651X_008	Optical Port
AN_651X_009	Temperature Compensation
AN_651X_013	Emulator Upgrade
AN_651X_016	EMC/EMI Guidelines
AN_651X_017	LCD
AN_651X_018	Chop Enable
AN_651X_019	RX Pin
AN_651X_022	Calibration Procedures
AN_6511_006	Current Shunt
AN_651X_020	Calibration for Shunt and CT
AN_651X_023	EMI-EMC Proof Meter Design Using the 6511

3

3 HARDWARE DESCRIPTION

3.1 4-LAYER BOARD DESCRIPTION: JUMPERS, SWITCHES, TEST POINTS

The items described in the following tables refer to the flags in Figure 3-1.

Item # (Figure 3.1)	Electrical Schematic & PCB Silk-Print Reference	Name	Use
1	JP1	PS_SEL[0]	Two-pin header. When the jumper is installed the on- board power supply (AC signal) is used to power the Demo Board. When not installed, the board must be powered by an external supply connect to J1. Normally installed.
2	J9	Neutral	This is the NEUTRAL line voltage input. It is connected to the 3.3V net of the 71M6511/71M6511H. This input comes in from the bottom of the board.
3	JP2, JP3 	PS_SEL[1], PS_SEL[2]	Two-pin headers. When both jumpers are installed, external power is not required for the Debug Board that attaches to the 71M6511 Demo Board at J2. Normally left open.  **Caution! Do not install JP2/JP3!**
4	J1	5 Volt supply	Plug for connection of the external 5 VDC power supply.
5	J4 	VA_IN	VA_IN is the line voltage input. It has a resistor divider that leads to the VA pin on the chip that is the voltage input to the A/D converter. This input comes in from the bottom of the board.  **Caution: High Voltage. Do not touch these pins!**
6	JP17	None	Two-pin header. When the jumper is installed the resistor divider for VA is referenced to V3P3. The jumper must be removed when the board is used with a shunt resistor/CT combination on the IA and IB inputs. Normally installed.
7	JP16	None	Two-pin header. When the jumper is installed V3P3 is connected to the 3.3V regulator D1. The jumper must be removed when the board is used with a shunt resistor/CT combination on the IA and IB inputs. Normally installed.

Table 3-1: 71M6511 Demo Board Description: 1/3

Item # (Figure 3.1)	Elec. Schematic & PCB Silk-print Reference	Name	Use
8	TP2	VA	Two-pin header test point. One pin is the VA line voltage input to the IC and the other pin is V3P3.
9	SW2	RESET	Chip reset switch: The RESTZ pin has an internal pull up that allows normal chip operation. When the switch is pressed, the RESTZ pin is pulled low which resets the IC into a known state.
10	SW1	Pulse Rate Select	Switch connected to the DIO17 pin (non functional in demo code). SW1 should always be kept in the lower position.
11	JP9	EEPROM Write Protect	Three-pin header that allows selection of the write protection or read/write capability for the EEPROM (U4) on the Demo Board. Default setting of the Demo Board is to place a jumper between terminal 1 and 2 of JP9.
12	J12	Supply and Optical Test Point	4-pin header. Pins 1 and 3 can be used to measure the supply voltage to the 6511 IC. Terminal 2 monitors the TX_OPT output of the 6511 IC. Terminal 4 monitors the OPT_RX input to the 6511 IC.
13	JP12	DIO Test Point	7-pin test point. For monitoring DIO15 to DIO21.
14	J2	DEBUG	Debug Board connection connector. 2x8 pin header.
15	J10, J11	LCD	LCD connection. The LCD daughter board connects between these two 2x12 header jumpers.
16	BT1	Battery Terminal	Two-pin header for connection of a 3.6V battery. The top pin is the positive terminal and the bottom pin is ground.
17	JP8	VBAT Selection	Three-pin header that allows selection of power to the VBAT pin. When the jumper is placed between terminals 1 and 2 (default setting for Demo Board) VBAT is tied to the IC supply. When placed between terminals 2 and 3 VBAT is powered by an external battery.
18, 19	TP17, TP18	Test Mode Test Points	TMUXOUT and CKTEST test point.
20	J14	EMULATOR I/F	2x10 emulator connector port for Signum ICE ADM-51.
21	J13	Voltage Connections	Five-pin header. Connect jumper to the bottom two pins as the default
22	TP7	VREFOUT	Two-pin header. The top terminal is VREF, the bottom terminal is ground
23	TP10	V1 Test Point	Two-pin header representing the comparator voltage input test point and ground. A jumper should be placed between V1 and V3P3 to disable the watchdog timer.
24	JP10	VLCD Select	Three-pin header for selecting the voltage to the LCD. The top pin is 5V and the bottom pin is 3.3V. The default setting for the jumper is 5V

Table 3-2: 71M6511 Demo Board Description: 2/3

Item # (Figure 3.1)	Elec. Schematic & PCB Silk-print Reference	Name	Use
25	TP11, TP12	XIN, XOUT	One-pin header test points that monitor the crystal inputs XIN and XOUT.
26	J3, J16	IA_IN, IB_IN	Current shunt connections. Two-pin headers on bottom of the PCB. One terminal is 3.3V; the other is the shunt current.
27	TP1, TP19	IA, IB	Two-pin headers that provide line current sense to the IC test points. One terminal is ground; the other is the respective line current sense input to the IC.
28	TP20	SSI	5x2 header. High-speed serial interface. One row is GND.

Table 3-3: 71M6511 Demo Board Description: 3/3

Table 3-4 summarizes the jumper settings required for CT operation (factory default).

Jumper Header	Default Setting	Function in Default (Factory) Setting
JP1	Installed	Enables the internal power supply
JP2/JP3	Not installed	Disconnects power and ground of the Demo Board from power and ground of the Debug Board. Headers are not populated on newer Demo Boards.
JP8	V3P3-VBAT	Terminates the VBAT input properly when no battery is used.
JP9	1-2	Enables read and write operations for the EEPROM (U5)
JP10	5V-VLCD	Selects 5V supply provided by the VLCD driver for LCD operation.
JP16	Installed	Enables function of the Demo Board in CT mode
JP17	Installed	Enables function of the Demo Board in CT mode
J13	V1IN-V3P3	Provides V3P3 to the V1 pin.
TP10	V1-V3P3	Provides V3P3 to the voltage divider used for V1 pin.

Table 3-4: Jumper Default Settings

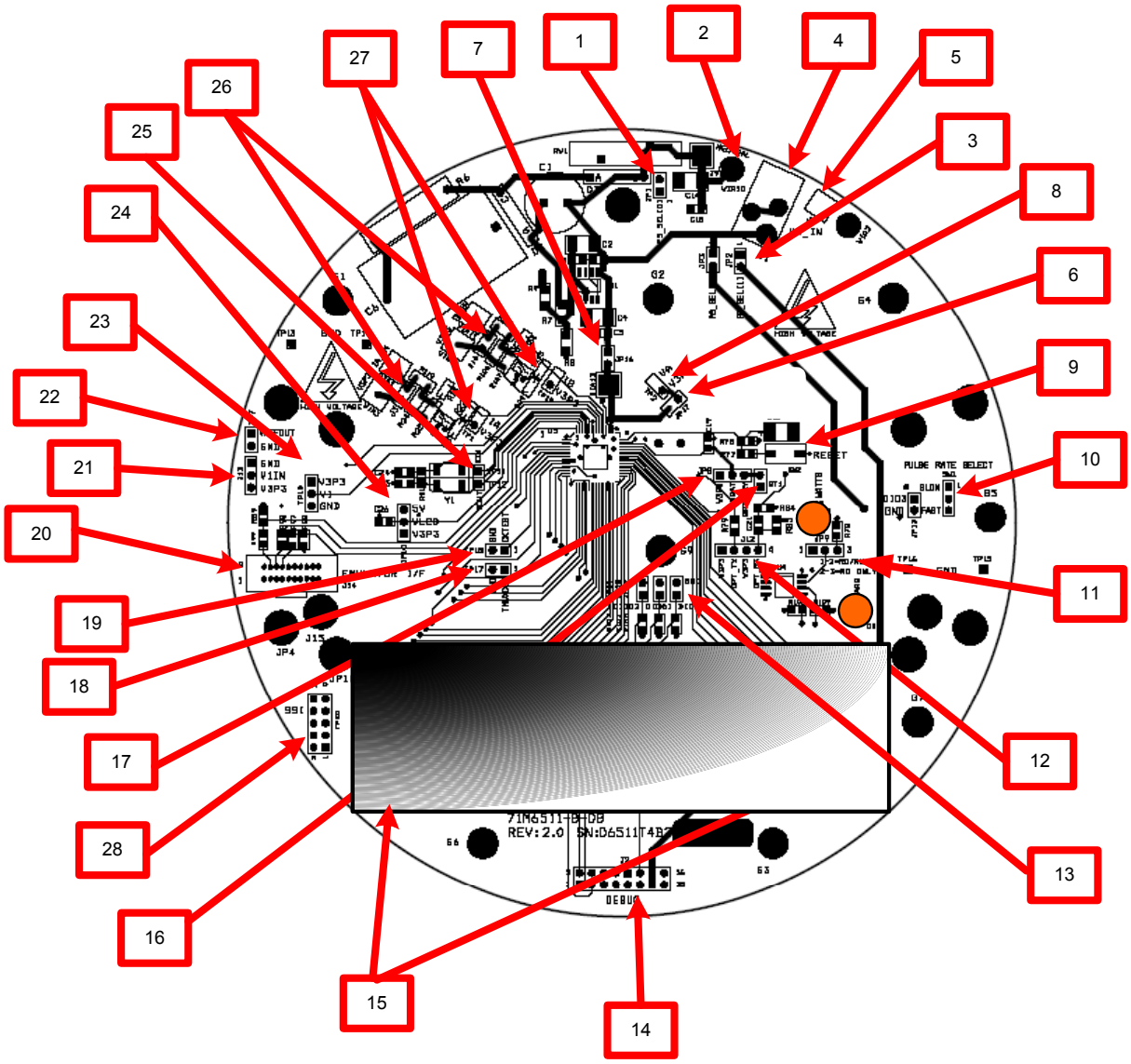


Figure 3-1: 71M6511 4-Layer Demo Board: Board Description

3.2 2-LAYER BOARD DESCRIPTION: JUMPERS, SWITCHES, TEST POINTS

Jumpers, headers, and connectors are largely identical for the two versions of the 2-Layer Demo Boards (capacitive and transformer power supply).

The items described in the following tables refer to the flags in Figure 3-2 and Figure 3-3.

Item # (Figure 3.2/3.3)	Schematic & PCB Silk Screen Reference	Name	Use
1	J1	5 Volt supply	Plug for connection of the external 5 VDC power supply.
2	D5	WATTS	LED emitting WATT pulses.
3	D6	VARS	LED emitting VAR pulses.
4	TP22	VARS	Test points for pulses generated by the VARS LED.
5	J2	DEBUG	Debug Board connector. 2x8 pin header.
6	TP21	WATTS	Test points for pulses generated by the WATTS LED.
7	J12	V3P3, OPT_TX, V3P3, OPT_RX, GND	5-pin header. Pins 1 and 3 carry the supply voltage to the 6511 IC. Pin 2 is the TX_OPT output of the 6511 IC. Pin 4 is the OPT_RX input to the 6511 IC. Pin 5 is ground.
8	JP8	V3P3, VBAT, GND	3-pin header for connection of a 3.6V battery. The battery is connected to pin 2 (+) and pin 3 (-). If no battery is used, a jumper is plugged over pins 1 and 2.
9	JP17	SHUNT I/O	2-pin header. In CT mode, a jumper must be plugged into JP17. In shunt mode, one wire from the shunt resistor is connected to pin 1.
10	TP17	TMUXOUT, CKTEST	2-pin header providing test points for TMUXOUT and CKTEST.
11	JP10	V3P3, VLCD, 5V	3-pin header for selecting the VLCD voltage. Pin 3 is 5V and pin 1 is 3.3V. The default setting for the jumper is 5V.
12	TP20	SSI	5x2 header. High-speed serial interface. One row is ground.
13	J14	EMULATOR I/F	2x10 emulator connector port for Signum ICE ADM-51.
14	TP10	V1, V3P3	2-pin header representing the V1 comparator voltage input test point and ground. A jumper should be placed between V1 and V3P3 to disable the watchdog timer.
15	J13	V3P3, V1IN	2-pin header. A jumper should be placed between V1IN and V3P3 to supply 3.3V to the resistor divider generating V1.
16	TP7	GND, VREFOUT	2-pin header. Pin 2 is ground; pin 1 is the VREF output of the IC.
17	TP19	IB	2-pin header test point. Pin is the IB input to the IC and the other pin is V3P3.
18	TP1	IA	2-pin header test point. Pin is the IA input to the IC and the other pin is V3P3.

Table 3-5: 71M6511 2-Layer Demo Board Description: 1/2

Item # in Figure 3.2/3.3	Schematic & PCB Silk Screen Reference	Name	Use
19	TP13, TP14	GND	Ground test points.
20	J3	IA_IN	3-pin header on the bottom of the board for connection of the CT for phase A. Pin 3 may be used to ground an optional cable shield. In shunt configuration, two wires from the shunt resistor representing the voltage across the shunt are connected to pins 1 and 2.
21	J16	IB_IN	3-pin header on the bottom of the board for connection of the CT for phase B. Pin 3 may be used to ground an optional cable shield.
22	J4 	LIVE	This is the line voltage input that feeds both the resistor divider leading to the VA pin on the chip and the internal power supply. The line voltage wire is connected to the spade terminal on the bottom of the board. **Caution: High Voltage. Do not touch this pin!**
23	TP2	V3P3, VA	2-pin header test point. Pin 1 is the VA line voltage input to the IC, pin 2 is V3P3.
24	JP1		2-pin header. When a jumper is installed, the on-board power supply (AC signal) is used to power the Demo Board. When not installed, the board must be powered by an external supply connected to J1. Normally installed.
25	SW2	RESET	Chip reset switch: The RESTZ pin has an internal pull up that allows normal chip operation. When the switch is pressed, the RESTZ pin is pulled low which resets the IC into a known state.
26	J9	NEUTRAL	This is the NEUTRAL line voltage input. It is connected to the 3.3V net of the 71M6511/71M6511H. The neutral wire is connected to the spade terminal on the bottom of the board.
27	TP15	GND	Ground test point.
28	JP4	SHUNT I/O	3-pin header on the bottom side of the board. A wire from the shunt resistor connects to pin 2, while an optional shield can be connected to pin 3. When operating in CT mode, a jumper is plugged across pins 1 and 2.

Table 3-6: 71M6511 2-Layer Demo Board Description: 2/3

Table 3-7 summarizes the jumper settings required for CT operation (factory default).

Jumper Header	Default Setting	Function in Default (Factory) Setting
JP1	Installed	Enables the internal power supply
JP8	V3P3-VBAT	Terminates the VBAT input properly when no battery is used.
JP9	1-2	Enables read and write operations for the EEPROM (U5)
JP10	5V-VLCD	Selects 5V supply provided by the VLCD driver for LCD operation.
JP4	1-2	Enables function of the Demo Board in CT mode
JP17	Installed	Enables function of the Demo Board in CT mode
J13	V1IN-V3P3	Provides V3P3 to the V1 pin.
TP10	V1-V3P3	Provides V3P3 to the voltage divider used for V1 pin.

Table 3-7: Jumper Default Settings

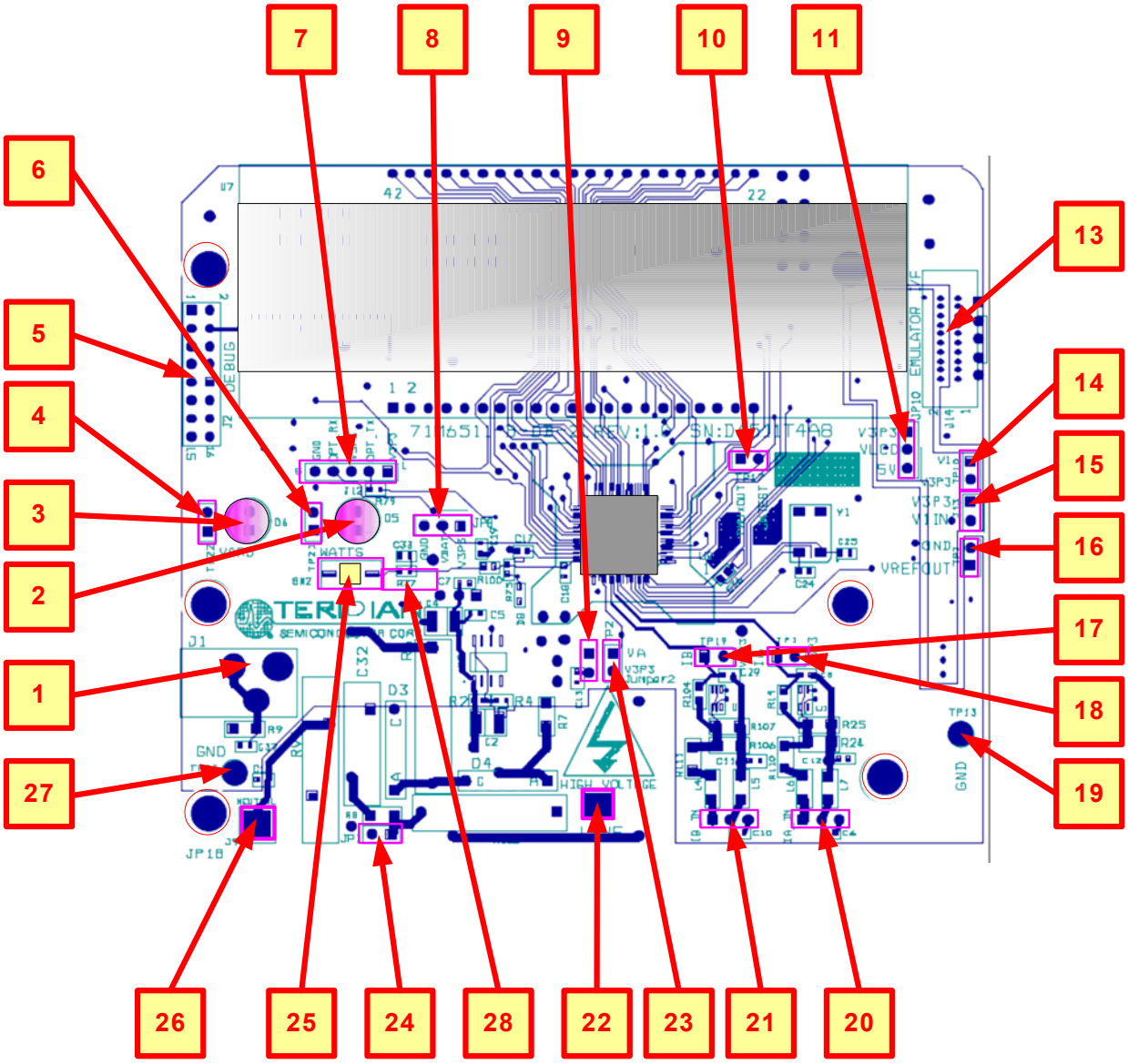


Figure 3-2: D6511T4A8 Two-Layer Demo Board with Capacitive Power Supply

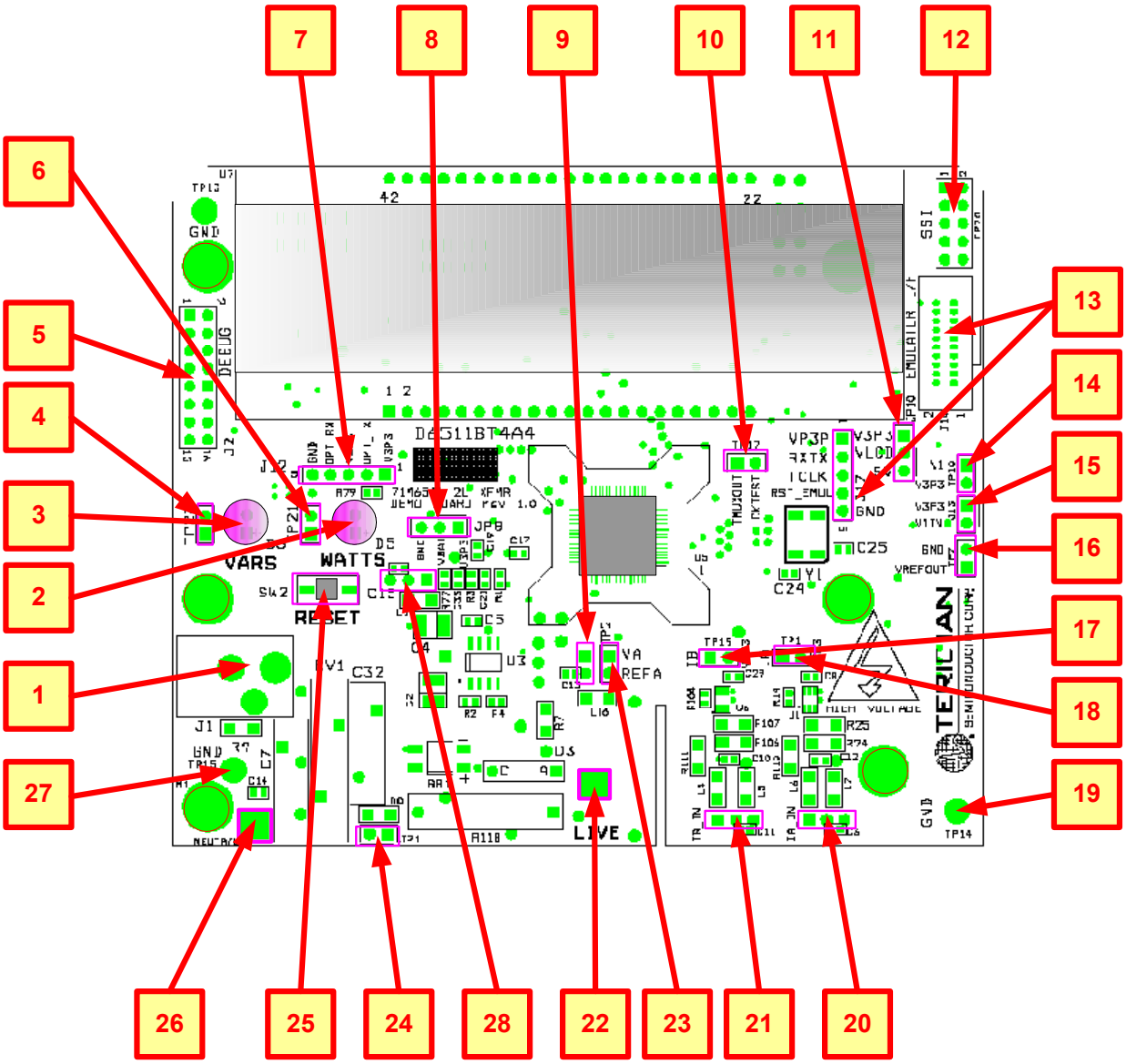


Figure 3-3: 71M6511 Two-Layer Demo Board with Transformer Power Supply

3.3 BOARD HARDWARE SPECIFICATIONS (4-LAYER)

PCB Dimensions

- Diameter — 6.5" (165.1mm)
- Thickness — 0.062" (1.6mm)
- Height w/ components and 3/8" spacers — 1.5" (38.1mm)

Environmental

- Operating Temperature — -40°…+85°C
  (function of crystal oscillator affected outside –10°C to +60°C)
- Storage Temperature — -40°C…+100°C

Power Supply

- Using AC Input Signal — 180V…700V rms
- DC Input Voltage (powered from DC supply) — 5VDC ±0.5V
- Supply Current — 25mA typical

Input Signal Range

- AC Voltage Signal (VA) — 0…240V rms
- AC Current Signals (IA, IB) from Transducer — 0…0.25V p/p

Interface Connectors

- DC Supply Jack (J1) to Wall Transformer — Concentric connector, 2.5mm
- Emulator (J14) — 10x2 Header, 0.05" pitch
- Input Signals — Spade terminals and 0.1" headers on PCB bottom
- Debug Board (J2) — 8x2 Header, 0.1" pitch
- Target Chip (U5) — LQFP64 Socket
- SSI Connector (TP19) — 5x2 Header, 0.1" pitch

Functional Specification

- Time Base Frequency — 32.768kHz, ±20PPM at 25°C
- Time Base Temperature Coefficient — -0.04PPM/°C2 (max)

Controls and Displays

- Reset — Button (SW2)
- Numeric Display — 8-digit LCD, 8-segments per digit, 12.7mm character height, 89.0 x 17.7mm view area
- "Watts", "VARS" — red LEDs (D5, D6)

Measurement Range

- Voltage — 120…700 V rms (resistor division ratio 1:3,398)
- Current — 1.7Ω termination for 2,000:1 CT input (200A)

3.4 BOARD HARDWARE SPECIFICATIONS (2-LAYER)

PCB Dimensions

- Dimensions — 4.5" x 3.8" (114.3mm x 96.5mm)
- Thickness — 0.062" (1.6mm)
- Height w/ components — 2.0" (51mm)

Environmental

- Operating Temperature — -40°…+85°C
  (function of crystal oscillator affected outside –10°C to +60°C)
- Storage Temperature — -40°C…+100°C

Power Supply

- Using AC Input Signal — 180V…700V rms
- DC Input Voltage (powered from DC supply) — 5VDC ±0.5V
- Supply Current — 25mA typical

Input Signal Range

- AC Voltage Signal (VA) — 0…240V rms
- AC Current Signals (IA, IB) from Transducer — 0…0.25V p/p

Interface Connectors

- DC Supply Jack (J1) to Wall Transformer — Concentric connector, 2.5mm
- Emulator (J14) — 10x2 Header, 0.05" pitch
- Input Signals — Spade terminals and 0.1" headers on PCB bottom
- Debug Board (J2) — 8x2 Header, 0.1" pitch
- Target Chip (U5) — LQFP64 Socket
- SSI Connector (TP19) — 5x2 Header, 0.1" pitch

Functional Specification

- Time Base Frequency — 32.768kHz, ±20PPM at 25°C
- Time Base Temperature Coefficient — -0.04PPM/°C^2 (max)

Controls and Displays

- Reset — Button (SW2)
- Numeric Display — 8-digit LCD, 8-segments per digit, 12.7mm character height, 89.0 x 17.7mm view area
- "Watts", "VARS" — red LEDs (D5, D6)

Measurement Range

- Voltage — 120…700 V rms (resistor division ratio 1:3,398)
- Current — 1.7Ω termination for 2,000 :1 CT input (200A)

4

4 DEMO BOARD ELECTRICAL SECTION

This section includes the following documentation, tables and drawings:

71M6511 4-Layer Demo Board Description

- 71M6511 Demo Board Electrical Schematic
- 71M6511 Demo Board Bill of Materials
- 71M6511 Demo Board PCB Silk screen layer – Top and Bottom side
- 71M6511 Demo Board PCB Metal Layer – Top and Bottom side
- 71M6511 Demo Board PCB Metal Layer – Middle 1, ground plane
- 71M6511 Demo Board PCB Metal Layer – Middle 2, supply plane

71M6511 2-Layer Demo Board Description

- 71M6511 Demo Board Electrical Schematic
- 71M6511 Demo Board Bill of Materials
- 71M6511 Demo Board PCB Silk screen layer – Top and Bottom side
- 71M6511 Demo Board PCB Metal Layer – Top and Bottom side

Debug Board Description

- Debug Board Electrical Schematic
- Debug Board Bill of Materials
- Debug Board PCB Silk screen layer – Top and Bottom side
- Debug Board PCB Metal Layer – Top and Bottom side signal layer
- Debug Board PCB Metal Layer – Middle 1, ground plane
- Debug Board PCB Metal Layer – Middle 2, supply plane

71M6511 Pin-Out and Mechanical Description

- 71M6511 Pin Description
- 71M6511 Pin-out

4.1 71M6511 4-LAYER DEMO BOARD ELECTRICAL SCHEMATIC

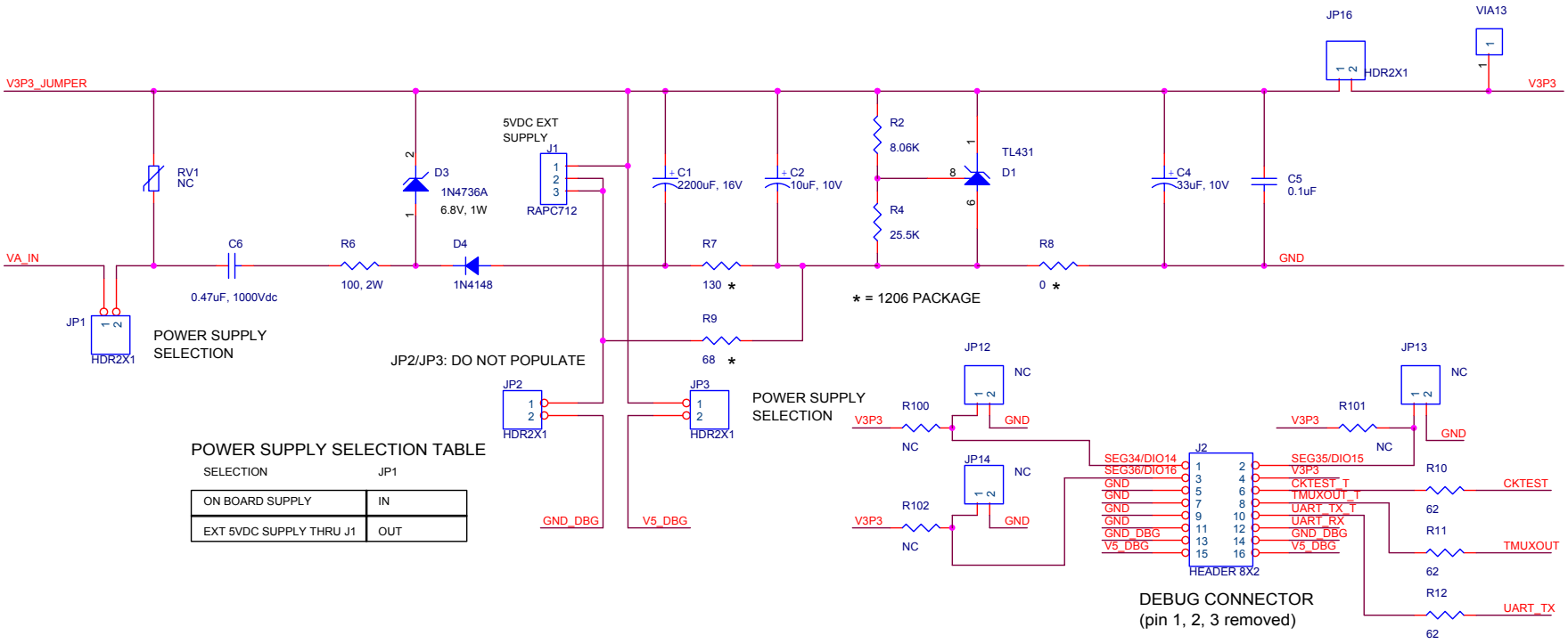


Figure 4-1: 71M6511 4-Layer Demo Board: Electrical Schematic 1/3

If the 4-Layer Demo Board has to be operated in an EMI environment, see Application Note 651X_016 and follow the schematic guidelines therein for necessary component modifications.

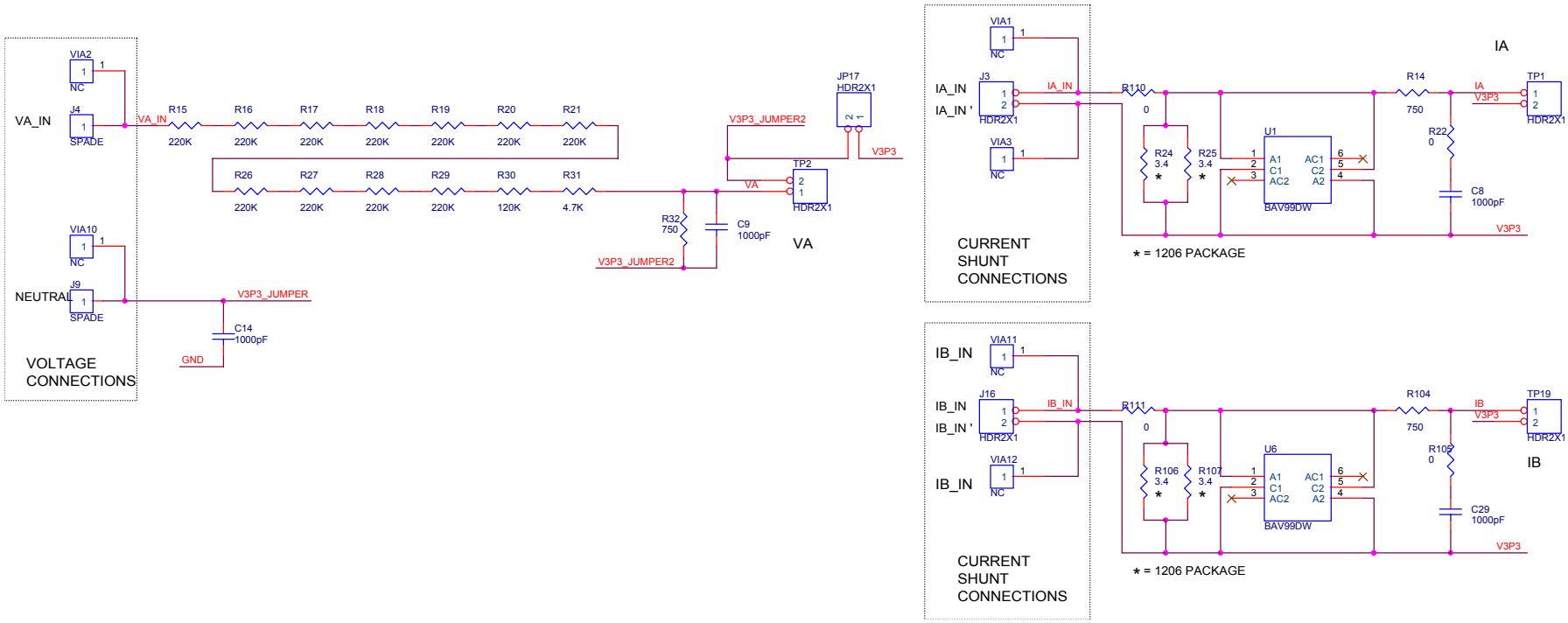


Figure 4-2: 71M6511 4-Layer Demo Board: Electrical Schematic 2/3

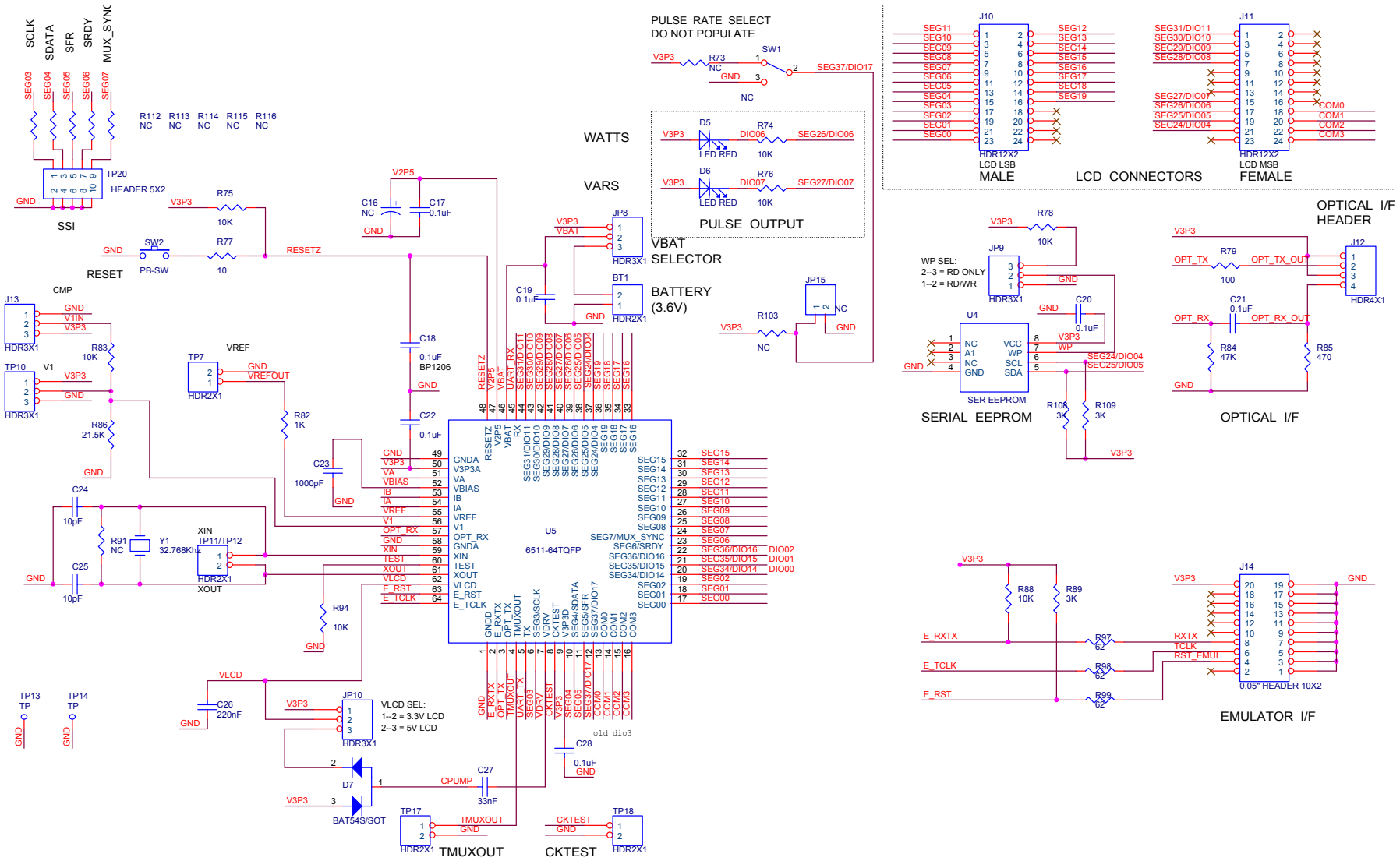


Figure 4-3: 71M6511 4-Layer Demo Board: Electrical Schematic 3/3

4.2 71M6511 2-LAYER DEMO BOARD WITH CAPACITIVE POWER SUPPLY - ELECTRICAL SCHEMATIC

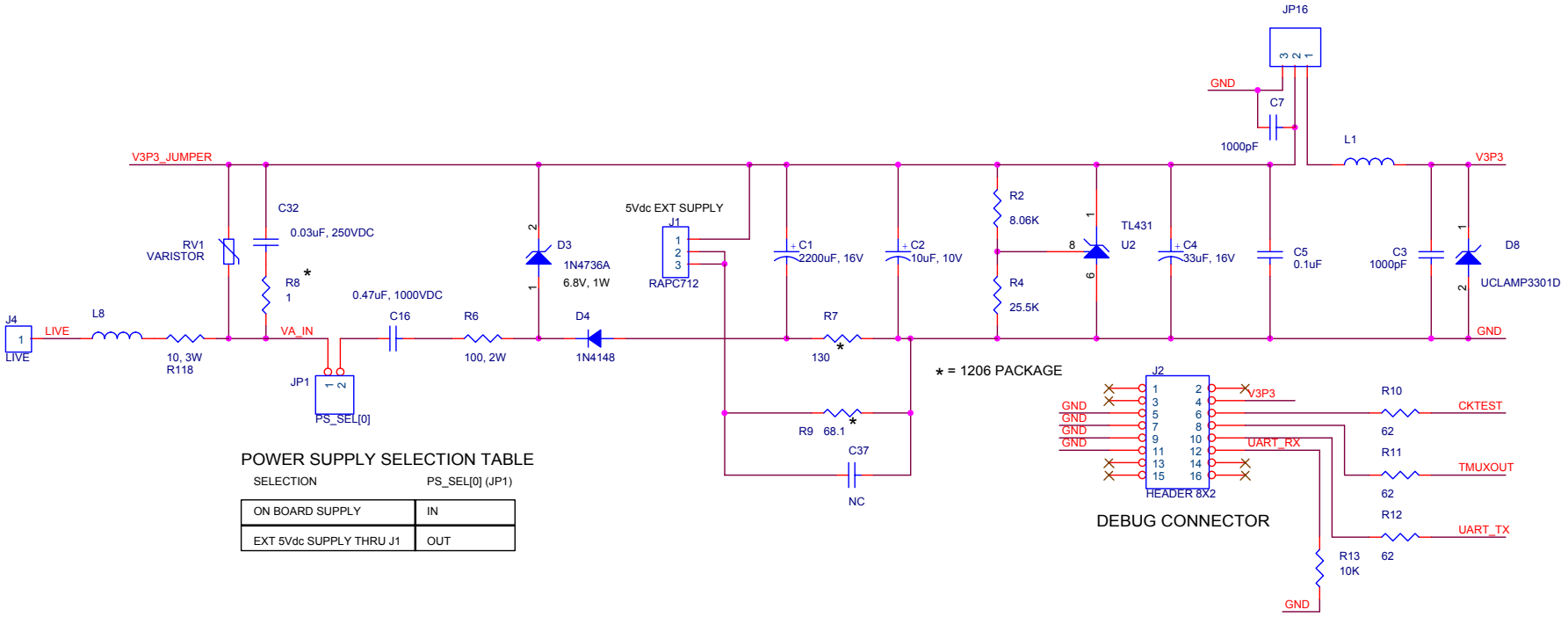


Figure 4-4: D6511T4A8 2-Layer Demo Board (Capacitve Power Supply): Electrical Schematic 1/3

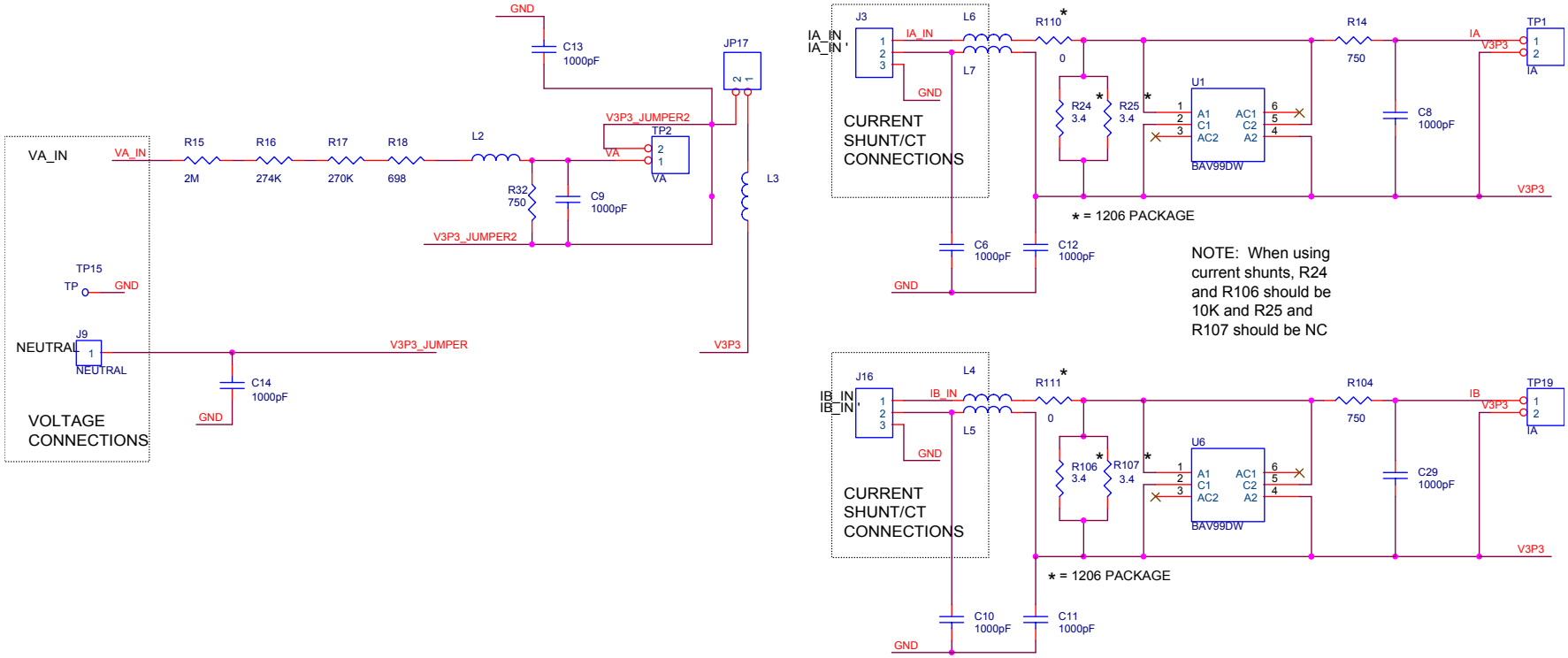


Figure 4-5: D6511T4A8 2-Layer Demo Board (Capacitve Power Supply): Electrical Schematic 2/3

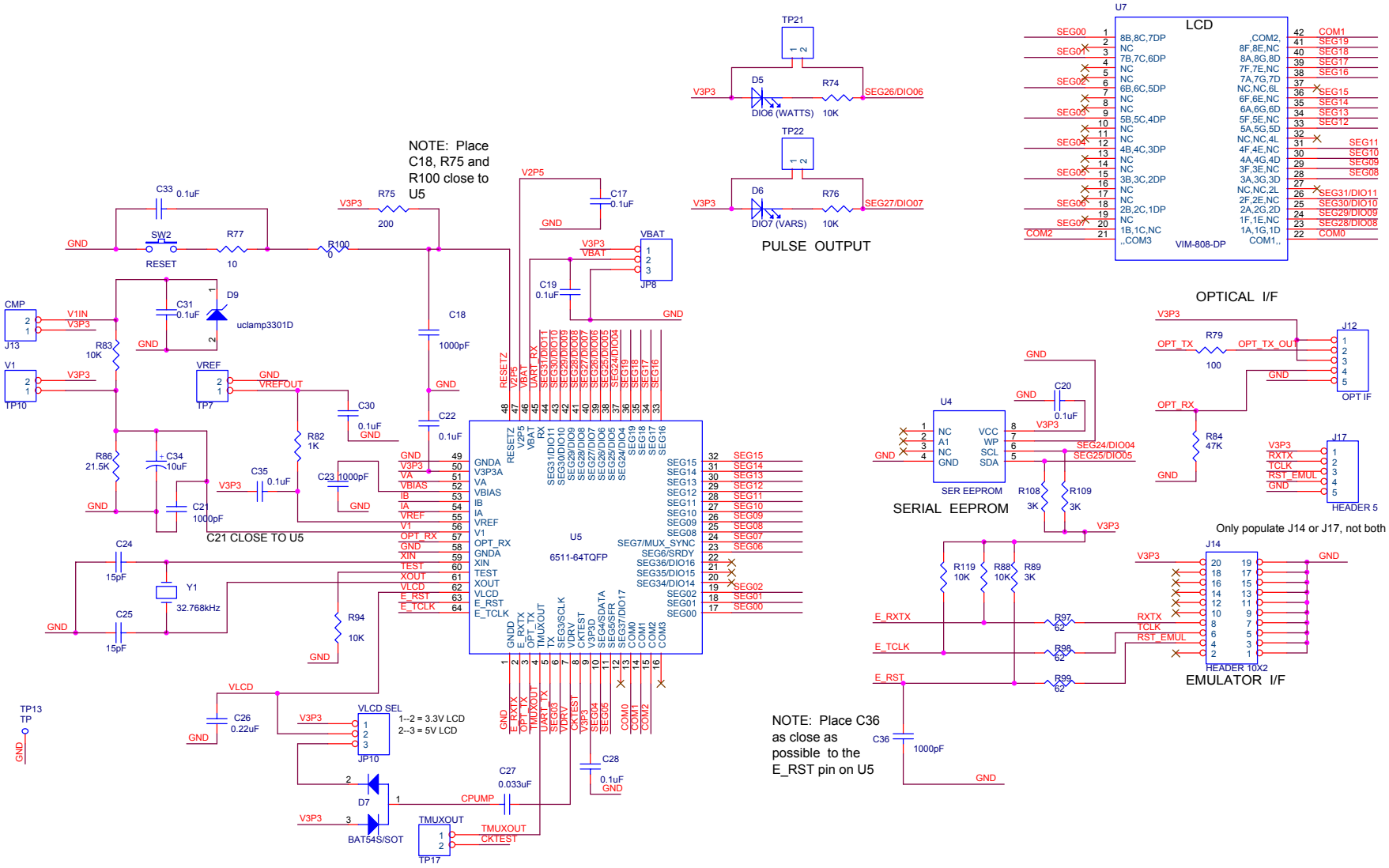


Figure 4-6: D6511T4A8 2-Layer Demo Board (Capacitve Power Supply): Electrical Schematic 3/3

4.3 71M6511 2-LAYER DEMO BOARD WITH TRANSFORMER - ELECTRICAL SCHEMATICS

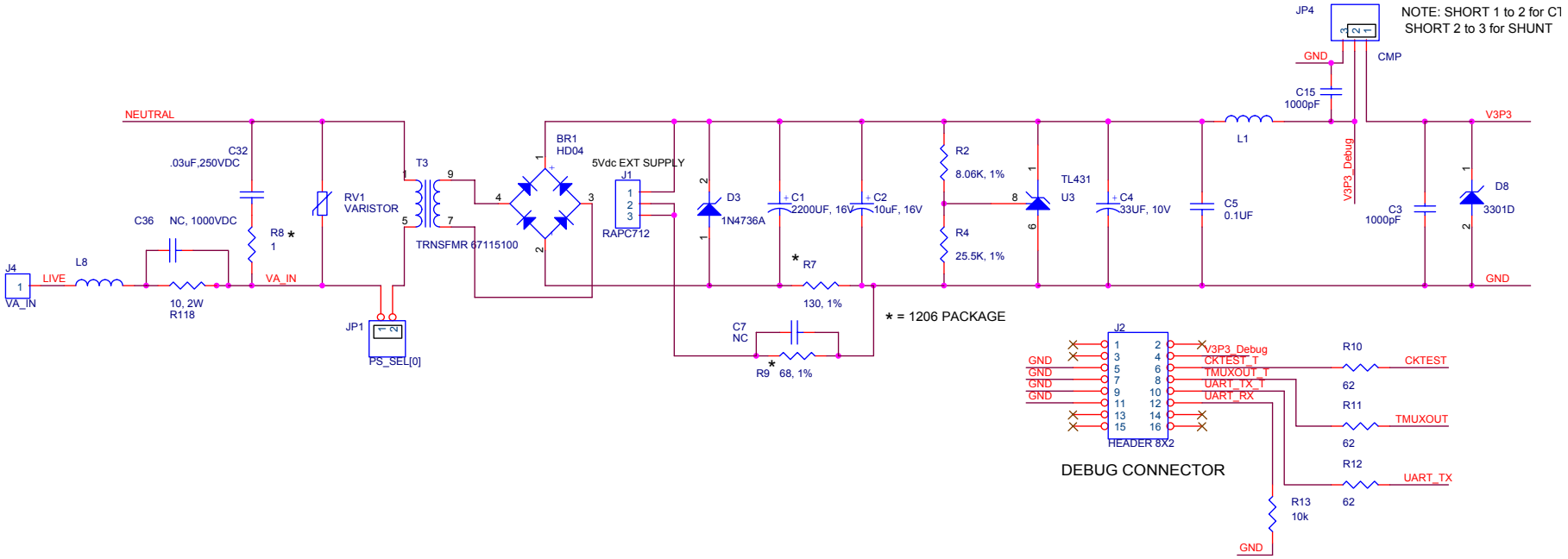


Figure 4-7: 71M6511 2-Layer Demo Board (Xformer Power Supply): Electrical Schematic 1/3

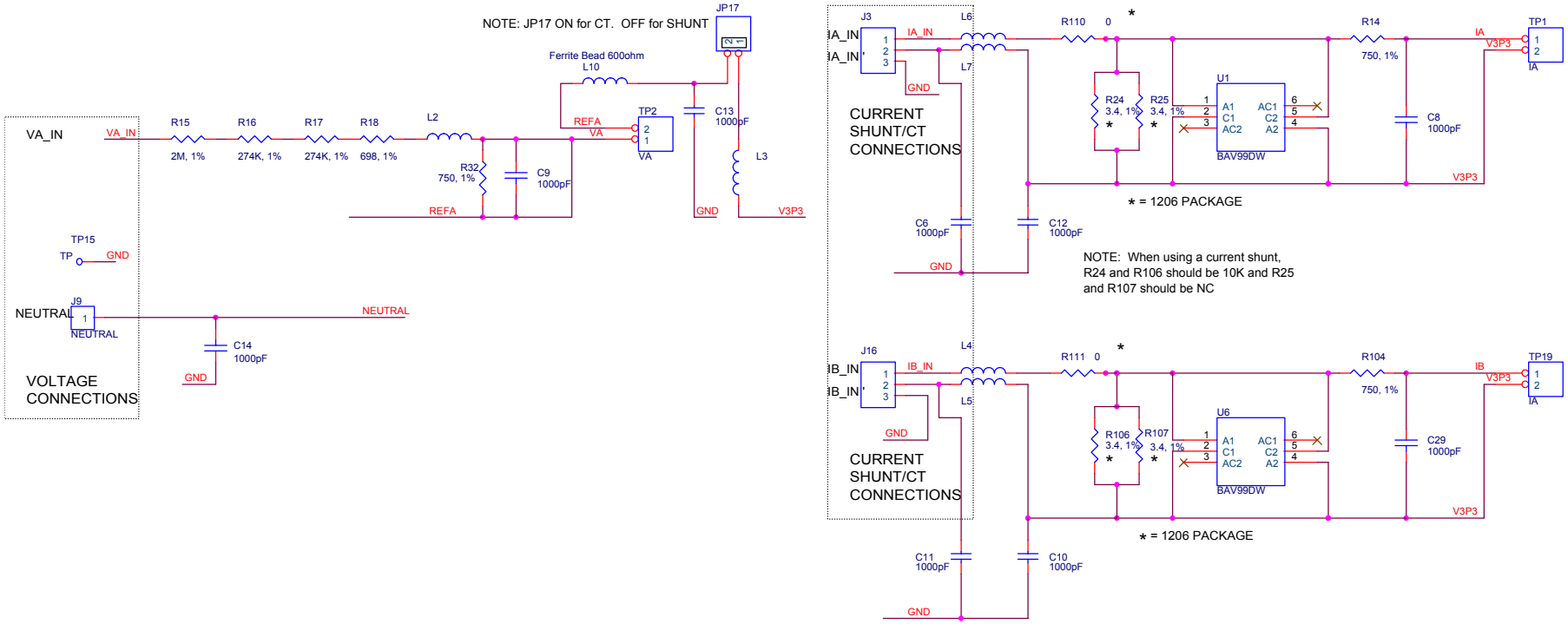


Figure 4-8: 71M6511 2-Layer Demo Board (Transformer Power Supply): Electrical Schematic 2/3

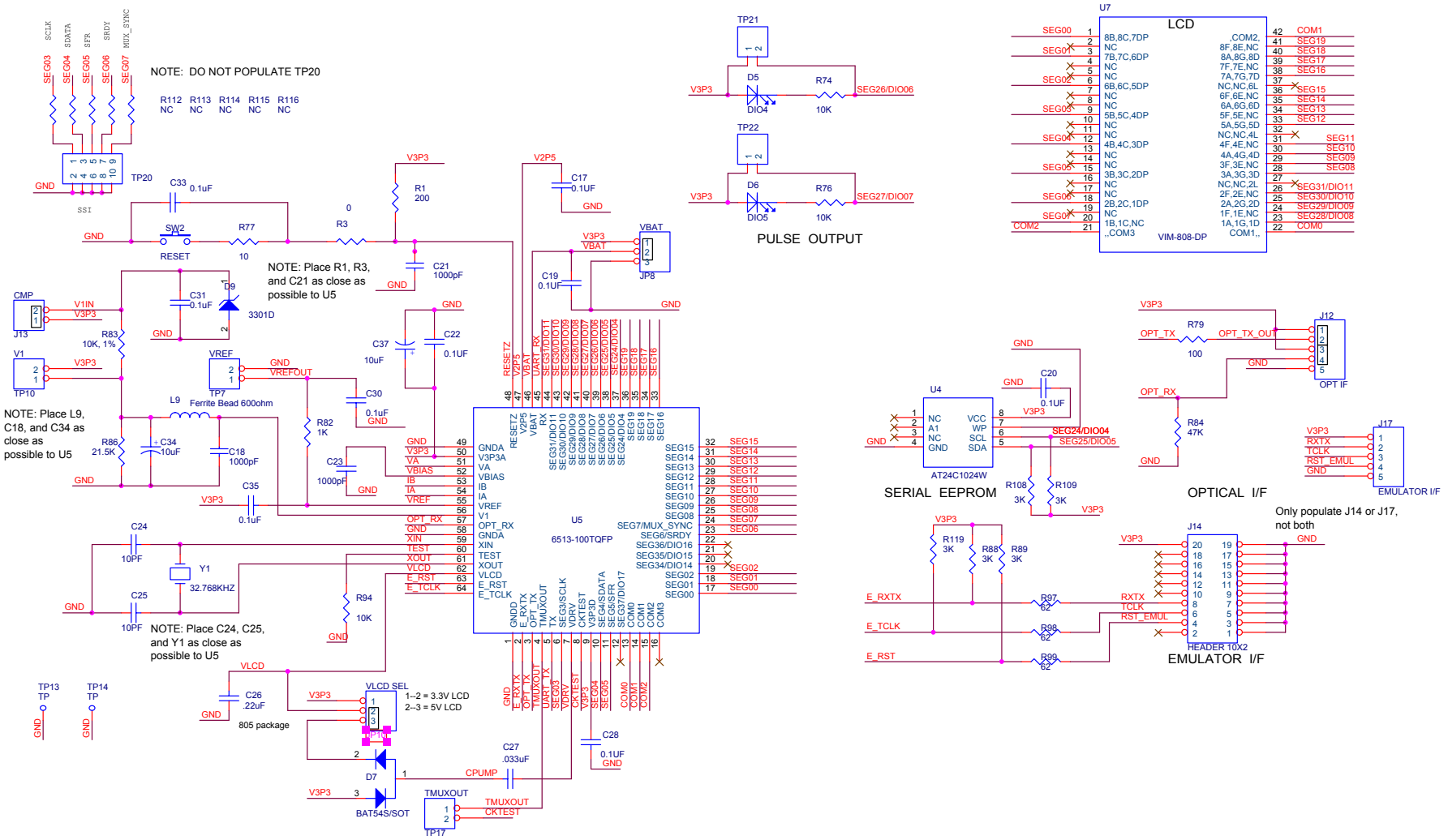


Figure 4-9: 71M6511 2-Layer Demo Board (Xformer Power Supply): Electrical Schematic 3/3

4.4 71M6511 4-LAYER DEMO BOARD BILL OF MATERIAL

Item	Quantity	Reference	Part	Footprint	Digi-Key P/N	P/N	Manufacturer
1	15	TP1-TP2,JP1-JP3,BT1,J3,	HDR2X1	HDR2X1	S1011-36-ND	PZC36SAAN	Sullins
		TP7,JP16,J16,TP17-TP19,					
		JP17,TP11/TP12					
2	1	C1	2200uF, 16V	Radial	P5143-ND	ECA-1CM222	Panasonic
3	1	C2	10uF, 10V	RC1812	478-1672-1-ND	TAJB106K010R	AVX
4	1	C4	33uF, 10V	RC1812	478-1687-1-ND	TAJB336K010R	AVX
5	8	C5,C15,C17,C19,C20-C22,C28	0.1uF	RC0805	445-1349-1-ND	C2012X7R1H104K	TDK
6	1	C6	0.47uF, 1000Vdc	RECT.	BC1918-ND	222 383 30474	BC Components
7	4	C8,C9,C23,C29	1000pF	RC0805	PCC221CGCT-ND	ECJ-2VC1H221J	Panasonic
8	1	C18	0.1uF	RC1206	PCC104BCT-ND	ECJ-3VB1H104K	Panasonic
9	4	SW1,C16,R91,R103	NC	N/A	N/A	N/A	N/A
10	2	C25,C24	10pF	RC0805	PCC100CNCT-ND	ECJ-2VC1H100D	Panasonic
11	1	C26	0.220uF	RC0805	445-1352-1-ND	C2012X7R1E224K	TDK
12	1	C27	0.033uF	RC0805	PCC1834CT-ND	ECJ-2VB1H333K	Panasonic
13	1	D1	TL431	SO8	296-1288-1-ND	TL431AIDR	TI
14	1	D3	1N4736A	DO41	1N4736ADICT-ND	1N4736A-T	DIODES
15	1	D4	1N4148	DO35	1N4148DICT-ND	1N4148-T	DIODES
16	2	D5,D6	LED RED	RADIAL	67-1612-ND	SSL-LX5093SRC/E	LUMEX
17	1	D7	BAT54S/SOT	SOT23	BAT54SDICT-ND	BAT54S-7	DIODES
18	18	VIA1-VIA3,G1-G9,JP4,JP11,	NC	N/A	N/A	N/A	N/A
		VIA10-VIA13,J15					
19	5	JP8,JP9,TP10,JP10,J13	HDR3X1	HDR3X1	S1011-36-ND	PZC36SAAN	Sullins
20	6	JP2,JP3,JP12-JP15	NC	HDR2X1	N/A	PZC36SAAN	Sullins
21	1	J1	RAPC712	DC CONN	SC1152-ND	RAPC712	Switchcraft
22	1	J2	HEADER 8X2	8X2PIN	S2011-36-ND	PZC36DAAN	Sullins
23	2	J4,J9	SPADE	SPADE	A24747CT-ND	62395-1	AMP
24	1	J10	HDR12X2	HDR12X2	WM6824-ND	10-89-1241	Molex/Waldom
25	1	J11	HDR12X2	HDR12X2	S4312-ND	PPPC122LFBN	Sullins
26	1	J12	HDR4X1	HDR4X1	S1011-36-ND	PZC36SAAN	Sullins
27	1	J14	0.05" HEADER 10X2	HDR0.05	A3210-ND	104068-1	AMP
28	4	RV1,R100,R101,R102	NC		N/A	N/A	N/A
29	1	R2	8.06K	RC0805	311-8.06KCCT-ND	9C08052A8061FKHFT	Yageo
30	1	R4	25.5K	RC0805	311-25.5KCCT-ND	9C08052A2552FKHFT	Yageo
31	1	R6	100, 2W	AXIAL	100W-2-ND	RSF200JB-100R	Yageo
32	1	R7	130	RC1206	311-130FCT-ND	9C12063A1300FGHFT	Yageo
33	3	R8,R110,R111	0	RC1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
34	1	R9	68	RC1206	311-68.0FCT-ND	9C12063A68R0FKHFT	Yageo
35	6	R10-R12,R97-R99	62	RC0805	P62ACT-ND	ERJ-6GEYJ620V	Panasonic
36	2	R22,R105	0	RC0805	P0.0ACT-ND	ERJ-6GEY0R00V	Panasonic
37	3	R14,R32,R104	750	RC0805	RR12P750DCT-ND	RR1220P-751-D	SUSUMU
38	11	R15-R21,R27-R29	220K	RC0805	RR08P220KBCT-ND	RR0816P-224-B-T5	SUSUMU
39	4	R24,R25,R106,R107	3.4	RC1206	311-3.4FCT-ND	9C12063A3R40FGHFT	Yageo
40	1	R30	120K	RC0805	RR12P120KBCT-ND	RR1220P-124-B-T5	SUSUMU
41	1	R31	4.7K	RC0805	RR12P4.7KBCT-ND	RR1220P-472-B-T5	SUSUMU
42	5	R74,R75,R76,R78,R94	10K	RC0805	P10KACT-ND	ERJ-GEYJ103V	Panasonic
43	1	R77	10	RC0805	P10ACT-ND	ERJ-GEYJ100V	Panasonic
44	1	R79	100	RC0805	P100ACT-ND	ERJ-GEYJ101V	Panasonic
45	1	R82	1k	RC0805	P1.0KACT-ND	ERJ-GEYJ102V	Panasonic
46	1	R83	10K	RC0805	P10.0KCCT-ND	ERJ-6ENF1872V	Panasonic
47	1	R84	47K	RC0805	P47KACT-ND	ERJ-6GEYJ473V	Panasonic
48	1	R85	470	RC0805	P470ACT-ND	ERJ-6GEYJ471V	Panasonic
49	1	R86	21.5K	RC0805	P21.5KCCT-ND	ERJ-6ENF2152V	Panasonic
50	4	R89,R88,R108,R109	3K	RC0805	P3.0KACT-ND	ERJ-6GEYJ302V	Panasonic
51	1	SW2	PB-SW	SMT SW	P8051SCT-ND	EVQ-PJX05M	Panasonic
52	4	TP13-TP16	TP	Paper Clip	N/A	N/A	TDK
53	1	TP20	HEADER 5X2	HDR5X2	S2011-36-ND		Sullins
54	2	U1,U6	BAV99DW	SOT263	BAV99DWDICT-ND	BAV99DW-7	DIODES
55	1	U4	SER EEPROM	SO8	AT24C1024W10SI2.7-ND	AT24C1024W-10SI-2.7	ATMEL
56	1	U5	6511-64TQFP	64TQFP	N/A	64TQFP SOCKET	YAMAICHI
57	1	Y1	32.768Khz	SMT XTAL	XC488CT-ND	ECS-.327-12.5-17-TR	ECS

Table 4-1: 71M6511 4-Layer Demo Board: Bill of Material

4.5 BOM FOR 71M6511 2-LAYER DEMO BOARD (CAPACITIVE POWER SUPPLY)

Item	Q	Reference	Part	PCB Footprint	Digi-Key/Mouser Part Number	Part Number	Manufacturer
1	1	C1	2200uF	Radial	P5143-ND	ECA-1CM222	Panasonic
2	2	C2,C34	10uF, 10V	RC1812	478-1672-1-ND	TAJB106K010R	AVX
3	14	C3,C6,C7,C8,C9,C10,C11,	1000pF	RC0603	445-1298-1-ND	C1608X7R2A102K	TDK
		C12,C13,C14,C18,C23,					
		C29,C36					
4	1	C4	33uF, 16V	RC1812	478-1688-1-ND	TAJB336K016R	AVX
5	10	C5,C17,C19,C20,C22,C28,	0.1uF	RC0603	445-1314-1-ND	C1608X7R1H104K	TDK
		C30,C31,C33,C35					
6	1	C16	0.47uF, 1000VDC	Block	BC1918-ND	222 383 30474	BC Components
7	2	C24,C25	10pF	RC0603	445-1269-1-ND	C1608COG1H100D	TDK
8	1	C26	0.22uF	RC0805	445-1350-1-ND	C2012X7R1H224K	TDK
9	1	C27	0.033uF	RC0603	PCC2284CT-ND	ECJ-1VB1H333K	Panasonic
10	1	C32	0.03uF, 250V	Axial	75-125LS30-R	125LS30-R	Vishay
11	1	D3	1N4736A	DO41	1N4736ADICT-ND	1N4736A-T	DIODES
12	1	D4	1N4148	DO35	1N4148DICT-ND	1N4148-T	DIODES
13	2	D5,D6	LED	RADIAL	67-1612-ND	SSL-LX5093SRC/E	LUMEX
14	1	D7	BAT54S/SOT	SOT23	BAT54S-FDICT-ND	BAT54S-7-F	DIODES
15	2	D8,D9	Tranzorb	SOD-323	X	UCLAMP3301D.TCT	SEMTECH
16	1	J1	DC Connector	RAPC712	SC1152-ND	RAPC712	Switchcraft
17	1	J2	HEADER 8X2	8X2PIN	S2011E-36-ND	PBC36DAAN	Sullins
18	2	J3,J16	HEADER 3	3X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
19	2	J4,J9	Faston		A24747CT-ND	62395-1	AMP
20	2	J12,J17	HEADER 5	5X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
21	1	J13	HEADER 2	2X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
22	1	J14	10X2 CONNECTOR		A3210-ND	104068-1	AMP
23	2	JP1,JP17	HEADER 2	2X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
24	3	JP8,JP10,JP16	HEADER 3	3X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
25	8	L1,L2,L3,L4,L5,L6,L7,L8	Ferrite bead, 600 Ohm	RC1206	445-1556-1-ND	MMZ2012S601A	TDK
26	1	RV1	VARISTOR	radial	581-VZD510XX	VE24M00511K	AVX
27	1	R2	8.06K, 1%	RC0603	P8.06KHCT-ND	ERJ-3EKF8061V	Panasonic
28	1	R4	25.5K, 1%	RC0603	P25.5KHCT-ND	ERJ-3EKF2552V	Panasonic
29	1	R6	100, 2W	Axial	100W-2-ND	RSF200JB-100R	Yageo
30	1	R7	130, 1%	RC1206	P130FCT-ND	ERJ-8ENF1300V	Panasonic
31	1	R8	1	RC1206	P1.0ECT-ND	ERJ-8GEYJ1R0V	Panasonic
32	1	R9	68.1, 1%	RC1206	P68.1FCT-ND	ERJ-8ENF68R1V	Panasonic
33	6	R10,R11,R12,R97,R98,R99	62	RC0603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
34	6	R13,R74,R76,R88,R94,	10K	RC0603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
		R119					
35	2	R14,R104	750, 1%	RC0805	P750CCT-ND	ERJ-6ENF7500V	Panasonic
36	1	R15	2M, 1%	Axial	71-RN65DF-2.0M	RN65D2004FB14	Dale
37	1	R16	274K, 1%	RC0805	P274KCCT-ND	ERJ-6ENF2743V	Panasonic
38	1	R17	270K, 1%	RC0805	RHM270KCCT-ND	MCR10EZHF2703	Rohm
39	1	R18	698, 1%	RC0805	P698CCT-ND	ERJ-6ENF6980V	Panasonic
40	4	R24,R25,R106,R107	3.4, 1%	RC1206	311-3.40FCT-ND	9C12063A3R40FGHFT	Yageo
41	1	R32	750, 1%	RC0603	P750HCT-ND	ERJ-3EKF7500V	Panasonic
42	1	R75	200	RC0603	P200GCT-ND	ERJ-3GEYJ201V	Panasonic
43	1	R77	10	RC0603	P10GCT-ND	ERJ-3GEYJ100V	Panasonic
44	1	R79	100	RC0603	P100GCT-ND	ERJ-3GEYJ101V	Panasonic
45	1	R82	1K	RC0603	P1.0KGCT-ND	ERJ-3GEYJ102V	Panasonic
46	1	R83	10.0K, 1%	RC0603	P10.0KHCT-ND	ERJ-3EKF1002V	Panasonic
47	1	R84	47K	RC0603	P47KGCT-ND	ERJ-3GEYJ473V	Panasonic
48	1	R86	21.5K, 1%	RC0603	P21.5KHCT-ND	ERJ-3EKF2152V	Panasonic
49	3	R89,R108,R109	3K	RC0603	P3.0KGCT-ND	ERJ-3GEYJ302V	Panasonic
50	1	R100	0	RC0603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
51	2	R110,R111	0	RC1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
52	1	R118	10, 3W	axial	71-CW2B-10	CW02B10R00JB12	Vishay
53	1	SW2	Pushbutton Switch		P8051SCT-ND	EVQ-PJX05M	Panasonic
54	8	TP1,TP2,TP7,TP10,TP17,	TP	2X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
		TP19,TP21,TP22					
55	1	TP15	TP	1X1PIN	S2011E-36-ND	PBC36SAAN	Sullins
56	2	U1,U6	BAV99DW	SOT363	BAV99DW-FDICT-ND	BAV99DW-7-F	DIODES
57	1	U2	REGULATOR, 1%	SO8	296-1288-1-ND	TL431AIDR	Texas Instruments
58	1	U4	Serial EEPROM		AT24C1024W-10SI-2.7-ND	AT24C1024W-10SI-2.7	ATMEL
59	1	U5	71M6511	64TQFP	X	71M6511-IGT	Teridian
	1	at U5	64TQFP Socket	64TQFP	X	IC149-064-169-S5	Yamaichi
60	1	U7	LCD		153-1056-ND	VIM-808-DP-RC-S-HV	VARITRONIX
61	1	Y1	32.768kHz		XC488CT-ND	ECS-.327-12.5-17-TR	ECS

Table 4-2: D6511T4A8 2-Layer Demo Board: Bill of Material

4.6 BOM FOR 71M6511 2-LAYER DEMO BOARD (TRANSFORMER POWER SUPPLY)

Item	Q	Reference	Part	PCB Footprint	Digi-Key/Mouser Part Number	Part Number	Manufacturer
1	1	BR1	Bridge Rectifier			HD04	
2	1	C1	2200uF	BULK/Radial	P5143-ND	ECA-1CM222	Panasonic
3	1	C2	10uF	RC1812	478-1672-1-ND	TAJB106K010R	AVX
4	14	C3,C6,C8-C15,C18,C21,C23	1000pF	RC0603	445-1298-1-ND	C1608X7R2A102K	TDK
		C29					
5	1	C4	33uF	RC1812	478-1688-1-ND	TAJB336K016R	AVX
6	10	C5,C17,C19,C20,C22,C28,	0.1uF	RC0603	445-1314-1-ND	C1608X7R1H104K	TDK
		C30,C31,C33,C35					
7	1	C7	NC	Axial	--	--	--
8	2	C24,C25	10pF	RC0603	445-1269-1-ND	C1608COG1H100D	TDK
9	1	C26	0.22uF	RC0805	445-1350-1-ND	C2012X7R1H224K	TDK
10	1	C27	0.033uF	RC0603	PCC1769CT-ND	ECJ-1VB1E333K	Panasonic
11	1	C32	0.03uF	Axial	75-125LS30	125LS30	Vishay
12	1	C36	NC	Axial			
13	1	D3	1N4736A	DO41	1N4736ADICT-ND	1N4736A-T	DIODES
14	2	D5,D6	LED	RADIAL	67-1612-ND	SSL-LX5093SRC/E	LUMEX
15	1	D7	BAT54S/SOT	SOT23	BAT54SDICT-ND	BAT54S-7	DIODES
16	2	D8,D9	UCLAMP3301D	SOD-323	--	UCLAMP3301D.TCT	SEMTECH
17	1	J1	DC Connector	RAPC712	SC1152-ND	RAPC712	Switchcraft
18	1	J2	HEADER 8X2	8X2PIN	S2011-36-ND	PZC36DAAN	Sullins
19	2	J3,J16	HEADER 3	3X1PIN	S1011-36-ND	PZC36SAAN	Sullins
20	1	J13	HEADER 2	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins

Table 4-3: 71M6511 2-Layer Demo Board (Transformer Power Supply): Bill of Material (1/2)

21	2	J4,J9	Spade Terminal		A24747CT-ND	62395-1	AMP
22	2	J12,J17	HEADER 5	5X1PIN	S1011-36-ND	PZC36SAAN	Sullins
23	1	J14	10X2 CONNECTOR		A3210-ND	104068-1	AMP
24	2	JP1,JP17	HEADER 2	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
25	4	JP4,JP8,JP10,JP16	HEADER 3	3X1PIN	S1011-36-ND	PZC36SAAN	Sullins
26	10	L1-L10	Ferrite bead, 600 Ohm	RC1206	445-1556-1-ND	MMZ2012S601A	TDK
27	1	RV1	VARISTOR	radial	581-VZD510XX	VE24M00511K	AVX
28	1	R1	200	RC0603	P200GCT-ND	ERJ-3GEYJ201V	Panasonic
29	1	R2	8.06K, 1%	RC0603	P8.06KHCT-ND	ERJ-3EKF8061V	Panasonic
30	1	R3	0	RC0603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
31	1	R4	25.5K, 1%	RC0603	P25.5KHCT-ND	ERJ-3EKF2552V	Panasonic
32	1	R7	130, 1%	RC1206	311-130FCT-ND	9C12063A1300FGHFT	Yageo
33	1	R8	1	RC1206	311-1.00FCT-ND	9C12063A1R00FGHFT	Yageo
34	1	R9	68, 1%	RC1206	311-68.0FCT-ND	9C12063A68R0FKHFT	Yageo
35	6	R10-R12,R97-R99	62	RC0603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
36	3	R14,R32,R104	750, 1%	RC0603	P750HCT-ND	ERJ-3EKF7500V	Panasonic
37	1	R15	2M, 1%	Axial	71-RN65DF-2.0M	RN65D2004FB14	Dale
38	2	R16,R17	274K, 1%	RC0805	P274KCCT-ND	ERJ-6ENF2743V	Panasonic
39	1	R18	698, 1%	RC0805	P698CCT-ND	ERJ-6ENF6980V	Panasonic
40	4	R24,R25,R106,R107	3.4, 1%	RC1206	311-3.40FCT-ND	9C12063A3R40FGHFT	Yageo
41	4	R13,R74,R76,R94	10K	RC0603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
42	1	R77	10	RC0603	P10GCT-ND	ERJ-3GEYJ100V	Panasonic
43	1	R79	100	RC0603	P100GCT-ND	ERJ-3GEYJ101V	Panasonic
44	1	R82	1K	RC0603	P1.0KGCT-ND	ERJ-3GEYJ102V	Panasonic
45	1	R83	10.0K, 1%	RC0603	P10.0KHCT-ND	ERJ-3EKF1002V	Panasonic
46	1	R84	47K	RC0603	P47KGCT-ND	ERJ-3GEYJ473V	Panasonic
47	1	R86	21.5K	RC0603	P21.5KHCT-ND	ERJ-3EKF2152V	Panasonic
48	5	R112-R116	NC	RC0603			
49	5	R88,R89,R108,R109,R119	3K	RC0603	P3.0KGCT-ND	ERJ-3GEYJ302V	Panasonic
50	2	R110,R111	0	RC1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
51	1	R118	10, 2W	Axial	10W-2-ND	RSF200JB-10R	Yageo
52	1	SW2	SWITCH		P8051SCT-ND	EVQ-PJX05M	Panasonic
53	1	T3	TRNSFMR 67115100				
54	8	TP1,TP2,TP7,TP10,TP17,	Test Point	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
55		TP19,TP21,TP22					
56	1	TP10	Test Point	3X1PIN	S1011-36-ND	PZC36SAAN	Sullins
57	3	TP13-TP15	Test Point	Test Point	5011K-ND	5011	Keystone
58	1	TP20	HEADER 5X2	5X2PIN	S2011-36-ND	PZC36DAAN	Sullins
59	2	U1,U6	BAV99DW	SOT363	BAV99DWDICT-ND	BAV99DW-7	DIODES
60	1	U3	REGULATOR, 1%	SO8	296-1288-1-ND	TL431AIDR	Texas Instruments
61	1	U4	EEPROM	SOIC8	AT24C1024W10SI2.7-ND	AT24C1024W-10SI-2.7	ATMEL
62	1	U5	71M6511	64TQFP	--	71M6511-IGT	TERIDIAN
63	1	at U5	64TQFP Socket	64TQFP	--	IC149-064-169-S5	Yamaichi
64	1	Y1	32.768kHz		XC488CT-ND	ECS-.327-12.5-17-TR	ECS
65	1	U7	LCD		153-1056-ND	VIM-808-DP-RC-S-HV	VARITRONIX

Table 4-4: 71M6511 2-Layer Demo Board (Transformer Power Supply): Bill of Material (2/2)

4.7 71M6511 4-LAYER DEMO BOARD PCB LAYOUT

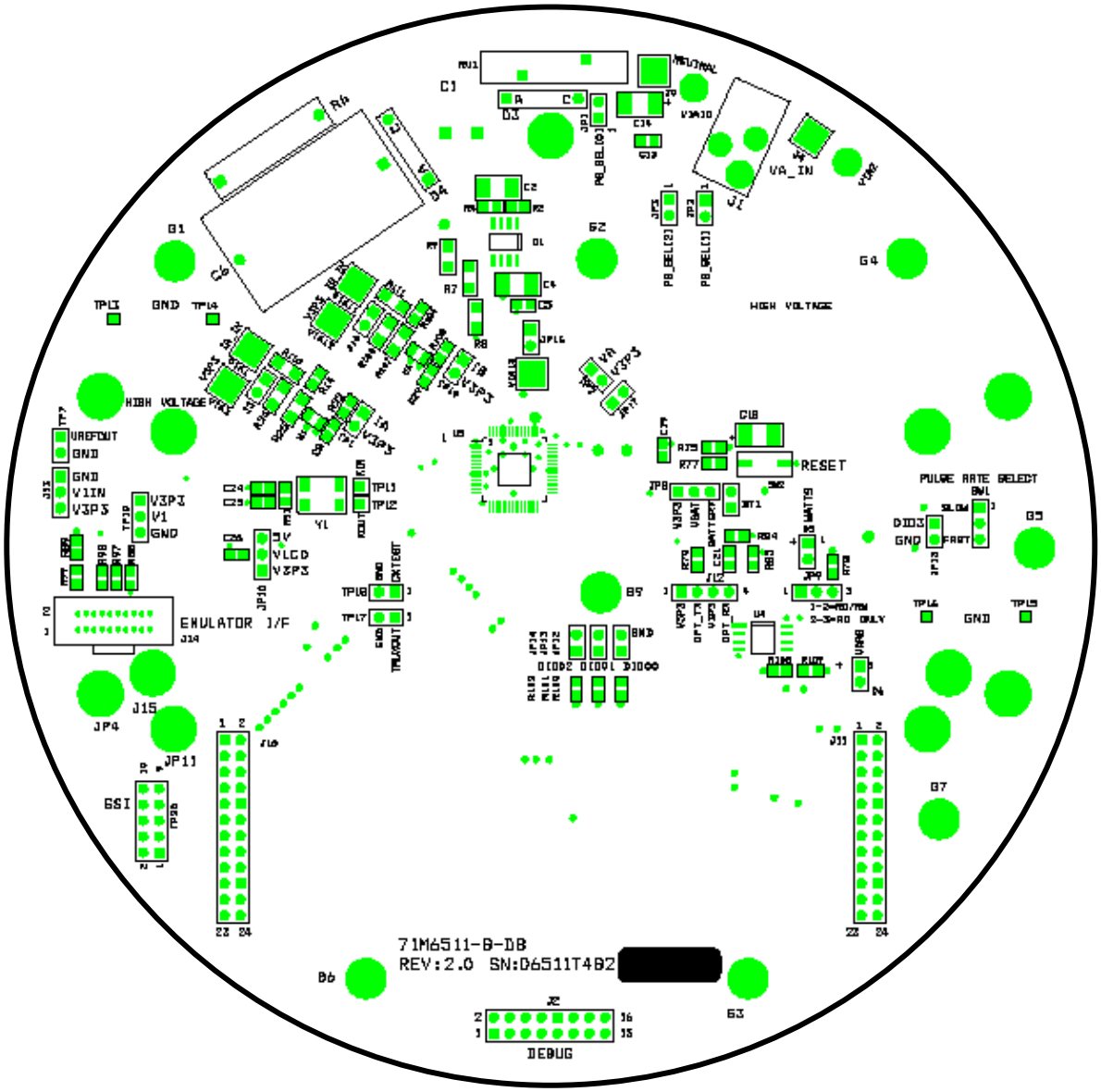


Figure 4-10: 71M6511 4-Layer Demo Board: Top View

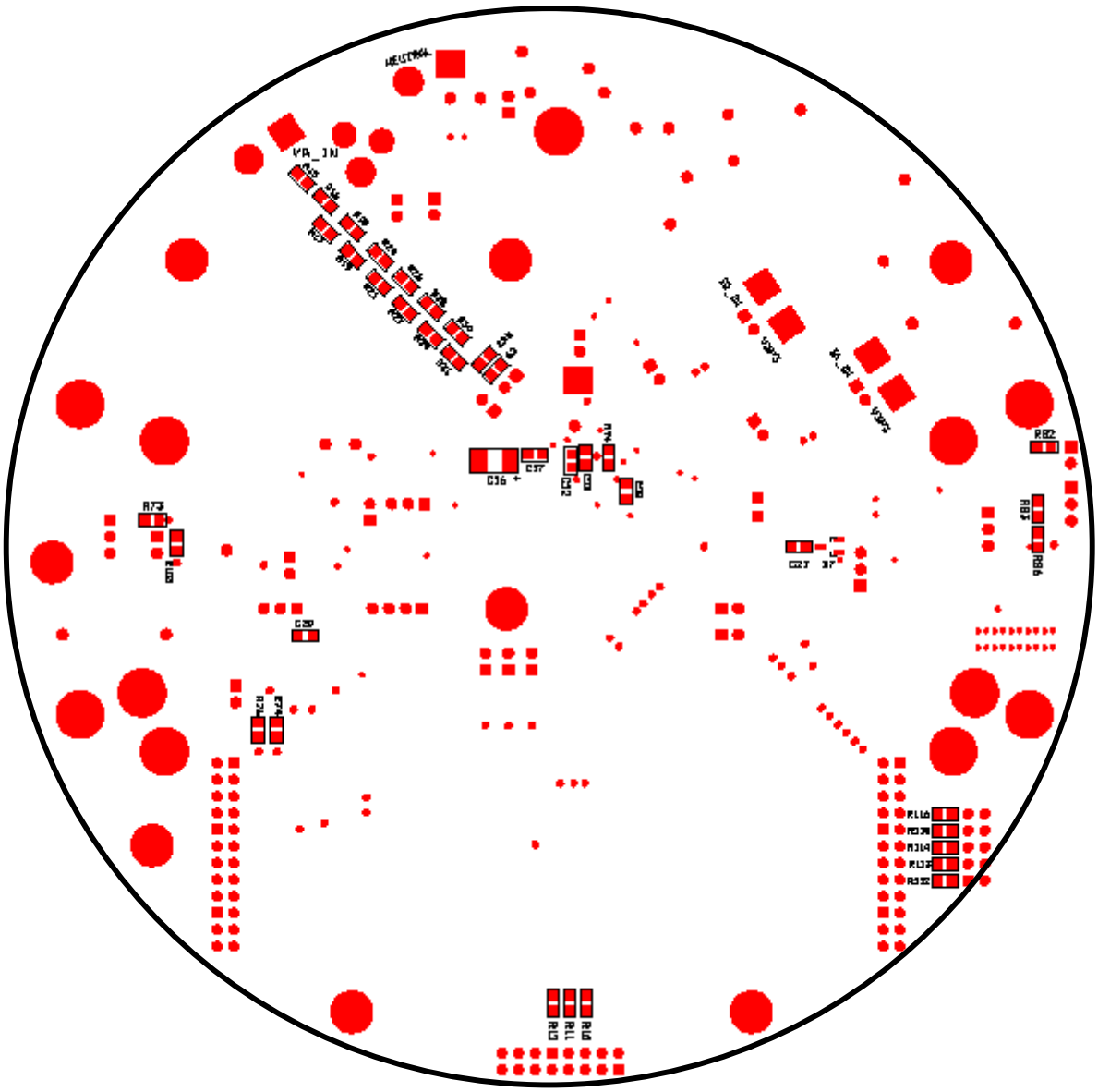


Figure 4-11: 71M6511 4-Layer Demo Board: Bottom View

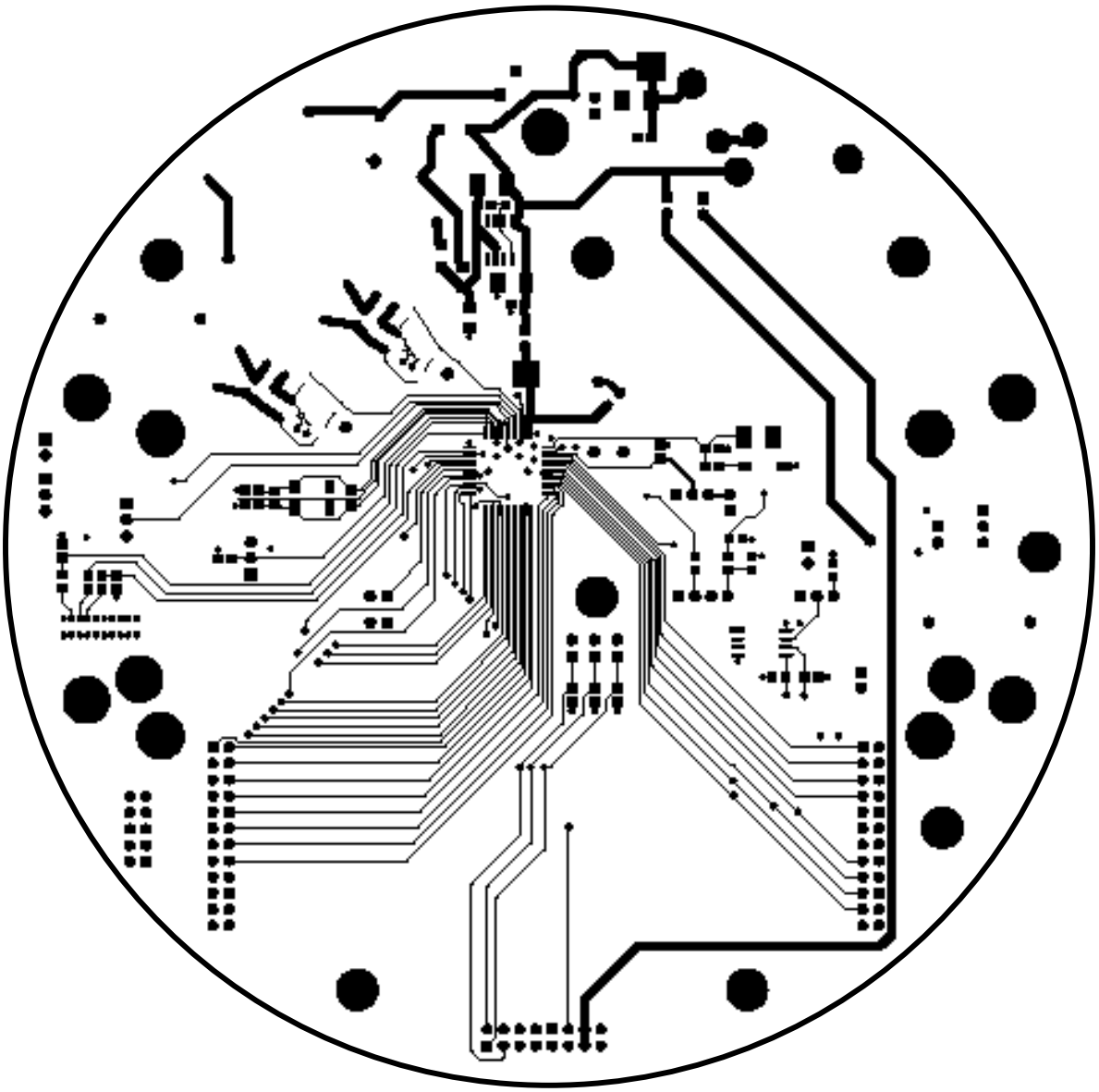


Figure 4-12: 71M6511 4-Layer Demo Board: Top Signal Layer

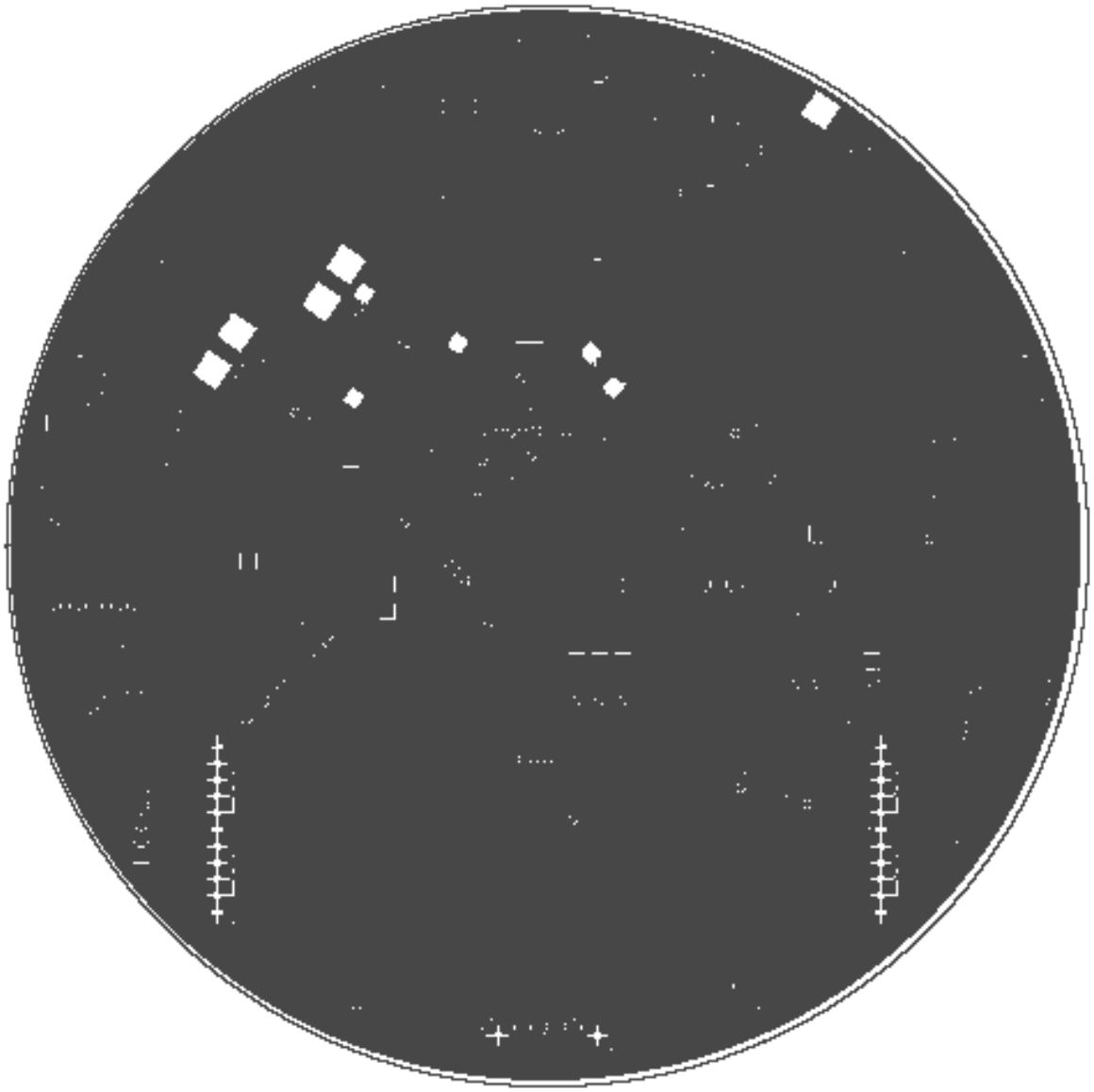


Figure 4-13: 71M6511 4-Layer Demo Board: Middle Layer 1, Ground Plane.

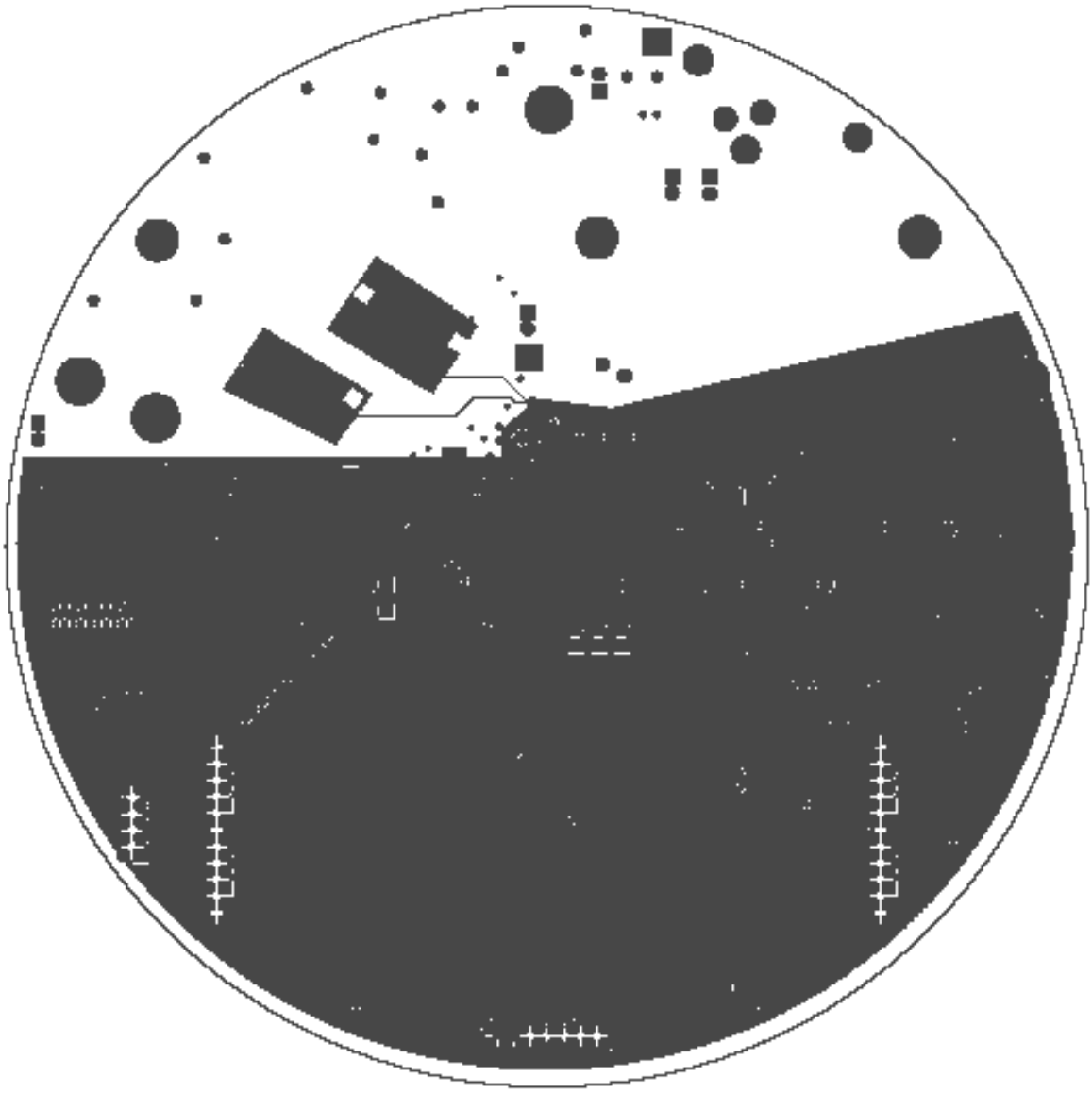


Figure 4-14: 71M6511 4-Layer Demo Board: Middle Layer 2, Supply Plane

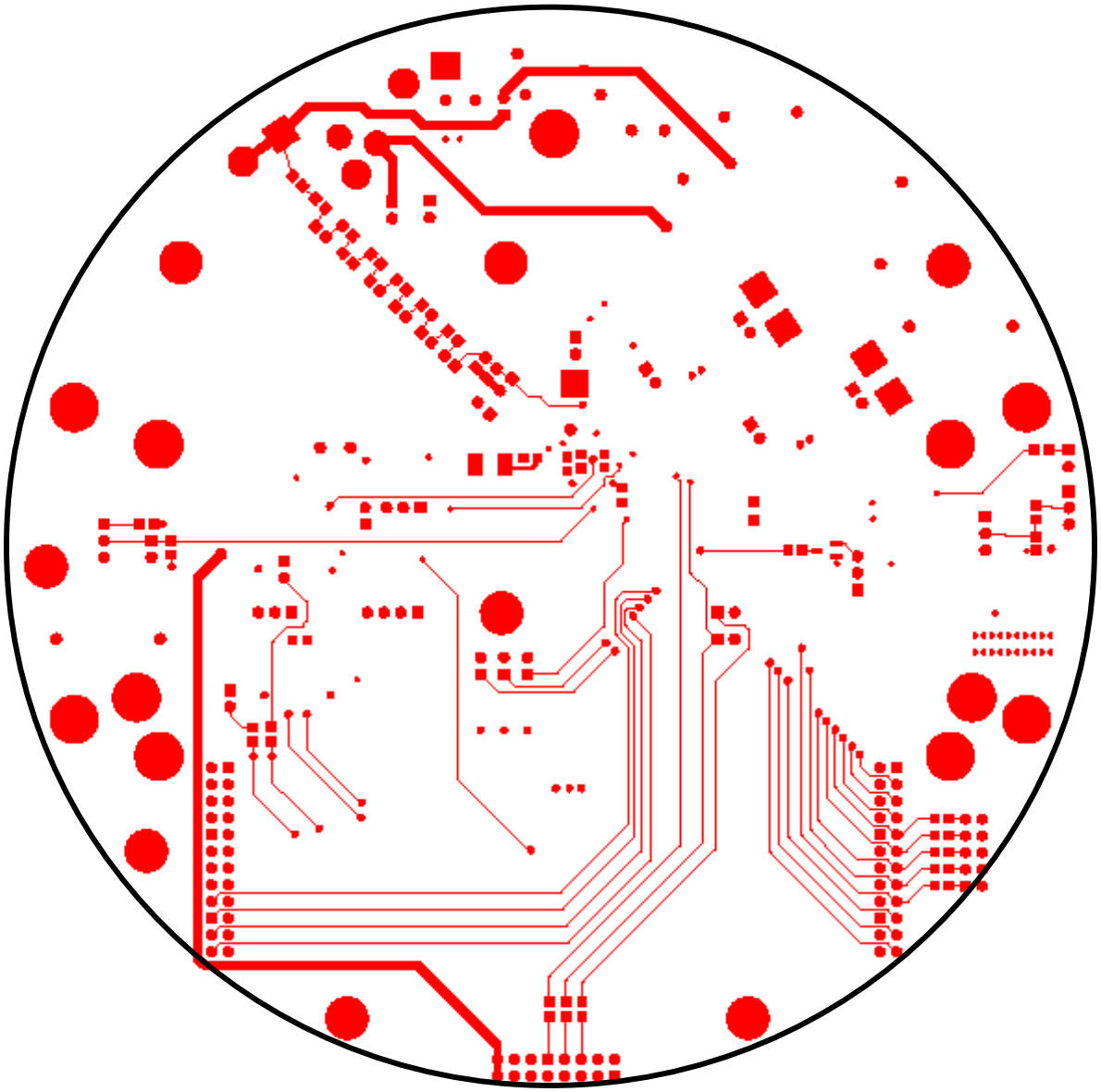


Figure 4-15: 71M6511 4-Layer Demo Board: Bottom Signal Layer

4.8 PCB LAYOUT FOR THE 71M6511 2-LAYER DEMO BOARD (CAPACITIVE POWER SUPPLY)

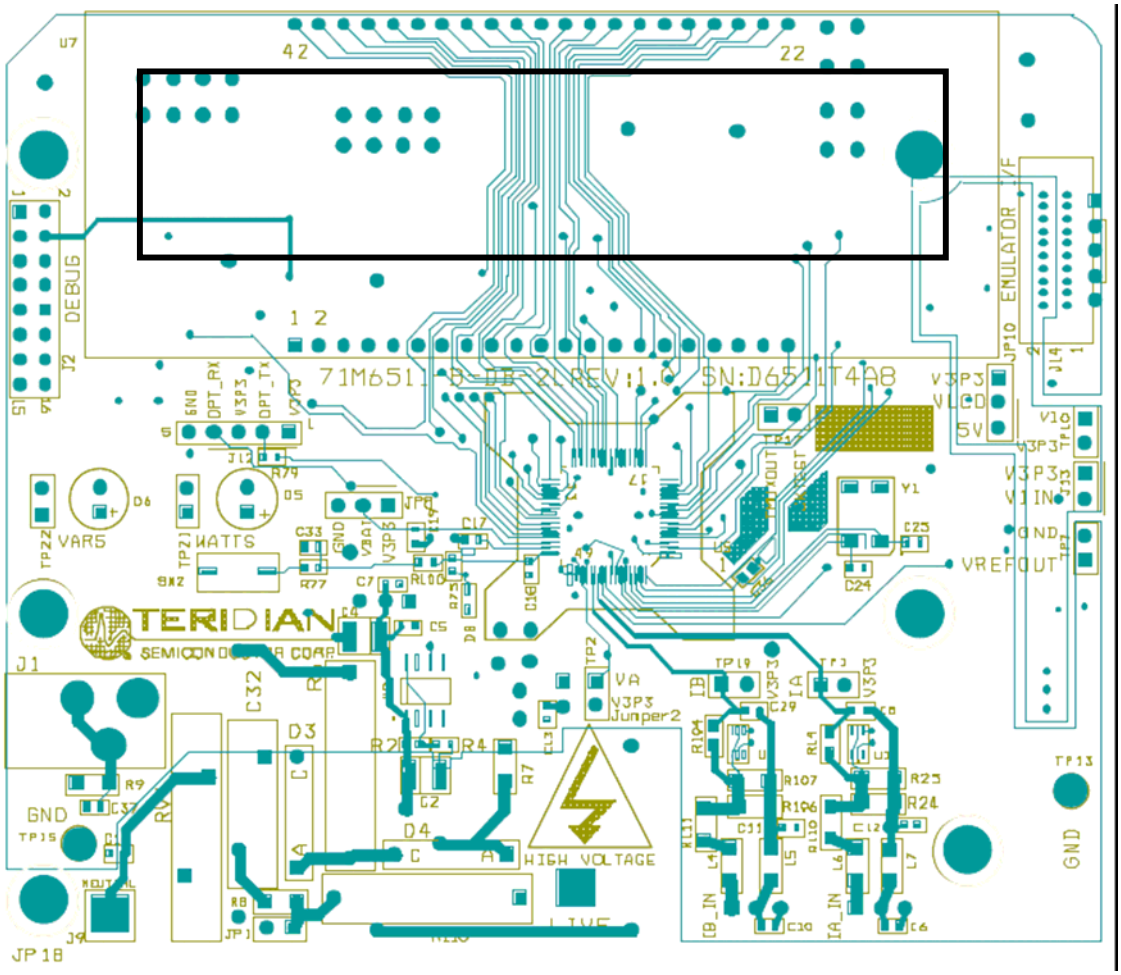


Figure 4-16: DM6511T4A8 2-Layer Demo Board (Capacitive Power Supply): Top View

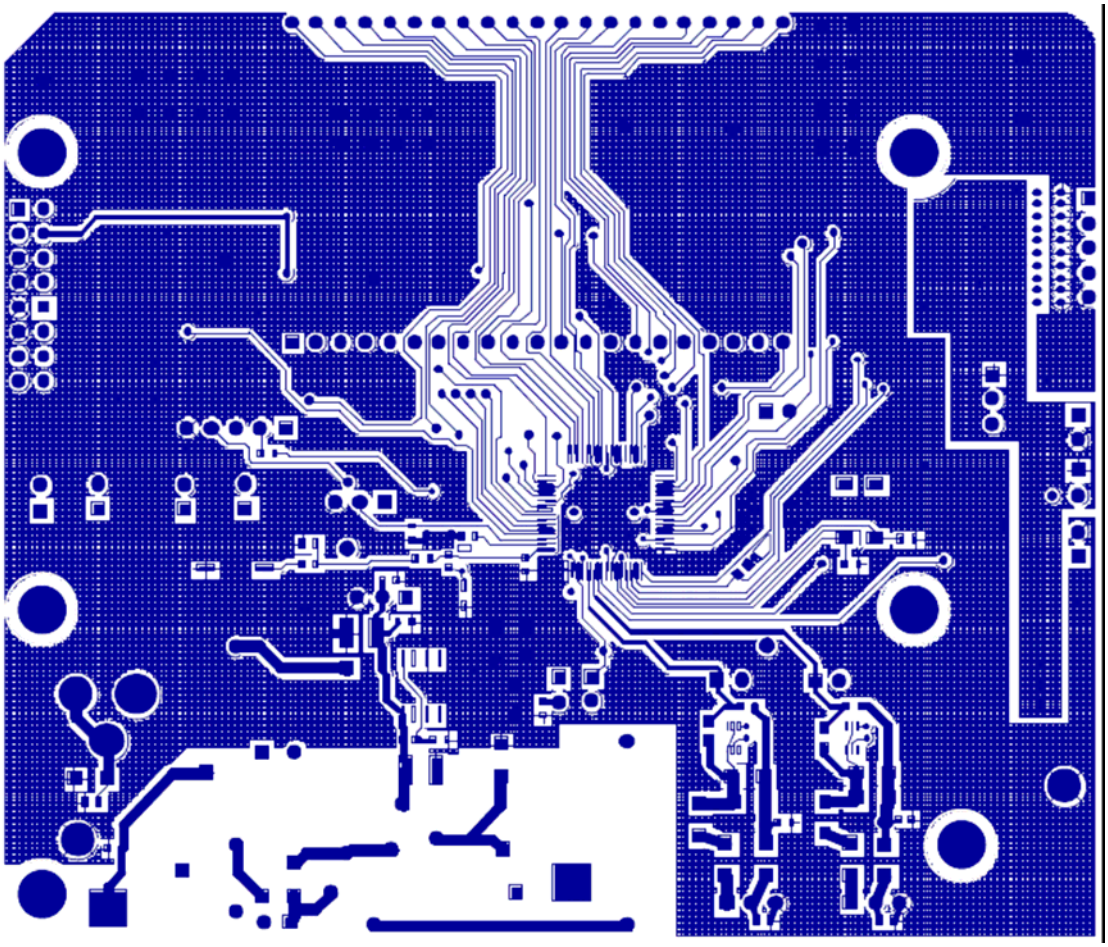


Figure 4-17: D6511T4A8 2-Layer Demo Board (Capacitive Power Supply): Top Copper Layer

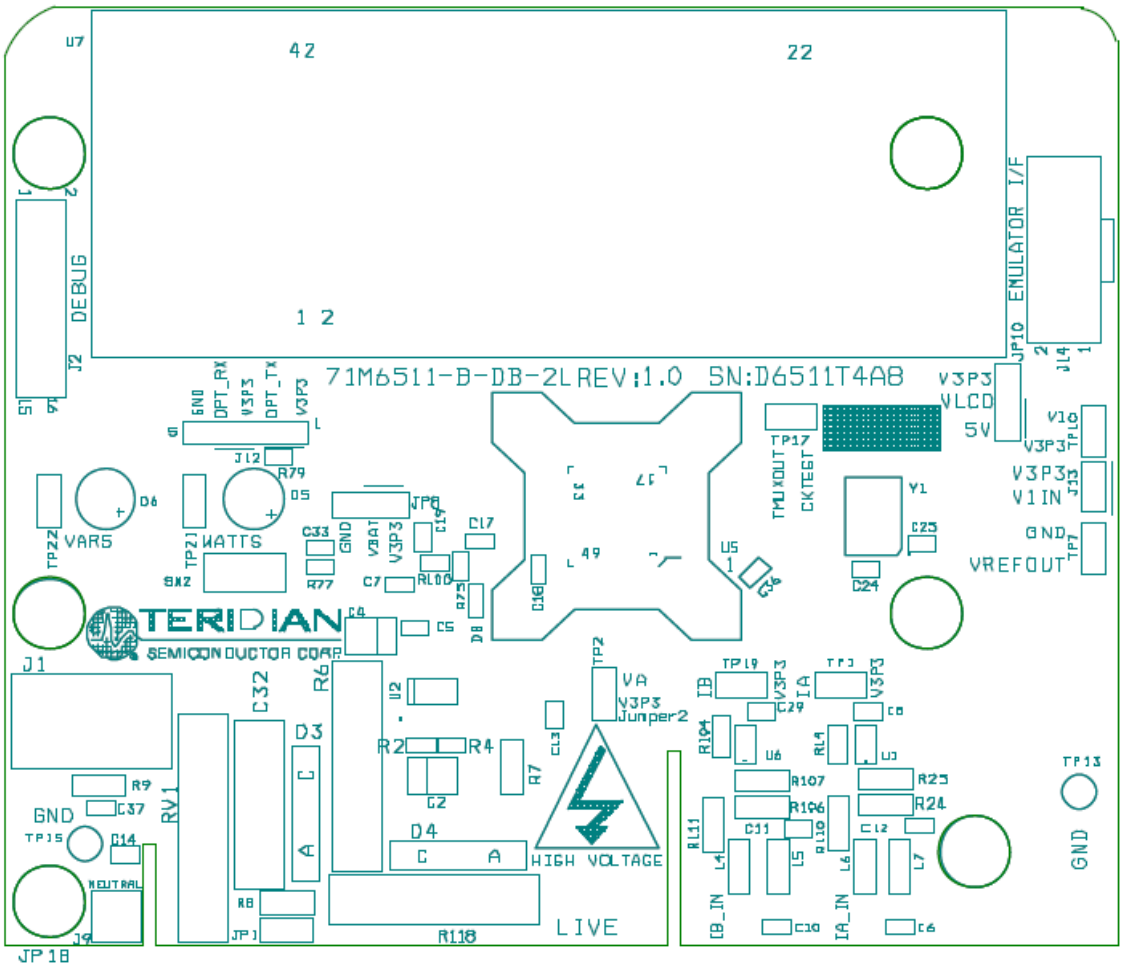


Figure 4-18: D6511T4A8 2-Layer Demo Board (Capacitive Power Supply): Top Silk-Screen View

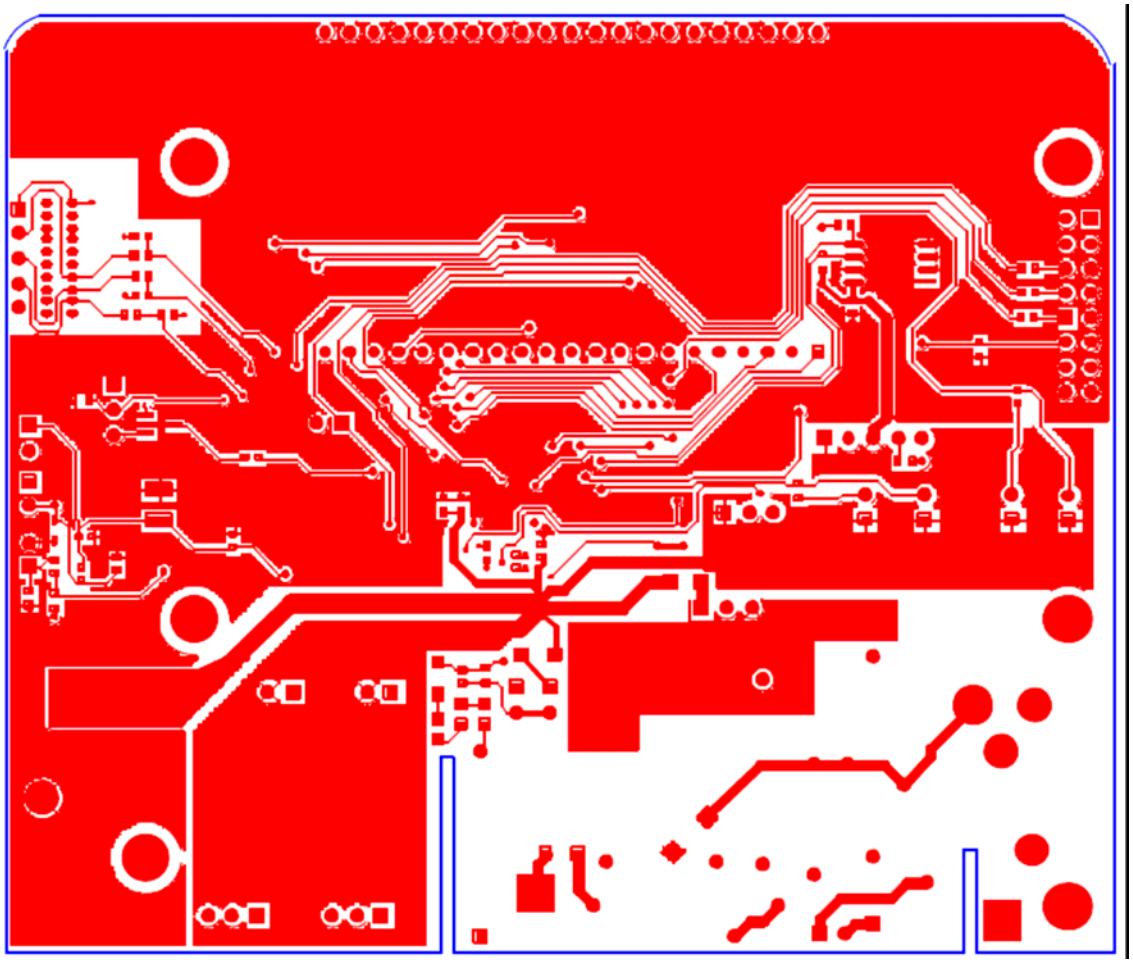


Figure 4-19: D6511T4A8 2-Layer Demo Board (Capacitive Power Supply): Bottom Copper Layer

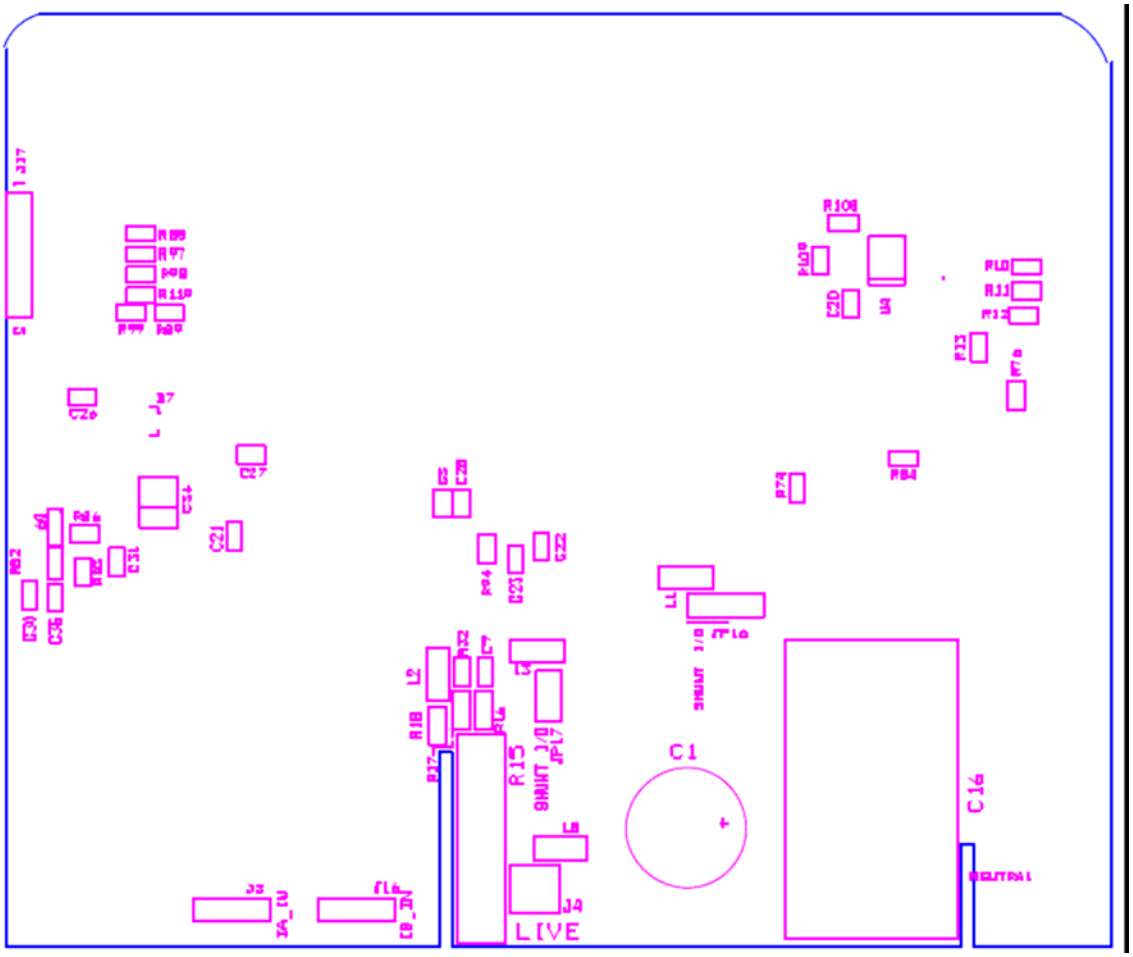


Figure 4-20: D6511T4A8 2-Layer Demo Board (Capacitive Power Supply): Bottom Silk Screen

4.9 PCB LAYOUT FOR THE 71M6511 2-LAYER DEMO BOARD (TRANSFORMER POWER SUPPLY)

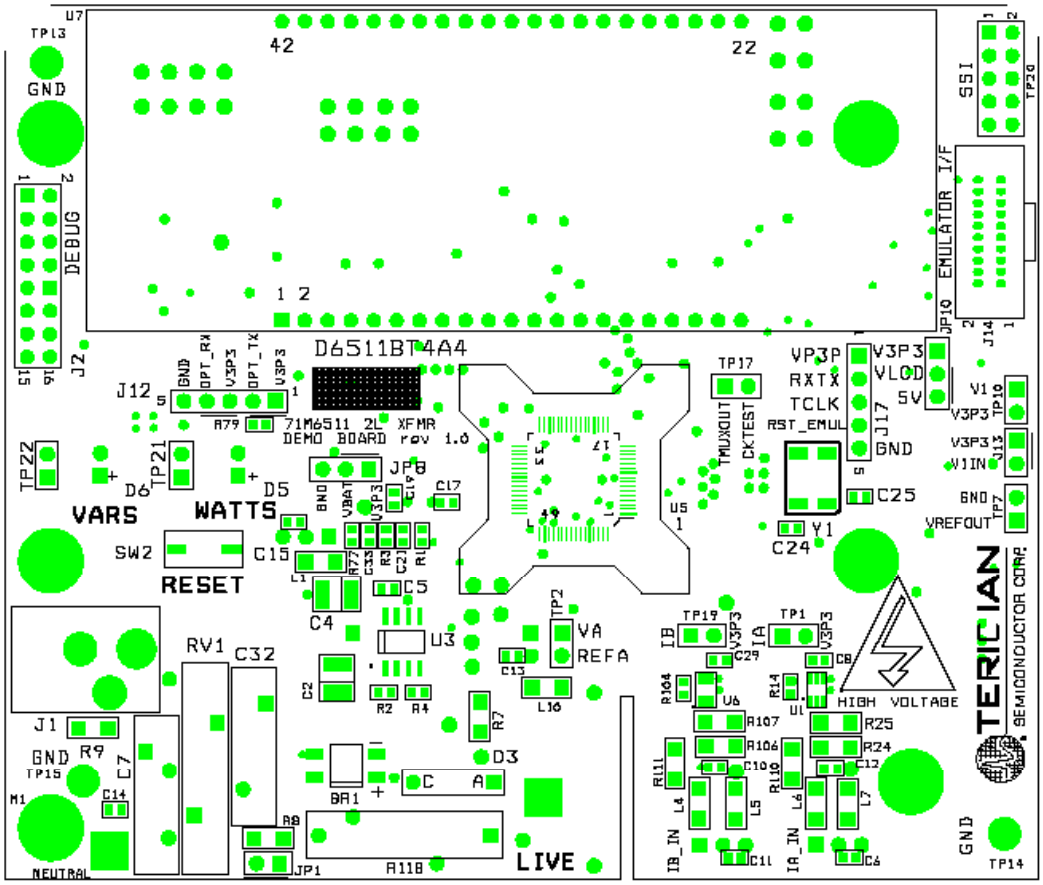


Figure 4-21: 71M6511 2-Layer Demo Board (Xformer Power Supply): Top View

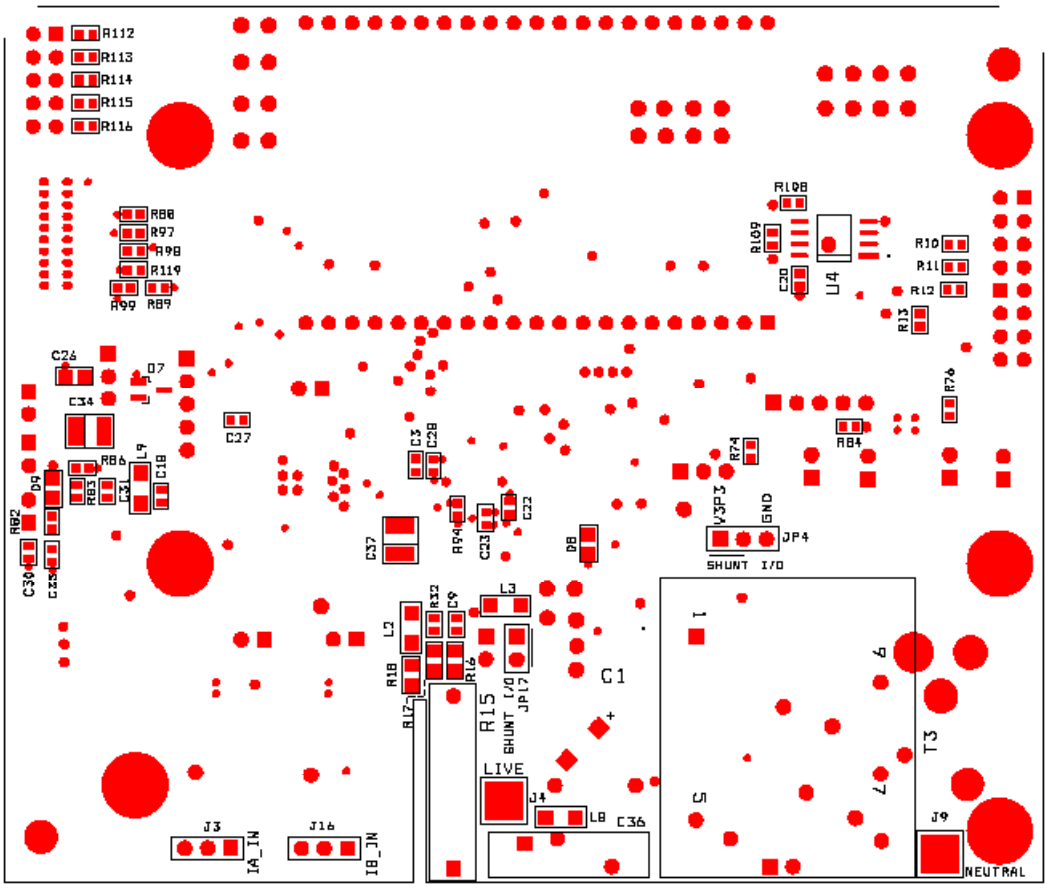


Figure 4-22: 71M6511 2-Layer Demo Board (Xformer Power Supply): Bottom View

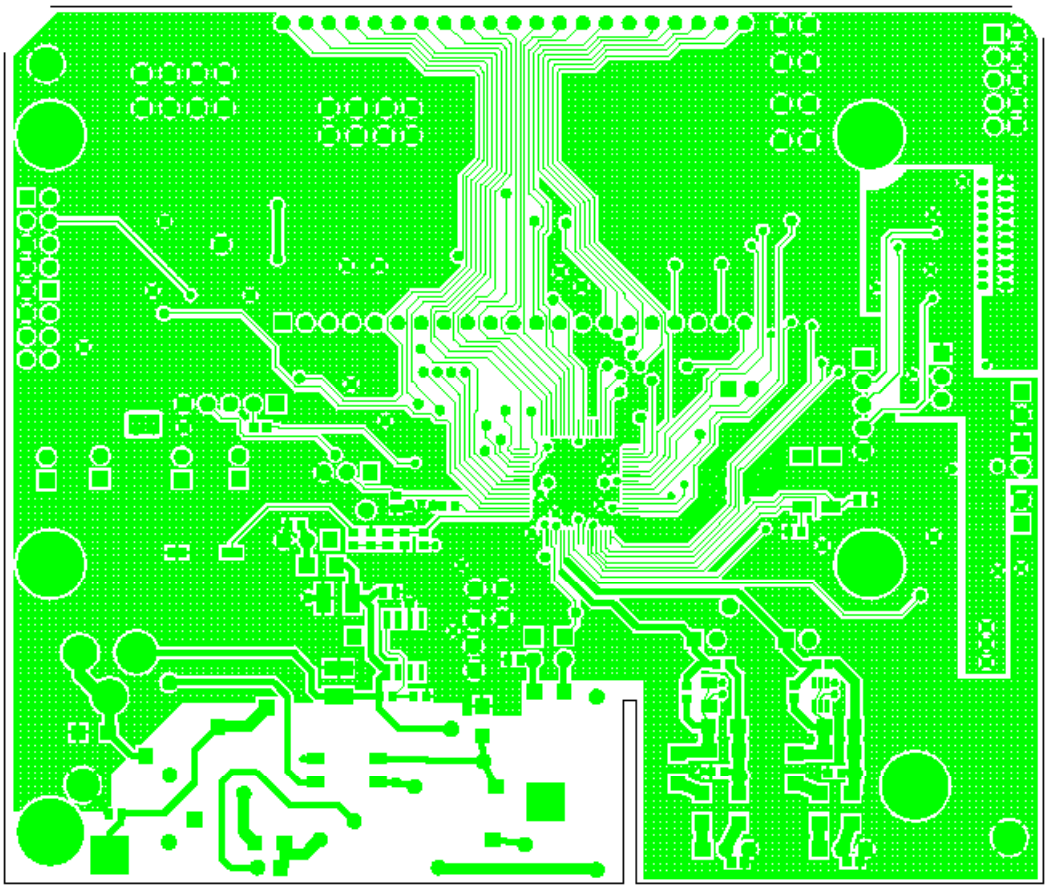


Figure 4-23: 71M6511 2-Layer Demo Board (Xformer Power Supply): Top Copper View

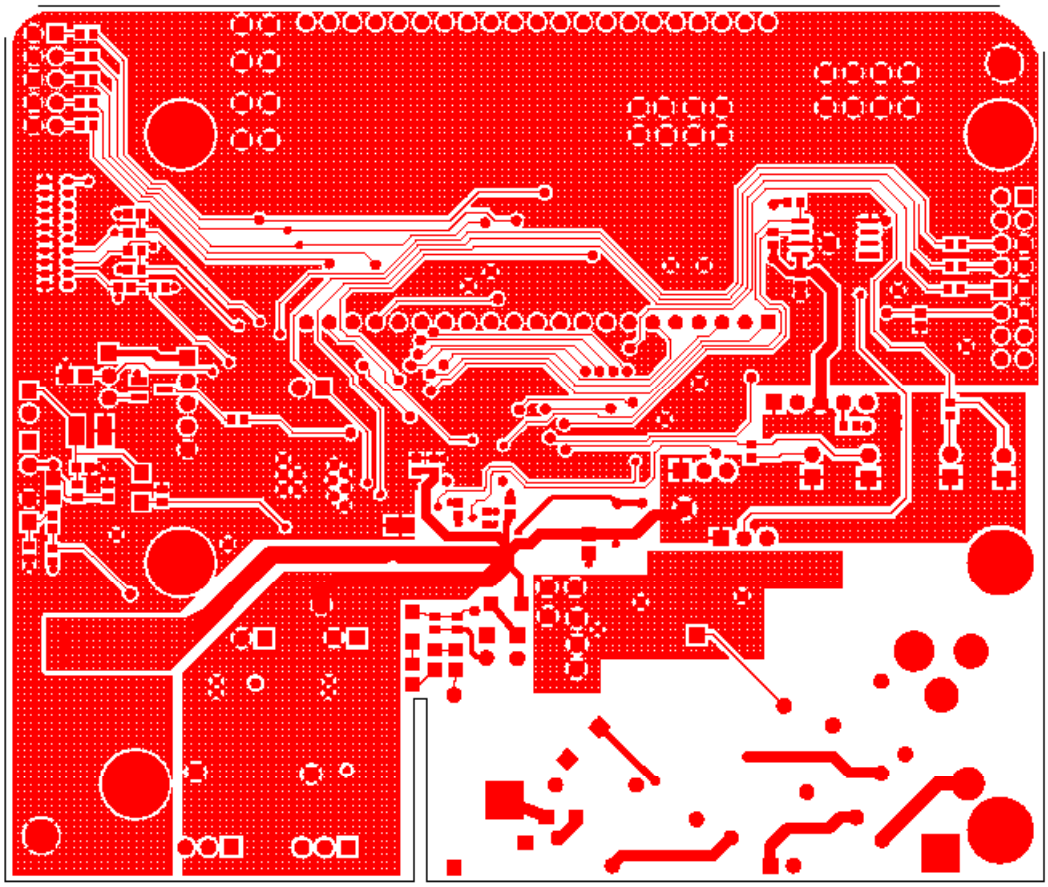


Figure 4-24: 71M6511 2-Layer Demo Board (Xformer Power Supply): Bottom Copper View

4.10 DEBUG BOARD BILL OF MATERIAL

Item	Quantity	Reference	Part	PCB Footprint	Digi-Key Part Number	Part Number	Manufacturer
1	21	C1-C3,C5-C10,C12-C23	0.1uF	RC0805	445-1349-1-ND	C2012X7R1H104K	TDK
2	1	C4	33uF, 10V	RC1812	478-1687-1-ND	TAJB336K010R	AVX
3	1	C11	10uF, 16V	RC1812	478-1673-1-ND	TAJB106K016R	AVX
4	2	D2,D3	LED	RC0805	160-1414-1-ND	LTST-C170KGKT	LITEON
5	4	G1,G2,G3,G4	Spacer	MTHOLE	2202K-ND	2202K-ND	Keystone Electronics
6	4		4-40, 1/4" screw		H342-ND	PMS 4400 - 0025 PH	Building Fasteners
7	2		4-40, 5/16" screw		H343-ND	PMS 4400- 0031 PH	Building Fasteners
8	2		4-40 nut		H216-ND	HNZ440	Building Fasteners
9	1	J1	DC Connector	RAPC712	SC1152-ND	RAPC712	Switchcraft
10	1	J2	DB9, right angle	DSUB9_SKT	A2100-ND	745781-4	AMP
11	1	J3	HEADER (F) 8X2	8X2PIN	929852-01-36-ND	929852-01-36-10	3M
12	4	JP1,JP2,JP3,JP4	HEADER 2	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
13	4	R1,R5,R7,R8	10K	RC0805	P10KACT-ND	ERJ-6GEYJ103V	Panasonic
14	2	R2,R3	1K	RC0805	P1.0KACT-ND	ERJ-6GEYJ102V	Panasonic
15	1	R4	NC	RC0805	N/A	N/A	N/A
16	1	R6	0	RC0805	P0.0ACT-ND	ERJ-6GEY0R00V	Panasonic
17	1	SW2	PB switch		P8051SCT-ND	EVQ-PJX05M	Panasonic
18	5	U1,U2,U3,U5,U6	ISOLATOR	SOIC8	ADUM1100AR-ND	ADUM1100AR	ADI
19	2	TP5,TP6	Test Point	--	5011K-ND	5011	Keystone Electronics
20	1	U4	RS232 DRIVER	28SSOP	MAX3237CAI-ND	MAX3237CAI	MAXIM

Table 4-5: Debug Board: Bill of Material

4.11 DEBUG BOARD SCHEMATICS

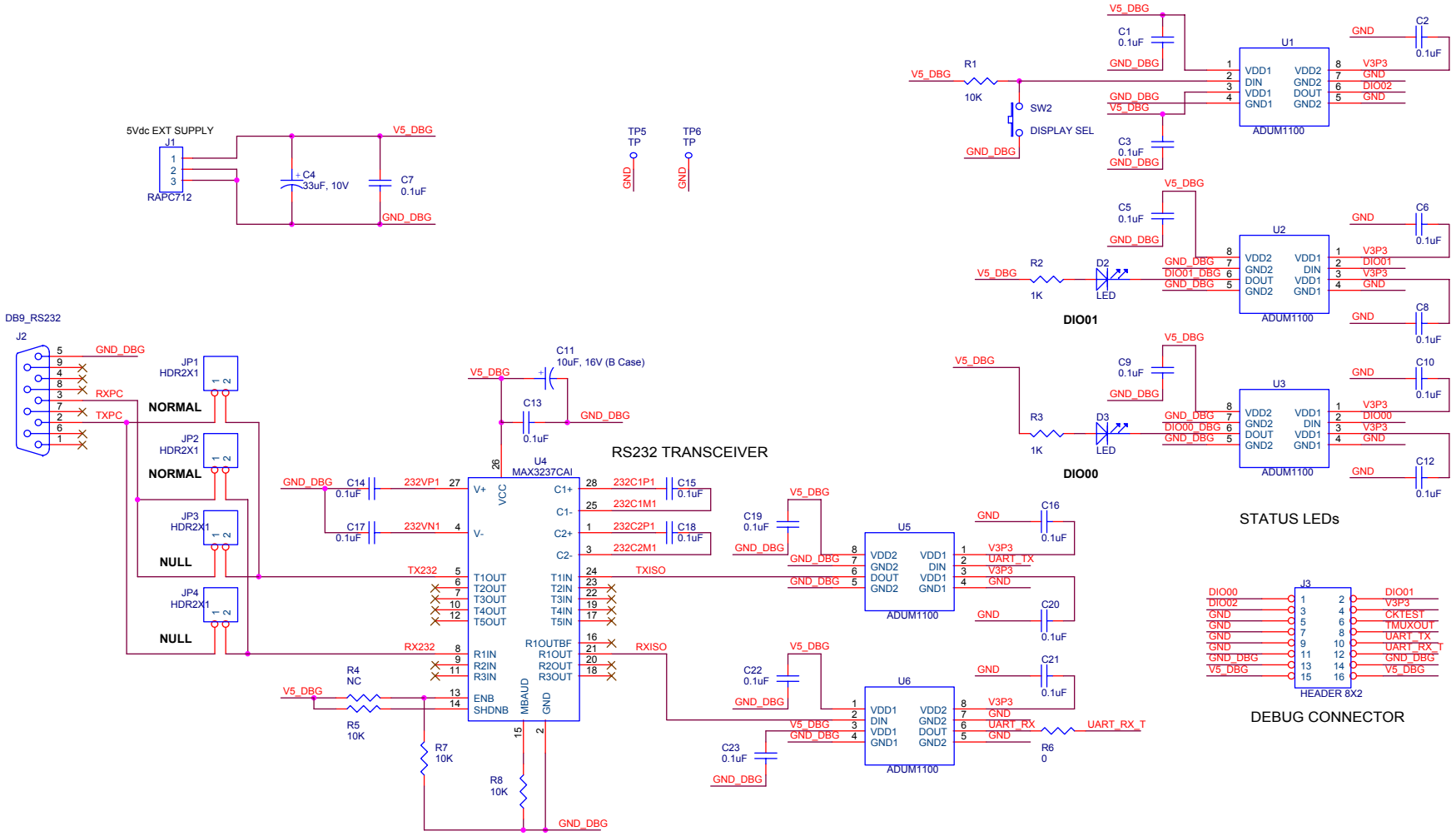


Figure 4-25: Debug Board: Electrical Schematic

4.12 DEBUG BOARD PCB LAYOUT

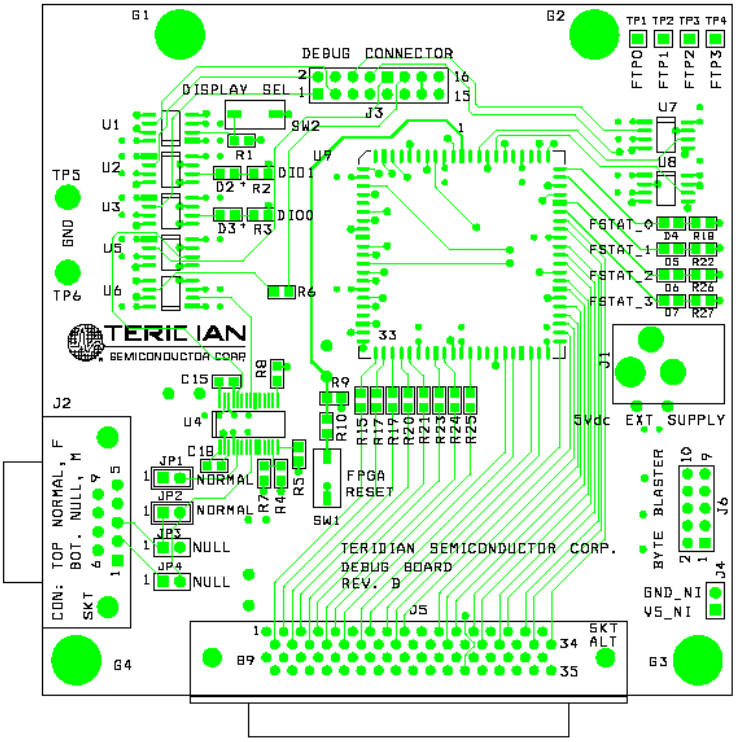


Figure 4-26: Debug Board: Top View

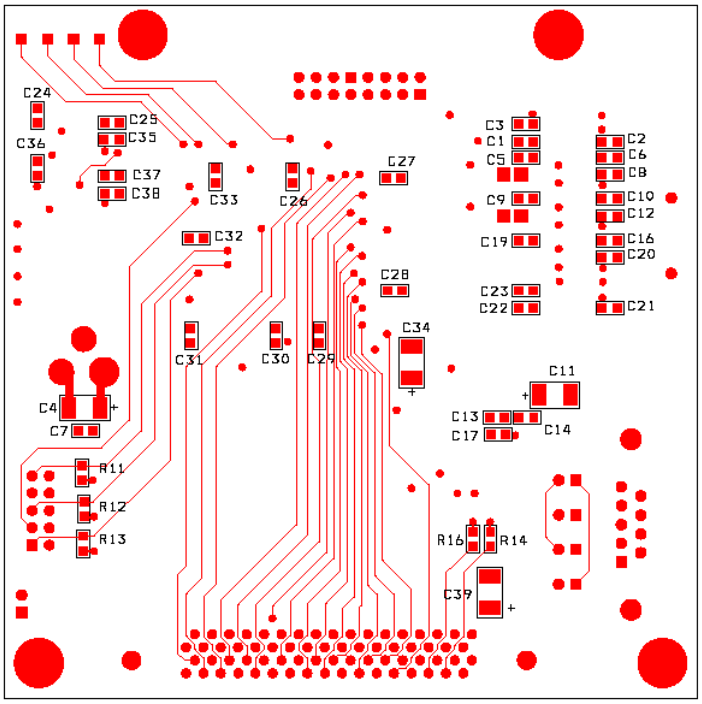


Figure 4-27: Debug Board: Bottom View

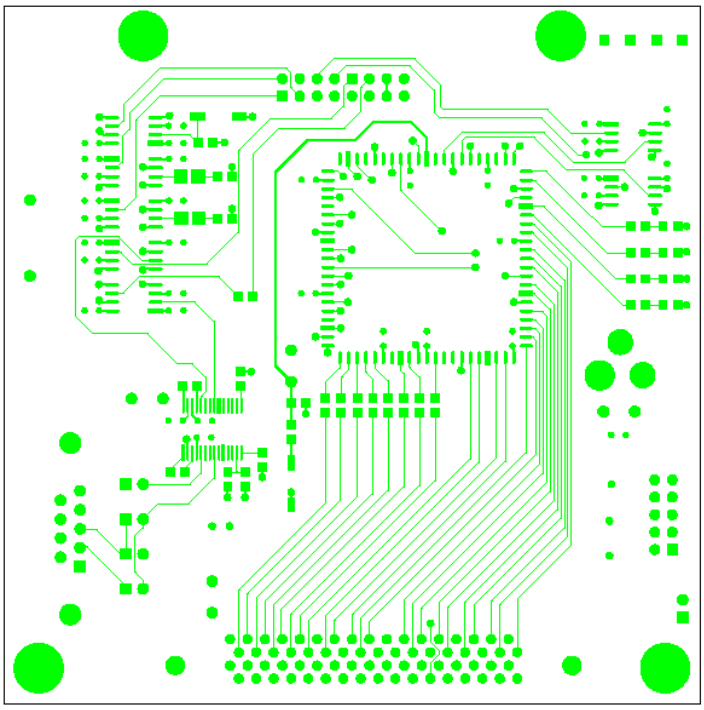


Figure 4-28: Debug Board: Top Signal Layer

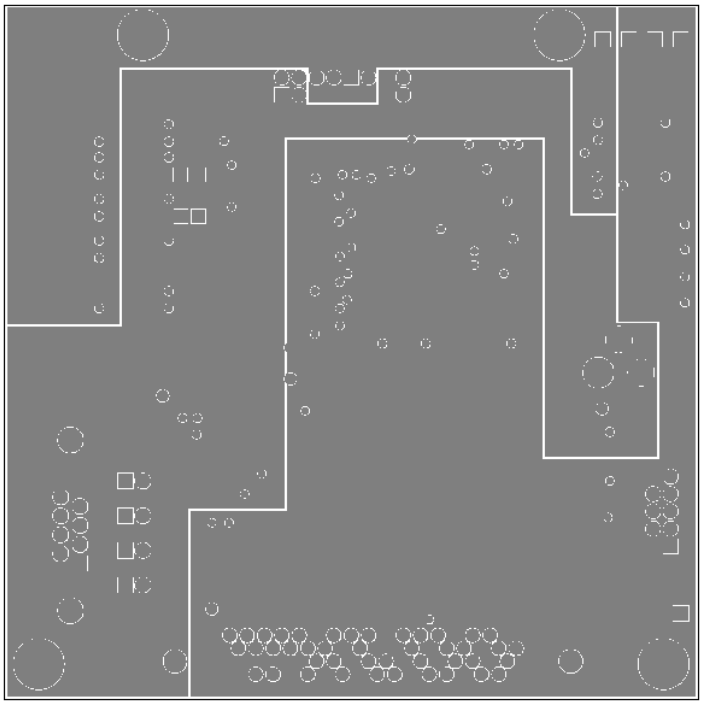


Figure 4-29: Debug Board: Middle Layer 1, Ground Plane

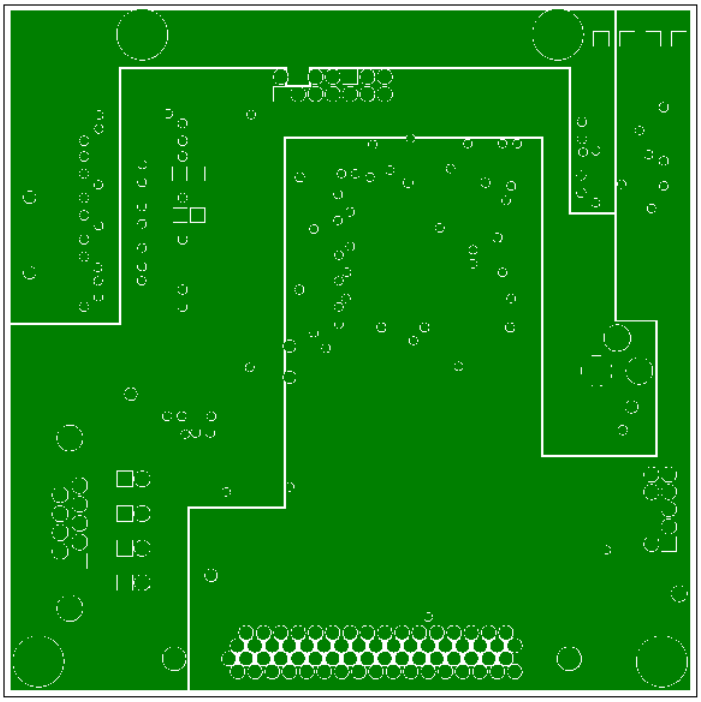


Figure 4-30: Debug Board: Middle Layer 2, Supply Plane

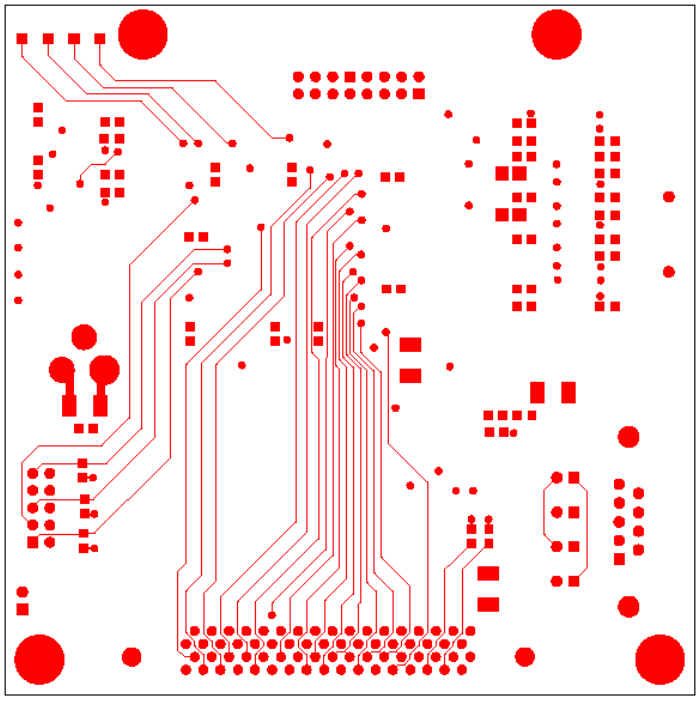


Figure 4-31: Debug Board: Bottom Trace Layer

4.13 TERIDIAN 71M6511/6511H PIN-OUT INFORMATION

***Power/Ground/NC Pins*:**

Name	Pin #	Type	Description
GNDA	49, 58	P	Analog ground: This pin should be connected directly to the ground plane.
GNDD	1	P	Digital ground: This pin should be connected directly to the ground plane.
V3P3A	50	P	Analog power supply: A 3.3V power supply should be connected to this pin.
V3P3D	9	P	Digital power supply: A 3.3V power supply should be connected to this pin.
VBAT	46	P	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
V2P5	47	O	Output of the internal 2.5V regulator. This pin should be bypassed to GND with a 0.1µF capacitor
VLCD	62	P	LCD power supply.

Analog Pins:

Name	Pin #	Type	Description
IA	54	I	Line Current Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a current transformer.
VA	51	I	Line Voltage Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a resistor divider.
IB	53	I	Line Current Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a current transformer.
V1	56	I	For normal operation, a voltage of 2.6V to 2.8V has to be supplied to this pin. A voltage below VBIAS will reset the chip. Clamping V1 to V3P3 will disable the hardware watchdog timer.
VREF	55	O	Voltage Reference for the ADC. A 0.1µF capacitor to GNDA should be connected to this pin.
VBIAS	52	O	The reference voltage used by the power fault detection circuit.
XIN XOUT	59 61	I	Crystal Inputs: A 32kHz style crystal should be connected across these pins. Typically, a 10pf capacitor is also connected from each pin to GNDA. It is important to minimize the capacitance between these pins. See crystal manufacturer datasheet for details.
VDRV	7	O	Voltage boost output.

Table 4-6: 71M6511 Pin Description Table 1/2

Digital Pins:

Name	Pin #	Type	Description
COM3, COM2, COM1, COM0	16 15 14 13	O	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG19…SEG8, SEG2…SEG0	See pinout	O	Dedicated LCD Segment Output.
SEG24/DIO4… SEG31/DIO11	See pinout	O	Multi-use pin, configurable as either LCD SEG driver or DIO.
SEG34/DIO14… SEG37/DIO17	See pinout	O	Multi-use pin, configurable as either LCD SEG driver or DIO.
SEG7/MUX_SYNC	24	O	Multi-use-pin LCD Segment Output/ MUX_SYNC is output for Synchronous serial interface
SEG6/SRDY	23	I/O	Multi-use-pin, LCD Segment Outputs/ SRDY input for Synchronous serial interface.
SEG5/SFR	11	O	Multi-use-pin, LCD Segment Output/ SFR output for Synchronous serial interface.
SEG4/SDATA	10	O	Multi-use-pin, LCD Segment Output/ SDATA output for Synchronous serial interface.
SEG3/SCLK	6	O	Multi-use-pin, LCD Segment Output/ SCLK output for Synchronous serial interface.
CKTEST	8	O	Clock PLL output. Can be enabled and disabled by *CKOUT_EN*.
TMUXOUT	4	O	Digital output test multiplexer. Controlled by *DMUX[3:0].*
OPT_RX	57	I	OPT LED Receive Input: This pin receives a signal from an external photo-detect diode used in an IR serial interface.
OPT_TX	3	O	OPT LED Transmit Output: This pin is designed to directly drive an LED for transmitting data in an IR serial interface. Can be tristated with *OPT_TXDIS* to be multiplexed with other GPIO pins.
RESETZ	48	I	Chip reset: This input pin is used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0. This pin has an internal 30µA (nom.) current source pull up. A 0.1µF capacitor to GNDD should be connected to this pin.
RX	45	I	UART input.
TX	5	O	UART output.
E_RXTX	2	I/O	Emulator serial data. This pin has an internal pull-up resistor.
E_TCLK	64	O	Emulator clock. This pin has an internal pull-up resistor.
E_RST	63	I/O	Emulator reset. This pin has an internal pull-up resistor.
TEST	60	I	Enables Production Test. Must be grounded in normal operation.

Table 4-7: 71M6511 Pin Description Table 2/2

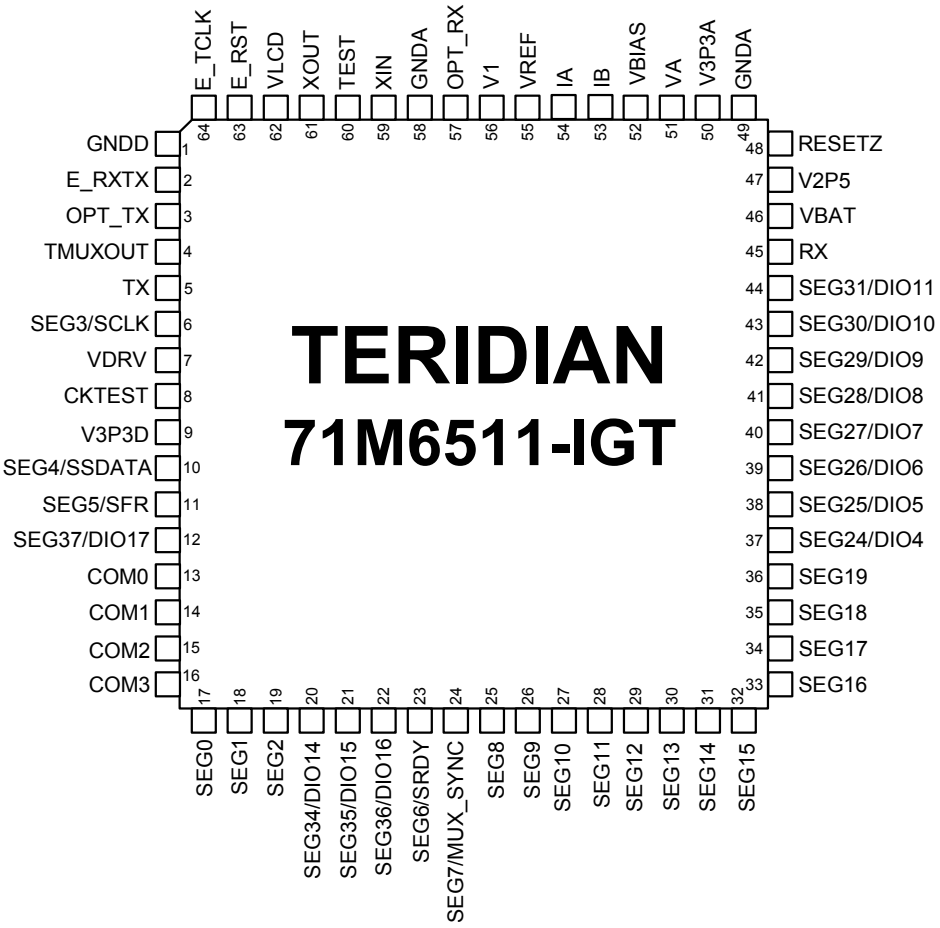


Figure 4-32: TERIDIAN 71M6511 LQFP64: Pinout (Top View)

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