nRF54LM20 DK Hardware

v0.3.4

User Guide

4541_018 / 2025-09-17

NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
September 2025	First release

Environmental and safety notices

Power supply

The nRF54LM20 DK must be powered by a PS1 class (IEC 62368-1) power supply with maximum power less than 15 W.

Skilled persons

The nRF54LM20 DK is intended for use only by skilled persons.

A skilled person is someone with relevant education or experience that enables them to identify potential hazards and takes appropriate action to reduce the risk of injury to themselves and others.

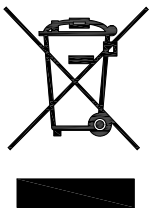
Hot surface

In the event of a fault, touchable surfaces can heat up significantly.

Electrostatic discharge

The nRF54LM20 DK is susceptible to *Electrostatic Discharge (ESD)*.

To avoid damage to your device, it should be used in an electrostatic free environment, such as a laboratory.



Environmental Protection

Waste electrical products should not be disposed of with household waste.

Please recycle where facilities exist. Check with your local authority or retailer for recycling advice.

1 Introduction

The nRF54LM20 DK is a hardware development platform used to design and develop application firmware on the nRF54LM20A SoC.

Key features

- nRF54LM20A SoC in CSP (FCCSP) package
- Support for the following wireless protocols:
  - *Bluetooth*® Low Energy
  - 802.15.4
  - Thread®
  - Zigbee®
  - 2.4 GHz proprietary
  - NFC
- 2.4 GHz and NFC antennas
- *Microwave coaxial connector with switch (SWF)* RF connector for direct RF measurements
- Four user-programmable LEDs
- Four user-programmable buttons
- SEGGER J-Link OB programmer/debugger
- Two *Universal Asynchronous Receiver/Transmitter (UART)* interfaces through virtual serial ports
- USB connection for powering and interfacing with the nRF54LM20A SoC
- USB connection to debugger for debugging, programming, and power
- Pins for measuring power consumption of the nRF54LM20A SoC
- nPM1300 *Power Management Integrated Circuit (PMIC)* providing a 1.8 V to 3.3 V user-programmable power supply from USB

Kit content

The nRF54LM20 DK includes hardware, preprogrammed firmware, documentation, hardware schematics, and layout files.

The nRF54LM20 DK (PCA10184) comes with an NFC antenna (PCA64110).

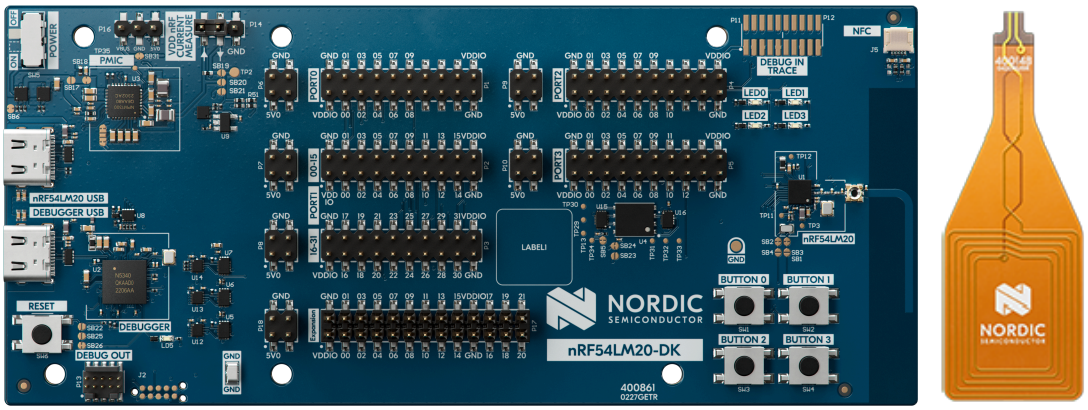


Figure 1: nRF54LM20 DK kit content

The hardware design files for the nRF54LM20 DK are available on the nRF54LM20 DK product page. They include the following resources:

- Schematics
- *Printed Circuit Board (PCB)* layout files
- Bill of materials
- Gerber files

2 Hardware description

The main components of the nRF54LM20 DK include the nRF54LM20A SoC and hardware peripherals that add functionality and configuration options.

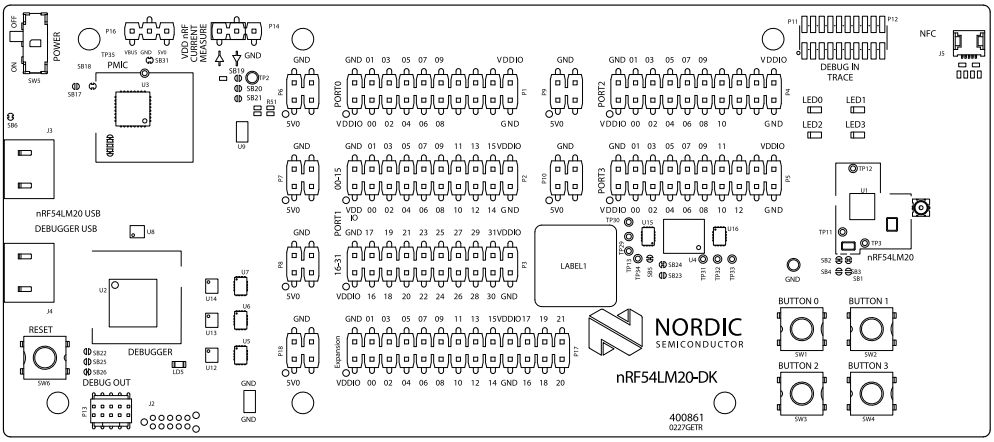


Figure 2: nRF54LM20 DK front view

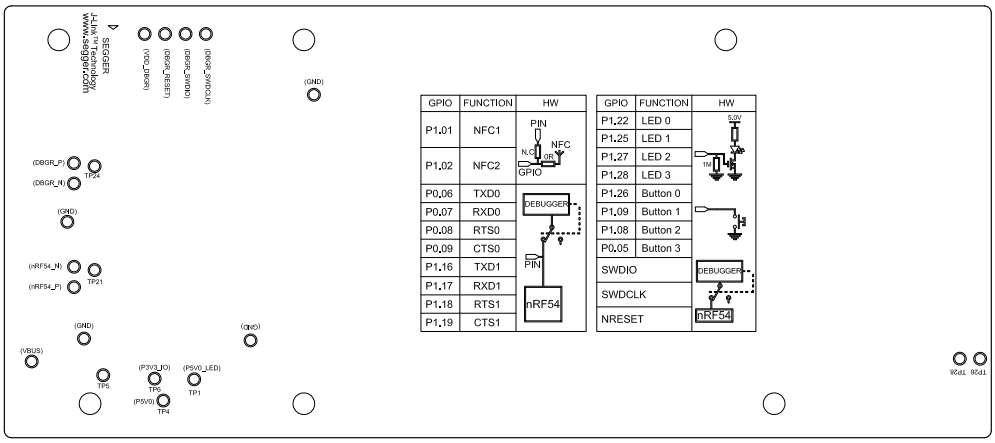


Figure 3: nRF54LM20 DK back view

The following figure shows the dimensions of the nRF54LM20 DK and the positions of the mounting holes in mm.

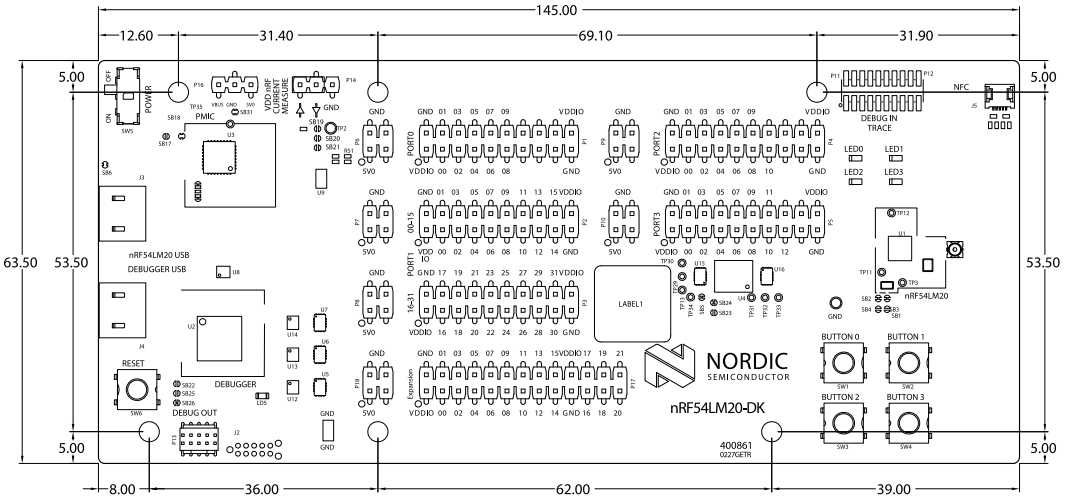


Figure 4: nRF54LM20 DK dimensions in mm

2.1 Block diagram

The block diagram illustrates the nRF54LM20 DK functional architecture.

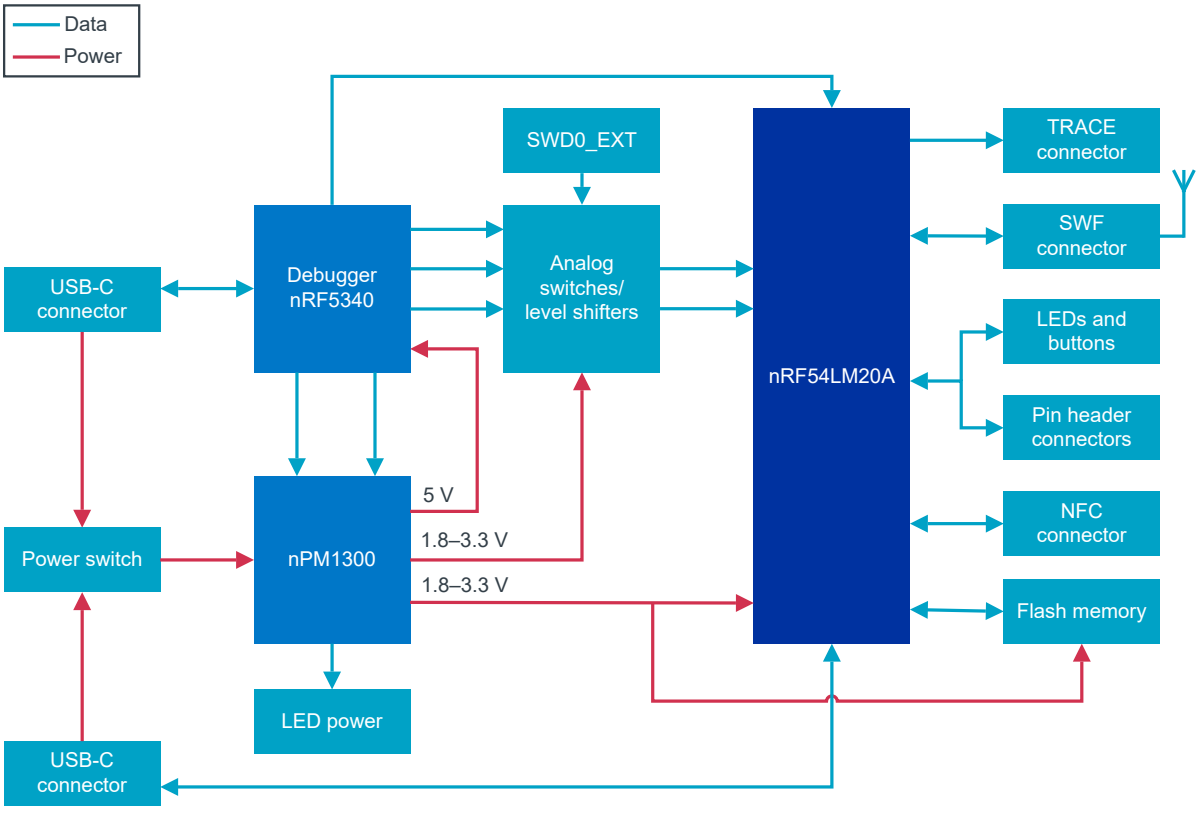


Figure 5: Block diagram

2.2 Power supply

The main supply voltage for the nRF54LM20 DK comes from the USB 5 V domain. The DK includes two USB connectors, **J3** and **J4**, which connect to the nPM1300 *PMIC*. Only one USB connector needs to be connected to power the nRF54LM20 DK.

The main power domains on the nRF54LM20 DK are the following.

- nRF:VDD programmable voltage from 1.8 V to 3.3 V
- VDD:IO buffered nRF:VDD voltage

The nPM1300 PMIC supplies the nRF54LM20A SoC VDD:nRF input with a default voltage of 1.8 V. To change the VDD:nRF voltage, use nRF Connect for Desktop's Board Configurator application.

The buffered VDD:nRF is called VDD:IO. The nRF54LM20 DK uses the VDD:nRF voltage follower to make sure that leakage currents are not drawn from the nRF54LM20A SoC device during low current measurements.

For more information about power sources, see nRF54LM20A SoC external power with DK functionality on page 9.

2.2.1 nRF54LM20A SoC external power with DK functionality

The nRF54LM20A SoC can be powered directly from an external power source with the rest of the nRF54LM20 DK being powered through the **J3** or **J4** USB connectors. This enables external supply for the nRF54LM20A SoC while serial interfaces, LEDs, and buttons remain functional.

Remove the jumper from **P14** and connect an external power source to the **P14** header. The allowed voltage range is from 1.7 V to 3.6 V.

Ensure that the nRF54LM20 DK is powered through **J3** or **J4** before powering on the nRF54LM20A SoC through the **P14** external supply header to avoid damaging the onboard circuitry.

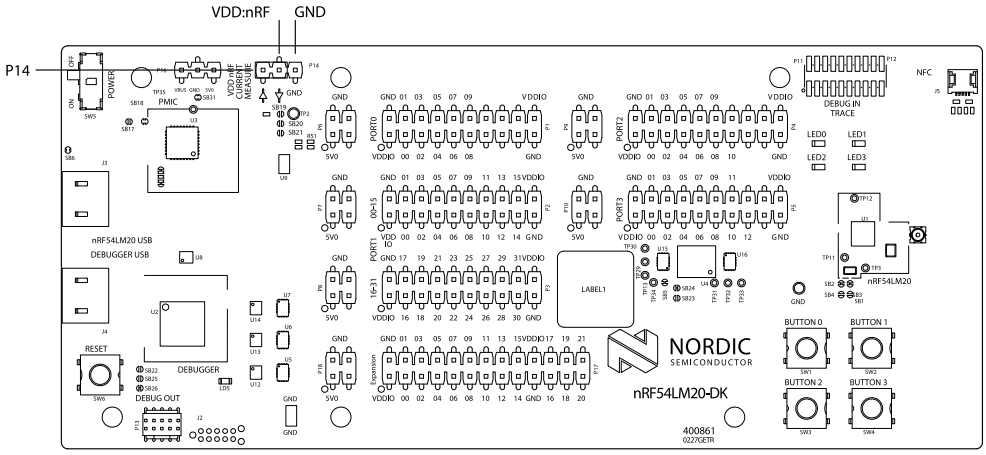


Figure 6: External VDD:nRF supply

2.2.2 nRF54LM20 DK stand-alone external supply

The nRF54LM20 DK can be manually configured to be supplied through the **P14** header without the need to supply power through the **J3** or **J4** USB connectors. In this configuration, the debugger, virtual serial ports, external flash, and LEDs are unavailable.

Remove the jumper from **P14** and connect an external power source to it. The allowed voltage range is from 1.7 V to 3.6 V.

The analog switches on the nRF54LM20 DK must be reconfigured to disconnect the nRF54LM20A SoC from the onboard debugger. Move the 0 Ω 0402 resistors from **R42** and **R44** to **R43** and **R51**.

2.3 GPIO interface

Access the nRF54LM20A SoC GPIOs through headers **P1**, **P2**, **P3**, **P4**, **P5**, and **P17**. Each GPIO pin header has a dedicated power header (**P6**, **P7**, **P8**, **P9**, **P10**, and **P18**) that can supply 5 V to any external device connected to the DK.

The expansion board header at **P17** supports the addition of future generic expansion boards for Nordic DKs. The GPIO pins in the expansion board header are also available at headers **P1**–**P5**.

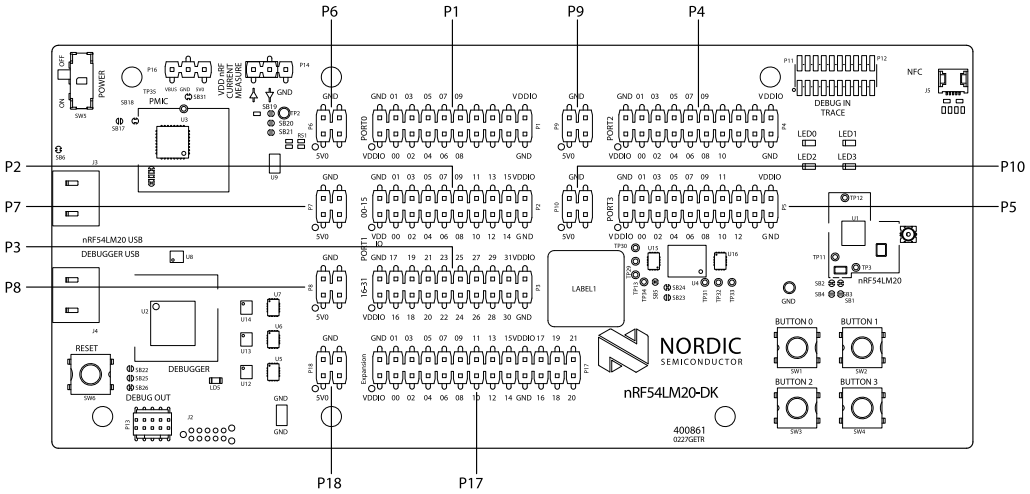


Figure 7: GPIO and power headers

Pin maps

GPIO pin	Function	Available on the expansion board header	Default connected to P1
P0.00			Yes
P0.01			Yes
P0.02			Yes
P0.03		Yes	Yes
P0.04		Yes	Yes
P0.05	BUTTON 3		Yes
P0.06	UART0_TXD		Yes
P0.07	UART0_RXD		Yes
P0.08	UART0_RST		Yes
P0.09	UART0_CST		Yes

Table 1: P0 pin map

GPIO pin	Function	Available on the expansion board header	Default connected to P2
P1.00			Yes.
P1.01	NFC1		Yes. Can be disconnected by removing **R33**.
P1.02	NFC2	Yes	Yes. Can be disconnected by removing **R34**.
P1.03		Yes	Yes.
P1.04		Yes	Yes.
P1.05		Yes	Yes.
P1.06		Yes	Yes.
P1.07		Yes	Yes.
P1.08	BUTTON 2		Yes.
P1.09	BUTTON 1		Yes.
P1.10			Yes.
P1.11			Yes.
P1.12			Yes.
P1.13		Yes	Yes.
P1.14			Yes.
P1.15			Yes.
P1.16	UART1_TXD		Yes.

Table 2: P1 pin map

GPIO pin	Function	Available on the expansion board header	Default connected to P3
P1.17	UART1_RXD		Yes.
P1.18	UART1_RST		Yes.
P1.19	UART1_CTS		Yes.
P1.20	32.768 kHz, XL1		No. Solder bridges must be configured. Short **SB3** to connect the GPIO to the pin header.
P1.21	32.768 kHz, XL2		No. Solder bridges must be configured. Short **SB4** to connect the GPIO to the pin header.
P1.22	LED 0		Yes.
P1.23			Yes.
P1.24			Yes.
P1.25	LED 1		Yes.
P1.26	Button 0		Yes.
P1.27	LED 2		Yes.
P1.28	LED 3		Yes.
P1.29			Yes.
P1.30			Yes.
P1.31	LED 3		Yes.

Table 3: P1 pin map

GPIO pin	Function	Available on the expansion board header	Default connected to P4
P2.00	QSPI_IO3/External flash	Yes	No
P2.01	QSPI_CLK/External flash	Yes	No
P2.02	SPI_IO0/External flash	Yes	No
P2.03	SPI_IO2/External flash	Yes	No
P2.04	SPI_IO1/External flash	Yes	No
P2.05	SPI_CS/External flash	Yes	No
P2.06	TRACECLK		Yes
P2.07	TRACEDATA[0]		Yes
P2.08	TRACEDATA[1]		Yes
P2.09	TRACEDATA[2]		Yes
P2.10	TRACEDATA[3]		Yes

Table 4: P2 pin map

GPIO pin	Function	Available on the expansion board header	Default connected to P5
P3.00		Yes	Yes
P3.01		Yes	Yes
P3.02		Yes	Yes
P3.03		Yes	Yes
P3.04		Yes	Yes
P3.05		Yes	Yes
P3.06		Yes	Yes
P3.07			Yes
P3.08			Yes
P3.09			Yes
P3.10			Yes
P3.11			Yes
P3.12			Yes

Table 5: P3 pin map

Headers **P6**, **P7**, **P8**, **P9**, **P10**, and **P18** are power supply pins that each provide 5.0 V for shields connected to GPIO ports.

P6, P7, P8, P9, P10, and P18 signal	Function
1	5V0 from PMIC
2	Ground
3	N.C.
4	Ground

Table 6: P6, P7, P8, P9, P10, and P18 signal map

The following figure shows the expansion board header.

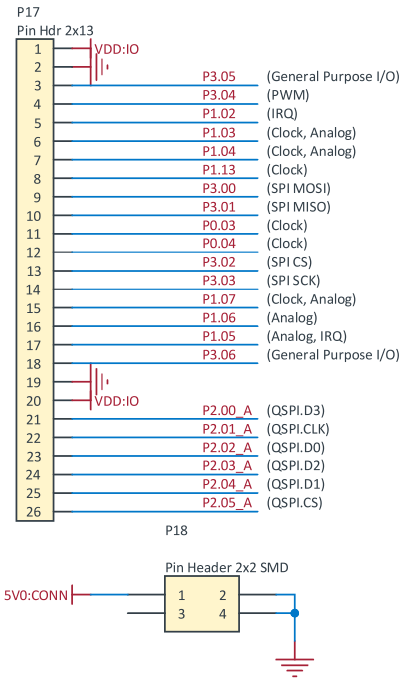


Figure 8: Expansion board header

2.4 External memory

The nRF54LM20 DK has a 64 Mb external flash memory that can be connected to the nRF54LM20A SoC. The memory is a multi-I/O memory supporting both *Serial Peripheral Interface (SPI)* and *Quad Serial Peripheral Interface (QSPI)*.

By default, the VDD:IO domain powers external memory. The power to the external memory can be configured to come from the VDD:nRF domain instead by cutting **SB23** and shorting **SB24**. If VDD:nRF is selected, the power consumption of the external memory is added to the nRF54LM20A SoC current measured on **P14**. See the following figure and table for more information.

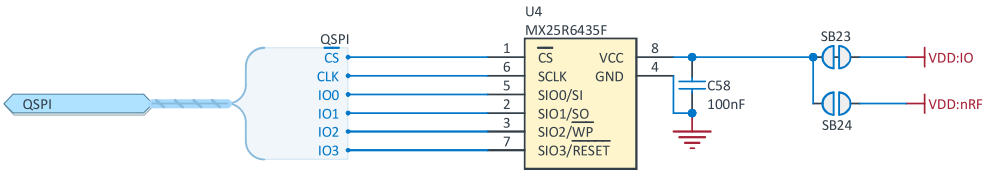


Figure 9: External flash memory

Power source	Solder bridge	Default state
VDD:IO	**SB23**	Closed
VDD:nRF	**SB24**	Open

Table 7: Flash memory power source configuration

GPIOs **P2.00**–**P2.05** can be enabled as QSPI signals for the external flash. Switches between the *System on Chip (SoC)* and the external flash determines if the GPIOs connect to the external flash or act as regular GPIO signals routed to pin headers **P4** and **P17**. The state of the switches is controlled by the board controller.

2.5 Buttons and LEDs

The four buttons and four LEDs on the nRF54LM20 DK are connected to dedicated GPIOs on the nRF54LM20A SoC.

GPIO	Part
P1.26	Button 0
P1.09	Button 1
P1.08	Button 2
P0.05	Button 3
P1.22	LED 0
P1.25	LED 1
P1.27	LED 2
P1.28	LED 3

Table 8: Button and LED connections

The buttons are active low, which means that input is connected to ground when the button is pressed. The buttons do not have an external pull-up resistor. Pins **P1.05**, **P1.08**, **P1.09**, and **P1.26** must be configured as input with an internal pull-up resistor to register that a button is pressed.

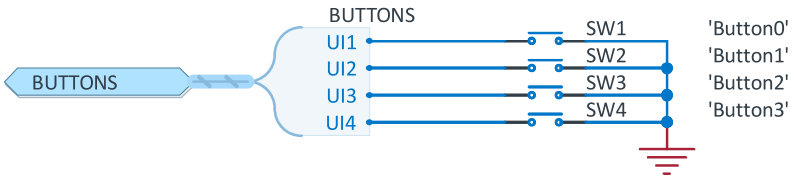


Figure 10: Button configuration

The LEDs are active high, which means that writing a logical `1` to the output pin turns on the LED. For the implementation, see Figure 11: LED configuration on page 16.

The LEDs are not directly connected to the SoC GPIOs but are buffered by a transistor. The transistor gate has a 1 MΩ resistor to ground.

The LEDs are powered by the nPM1300 *PMIC*. The power to the LEDs can be disabled using nRF Connect for Desktop's Board Configurator application.

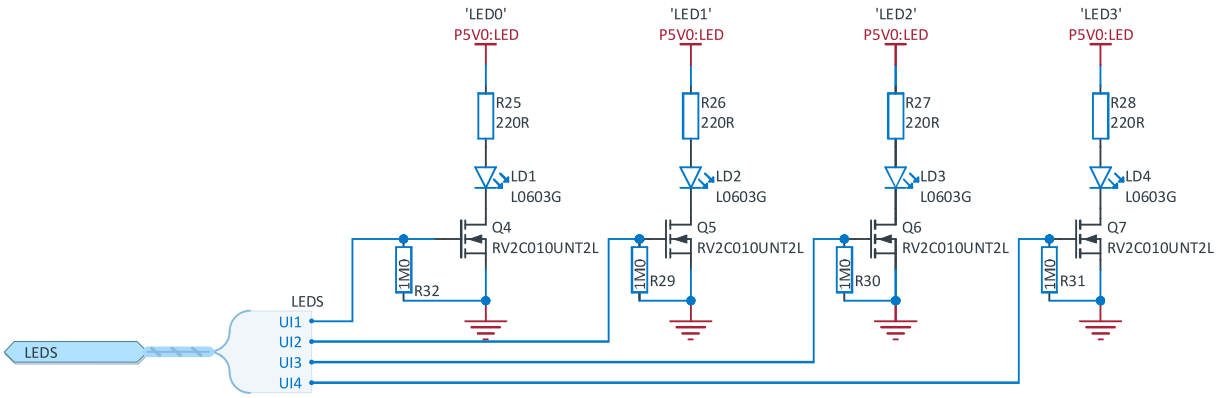


Figure 11: LED configuration

2.6 32.768 kHz crystal

The nRF54LM20A SoC can use the optional 32.768 kHz crystal **X2** for higher accuracy and lower average power consumption.

On the nRF54LM20 DK, **P1.20** and **P1.21** are used for the 32.768 kHz crystal by default and are not available as GPIOs on the headers.

By cutting solder bridges **SB1** and **SB2** and soldering **SB3** and **SB4**, crystal **X2** is disconnected and GPIOs **P1.20** and **P1.21** are connected to the header for general use.

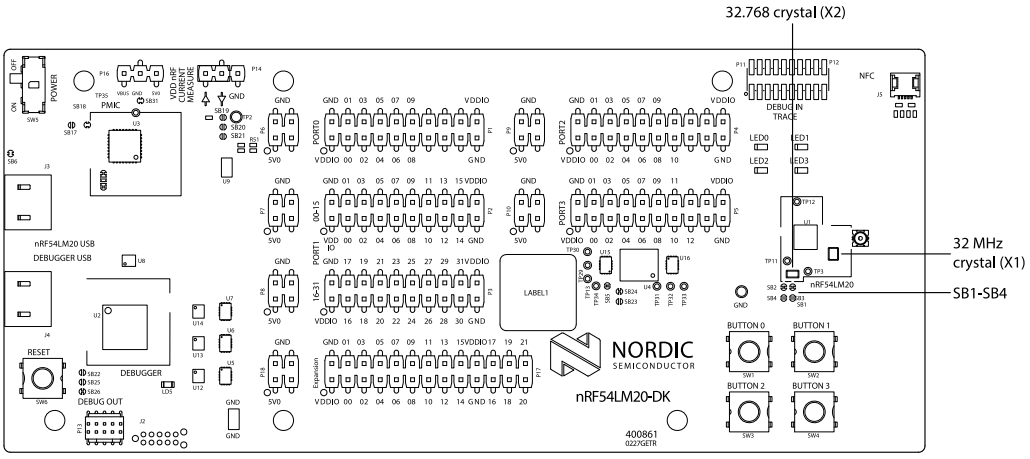


*Figure 12: 32.768 kHz crystal X1 and **SB1–SB4***

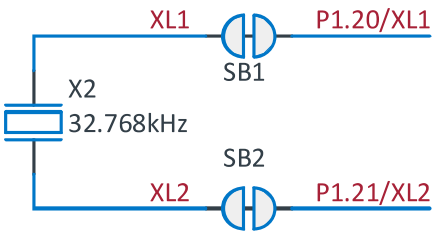


*Figure 13: 32.768 kHz crystal and **SB1** and **SB2***

2.7 NFC antenna interface

The nRF54LM20 DK supports an NFC tag.

NFC-A Listen Mode operation is supported on the nRF54LM20A SoC. The NFC antenna input is available on connector **J5** on the nRF54LM20 DK.

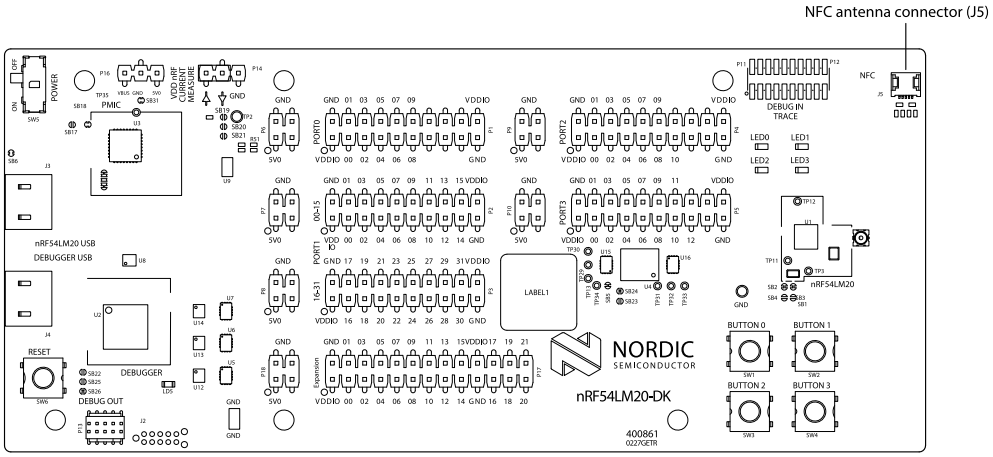


Figure 14: NFC antenna connector

NFC connects to the antenna using two pins, **NFC1** and **NFC2**, which are shared with GPIOs **P1.01** and **P1.02**. These pins are by default configured to use the NFC antenna.

Configuring NFC pins as GPIOs

To use pins **P1.01** (**NFC1**) and **P1.02** (**NFC2**) as GPIOs, move the 0 Ω 0402 resistors from **R33** and **R34** to **R3** and **R4**. Disable the NFC peripheral by adding `&uicr { nfct-pins-as-gpios; };` to your board devicetree files. See Configuring and building for instructions.

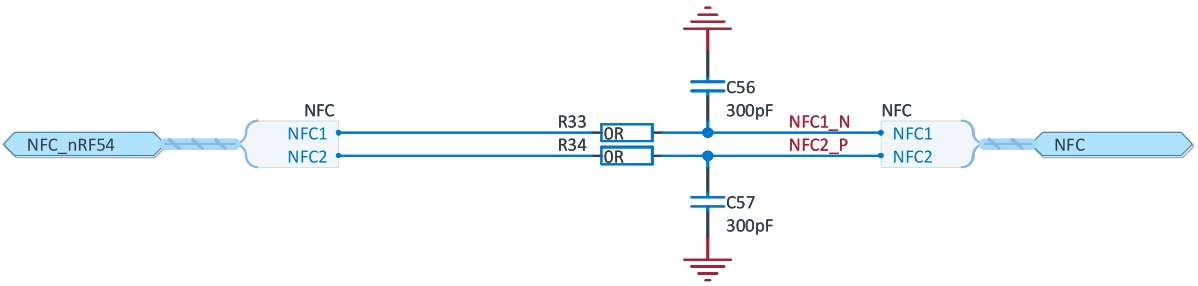


Figure 15: NFC network

2.8 Solder bridge configuration

The nRF54LM20 DK has a range of solder bridges for enabling or disabling functionality on the nRF54LM20 DK.

The following table is an overview of the solder bridges on the nRF54LM20 DK.

Solder bridge	Default	Function
SB1	Closed	Cut to disconnect the 32.768 kHz from **P1.20**.
SB2	Closed	Cut to disconnect the 32.768 kHz from **P1.21**.
SB3	Open	Short to enable **P1.20** as GPIO.
SB4	Open	Short to enable **P1.21** as GPIO.

Solder bridge	Default	Function
SB5	Closed	Cut to disconnect the IO3 signal for external flash from the nRF54LM20A SoC.
SB6	Closed	Cut to disconnect VBUS:nRF from the power switch.
SB17	Open	Short to bypass the 5V domain for the nPM1300 PMIC.
SB18	Closed	Cut to disconnect VSYS from P5V0.
SB19	Open	Short to connect VDD:nRF and VDD:IO.
SB20	Open	Short to disconnect VDD:_nRF_PMIC and VDD:IO.
SB21	Open	Short to connect VOUT2 and VDD:IO.
SB22	Open	Short to enable the 100 kΩ pull up resistor for the RESET_BUTTON signal
SB23	Closed	Cut to disconnect the VDD:IO domain from external flash power.
SB24	Open	Short to connect the VDD:nRF domain for supplying power to the external flash.
SB25	Open	Short to connect RESET button to the nRF54_RESET.
SB26	Closed	Cut to disconnect debugger from the RESET button line.
SB27	Open	Short to use VDD:nRF_PMIC as the source for LDO1.
SB28	Closed	Cut to disconnect P5V0 as the source for LDO1.
SB29	Closed	Cut to disconnect P5V0 as the source for LDO2.
SB30	Open	Short to use VDD:nRF_PMIC as the source for LDO2.
SB31	Closed	Cut to disconnect VBUS from 5V0:CONN.

Table 9: Solder bridge configuration

2.9 Board control

The debugger contains a board controller that controls the signals which enable and disable features on the nRF54LM20 DK.

All features on the nRF54LM20 DK have a default setting that is applied at the first boot. The configuration of the board controller can be changed through nRF Connect for Desktop's Board Configurator application. If the configuration is modified from the default factory setting, the board controller loads the modified configuration every time the nRF54LM20 DK is restarted.

For more information, see Board Configurator app.

3 Program and debug

The debugger on the nRF54LM20 DK programs and debugs the nRF54LM20A SoC application firmware.

3.1 Debugger

The debugger on the nRF54LM20 DK runs SEGGER J-Link *Onboard (OB)* interface firmware. It connects through USB connector **J4**.

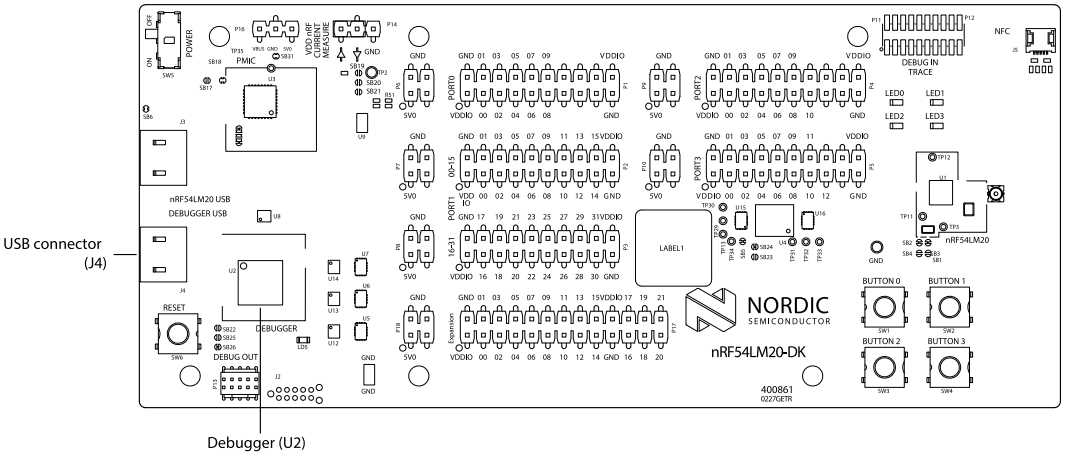


Figure 16: Debugger and USB connector J4

3.1.1 RESET button

The nRF54LM20 DK is equipped with a RESET button **SW6** connected to the debugger. The debugger reads the status of the RESET_BUTTON signal and resets the nRF54LM20A SoC through the *Serial Wire Debug (SWD)*. Devices directly connected to the RESET_BUTTON signals through programming connectors are reset directly.

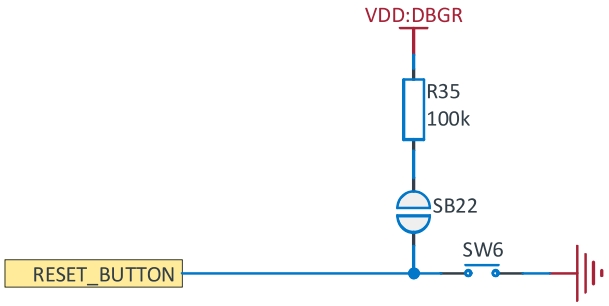


Figure 17: nRF54LM20 DK RESET button

The RESET button can be connected directly to the nRF54LM20A SoC by shorting the **SB25** solder bridge and cutting the **SB26** solder bridge.

An optional pull-up resistor can be connected through **SB22** to the RESET button node.

> **Note:** Pull-up resistor **R35** is for internal use only. Do not connected it to the RESET_BUTTON signal.

3.1.2 Virtual serial ports

The debugger has two virtual serial ports. Each of them has a *UART* interface.

The serial ports have the following features:

- Flexible baud rate setting up to 1 Mbps (baud rate 921,600 bps is not supported)
- Dynamic *Hardware Flow Control (HWFC)*
- Tri-stated UART lines when no terminal is connected

The following table lists the nRF54LM20A SoC UART GPIO pins and their signals.

Signal	nRF54LM20A SoC UART_0 - Serial Port 0	nRF54LM20A SoC UART_1 - Serial Port 1
TXD	P0.06	P1.16
RXD	P0.07	P1.17
RTS	P0.08	P1.18
CTS	P0.09	P1.19

Table 10: nRF54LM20A SoC GPIOs mapped to serial port/UART signals

The UART pins connected to the debugger are tri-stated when no terminal is connected to the virtual serial port on the computer. The terminal software must send a *Data Terminal Ready (DTR)* signal to configure the UART debugger pins.

P0.08/P1.18 *Request to Send (RTS)* and **P0.09/P1.19** *Clear to Send (CTS)* can be used for other purposes when HWFC is disabled on the nRF54LM20A SoC.

The UART signals are routed to the debugger through analog switches **U5** and **U6**.

UART pins for other tasks

For each UART instance, the TXD/RXD signals can be disconnected from the debugger as a group. For the UARTs in use, the RTS/CTS signals can be connected and disconnected from the debugger as a group depending on the HWFC usage. This can be done through nRF Connect for Desktop's Board Configurator application.

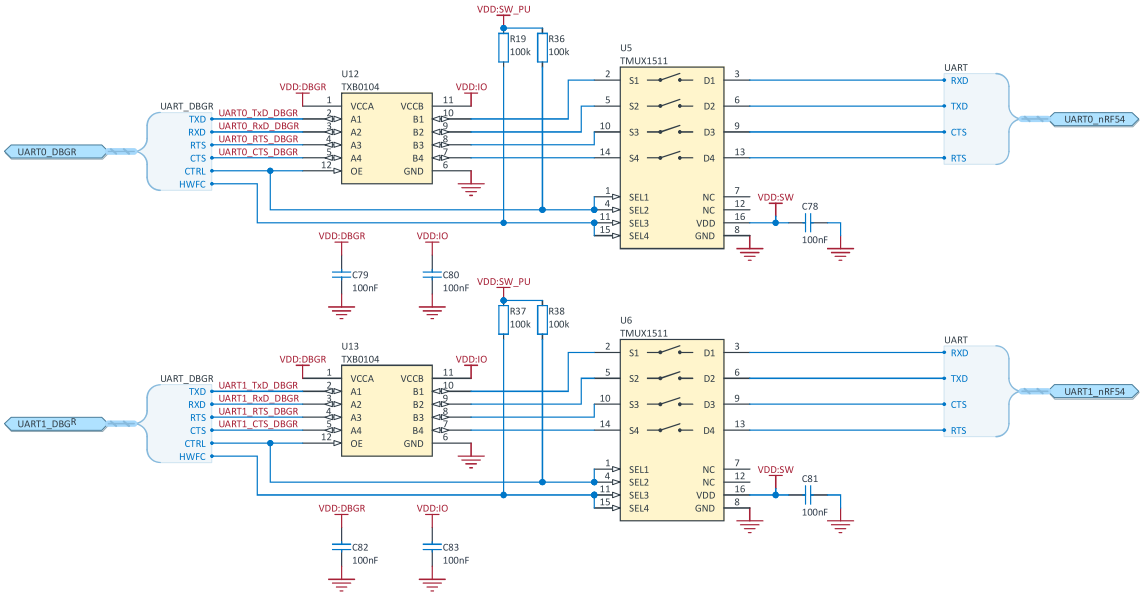


Figure 18: Analog switches between debugger and nRF54LM20A SoC

3.1.3 Dynamic hardware flow control

When the debugger receives a *DTR* signal from a terminal, it performs automatic *HWFC* detection.

Automatic HWFC detection is done by driving *CTS* from the debugger and evaluating the state of *RTS* when data is first sent or received. If the state of RTS is high, it is assumed HWFC is not in use. If HWFC is not detected, pins **P0.08/P1.18** (CTS) and **P0.09/P1.19** (RTS) are free for the nRF application to use.

After a power-on reset of the debugger, all UART lines are tri-stated when no terminal is connected to the virtual serial port. If HWFC has been used and detected, **P0.09/P1.19** (CTS) is driven by the debugger until a power-on reset has been performed or until a new DTR signal is received and the detection is redone.

The debugger has pull-down 100 kΩ resistors connected from CTS to ground through **R9** and **R10**.

3.2 Debug input and trace

Use the footprint on **P11** to connect a header for external debuggers.

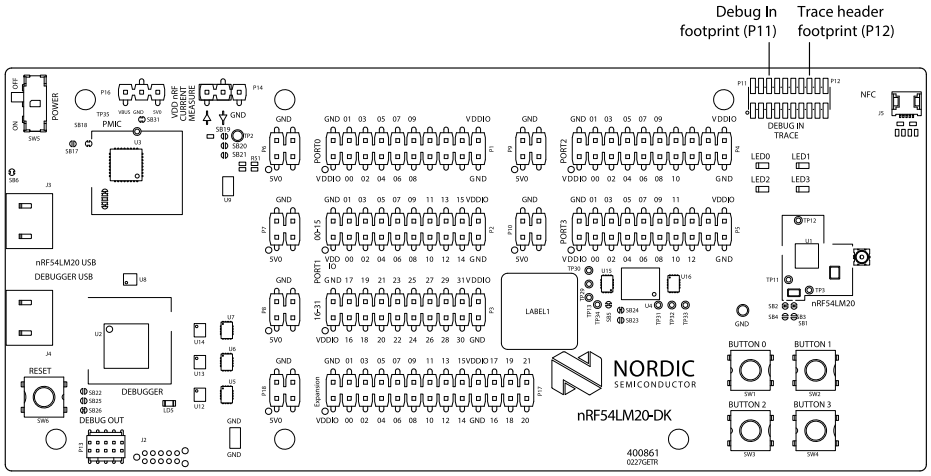


Figure 19: Debug input and trace header footprint

For trace, a 20-pin header footprint **P12** is available. If trace functionality is required, it is possible to mount a 1.27 mm 2x10 pin pitch surface-mount pin header. The Debug In header **P11** partially shares the same footprint as **P12**, so the 2x5 SWD Debug In **P11** header must first be removed.

The reference voltage for the debug input and trace is connected to **VDD:IO**.

GPIO	Trace	Default use
P2.06	TRACECLK	No peripheral connected
P2.07	TRACEDATA[0]	No peripheral connected
P2.08	TRACEDATA[1]	No peripheral connected
P2.09	TRACEDATA[2]	No peripheral connected
P2.10	TRACEDATA[3]	No peripheral connected

Table 11: Default and trace GPIOs

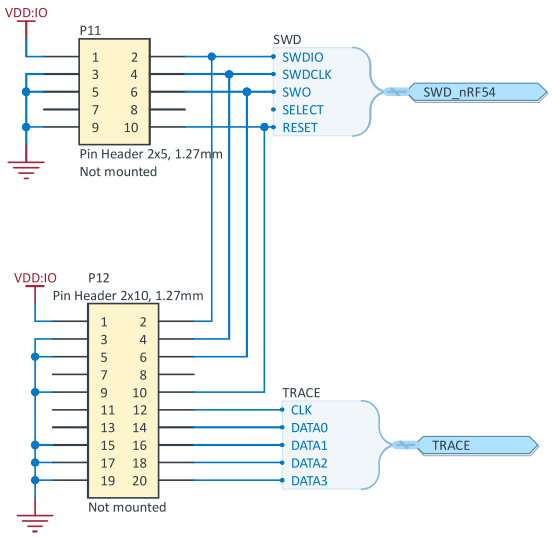


Figure 20: Debug In and trace headers

3.3 Debug out for programming external boards

The nRF54LM20 DK supports programming and debugging external boards with the nRF51 Series, nRF52 Series, nRF53 Series, or nRF54 Series SoCs and nRF91 Series SiPs.

To program or debug an external board, connect to the Debug out header **P13** using a 10-pin cable. The external board can be powered through a *SWD* cable by supplying power through **P5** pin 3 labeled **VDD SWD0**.

Note: The programming cable used to connect to the external board must be no longer than 10 cm. Power the external board separately from the nRF54LM20 DK. The VDD SWD0 voltage must be within the range of 1.8 V and 3.6 V.

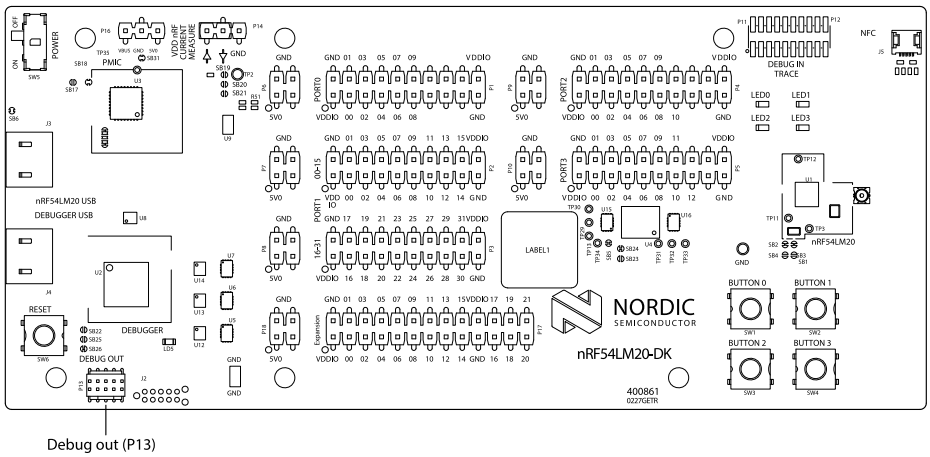


Figure 21: Debug output header

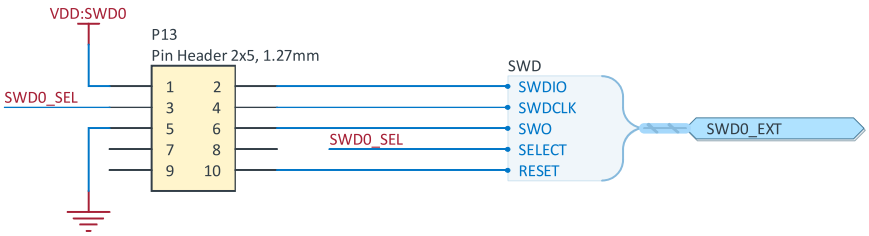


Figure 22: Debug out header

The following table describes the pinout of the **P13** header.

Pin number	Signal	Description
1	SWD0_VTG	I/O voltage reference input from the external target.
2	SWD0_SWDIO	*SWD* data I/O.
3	SWD0_SELECT	Debug out select signal. Connect to ground on the external board.
4	SWD0_SWDCLK	Serial Wire Clock line.
5	GND	Ground.
6	SWD0_SW0	*Serial Wire Output (SWO)* line is not used for programming and debugging over SWD.
7	N.C.	Not used.
8	N.C.	Not used.
9	N.C.	Not used.
10	SWD0_RESET	Reset line.

*Table 12: Header **P13** pinout for programming external targets*

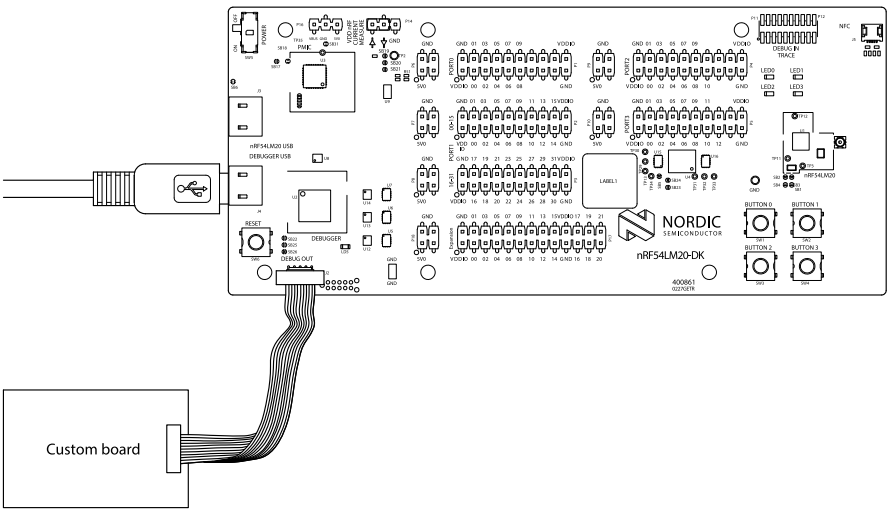


Figure 23: Connecting an external board to P13

The debugger programs or debugs the target chip on the external board instead of the onboard nRF54LM20A SoC when pin 3 (**`SWD0_SELECT`**) of **P13** is connected to **GND** through the 10-pin flat cable.

4 Measurements

Current and RF signal can be measured on the nRF54LM20 DK.

4.1 Current measurements

The current drawn by the application nRF54LM20A SoC can be monitored on the nRF54LM20 DK.

Current can be measured using any of the following test instruments:

- Power Profiler Kit II (PPK2)
- Oscilloscope
- Ampere meter
- Power analyzer

The following sections provide information on the nRF54LM20 DK measurement setup. If the PPK2 is used for measuring current, see Power Profiler Kit II for more information. Power analyzer measurements are not described in this document.

The nRF54LM20 DK can measure current on VDDM using **P14**.

> **Note:** The measurement readings might introduce noise if the virtual serial port is open.

For more information on current measurement, see Current measurement guide: Introduction.

4.1.1 Set up the DK

Perform the following tasks to set up the nRF54LM20 DK for minimal current consumption.

- Disconnect the virtual serial ports as described in Virtual serial ports on page 20.
- If a circuitry is connected to the **P13** Debug out header, disconnect it.
- Remove the jumper from the **P14** header.

To reprogram the nRF54LM20A SoC while the nRF54LM20 DK is prepared for current measurements, replace the measurement devices on **P14** with the jumper.

4.1.2 Measure current profile with an oscilloscope

An oscilloscope can be used to measure the average current over a given time interval and capture the current profile.

1. Prepare the nRF54LM20 DK as described in Set up the DK.
2. Mount a 10 Ω ±0.1% 0402 resistor to **R15** which is located at the back of the nRF54LM20 DK.
3. Set the oscilloscope to differential mode or a mode that is similar.
4. Connect the oscilloscope using two probes on the pins of the **P14** header, as shown in the following figure.
5. Calculate or plot the instantaneous current from the voltage drop across the **R24** resistor by taking the difference of the voltages measured on the two probes.

   The voltage drop is proportional to the current. The 10 Ω resistor causes a 10 mV drop for each 1 mA drawn by the circuit being measured.

The plotted voltage drop can be used to calculate the current at a given point in time. The current can then be averaged or integrated to analyze current and energy consumption over a period.

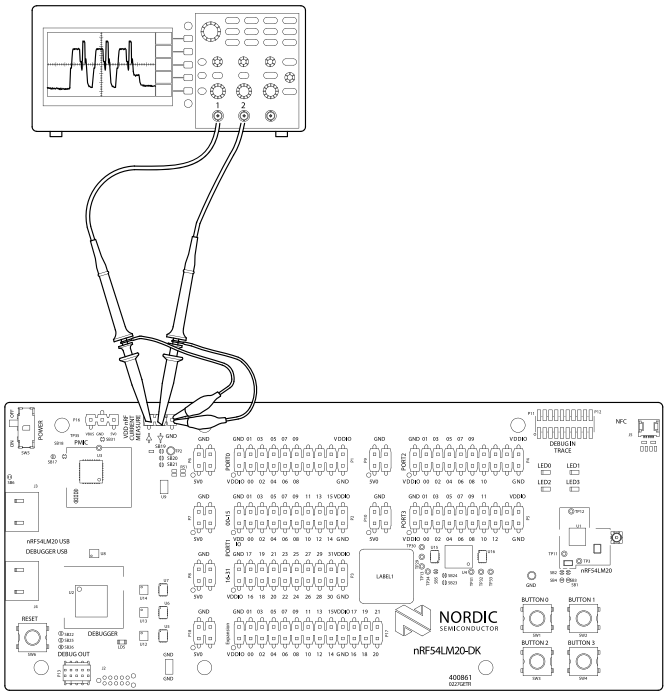


Figure 24: Current measurement with an oscilloscope

To reduce noise, do the following:

- Use GND leads that are as short as possible.
- Use probes with 1x attenuation.
- Enable averaging mode to reduce random noise.
- Enable high-resolution function if it is available.

Use a minimum of 200 kSa/s (one sample every 5 µs) to get a reliable average current measurement.

To accurately measure the current consumption of the nRF54LM20 DK, configure the oscilloscope to display the full range of currents you want to measure in the selected time window. Adjust the vertical scale in the oscilloscope to cover the full range of currents without clipping. Leave a small margin at the top or bottom of the vertical axis. Use an oscilloscope with high dynamic range (16 bits or more) to measure both small and large changes in current accurately.

4.1.3 Measure average current with an ampere meter

The average current drawn by the application nRF54LM20A SoC can be measured using an ampere meter. This method monitors the current in series with the nRF device. A true *Root Mean Square (RMS)* ampere meter is recommended.

1. Prepare the nRF54LM20 DK as described in Set up the DK.
2. Connect an ampere meter between pin 1 and pin 2 on header **P14** as shown in the following figure.
3. Set the average timing of the ampere meter to a long interval, such as 1 s or longer.
4. Set the dynamic range of the ampere meter between 1 µA and 15 mA, so that it is wide enough to provide accurate measurements.

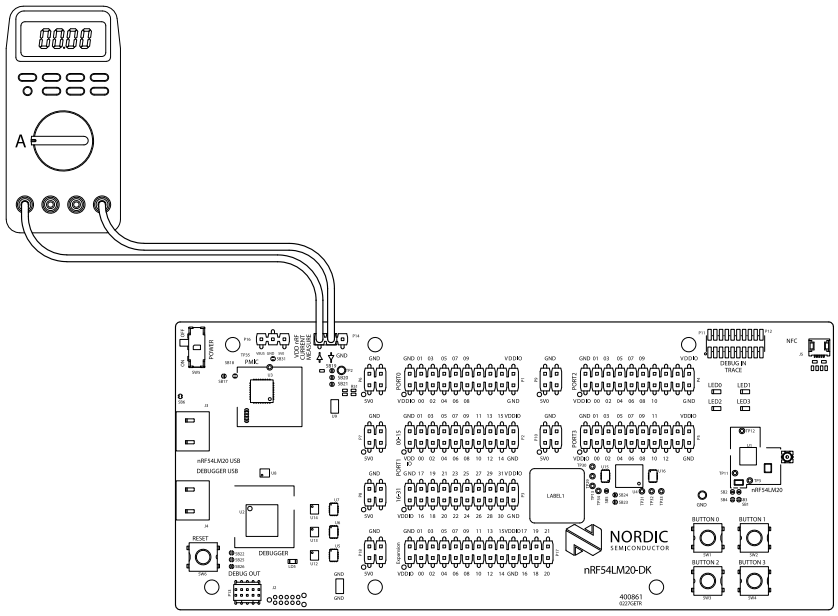


Figure 25: Current measurement with an ampere meter

Measure the average current consumption when the nRF54LM20A SoC is in a steady state, such as sleep mode, continuous TX, or RX. For applications with rapid changes in current consumption, consider using an oscilloscope, the PPK2, or a power profiler.

4.2 RF measurements

The nRF54LM20 DK is equipped with a small coaxial connector (**J1**) to measure the RF signal with a spectrum analyzer.

The connector is an SWF type (Murata part no. MM8130-2600) with an internal switch. By default, when a cable is not attached, the RF signal is routed to the onboard trace antenna.

In this example, a test probe (Murata part no. MXHS83QE3000) is used with a standard *SubMiniature Version A (SMA)* connection on the other end for connecting instruments. The test probe is not included in the kit. When connecting the test probe, the internal switch in the SWF connector disconnects the onboard antenna and connects the RF signal from the nRF54LM20A SoC to the test probe.

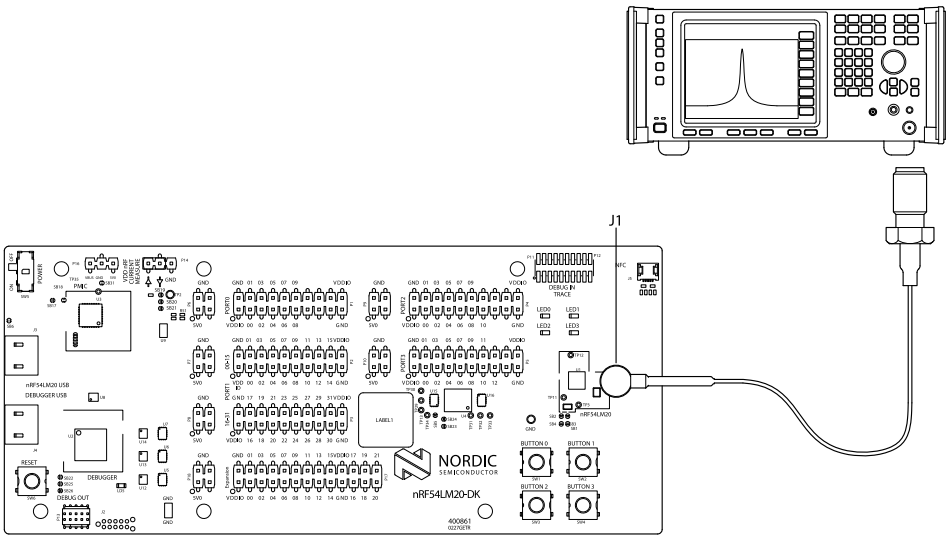


Figure 26: Connecting a spectrum analyzer

The connector and test probe add loss to the RF signal. See the following table for more information or consult the test probe user guide if you are using another model.

Frequency (MHz)	Loss (dB)
2440	1.0
4880	1.7
7320	2.6

Table 13: Typical loss in connector and test probe, using Murata part no. MXHS83QE3000

Glossary

Clear to Send (CTS)

In flow control, the receiving end is ready and telling the far end to start sending.

Data Terminal Ready (DTR)

A control signal in RS-232 serial communications transmitted from data terminal equipment, such as a computer, to data communications equipment.

Development Kit (DK)

A hardware development platform used for application development.

Electrostatic Discharge (ESD)

A sudden discharge of electric current between two electrically charged objects.

Hardware Flow Control (HWFC)

A handshaking mechanism used to prevent an overflow of bytes in modems. It uses two dedicated pins on the RS-232 connector, Request to Send and Clear to Send.

Integrated Circuit (IC)

A semiconductor chip consisting of fabricated transistors, resistors, and capacitors.

Mass Storage Device (MSD)

Any storage device that makes it possible to store and port large amounts of data in a permanent and machine-readable fashion.

Microcontroller Unit (MCU)

A small computer on a single metal-oxide-semiconductor integrated circuit chip.

Microwave coaxial connector with switch (SWF)

A small, RF surface-mount switch connector series for wireless applications.

NFC-A Listen Mode

Initial mode of an NFC Forum Device when it does not generate a carrier. The device listens for the remote field of another device. See Near Field Communication (NFC).

Onboard (OB)

A function that is delivered on the chip microcontroller.

Power Management Integrated Circuit (PMIC)

A chip used for various functions related to power management.

Printed Circuit Board (PCB)

A board that connects electronic components.

Quad Serial Peripheral Interface (QSPI)

A Serial Peripheral Interface (SPI) controller that allows the use of multiple data lines.

Receive Data (RXD)

A signal line in a serial interface that receives data from another device.

Request to Send (RTS)

In flow control, the transmitting end is ready and requesting the far end for a permission to transfer data.

Root Mean Square (RMS)

An RMS meter calculates the equivalent Direct Current (DC) value of an Alternating Current (AC) waveform. A true RMS meter can accurately measure both pure waves and the more complex nonsinusoidal waves.

Serial Peripheral Interface (SPI)

Synchronous serial communication interface specification used for short-distance communication.

Serial Wire Debug (SWD)

A standard two-wire interface for programming and debugging Arm® CPUs.

Serial Wire Output (SWO)

A data line for tracing and logging.

SubMiniature Version A (SMA)

A semi-precision coaxial RF connector for coaxial cables with a screw-type coupling mechanism.

System in Package (SiP)

Several integrated circuits, often from different technologies, enclosed in a single module that performs as a system or subsystem.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Transmit Data (TXD)

A signal line in a serial interface that transmits data to another device.

Universal Asynchronous Receiver/Transmitter (UART)

A hardware device for asynchronous serial communication between devices.

Universal Serial Bus (USB)

An industry standard that establishes specifications for cables and connectors and protocols for connection, communication, and power supply between computers, peripheral devices, and other computers.

User Information Configuration Registers (UICR)

Non-volatile memory registers used to configure user-specific settings.

Recommended reading

In addition to the information in this document, you may need to consult other documents.

Nordic documentation

- nRF54LM20A Preliminary Datasheet

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