FEATURES

MitySOM-C10L Development Board

MitySOM-C10L SoM Module

Additional Hardware Included:

- USB Cable
- Ethernet Cable
- AC to DC 12V Adapter

Integrated +5V/+3.3V/+2.5V/1.8V Power Supplies

Digital Interfaces:

- 10/100/1000 Mb Ethernet Interface
- Debug UART to USB
- USB-Blaster JTAG Port
- FMC Low Pin Count Interface
- 5 Pushbuttons
- 4 LEDs.

Expansion

- 400 Pin FPGA Mezzanine Card Low Pin Count (FMC LPC)
- 2x60 pin Expansion Headers

Software and Documentation

- Reference Quartus Project
- Reference QSPI Flash Image
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

APPLICATIONS

- MitySOM-C10L Evaluation
- Test and Measurement
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Test and Measurement
- Rapid Prototyping

DESCRIPTION

The MitySOM-C10L Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-C10L System on Module. The MitySOM-C10L Development Kit comes complete with a MitySOM-C10L module that meets your project's needs.

The MitySOM-C10L Development Kit includes on-board Debug UART to USB converter and 10/100/1000 Gb Ethernet communication interfaces, FMC LPC connector that is compatible with a wide range of existing add-on cards, and two 60 pin dual row connectors that provide additional IO expansion options. All powered from a single 12VDC input (adapter included) with onboard +3.3V/+5V/2.5V/1.8V power supplies.

A block diagram of the MitySOM-C10L Development Kit is illustrated in Figure 1. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-C10L module.

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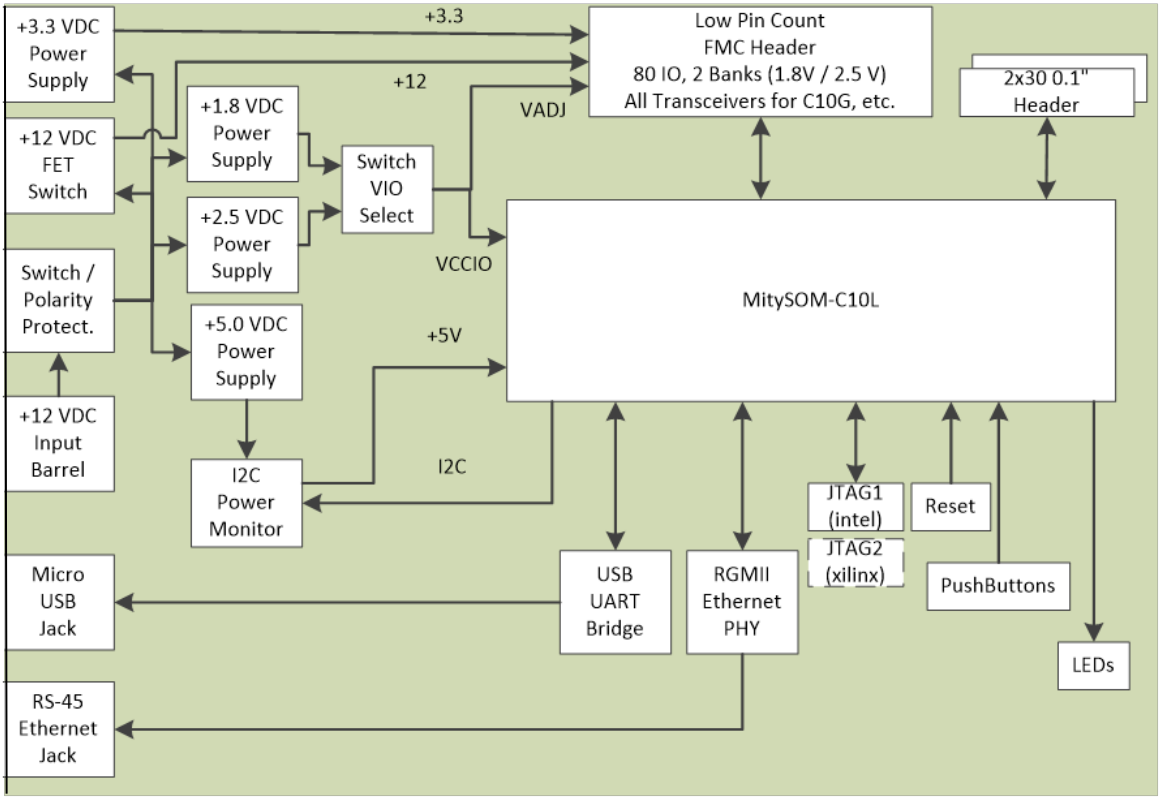

Figure 1: MitySOM-C10L Development Kit Block Diagram

Additional details about the Cylone 10 LP FPGA, available peripheral IP, its features and FPGA IO details are provided in the data sheet at the Intel website (https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/10/lp.html).

Feature Descriptions

Electrical Interface Descriptions

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Debug UART to USB Interface Description

The on-board UART to USB Bridge, FTDI FT230X, provides a serial interface at data rates up to 115,200 baud. The USB serial interface, J4 - Console, is routed to the MitySOM-C10L general IO pins. It allows for general module debug and console interaction if a NIOS soft core is instantiated in the FPGA.

When connected to a Windows PC no drivers are required as Windows Update is used to obtain the drivers.

Intel USB-Blaster JTAG Interface

To support programming the MitySOM-C10L, the C10L Development Kit includes J2, which is a USB-Blaster compatible interface. J3 is a reserved connector.

Gigabit Ethernet Interface Description

The on-board Ethernet interface features a Micrel KSZ9131 Ethernet PHY capable of running at 10/100/1000Mbit including link auto-negotiation and RGMII/MDIO capability. An industry standard RJ-45 connector, J5, is provided for external connection. This PHY and MDIO interface is connected to general IO pins on the Cyclone 10 LP FPGA of the MitySOM-C10L.

FMC LPC Interface Description

The FPGA Mezzanine Card Low Pin Count (FMC LPC) interface, J6, allows for the use of add-on cards that are designed for the Intel Cyclone 10 LP on the MitySOM-C10L module. Several “off the shelf” boards/kits are available from third parties that are compatible with this interface.

Dual Row 60 pin expansion Interface Description

Two 60 pin female 0.1” dual row headers, P2 and P3, are available for developing expansion interfaces and are connected to the VCCIO power, system +5V, and spare FPGA IO pins of the MitySOM-C10L module.

Reconfigure Switch Description

The C10L Development Kit has a cold reset button that can be used to reconfigure the Intel Cyclone 10 LP FPGA from on-board QSPI Flash (if programmed). This button is located at S1.

General Switch Description

The C10L Development Kit includes 4 general purpose normally open push button inputs connected to the Cyclone 10 LP FPGA on the SOM. These are switches S2, S3, S4, and S5.

User LEDs

The C10L Development Kit includes 4 general purpose LEDs connected to the Cyclone 10 LP FPGA on the SOM. These are LEDs D3, D4, D5, and D6.

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IO voltage Select Switch Description

The C10L Development Kit provides a 1.8V as well as a 2.5V DC supply. Either supply may be connected to the VCCIO banks of the MitySOM-C10LP FPGA bank IO pins. The selected voltage is configured by S7. ***Important Note***: S7 must only be changed while the Carrier card is powered off.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact Critical Link at info@criticallink.com.

Table 1: Absolute Maximums

Parameter	Min	Max	Units
Operating Supply Voltage	10.8	13.2	V
Operating Temperature for MitySOM-C10L/Baseboard	0	70	C
Operating Temperature for AC to DC Power Supply	0	50	C
Storage Temperature	-40	85	C
Humidity	0	95	% Non-condensing

ELECTRICAL CHARACTERISTICS

Table 2: Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter) all components			5.0	A
I_{Max}	12.0V Supply[1] for external components			1.0	A
I_{Max}	3.3V Supply[1] for external components			2.0	A
I_{Max}	1.8V Supply[1] for external components			4.0	A
Power Dissipation					
V_S	Supply Voltage		12±5%		V
I_S	Supply Current[2]		800		mA

Notes:

1. The maximum current supplied to external components should be limited to the specified maximum for all externally connected power supplies
2. FMC cards not attached, FPGA programmed, RS-232 and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P1

The MitySOM-C10L Development Kit power interface, P1, requires a single +12Volt power supply. An input supply rating of at least 3A is recommended.

Table 3: Input Power Interface Pin Description

Signal	P1 Position
+12V	1
GND	2

Main Power Switch – S6

An input power switch is present on the Development Kit, S6, which controls the power input to the development kit, including the module, on or off, from P1.

FPGA IO Bank Voltage Power Switch – S7

The MitySOM-C10L Development Kit supports operating the FPGA bank voltages (all are tied together) from either a 1.8V or 2.5V on-board switching supply. S7 defines which voltage is selected. S7 must only be changed while the main power supply is off.

Push Button Switches (S1-S5)

The MitySOM-C10L Development Kit includes 5 debounced normally open push buttons connected to the MitySOM-C10L FPGA according to Table 4. When activated, these buttons will connect the reference signal to ground. When released, these signals are pulled high to VCCIO.

Table 4 Push Button Functions

Switch ID	SoM Interface Signal	Pin on SoM	FPGA Ball
S1	nCONFIG	23	K5
S2	SW_1	88	Y6
S3	SW_2	90	Y10
S4	SW_3	92	AA10
S5	SW_4	94	AB10

Debug LED Interface (D3 - D6)

The MitySOM-C10L Development Kit includes 4 debug LEDs according to Table 5. The LED signal should be driven to GND / low to activate the LED. To disable the LED, drive the signal high or tri-state it.

Table 5 LED Interface

ID	SoM Interface Signal	Pin on SoM	FPGA Ball
D3	LED_1	96	W8
D4	LED_2	98	V10
D5	LED_3	100	U10
D6	LED_4	102	U11

USB-Blaster JTAG Interface – J2

The USB-Blaster interface pin out for J2 is shown in Table 6 below.

Table 6 J2 USB Blaster JTAG Interface

J2-Pin	SoM Interface Signal	Pin on SoM	FPGA Ball
1	TCK	20	L1
2	GND	-	-
3	TDO	18	L4
4	V_JTAG	19	+2.5V
5	TMS	22	L2
6	N/C	-	-
7	N/C	-	-
8	N/C	-	-
9	TDI	16	L5
10	GND	-	-

Debug/Boot UART to USB Interface – J4

The Micro-USB pin out for J4 is shown in Table 7 below.

Table 7: J4 Micro USB Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VBUS	Power	-	
2	D-	I/O	USB 2.0	USB data minus line
3	D+	I/O	USB 2.0	USB data plus line
4	GND	GND	-	
5	SHIELD	GND	-	

The FTDI FT230XS-U UART to USB controller, used to drive J4 on the Development Kit board is connected to general FPGA IO pins on the MityCAM-C10L, as shown in Table 8 below.

Table 8 USB Controller to UART Interface

FTD230XS Signal	SoM Interface Signal	Pin on SoM	FPGA Ball
TXD	UART0_RX	J1 – 74	V11
RXD	UART0_TX	J1 - 76	W10
RTS#	No Connect	No Connect	
CTS#	No Connect – 1.1k to GND resistor	No Connect	

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Expansion Interface 1 – P2

Table 9 describes the pin-out of the P2 interface on the MitySOM-C10L development board. The I/O "type" is in reference to the signal direction from the SoM/development board or a power input pin.

Table 9: P2 Pin Assignments

P2 Pin	Dev Kit Signal	Pin on SoM	FPGA Ball	Type	Notes
1	GND	-	-	POWER	
2	VCCIO	-	-	POWER	Note 2
3	+5V	-	-	POWER	Note 1
4	VCCIO	-	-	POWER	Note 2
5	GND	-	-	POWER	
6	GND	-	-	POWER	
7	EXT1_DIO1_N	83	M6	IO	
8	EXT1_DIO2_N	79	M3	IO	
9	EXT1_DIO1_P	81	N1	IO	
10	EXT1_DIO2_P	77	P1	IO	
11	EXT1_DIO3_N	75	M1	IO	
12	EXT1_DIO10_N	71	P3	IO	
13	EXT1_DIO3_P	73	M2	IO	
14	EXT1_DIO10_P	69	P4	IO	
15	EXT1_DIO11_N	63	N1	IO	
16	EXT1_DIO8_N	59	P1	IO	
17	EXT1_DIO11_P	65	N2	IO	
18	EXT1_DIO8_P	61	P2	IO	
19	EXT1_DIO9_N	55	R1	IO	
20	EXT1_DIO6_N	51	U1	IO	
21	EXT1_DIO9_P	57	R2	IO	
22	EXT1_DIO6_P	53	U2	IO	
23	EXT1_DIO7_N	47	V1	IO	
24	EXT1_DIO4_N	43	W1	IO	
25	EXT1_DIO7_P	45	V2	IO	
26	EXT1_DIO4_P	41	W2	IO	
27	EXT1_DIO5_P	37	Y2	IO	
28	EXT1_CLK0_N	35	T1	I	
29	EXT1_DIO5_N	39	Y1	IO	
30	EXT1_CLK0_P	33	T2	I	
31	EXT1_DIO25	128	AA20	IO	
32	EXT1_DIO23	130	AB20	IO	
33	EXT1_DIO26	124	AA16	IO	
34	EXT1_DIO24	126	AB16	IO	
35	EXT1_DIO29	118	AA15	IO	
36	EXT1_DIO27	120	AB15	IO	
37	EXT1_DIO30	114	AA14	IO	
38	EXT1_DIO28	116	AB14	IO	
39	EXT1_DIO33	112	AB13	IO	
40	EXT1_DIO31	38	AA4	IO	
41	EXT1_DIO34	110	AA13	IO	
42	EXT1_DIO32	40	AB4	IO	
43	EXT1_DIO37	99	P5	IO	
44	EXT1_DIO35	101	N6	IO	
45	EXT1_DIO38	95	T4	IO	
46	EXT1_DIO36	97	T5	IO	
47	EXT1_DIO41	91	V3	IO	

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P2 Pin	Dev Kit Signal	Pin on SoM	FPGA Ball	Type	Notes
48	EXT1_DIO39	93	R5	IO	
49	EXT1_DIO42	87	N5	IO	
50	EXT1_DIO40	89	V4	IO	
51	EXT1_CLK1_P	70	AA11	I	
52	SCL	84	V5	IO	
53	EXT1_CLK1_N	72	AB11	I	
54	SDA	82	W6	IO	
55	GND	-	-	POWER	
56	GND	-	-	POWER	
57	NC	-	-		
58	NC	-	-		
59	NC	-	-		
60	GND	-	-	POWER	

Notes:
1. The maximum total current supplied to external components from the +5.0V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the VCCIO supply should be limited to less than 1.0A. The maximum current allowed per connector pin is 1A.

Expansion Interface 2 – P3

Table 10 describes the pin-out of the P3 interface on the MitySOM-C10L development board. The I/O "type" is in reference to the signal direction from the SoM/development board or a power pin.

Table 10: P3 Pin Assignments

P3 Pin	Dev Kit Signal	Pin on SoM	FPGA Ball	Type	Notes
1	GND	-	-	POWER	
2	VCCIO	-	-	POWER	Note 2
3	+5V	-	-	POWER	Note 1
4	VCCIO	-	-	POWER	Note 2
5	GND	-	-	POWER	
6	GND	-	-	POWER	
7	EXT2_DIO11_N	248	C3	IO	
8	EXT2_DIO9_N	240	A4	IO	
9	EXT2_DIO11_P	246	C4	IO	
10	EXT2_DIO9_P	238	B4	IO	
11	EXT2_DIO10_N	244	A3	IO	
12	EXT2_DIO7_N	230	A6	IO	
13	EXT2_DIO10_P	242	B3	IO	
14	EXT2_DIO7_P	228	B6	IO	
15	EXT2_DIO8_N	236	F7	IO	
16	EXT2_DIO5_N	222	C8	IO	
17	EXT2_DIO8_P	234	G7	IO	
18	EXT2_DIO5_P	220	C7	IO	
19	EXT2_DIO6_N	226	A7	IO	
20	EXT2_DIO3_N	212	A9	IO	
21	EXT2_DIO6_P	224	B7	IO	
22	EXT2_DIO3_P	210	B9	IO	

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P3 Pin	Dev Kit Signal	Pin on SoM	FPGA Ball	Type	Notes
23	EXT2_DIO4_N	218	A8	IO	
24	EXT2_DIO1_N	204	F9	IO	
25	EXT2_DIO4_P	216	B8	IO	
26	EXT2_DIO1_P	202	F10	IO	
27	EXT2_DIO2_N	208	A10	IO	
28	EXT2_CLK0_N	200	A11	I	
29	EXT2_DIO2_P	206	B10	IO	
30	EXT2_CLK0_P	198	B11	I	
31	EXT2_DIO29	192	C10	IO	
32	EXT2_DIO30	194	D10	IO	
33	EXT2_DIO27	188	B5	IO	
34	EXT2_DIO28	190	A5	IO	
35	EXT2_DIO26	186	C6	IO	
36	EXT2_DIO25	184	F8	IO	
37	EXT2_DIO23	180	E5	IO	
38	EXT2_DIO24	182	E6	IO	
39	EXT2_DIO33	174	T18	IO	
40	EXT2_DIO34	176	M16	IO	
41	EXT2_DIO31	170	AB18	IO	
42	EXT2_DIO32	172	AA18	IO	
43	EXT2_DIO35	166	R14	IO	
44	EXT2_DIO36	168	T15	IO	
45	EXT2_DIO37	162	T16	IO	
46	EXT2_DIO38	164	R16	IO	
47	EXT2_DIO41	136	W17	IO	
48	EXT2_DIO42	138	Y17	IO	
49	EXT2_DIO39	132	W13	IO	
50	EXT2_DIO40	134	Y13	IO	
51	EXT2_CLK1_P	106	AA12	I	
52	SCL	84	V5	IO	
53	EXT2_CLK1_N	108	AB12	I	
54	SDA	82	W6	IO	
55	GND	-	-	POWER	
56	GND	-	-	POWER	
57	NC	-	-		
58	NC	-	-		
59	NC	-	-		
60	GND	-	-	POWER	

Notes:

1. The maximum total current supplied to external components from the +5.0V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the VCCIO supply should be limited to less than 1.0A. The maximum current allowed per connector pin is 1A.

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FMC Interface- J6

Table 11 describes the pin-out of the FMC interface on the MitySOM-C10L development board. The I/O "type" is in reference to the signal direction from the SoM/development board or power pin.

Table 11.1: J6 FMC Connector Pin A1-A40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
A1	GND	GND	-	POWER
A2	DP1_M2C_P	-	-	-
A3	DP1_M2C_N	-	-	-
A4	GND	GND	-	POWER
A5	GND	GND	-	POWER
A6	DP2_M2C_P	-	-	-
A7	DP2_M2C_N	-	-	-
A8	GND	GND	-	POWER
A9	GND	GND	-	POWER
A10	DP3_M2C_P	-	-	-
A11	DP3_M2C_N	-	-	-
A12	GND	GND	-	POWER
A13	GND	GND	-	POWER
A14	DP4_M2C_P	-	-	-
A15	DP4_M2C_N	-	-	-
A16	GND	GND	-	POWER
A17	GND	GND	-	POWER
A18	DP5_M2C_P	-	-	-
A19	DP5_M2C_N	-	-	-
A20	GND	GND	-	POWER
A21	GND	GND	-	POWER
A22	DP1_C2M_P	-	-	-
A23	DP1_C2M_N	-	-	-
A24	GND	GND	-	POWER
A25	GND	GND	-	POWER
A26	DP2_C2M_P	-	-	-
A27	DP2_C2M_N	-	-	-
A28	GND	GND	-	POWER
A29	GND	GND	-	POWER
A30	DP3_C2M_P	-	-	-
A31	DP3_C2M_N	-	-	-
A32	GND	GND	-	POWER
A33	GND	GND	-	POWER
A34	DP4_C2M_P	-	-	-
A35	DP4_C2M_N	-	-	-
A36	GND	GND	-	POWER
A37	GND	GND	-	POWER
A38	DP5_C2M_P	-	-	-
A39	DP5_C2M_N	-	-	-
A40	GND	GND	-	POWER

Table 11.2: J6 FMC Connector Pin B1-B40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
B1	CLK_DIR	-	-	-
B2	GND	GND	-	POWER
B3	GND	GND	-	POWER
B4	DP9_M2C_P	-	-	-
B5	DP9_M2C_N	-	-	-
B6	GND	GND	-	POWER
B7	GND	GND	-	POWER
B8	DP8_M2C_P	-	-	-
B9	DP8_M2C_N	-	-	-
B10	GND	GND	-	POWER
B11	GND	GND	-	POWER
B12	DP7_M2C_P	-	-	-
B13	DP7_M2C_N	-	-	-
B14	GND	GND	-	POWER
B15	GND	GND	-	POWER
B16	DP6_M2C_P	-	-	-
B17	DP6_M2C_N	-	-	-
B18	GND	GND	-	POWER
B19	GND	GND	-	POWER
B20	GBTCLK1_M2C_P	-	-	-
B21	GBTCLK1_M2C_N	-	-	-
B22	GND	GND	-	POWER
B23	GND	GND	-	POWER
B24	DP9_C2M_P	-	-	-
B25	DP9_C2M_N	-	-	-
B26	GND	GND	-	POWER
B27	GND	GND	-	POWER
B28	DP8_C2M_P	-	-	-
B29	DP8_C2M_N	-	-	-
B30	GND	GND	-	POWER
B31	GND	GND		POWER
B32	DP7_C2M_P	-	-	-
B33	DP7_C2M_N	-	-	-
B34	GND	GND	-	POWER
B35	GND	GND	-	POWER
B36	DP6_C2M_P	-	-	-
B37	DP6_C2M_N	-	-	-
B38	GND	GND	-	POWER
B39	GND	GND	-	POWER
B40	RES0	-	-	-

Table 11.3: J6 FMC Connector Pin C1-C40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	FPGA Ball	Type
C1	GND	GND	-	-	POWER
C2	DP0_C2M_P	-	-	-	-
C3	DP0_C2M_N	-	-	-	-
C4	GND	GND	-	-	POWER
C5	GND	GND	-	-	POWER
C6	DP0_M2C_P	-	-	-	-
C7	DP0_M2C_N	-	-	-	-
C8	GND	GND	-	-	POWER
C9	GND	GND	-	-	POWER
C10	LA06_P	LA06_P	245	H17	IO
C11	LA06_N	LA06_N	247	G18	IO
C12	GND	GND	-	-	POWER
C13	GND	GND	-	-	POWER
C14	LA10_P	LA10_P	227	B21	IO
C15	LA10_N	LA10_N	229	B22	IO
C16	GND	GND	-	-	POWER
C17	GND	GND	-	-	POWER
C18	LA14_P	LA14_P	167	N19	IO
C19	LA14_N	LA14_N	165	N20	IO
C20	GND	GND	-	-	POWER
C21	GND	GND	-	-	POWER
C22	LA18_P_CC	LA18_P	149	U19	IO
C23	LA18_N_CC	LA18_N	147	U20	IO
C24	GND	GND	-	-	POWER
C25	GND	GND	-	-	POWER
C26	LA27_P	LA27_P	183	J18	IO
C27	LA27_N	LA27_N	185	F17	IO
C28	GND	GND	-	-	POWER
C29	GND	GND	-	-	POWER
C30	SCL	SCL_3V3	84[1]	V5	O
C31	SDA	SDA_3V3	82[1]	W6	IO
C32	GND	GND	-	-	POWER
C33	GND	GND	-	-	POWER
C34	GA0	GND	-	-	-
C35	12P0V	+12V	-	-	POWER
C36	GND	GND	-	-	POWER
C37	12P0V	+12V	-	-	POWER
C38	GND	GND	-	-	POWER
C39	3P3V	+3.3V	-	-	POWER
C40	GND	GND	-	-	POWER

Note 1: The SCL and SDA are level translated from VCCIO (1.8 or 2.5 V based on S7) to +3.3Von the DevKit Carrier card.

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Table 11.4: J6 FMC Connector Pin D1-D40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	FPGA Ball	Type
D1	PG_C2M	-	-	-	-
D2	GND	GND	-	-	POWER
D3	GND	GND	-	-	POWER
D4	GBTCLK0_M2C_P	-	-	-	-
D5	GBTCLK0_M2C_N	-	-	-	-
D6	GND	GND	-	-	POWER
D7	GND	GND	-	-	POWER
D8	LA01_P_CC	LA01_P	191	K21	IO
D9	LA01_N_CC	LA01_N	193	K22	IO
D10	GND	GND	-	-	POWER
D11	LA05_P	LA05_P	215	E21	IO
D12	LA05_N	LA05_N	217	E22	IO
D13	GND	GND	-	-	POWER
D14	LA09_P	LA09_P	233	D20	IO
D15	LA09_N	LA09_N	235	C20	IO
D16	GND	GND	-	-	POWER
D17	LA13_P	LA13_P	171	M19	IO
D18	LA13_N	LA13_N	169	M20	IO
D19	GND	GND	-	-	POWER
D20	LA17_P_CC	LA17_CC_P	143	R19	IO
D21	LA17_N_CC	LA17_CC_N	141	R18	IO
D22	GND	GND	-	-	POWER
D23	LA23_P	LA23_P	129	U21	IO
D24	LA23_N	LA23_N	127	U22	IO
D25	GND	GND	-	-	POWER
D26	LA26_P	LA26_P	115	Y21	IO
D27	LA26_N	LA26_N	113	Y22	IO
D28	GND	GND	-	-	POWER
D29	TCK	-	-	-	NC
D30	TDI	-	-	-	NC
D31	TDO	-	-	-	NC
D32	3P3VAUX	+3.3V	-	-	POWER
D33	TMS	-	-	-	NC
D34	TRST_L	+3.3V	-	-	-
D35	GA1	GND	-	-	POWER
D36	3P3V	+3.3V	-	-	POWER
D37	GND	GND	-	-	POWER
D38	3P3V	+3.3V	-	-	POWER
D39	GND	GND	-	-	POWER
D40	3P3V	+3.3V	-	-	POWER

Table 11.5: J6 FMC Connector Pin E1-E40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
E1	GND	GND	-	POWER
E2	HA01_P_CC	-	-	-
E3	HA01_N_CC	-	-	-
E4	GND	GND	-	POWER
E5	GND	GND	-	POWER
E6	HA05_P	-	-	-
E7	HA05_N	-	-	-
E8	GND	GND	-	POWER
E9	HA09_P	-	-	-
E10	HA09_N	-	-	-
E11	GND	GND	-	POWER
E12	HA13_P	-	-	-
E13	HA13_N	-	-	-
E14	GND	GND	-	POWER
E15	HA16_P	-	-	-
E16	HA16_N	-	-	-
E17	GND	GND	-	POWER
E18	HA20_P	-	-	-
E19	HA20_N	-	-	-
E20	GND	GND	-	POWER
E21	HB03_P	-	-	-
E22	HB03_N	-	-	-
E23	GND	GND	-	POWER
E24	HB05_P	-	-	-
E25	HB05_N	-	-	-
E26	GND	GND	-	POWER
E27	HB09_P	-	-	-
E28	HB09_N	-	-	-
E29	GND	GND	-	POWER
E30	HB13_P	-	-	-
E31	HB13_N	-	-	-
E32	GND	GND	-	POWER
E33	HB19_P	-	-	-
E34	HB19_N	-	-	-
E35	GND	GND	-	POWER
E36	HB21_P	-	-	-
E37	HB21_N	-	-	-
E38	GND	GND	-	POWER
E39	VADJ	VCCIO	-	POWER
E40	GND	GND	-	POWER

Table 11.6: J6 FMC Connector Pin F1-F40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
F1	PG_M2C	-	-	-
F2	GND	GND	-	POWER
F3	GND	GND	-	POWER
F4	HA00_P_CC	-	-	-
F5	HA00_N_CC	-	-	-
F6	GND	GND	-	POWER
F7	HA04_P	-	-	-
F8	HA04_N	-	-	-
F9	GND	GND	-	POWER
F10	HA08_P	-	-	-
F11	HA08_N	-	-	-
F12	GND	GND	-	POWER
F13	HA12_P	-	-	-
F14	HA12_N	-	-	-
F15	GND	GND	-	POWER
F16	HA15_P	-	-	-
F17	HA15_N	-	-	-
F18	GND	GND	-	POWER
F19	HA19_P	-	-	-
F20	HA19_N	-	-	-
F21	GND	GND	-	POWER
F22	HB02_P	-	-	-
F23	HB02_N	-	-	-
F24	GND	GND	-	POWER
F25	HB04_P	-	-	-
F26	HB04_N	-	-	-
F27	GND	GND	-	POWER
F28	HB08_P	-	-	-
F29	HB08_N	-	-	-
F30	GND	GND	-	POWER
F31	HB12_P	-	-	-
F32	HB12_N	-	-	-
F33	GND	GND	-	POWER
F34	HB16_P	GND	-	-
F35	HB16_N	GND	-	-
F36	GND	GND	-	POWER
F37	HB20_P	GND	-	-
F38	HB20_N	GND	-	-
F39	GND	GND	-	POWER
F40	VADJ	VCCIO	-	POWER

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Table 11.7: J6 FMC Connector Pin G1-G40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	FPGA Ball	Type
G1	GND	GND	-	-	POWER
G2	CLK1_M2C_P	CLK1_M2C_P	131	T21	I
G3	CLK1_M2C_N	CLK1_M2C_N	133	T22	I
G4	GND	GND	-	-	POWER
G5	GND	GND	-	-	POWER
G6	LA00_P_CC	LA00_CC_P	199	G21	I
G7	LA00_N_CC	LA00_CC_N	197	G22	I
G8	GND	GND	-	-	POWER
G9	LA03_P	LA03_P	205	H21	IO
G10	LA03_N	LA03_N	207	H22	IO
G11	GND	GND	-	-	POWER
G12	LA08_P	LA08_P	219	D21	IO
G13	LA08_N	LA08_N	221	D22	IO
G14	GND	GND	-	-	POWER
G15	LA12_P	LA12_P	237	F19	IO
G16	LA12_N	LA12_N	239	F20	IO
G17	GND	GND	-	-	POWER
G18	LA16_P	LA16_P	163	M21	IO
G19	LA16_N	LA16_N	161	M22	IO
G20	GND	GND	-	-	POWER
G21	LA20_P	LA20_P	153	P21	IO
G22	LA20_N	LA20_N	151	P22	IO
G23	GND	GND	-	-	POWER
G24	LA22_P	LA22_P	125	V21	IO
G25	LA22_N	LA22_N	123	V22	IO
G26	GND	GND	-	-	POWER
G27	LA25_P	LA25_P	111	AA21	IO
G28	LA25_N	LA25_N	109	AA22	IO
G29	GND	GND	-	-	POWER
G30	LA29_P	LA29_P	179	K19	IO
G31	LA29_N	LA29_N	181	H18	IO
G32	GND	GND	-	-	POWER
G33	LA31_P	LA31_P	156	V13	IO
G34	LA31_N	LA31_N	158	V14	IO
G35	GND	GND	-	-	POWER
G36	LA33_P	LA33_P	148	U15	IO
G37	LA33_N	LA33_N	150	U14	IO
G38	GND	GND	-	-	POWER
G39	VADJ	VCCIO	-	-	POWER
G40	GND	GND	-	-	POWER

Table 11.8: J6 FMC Connector Pin H1-H40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	FPGA Ball	Type
H1	VREF_A_M2C	-	-	-	NC
H2	PRSNT_M2C_L	-	-	-	NC
H3	GND	GND	-	-	POWER
H4	CLK0_M2C_P	CLK0_M2C_P	201	J21	IO
H5	CLK0_M2C_N	CLK0_M2C_N	203	J22	IO
H6	GND	GND	-	-	POWER
H7	LA02_P	LA02_P	187	L21	IO
H8	LA02_N	LA02_N	189	L22	IO
H9	GND	GND	-	-	POWER
H10	LA04_P	LA04_P	209	F21	IO
H11	LA04_N	LA04_N	211	F22	IO
H12	GND	GND	-	-	POWER
H13	LA07_P	LA07_P	223	C21	IO
H14	LA07_N	LA07_N	225	C22	IO
H15	GND	GND	-	-	POWER
H16	LA11_P	LA11_P	241	H19	IO
H17	LA11_N	LA11_N	243	H20	IO
H18	GND	GND	-	-	POWER
H19	LA15_P	LA15_P	157	N21	IO
H20	LA15_N	LA15_N	155	N22	IO
H21	GND	GND	-	-	POWER
H22	LA19_P	LA19_P	137	R21	IO
H23	LA19_N	LA19_N	135	R22	IO
H24	GND	GND	-	-	POWER
H25	LA21_P	LA21_P	119	W21	IO
H26	LA21_N	LA21_N	117	W22	IO
H27	GND	GND	-	-	POWER
H28	LA24_P	LA24_P	107	W19	IO
H29	LA24_N	LA24_N	105	W20	IO
H30	GND	GND	-	-	POWER
H31	LA28_P	LA28_P	173	N18	IO
H32	LA28_N	LA28_N	175	R20	IO
H33	GND	GND	-	-	POWER
H34	LA30_P	LA30_P	152	V12	IO
H35	LA30_N	LA30_N	154	U12	IO
H36	GND	GND	-	-	POWER
H37	LA32_P	LA32_P	142	V15	IO
H38	LA32_N	LA32_N	144	W15	IO
H39	GND	GND	-	-	POWER
H40	VADJ	VCCIO	-	-	POWER

Table 11.9: J6 FMC Connector Pin J1-J40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
J1	GND	GND	-	POWER
J2	CLK3_BIDIR_P	-	-	NC
J3	CLK3_BIDIR_N	-	-	NC
J4	GND	GND	-	POWER
J5	GND	GND	-	POWER
J6	HA03_P	-	-	NC
J7	HA03_N	-	-	NC
J8	GND	GND	-	POWER
J9	HA07_P	-	-	NC
J10	HA07_N	-	-	NC
J11	GND	GND	-	POWER
J12	HA11_P	-	-	NC
J13	HA11_N	-	-	NC
J14	GND	GND	-	POWER
J15	HA14_P	-	-	NC
J16	HA14_N	-	-	NC
J17	GND	GND	-	POWER
J18	HA18_P	-	-	NC
J19	HA18_N	-	-	NC
J20	GND	GND	-	POWER
J21	HA22_P	-	-	NC
J22	HA22_N	-	-	NC
J23	GND	GND	-	POWER
J24	HB01_P	-	-	NC
J25	HB01_N	-	-	NC
J26	GND	GND	-	POWER
J27	HB07_P	-	-	NC
J28	HB07_N	-	-	NC
J29	GND	GND	-	POWER
J30	HB11_P	-	-	NC
J31	HB11_N	-	-	NC
J32	GND	GND	-	POWER
J33	HB15_P	-	-	NC
J34	HB15_N	-	-	NC
J35	GND	GND	-	POWER
J36	HB18_P	-	-	NC
J37	HB18_N	-	-	NC
J38	GND	GND	-	POWER
J39	VIO_B_M2C	-	-	NC
J40	GND	GND	-	POWER

Table 11.10: J6 FMC Connector Pin K1-K40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
K1	VREF_B_M2C	-	-	NC
K2	GND	GND	-	POWER
K3	GND	GND	-	POWER
K4	CLK2_BIDIR_P	-	-	NC
K5	CLK2_BIDIR_N	-	-	NC
K6	GND	GND	-	POWER
K7	HA02_P	-	-	NC
K8	HA02_N	-	-	NC
K9	GND	GND	-	POWER
K10	HA06_P	-	-	NC
K11	HA06_N	-	-	NC
K12	GND	GND	-	POWER
K13	HA10_P	-	-	NC
K14	HA10_N	-	-	NC
K15	GND	GND	-	POWER
K16	HA17_P_CC	-	-	NC
K17	HA17_N_CC	-	-	NC
K18	GND	GND	-	POWER
K19	HA21_P	-	-	NC
K20	HA21_N	-	-	NC
K21	GND	GND	-	POWER
K22	HA23_P	-	-	NC
K23	HA23_N	-	-	NC
K24	GND	GND	-	POWER
K25	HB00_P_CC	-	-	NC
K26	HB00_N_CC	-	-	NC
K27	GND	GND	-	POWER
K28	HB06_P_CC	-	-	NC
K29	HB06_N_CC	-	-	NC
K30	GND	GND	-	POWER
K31	HB10_P	-	-	NC
K32	HB10_N	-	-	NC
K33	GND	GND	-	POWER
K34	HB14_P	-	-	NC
K35	HB14_N	-	-	NC
K36	GND	GND	-	POWER
K37	HB17_P_CC	-	-	NC
K38	HB17_N_CC	-	-	NC
K39	GND	GND	-	POWER
K40	VIO_B_M2C	-	-	NC

Please see the following VITA documentation concerning the FMC specification (https://www.vita.com/fmc).

10/100/1000 Ethernet Interface – J5

The MitySOM-C10L Development Kit provides an RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table 12 below.

Table 12: J500 Ethernet RJ45 Pin Assignments

Pin	Signal	Type
1	TXRXA_P	I/O
2	TXRXA_N	I/O
3	TXRXB_P	I/O
4	TXRXB_N	I/O
5	TXRXC_P	I/O
6	TXRXC_N	I/O
7	TXRXD_P	I/O
8	TXRXD_N	I/O

The Ethernet PHY located on the Development Kit, Micrel KSZ9131, will auto negotiate to the speed of the device it is connected to. The Ethernet PHY is connected to the module through FPGA IO pins as shown in Table 13 below.

Table 13: Ethernet PHY to SoM / FPGA Interface

PHY to SoM Interface Signal	Pin on SoM	FPGA Ball
RGMII1_RXD0	54	AB7
RGMII1_RXD1	56	AA8
RGMII1_RXD2	58	AB8
RGMII1_RXD3	60	AA9
RGMII1_RX_CLK	62	AB9
RGMII1_RX_CTL	64	U9
RGMII1_TXD0	42	AA5
RGMII1_TXD1	44	AB5
RGMII1_TXD2	46	W7
RGMII1_TXD3	48	Y7
RGMII1_TX_CLK	34	AA3
RGMII1_TX_CTL	36	AB3
RGMII_MDIO	78	Y8
RGMII_MDC	80	Y3
RGMII_RESETn	66	V8

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

Four mounting holes are available for mounting standoffs to the devkit PCB. Figure 2 shows the location of the mounting holes as well as the location holes for the FMC interface (J6). Refer to the MitySOM-C10L datasheet for locations of the PEM nut positions (P4 and P5) with respect to the SODIMM DDR4 connector.

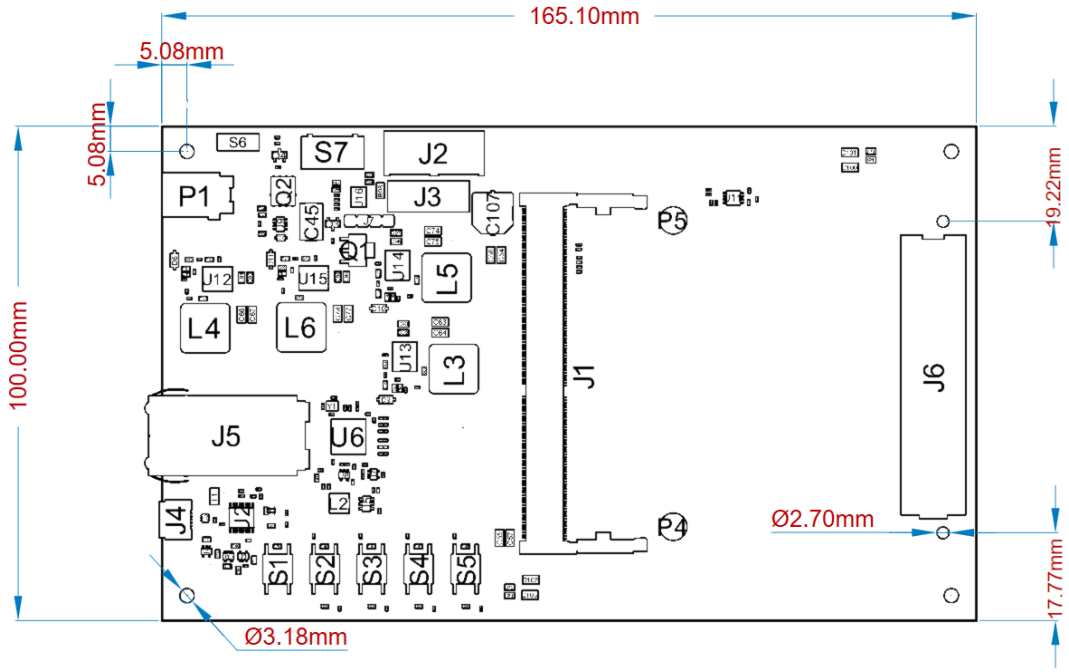

Figure 2 MitySOM-C10L Development Kit Outline, Mounting Hole Locations (Top View, inches)

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Figure 3 shows the locations of Pin 1 and the mechanical center of the 2x30 female headers for each of the expansion ports.

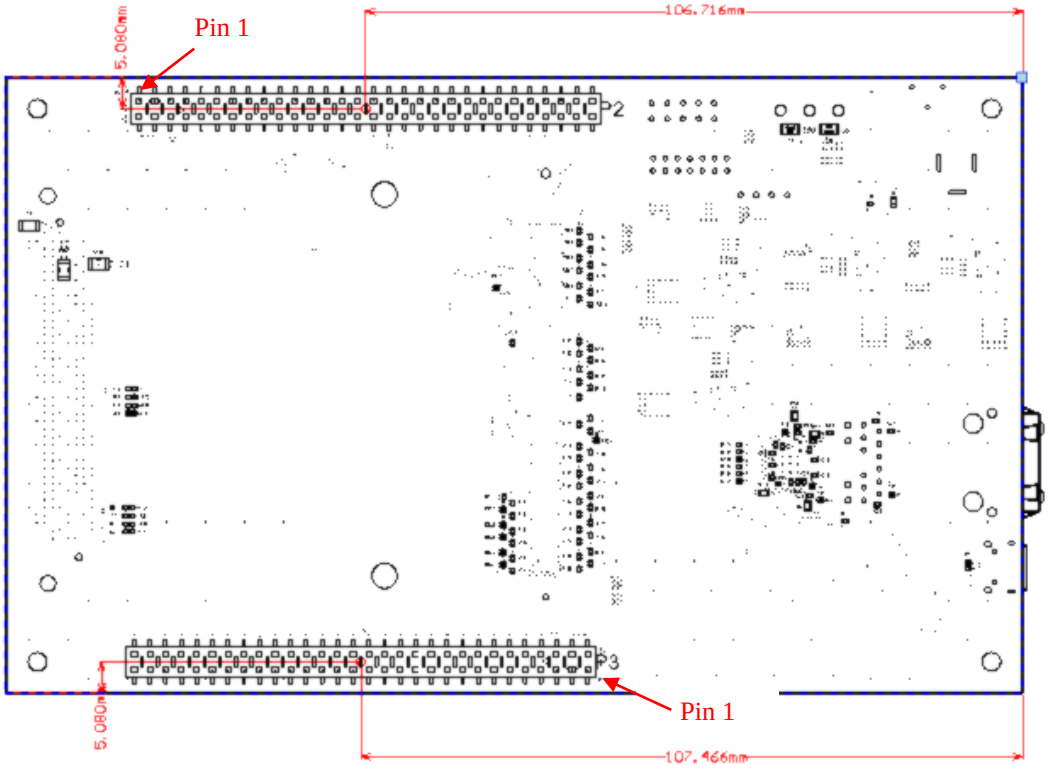

Figure 3 MitySOM-C10L Development Kit Outline, Bottom View / Connector Locations

Figure 4 shows, with callouts, the location of each of the external interfaces on the MityCAM-C10L development kit.

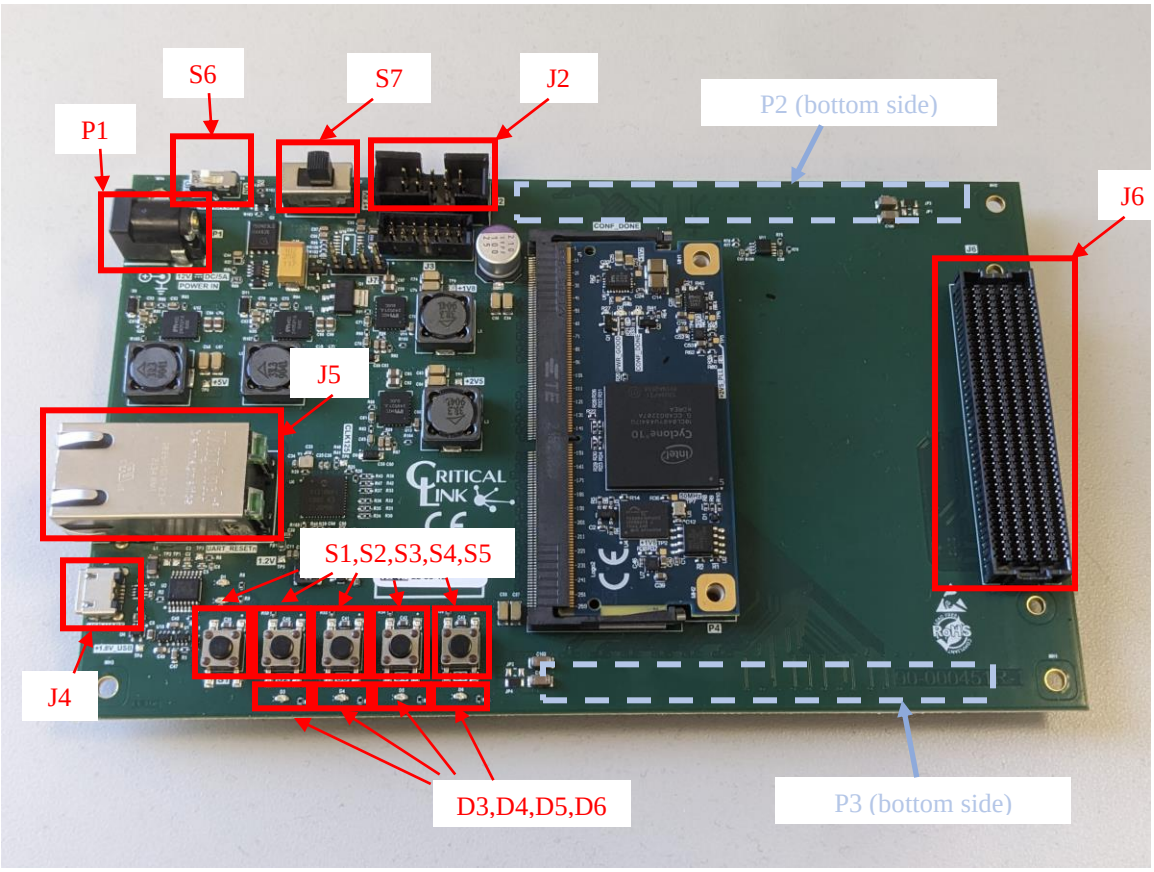

Figure 4 MitySOM-C10L Development Kit, Annotated Photo

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ORDERING INFORMATION

Included Components

Table 14 lists the components that are included with a MitySOM-C10L Development Kit. See Table 15 for specific development kit ordering information. Figure 4 shows the Development Kit Board, noting some key features.

Table 14: Included Items

Description	Interface Port	Qty. Included
MitySOM-C10L Development Kit Board	n/a	Qty. 1
MitySOM-C10L Module	J1	Qty. 1
Micro USB Cable for Debug Console	J4	Qty. 1
12V 5A AC to DC Supply	P1	Qty. 1
Ethernet cable	J5	Qty. 1
Development Kit Quick Start Guide	n/a	

Development Kits

The following table lists the standard MitySOM-C10L Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 15: Standard Model Numbers

Development Kit Model	Module Included
80-001650	C10L-7N-3XX-RI
80-001651	C10L-7Q-3X3-RI

REVISION HISTORY

Date	Change Description
03/02/2023	Initial Release

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