

NOTES:

- 1. ORDERS WILL BE PACKAGED ACCORDING TO THE SAMTEC PACKAGING EFFICIENCY STANDARDS (SPES) FOUND ON WWW.SAMTEC.COM.
- 2. ATTACH LABEL -4x2 TO EACH REEL
- 3. -01, -04 & -08 LANES PARTS TO BE PACKAGED IN TAPE & REEL, -16 LANES PARTS TO BE PACKAGED IN TRAY.
- 4. K-DOT PROVIDED AS STANDARD.
- 5. NOTE DELETED.

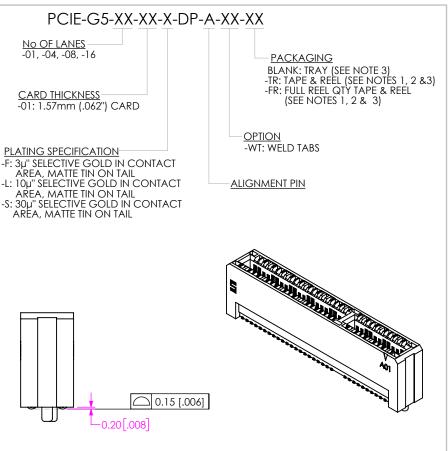


TABLE 1						
No OF LANES "A"		"B"	"C"	"D"	"E"	
-01	24.40 [.961]	19.00 [.748]	21.10 [.831]	19.00 [.748]	22.00 [.866]	
-04	38.40 [1.512]	33.00 [1.299]	35.10 [1.382]	33.00 [1.299]	36.00 [1.417]	
-08	55.40 [2.181]	50.00 [1.969]	52.10 [2.051]	50.00 [1.969]	53.00 [2.087]	
-16	88.40 [3.480]	83.00 [3.268]	85.10 [3.350]	83.00 [3.268]	86.00 [3.386]	

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DO NOT SCALE DRAWING DESCRIPTION MATERIAL: SHEET SCALE: 2.5:1 INSULATOR: LCP CONTACT: COPPER ALLOY



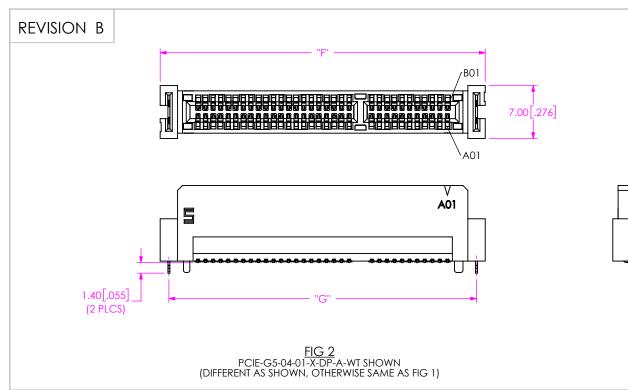
520 PARK EAST BLVD, NEW ALBANY, IN 47150 PHONE: 812-944-6733 FAX: 812-948-5047 e-Mail info@SAMTEC.com

PCIE-G5 ASSEMBLY

DWG. NO. PCIE-G5-XX-XX-X-DP-A-XX-XX

F:\DWG\MISC\MKTG\PCIE-G5-XX-XX-X-DP-A-XX-XX-MKT.SLDDRW

BY: JERRY SU 10/09/2018 | SHEET 1 OF 3



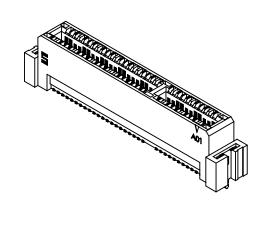
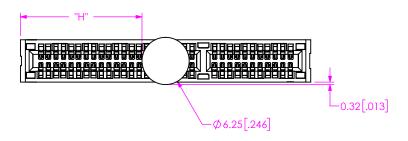


TABLE 3				
No. OF LANES	"F"	"G"		
-01	29.00 [1.142]	26.70 [1.051]		
-04	43.00 [1.693]	40.70 [1.602]		
-08	60.00 [2.362]	57.70 [2.272]		
-16	93.00 [3.661]	90.70 [3.571]		





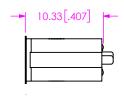


	TABLE 4			
OPTION	No OF LANES	"H"		
	-01	("A" - 6.25[.246]) / 2		
NONE	-04	("A" - 6.25[.246]) / 2		
NONL	-08	("A" - 6.25[.246]) / 2		
	-16	("A" - 6.25[.246]) / 2		
	-01	("F" - 6.25[.246]) / 2		
-WT	-04	("F" - 6.25[.246]) / 2		
-001	-08	("F" - 6.25[.246]) / 2		
	-16	("F" - 6.25[.246]) / 2		

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DESCRIPTION:

PCIE-G5 ASSEMBLY

DWG. NO.

PCIE-G5-XX-XX-X-DP-A-XX-XX
BY: JERRY SU 10/09/2018 SHEET 2 OF 3

REVISION B

		ſ				TABLE 5	5		
		Ī			SIDE B			SIDE A	
				NAME	DESCIPTION	TYPE	NAME	DESCIPTION	TYPE
			2	+12V +12V	12 V pow er 12 V pow er	S-R G-L	PRSNT1# +12V	Hot-plug detect 12 V pow er	G-R G-L
			3	+12V	12 V pow er	G-R	+12V	12 V pow er	S-R
			4	GND	GROUND	S-L	GND	GROUND	S-L
			5	SMCLK	SM Bus Clock	S-R	JTAG2	TCK (test clock)	G-R
			6	SMDA TA	SM Bus Data	G-L	JTAG3	TDI (test input data)	G-L
1			7 8	GND	GROUND	G-R	JTAG4	TDO (test data output)	S-R S-L
			9	+3.3V JTAG1	3.3 V pow er TRST# (test resest)	S-L S-R	JTAG5 +3.3V	TMS (test mode select) 3.3 V pow er	G-R
		lŀ	10	+3.3V aux	3.3 V aux pow er	G-L	+3.3V	3.3 V pow er	G-L
4			11	WAKE#	Signal for link	G-R	PERST#	Fundamental reset	S-R
			10	Devid	DECEDIVED	MECHANICAL		CDOLIND	<u> </u>
			12 13	RSV D GND	RESERVED GROUND	G-L G-R	GND REFCLK+	GROUND Reference clock	G-L S-R
0			14	PETp0	Transmitter, DP	S-L	REFCLK-	Diff pair	S-L
S		l	15	PETn0	LANE 0	S-R	GND	GROUND	G-L
P			16	GND	GROUND	G-L	PERp0	Receiver, DP	S-R
∣₹			17	PRSNT2#	Hot-plug detect	G-R	PERn0	LANE 0	S-L
OF LANES			18	GND	GROUND	(SEE TABLE 7) ND OF 01 CONNECTO	GND	GROUND	G-R
Ιŏ			19	PETp1	Transmitter, DP	S-L	RSVD	RESERVED	G-R
2			20	PETP1 PETn1	LANE 1	S-L S-R	GND	GROUND	G-R G-L
	8		21	GND	GROUND	G-L	PERp1	Receiver, DP	S-R
	= 08		22	GND	GROUND	G-R	PERn1	LANE 1	S-L
			23	PETp2	Transmitter, DP	S-L	GND	GROUND	G-R
	OF LANES	[24	PETn2	LANE 2	S-R	GND	GROUND	G-L
	S		25	GND	GROUND	G-L	PERp2	Receiver, DP	S-R
	逆		26 27	GND DETn3	GROUND Transmitter DP	G-R	PERn2 GND	LANE 2 GROUND	S-L G-R
	5		28	PETp3 PETn3	Transmitter, DP LANE 3	S-L S-R	GND	GROUND	G-R G-L
	No		29	GND	GROUND	G-L	PERp3	Receiver, DP	S-R
			30	RSVD	RESERVED	G-R	PERn3	LANE 3	S-L
		l	31	PRSNT2#	Hot-plug detect	(SEE TABLE 7)	GND	GROUND	G-R
			32	GND	GROUND	(SEE TABLE 7) END OF 04 CON	RSVD	RESERVED	G-L
	1								
			33	PETp4	Transmitter, DP	S-L	RSVD	RESERVED	G-R
		l	34 35	PETn4 GND	LANE 4 GROUND	S-R G-L	GND PERp4	GROUND Receiver, DP	G-L S-R
		l	36	GND	GROUND	G-R	PERn4	LANE 4	S-L
		16	37	PETp5	Transmitter, DP	S-L	GND	GROUND	G-R
		= 1	38	PETn5	LANE 5	S-R	GND	GROUND	G-L
			39	GND	GROUND	G-L	PERp5	Receiver, DP	S-R
		쀨	40	GND	GROUND	G-R	PERn5	LANE 5	S-L
		OF LANES	41	PETp6	Transmitter, DP	S-L	GND	GROUND	G-R
		ᇤ	42 43	PETn6 GND	LANE 6 GROUND	S-R G-L	GND PERp6	GROUND Receiver, DP	G-L
		၂လ	44	GND	GROUND	G-R	PERP6	LANE 6	S-R S-L
		S.	45	PETp7	Transmitter, DP	S-L	GND	GROUND	G-R
			46	PETn7	LANE 7	S-R	GND	GROUND	G-L
			47	GND	GROUND	G-L	PERp7	Receiver, DP	S-R
			48	PRSNT2#	Hot-plug detect	G-R	PERn7	LANE 7	S-L
			49	GND	GROUND	(SEE TABLE 7) END OF 08 CON	GND	GROUND	G-R
	\vdash	1 -	50	PETp8	Transmitter, DP	S-L	RSVD	RESERVED	G-R
			51	PETP8	LANE 8	S-R	GND	GROUND	G-R G-L
			52	GND	GROUND	G-L	PERp8	Receiver, DP	S-R
			53	GND	GROUND	G-R	PERn8	LANE 8	S-L
			54	PETp9	Transmitter, DP	S-L	GND	GROUND	G-R
		[55	PETn9	LANE 9	S-R	GND	GROUND	G-L
			56 57	GND GND	GROUND GROUND	G-L G-R	PERp9 PERn9	Receiver, DP	S-R
			58	PETp10	Transmitter, DP	G-R S-L	GND	LANE 9 GROUND	S-L G-R
			59	PETn10	LANE 10	S-R	GND	GROUND	G-L
			60	GND	GROUND	G-L	PERp10	Receiver, DP	S-R
			61	GND	GROUND	G-R	PERn10	LANE 10	S-L
			62	PETp11	Transmitter, DP	S-L	GND	GROUND	G-R
		[63	PETn11	LANE 11	S-R	GND	GROUND	G-L
			64	GND	GROUND GROUND	G-L	PERp11	Receiver, DP	S-R
			65 66	GND PETp12	Transmitter, DP	G-R S-L	PERn11 GND	LANE 11 GROUND	S-L G-R
			67	PETn12	LANE 12	S-R	GND	GROUND	G-L
			68	GND	GROUND	G-L	PERp12	Receiver, DP	S-R
			69	GND	GROUND	G-R	PERn12	LANE 12	S-L
			70	PETp13	Transmitter, DP	S-L	GND	GROUND	G-R
			71	PETn13	LANE 13	S-R	GND	GROUND	G-L
			72	GND	GROUND	G-L	PERp13	Receiver, DP LANE 13	S-R
			73 74	GND PETp14	GROUND Transmitter, DP	G-R S-L	PERn13 GND	GROUND	S-L G-R
			75	PETp14 PETn14	LANE 14	S-L S-R	GND	GROUND	G-R G-L
			76	GND	GROUND	G-L	PERp14	Receiver, DP	S-R
			70 1	GND	GROUND	G-R	P⊞Rn14	LANE 14	S-L
			77					GROUND	G-R
			77 78	PETp15	Transmitter, DP	S-L	GND		
			77 78 79	PETp15 PETn15	LANE 15	S-R	GND	GROUND	G-L
			77 78 79 80	PETp15 PETn15 GND	LANE 15 GROUND	S-R G-L	GND PERp15	GROUND Receiver, DP	G-L S-R
			77 78 79	PETp15 PETn15	LANE 15	S-R	GND	GROUND	G-L

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PCIE-G5 ASSEMBLY

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