Apacer

RoHS Recast Compliant

Industrial Secure Digital Card

H1-M Product Specifications

(Toshiba 15nm)

October 1, 2021

Version 2.4

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Apacer

Specifications Overview:

- **Fully Compatible with SD Memory Card Standard Specifications**
  - Part 1, Physical Layer Specification, Ver 3.01 Final
  - Part 2, File System Specification, Ver 3.00
  - Part 3, Security Specification, Ver 3.00 Final
- **Capacity**
  - 8,16, 32, 64, 128 GB
- **Performance***
  - Sequential read: Up to 43 MB/sec
  - Sequential write: Up to 30 MB/sec
- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Bad block management
  - S.M.A.R.T.
  - DataDefender™
  - SMART Read Refresh™
- **Bus Speed Mode:** Support Class 10 with UHS-I
- **SD-Protocol Compatible**
- **Support SPI Mode**
- **NAND Flash Type:** MLC
- **Endurance (in Terabytes Written: TBW)**
  - 8 GB: 4 TBW
  - 16 GB: 9 TBW
  - 32 GB: 18 TBW
  - 64 GB: 37 TBW
  - 128 GB: 75 TBW
- **Temperature Range**
  - Operating:
    Standard: -25°C to 85°C
    Wide: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Operating Voltage**: 2.7V ~ 3.6V
- **Power Consumption***
  - Active mode: 145 mA
  - Idle mode: 235 µA
- **Physical Dimensions**
  - 32 (L) x 24 (W) x 2.1(H), unit: mm
- **RoHS Recast Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

Table of Contents

1. General Descriptions

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's SD card is designed specifically for rigorous applications by offering maximum endurance, reliability, and agility, where extreme traceability, enhanced data integrity, and exceptionally velocity are required.

Regarding compatibility, this industrial SD card is compatible with SD Memory Card Specifications, Physical Layer specification, File System Specification and Part 3 Security Specification. Furthermore, the SD card is compatible with SD protocol. With built-in ECC, Global Wear Leveling and bad block management, this industrial SD card serves as an ideal portable storage solution.

1.1 Functional Block

The SD contains a flash controller and flash media with SD standard interface.

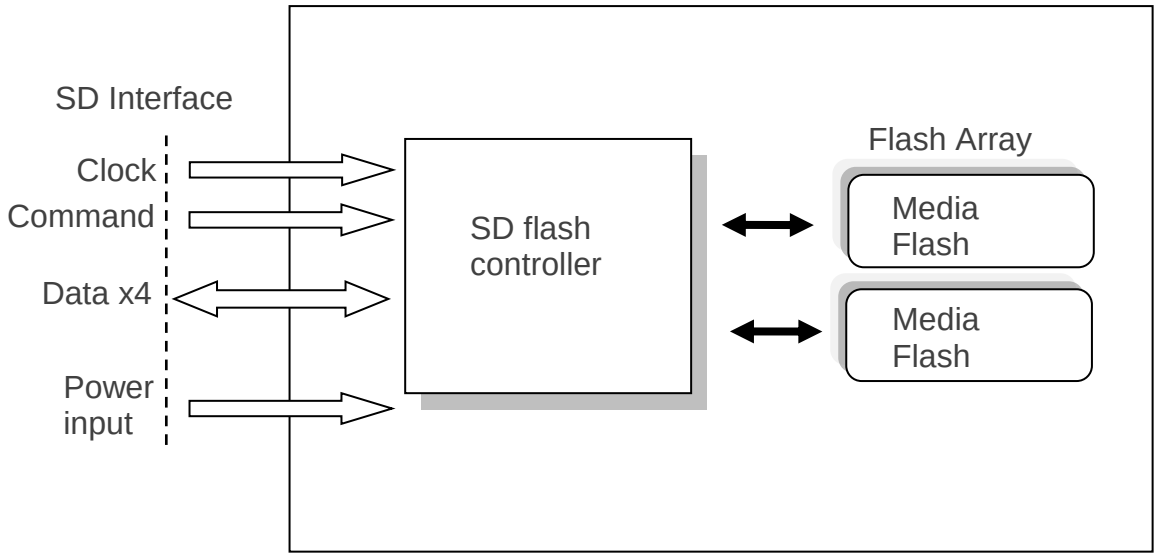


Figure 1-1 Functional Block Diagram

1.2 Flash Management

1.2.1 Bad Block Management

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD replaces this bad bit with a spare bit within the sector header. If necessary, the SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.2.2 ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, this SD card applies the BCH ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.2.3 S.M.A.R.T

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

1.2.4 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.5 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

1.2.6 DataDefender™

Apacer's DataDefender combines both firmware and hardware mechanisms to ensure data integrity. When power disruption occurs, the hardware mechanism will notice and trigger the controller to run multiple write-to-flash cycles to store data. Then the firmware will check that the data was correctly written to the NAND flash after the power disruption, preventing data loss.

2. Electrical Characteristics

2.1 Card Architecture

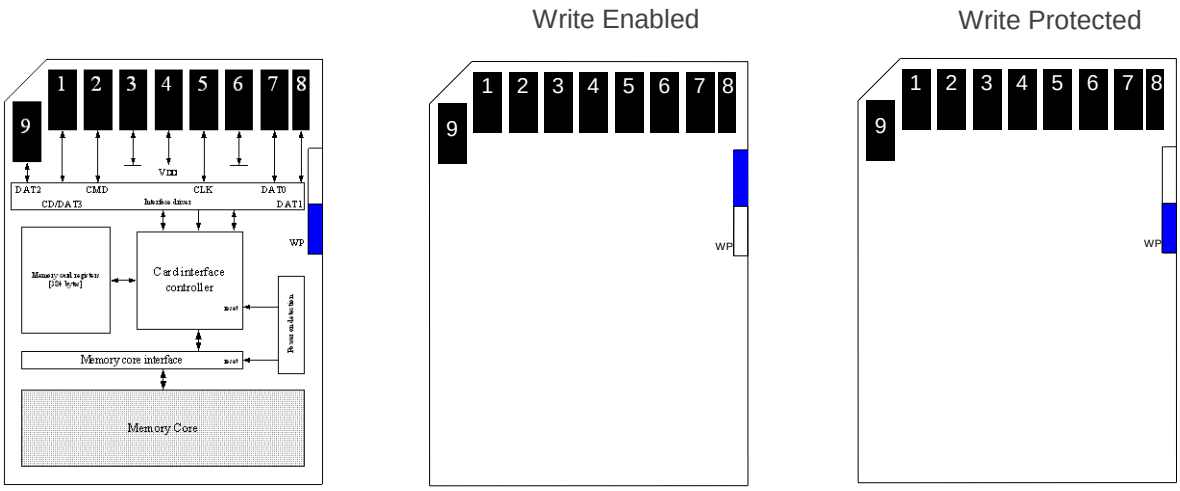


Figure 2-1 Card Architecture

2.2 Pin Assignments

Table 2-1 Pin Assignments

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]	CS	Chip select
2	CMD	Command/Response	DI	Data in
3	VSS1	Supply voltage ground	VSS	Supply voltage ground
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS2	Supply voltage ground	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]	DO	Data out
8	DAT1	Data line[Bit 1]	Reserved	
9	DAT2	Data line[Bit 2]	Reserved	

2.3 Capacity

Capacity specifications of the SD card are available as shown in Table 2-2.

Table 2-2 Capacity Specifications

Capacity	Total Bytes
8 GB	7,960,788,992
16 GB	15,997,075,456
32 GB	32,082,231,296
64 GB	64,156,073,984
128 GB	128,278,593,536

Note: The statistics may vary depending on file systems of various OS. User data bytes do not indicate total useable bytes. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

2.4 Performance

Performance of the SD card is listed below in Table 2-3.

Table 2-3 Performance Specifications

Capacity / Performance	8 GB	16 GB	32 GB	64 GB	128 GB
Sequential Read* (MB/s)	43	43	43	43	43
Sequential Write* (MB/s)	26	23	30	22	22

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

2.5 DC Power Supply

Table 2-4 DC Power Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.3	3.6	V

2.6 Power Consumption

Table 2-5 Power Consumption

Capacity / Mode	8 GB	16 GB	32 GB	64 GB	128 GB
Operating (mA)	75	75	110	135	145
Standby (µA)	200	185	180	195	235

Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

2.7 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 2-6 Endurance Specifications

Capacity	TeraBytes Written
8 GB	4
16 GB	9
32 GB	18
64 GB	37
128 GB	75

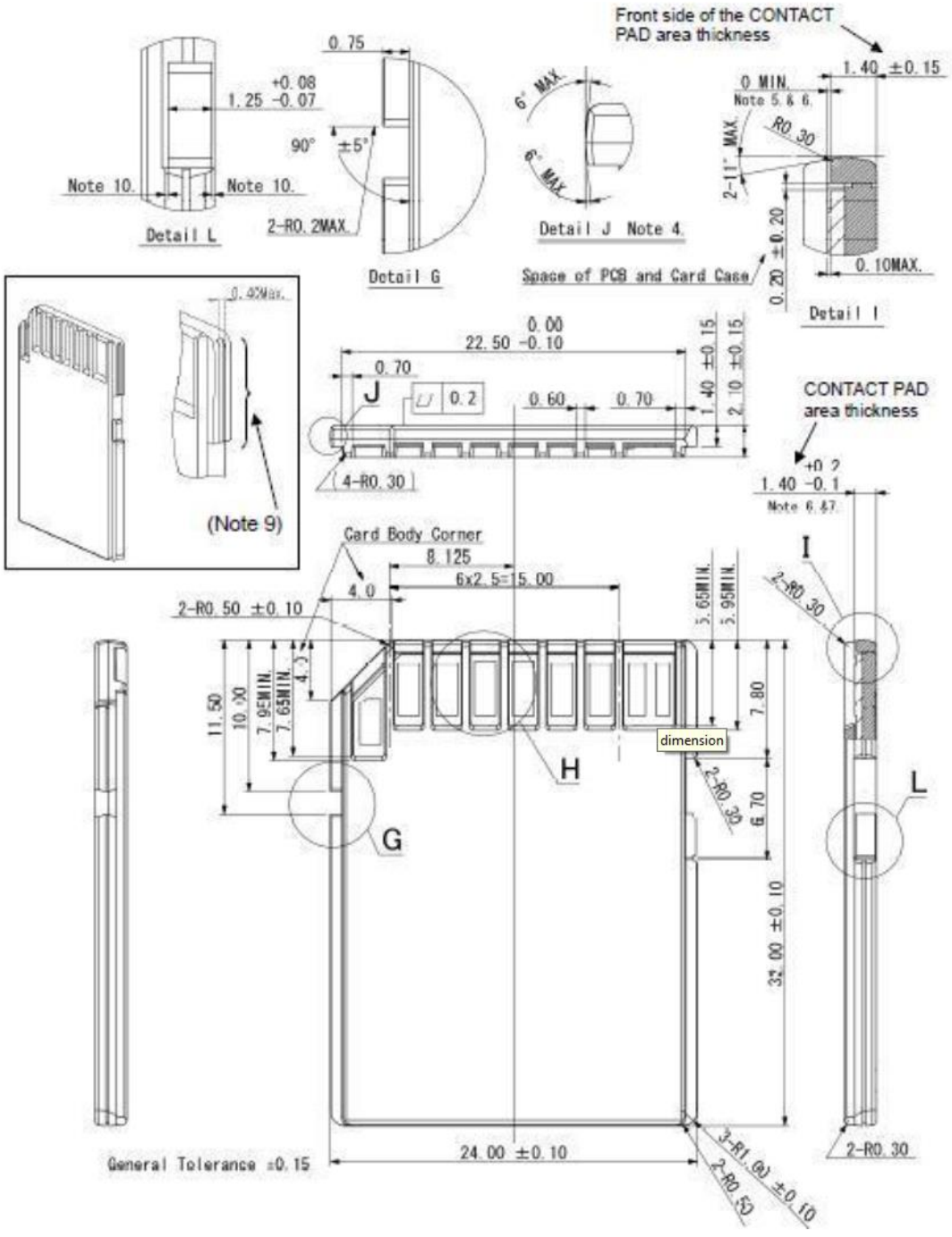
Note:

- This estimation complies with Apacer internal workload.
- Flash vendor guaranteed MLC P/E cycle : Toshiba - 3K
- The WLE/WAF values may vary with the real application on user platform.
- 1 Terabyte = 1,000 GB

3. Physical Characteristics

3.1 Physical Dimensions

Dimensions: 32 mm (L) x 24 mm (W) x 2.1 mm (H)



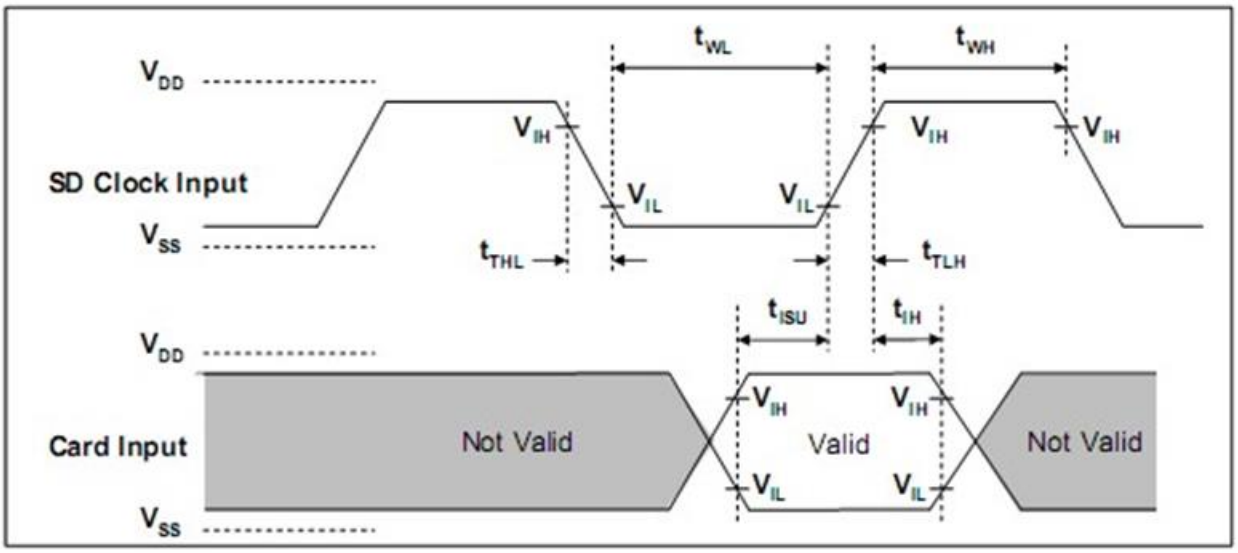
3.2 Durability Specifications

Table 3-1 Durability Specifications

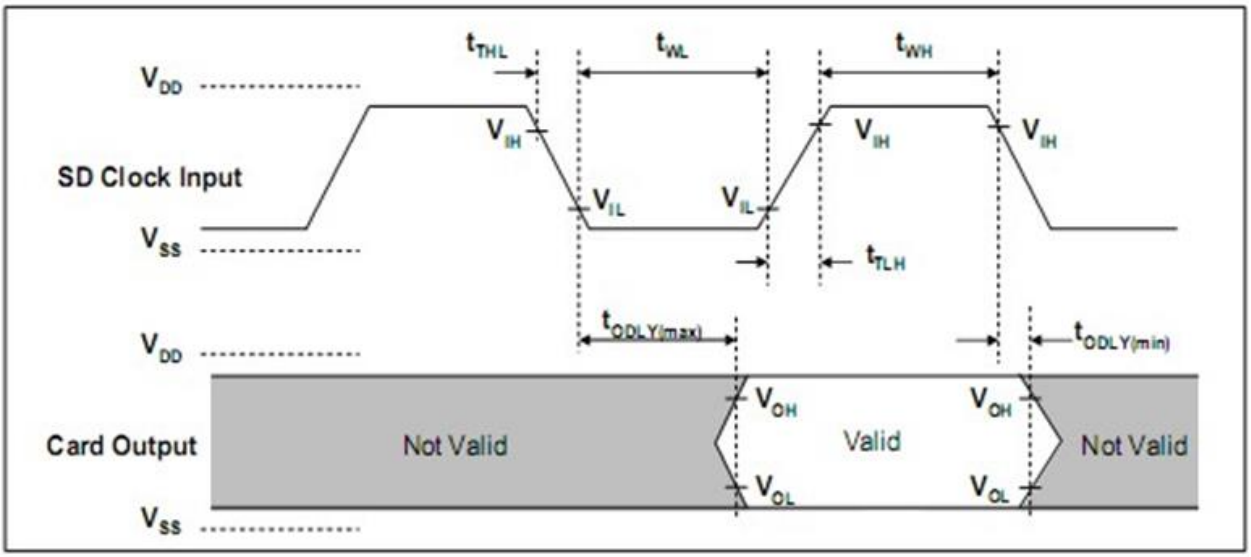
Item	Specifications
Temperature	-25°C to 85°C (Standard) -40°C to 85°C (Wide)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	1.5m free fall, 6 surfaces of each
Bending	≧ 10N, hold 1min/5times
Torque	0.15N-m or 2.5deg, hold 30 seconds/ 5 times
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance, Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card ;storage for 30 mins)
Switch cycle	0.4~0.5N, 1000 times
Durability	10,000 times mating cycle
ESD	Contact: +/-4KV each item 25 times Air: +/-8KV 10 times

4. DC Characteristics

4.1 SD Interface Timing (Default)



Card input Timing (Default Speed Card)

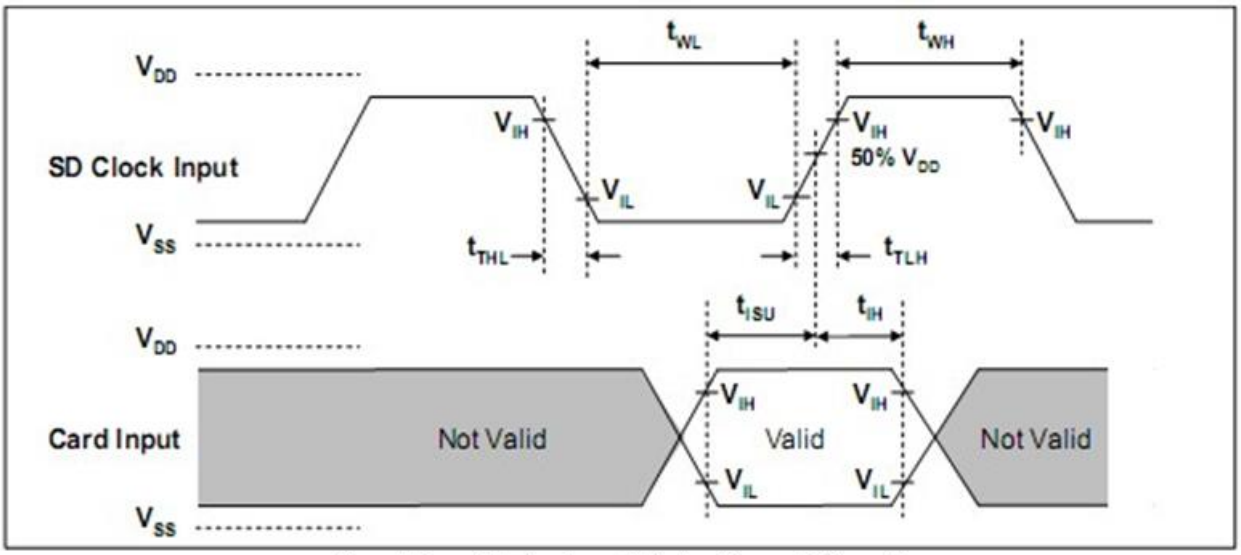


Card Output Timing (Default Speed Mode)

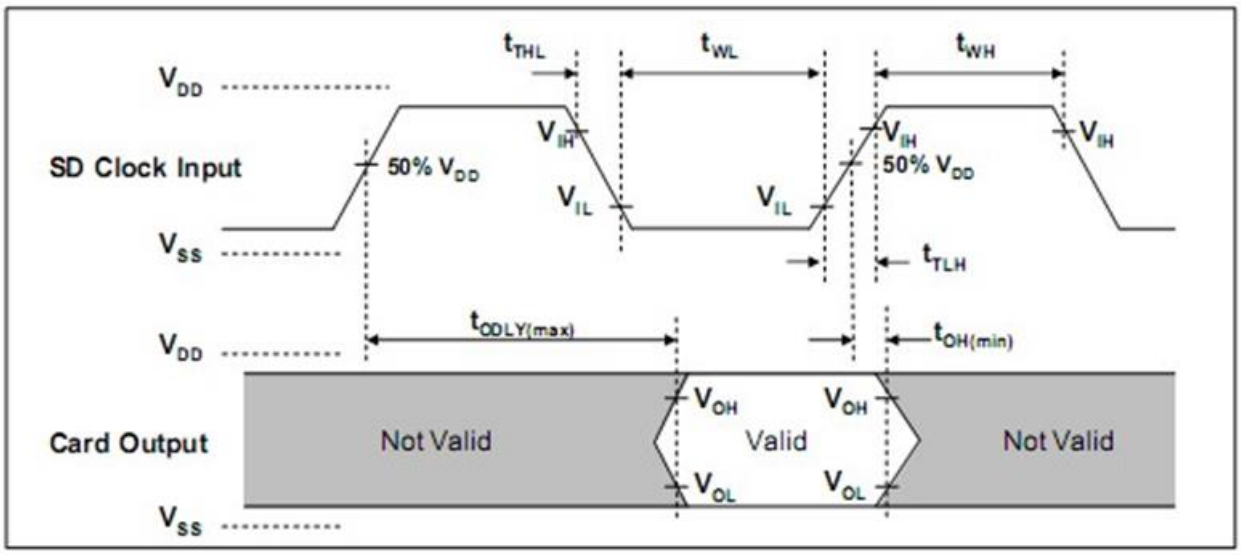
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	25	MHz	C_{card} ≤ 10 pF (1 card)
f_{OD}	Clock frequency identification	0(1)/100	400	KHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	10	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	5	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TH}	Input hold time	5	-	ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer mode	0	14	ns	C_L ≤ 40 pF (1 card)
t_{OH}	Output hold time	0	50	ns	C_L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 SD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



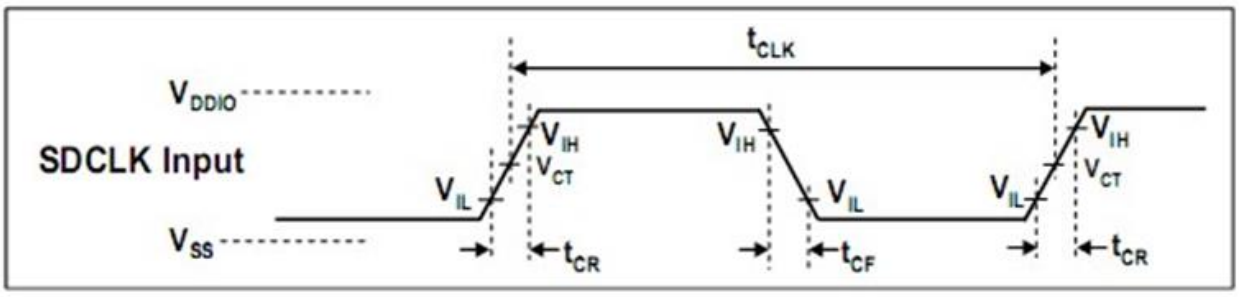
Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	Ccard ≤ 10 pF (1 card)
t_{WL}	Clock low time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{WH}	Clock high time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	Ccard ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	3	ns	Ccard ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	Ccard ≤ 10 pF (1 card)
t_{TH}	Input hold time	2	-	ns	Ccard ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

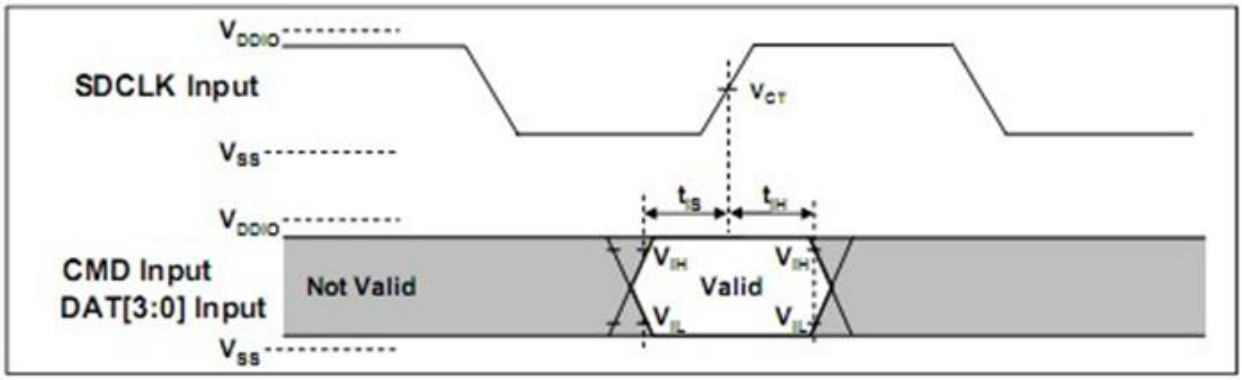
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

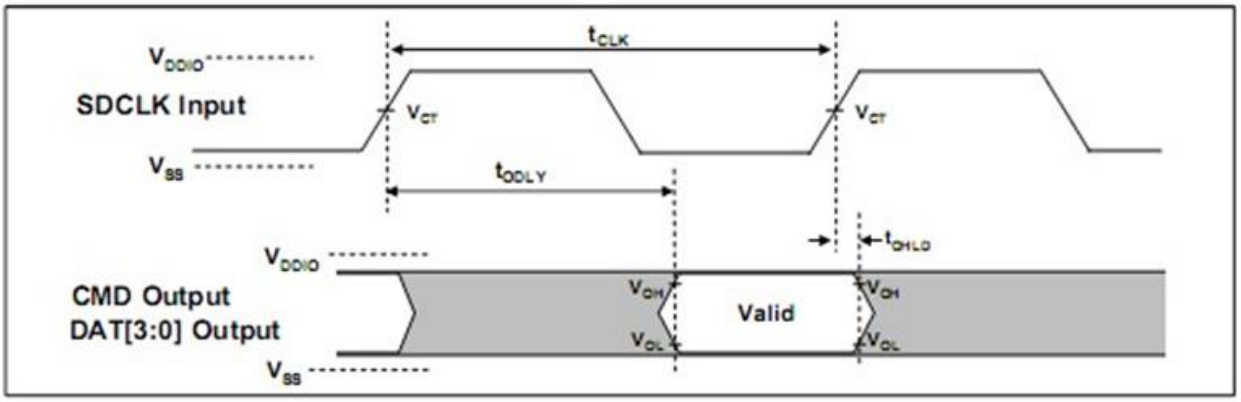
4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
SYMBOL	**MIN**	**MAX**	**UNIT**	**SDR12, SDR25 and SDR50 MODES**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

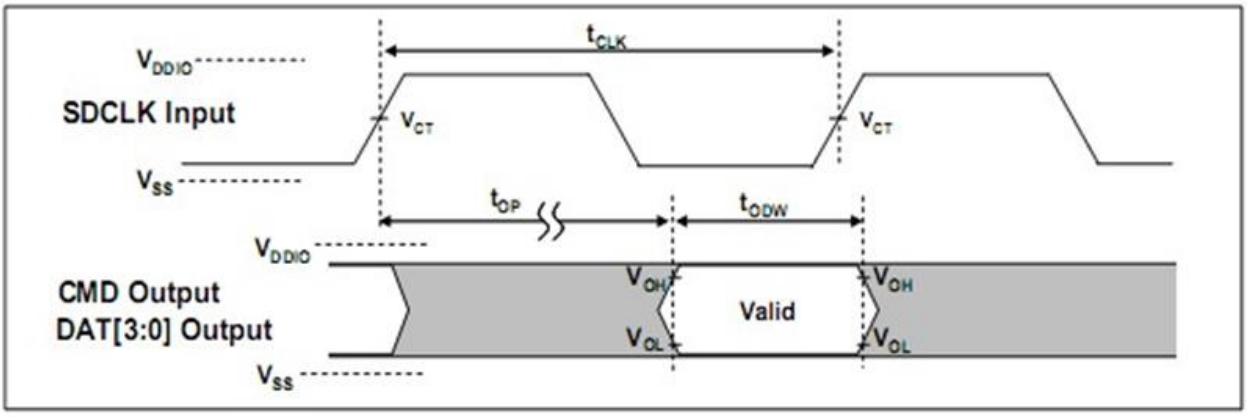
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). CL=15pF

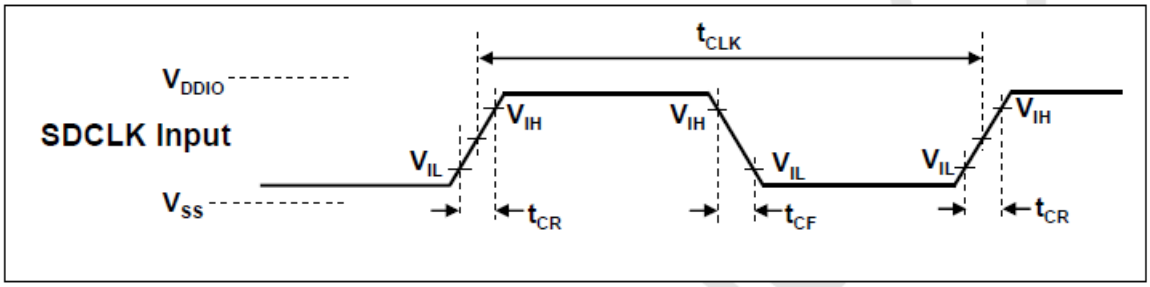
4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window

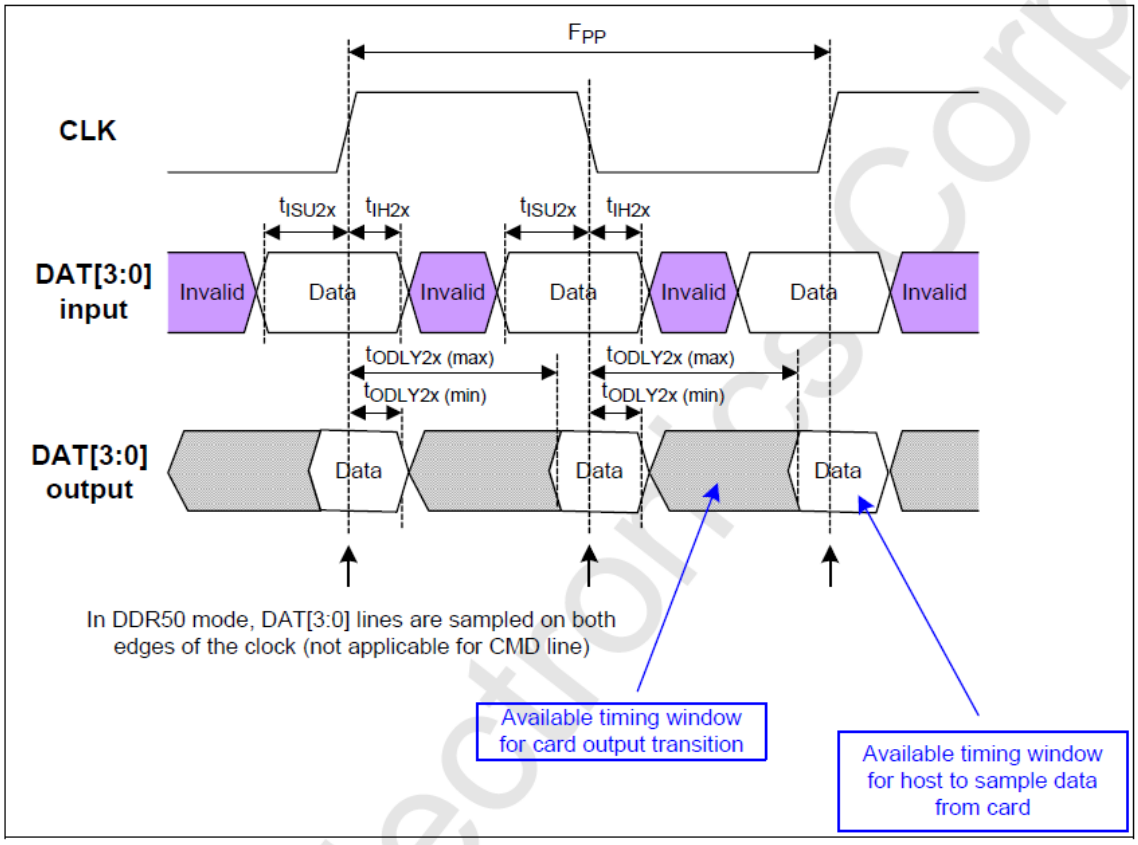
SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

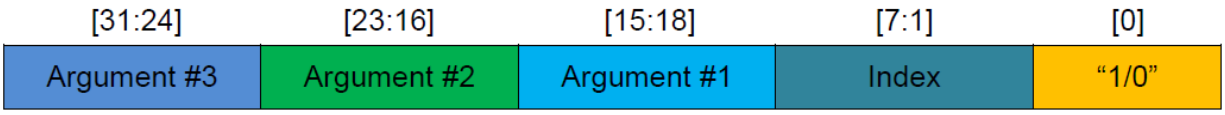
4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	C_L≤30 pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	C_L≤25 pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)

5. S.M.A.R.T.

5.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.
- Bit [7:1]: Indicates the index of the function to be executed:
  - Read Mode: Index = 0x10 Get SMART Command Information
  - Write Mode: Index = 0x08 Pre-Load SMART Command Information
- Bit [15:8]: Function argument #1 (1-byte)
- Bit [23:16]: Function argument #2 (1-byte)
- Bit [31:24]: Function argument #3 (1-byte)

5.2 Process for Retrieving SMART Data

Retrieving SMART data requires the following two commands executed in sequence and in accordance with the SD Association standard flowchart for CMD56 (see below).

Step 1: Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] “0” (Write Mode) [1:7] “0001 000” (Index = 0x08) [8:511] All ‘0’ (Reserved)	No expected data

Step 2: Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	1 sector (512 bytes) of response data byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

*Please refer to technical note for High/Low byte definition.

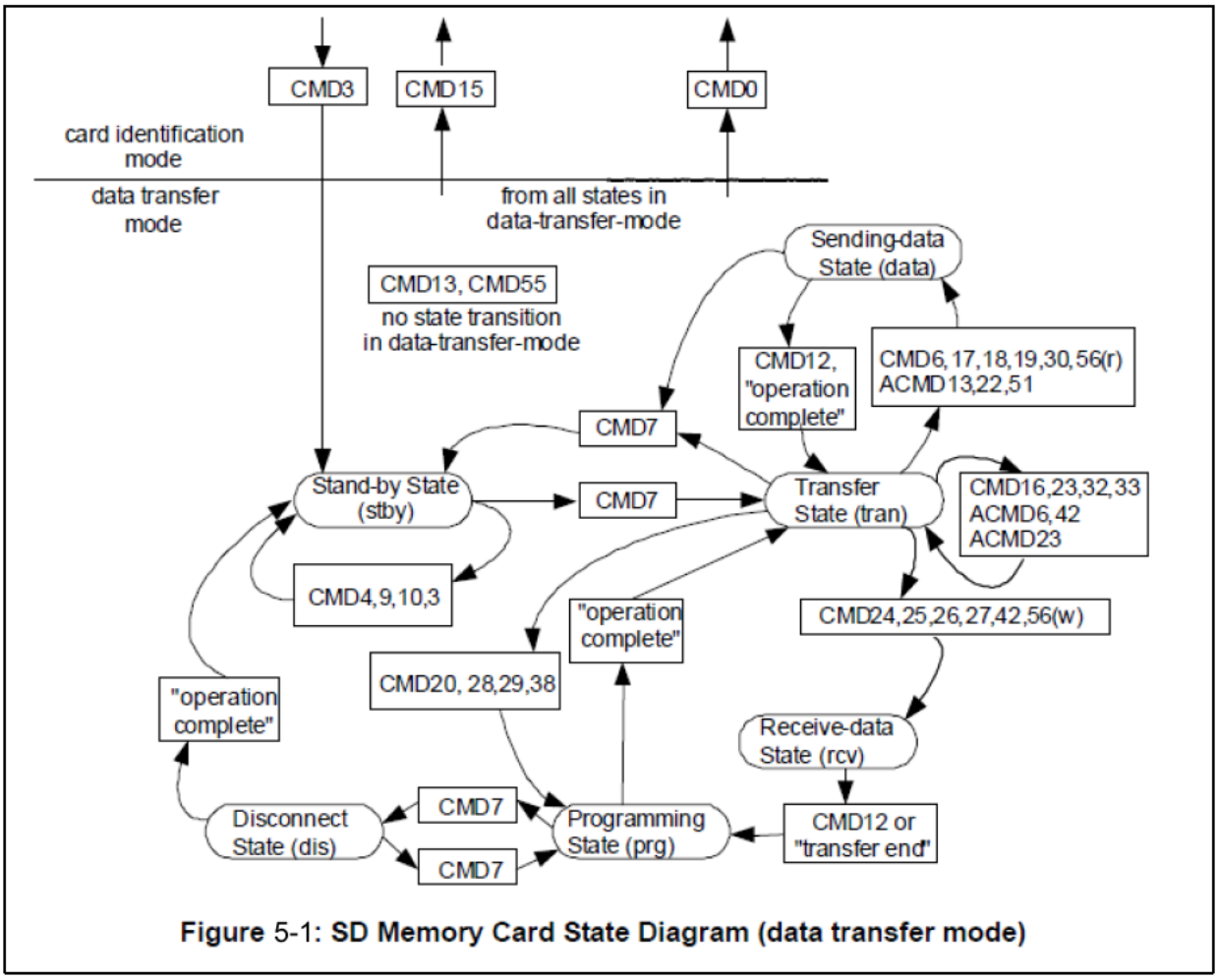


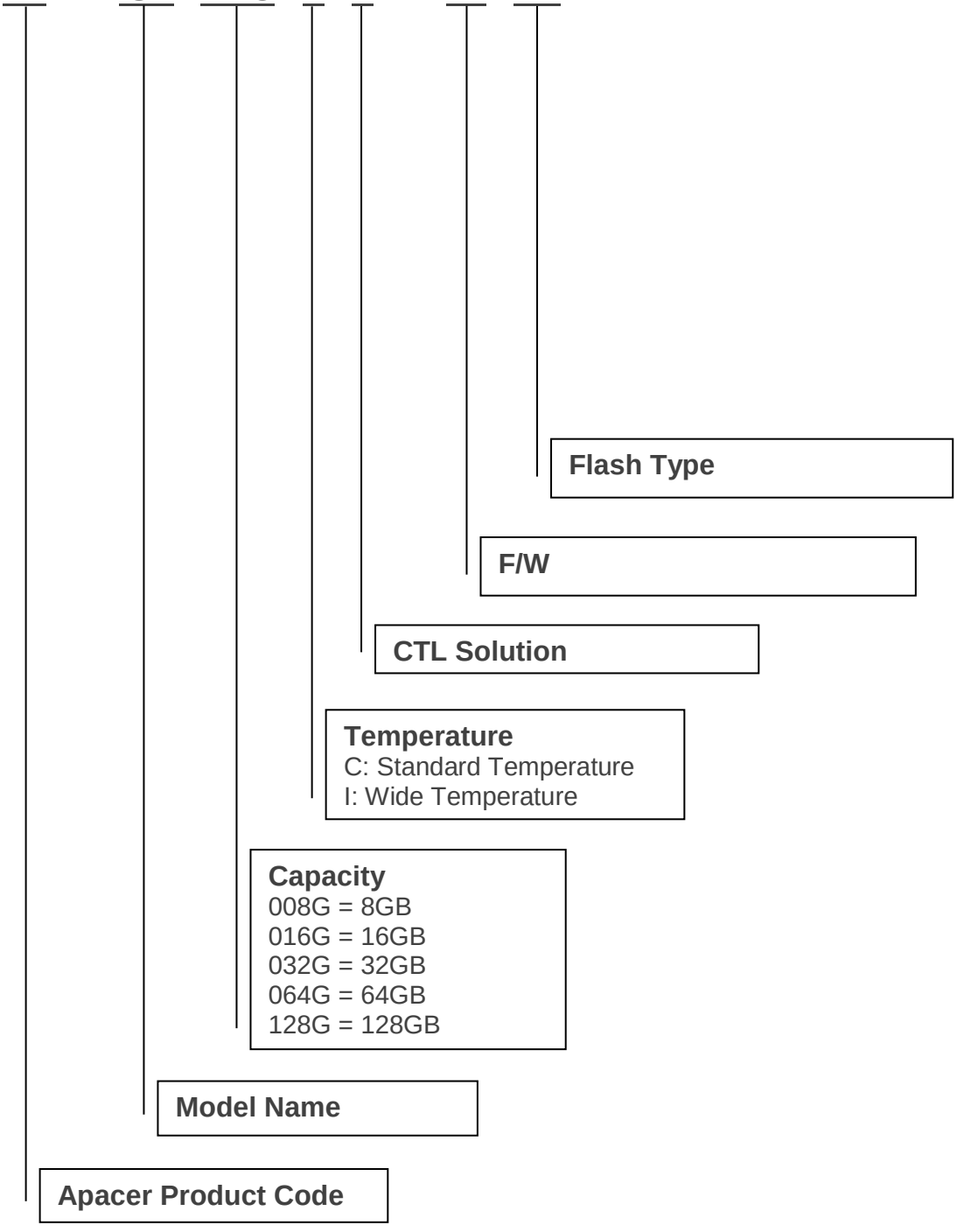
Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

6. Product Ordering Information

6.1 Product Code Designations

AP – ISD xxxG X A – 1X TM



6.2 Valid Combinations

Capacity	Standard Temperature	Wide Temperature
8GB	AP-ISD008GCA-1HTM	AP-ISD008GIA-1HTM
16GB	AP-ISD016GCA-1HTM	AP-ISD016GIA-1HTM
32GB	AP-ISD032GCA-1HTM	AP-ISD032GIA-1HTM
64GB	AP-ISD064GCA-1FTM	AP-ISD064GIA-1FTM
128GB	AP-ISD128GCA-1FTM	AP-ISD128GIA-1FTM

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	11/16/2015
1.1	Added CMD56 argument for SMART	12/16/2015
1.2	Added SMART section	12/23/2015
1.3	Added performance and power consumption for 4GB	2/2/2016
1.4	Revised performance and power consumption values	2/5/2016
1.5	Revised product ordering information for 4GB, 8GB, 16GB and 32GB due to FW update	3/15/2016
1.6	Revised capacity specifications	4/19/2016
1.7	- Revised performance for 4GB-32GB due to FW change (82.105) - Revised product ordering information for 4GB-32GB	7/29/2016
1.8	Added Power Failure Management to Features and General Description	10/27/2016
1.9	Modified the argument of Step 2: Read Mode – [0x10] Get SMART Command Information for S.M.A.R.T.	10/27/2016
2.0	- Changed Wear-leveling to Global Wear Leveling - Added Read Disturb Management to Flash Management on Features page	11/15/2017
2.1	- Renamed extended temperature to wide temperature - Added Endurance to Specifications Overview page and 2.7 Endurance - Renamed Power Failure Management to DataDefender at Flash Management on Specifications Overview page and 1.2.6 section and updated the technology description	12/20/2018
2.2	- Updated the first note at 2.7 Endurance - Renamed Read Disturb Management to SMART Read Refresh and updated its description at 1.2.5 section	5/20/2019
2.3	Updated power consumption for 32GB at 2.6 Power Consumption	11/26/2020
2.4	Removed 4GB support	10/1/2021

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